

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
CONVERTER PERFORMANCE						
Accuracy	±5.3 max	±15.3 max	±8.5 max	arc min	Output Coding Parallel Natural Binary	1, 3
Tracking Rate	27 min	18 min	**	rev/s		4
Resolution	14 (1 LSB = 1.3 arc min)	12 (1 LSB = 5.3 arc min)	**	Bits		
Signal & Reference Frequency	400 2.6	* *	* *	Hz kHz	Option X1Z Option X4Z	
Repeatability of Position Output	1	*	*	LSB		4
Bandwidth	130	150	**	Hz		4
SIGNAL INPUT IMPEDANCE						
90V Signal	200	*	*	kΩ	Resistive Tolerance ±2%	4
26V Signal	57.7	*	*	kΩ		4
11.8V Signal	26	*	*	kΩ		4
REFERENCE INPUTS						
Reference Voltage	11.8, 26, 115	*	*	V rms	See Ordering Information Resistive Tolerance ±5%	
Reference Impedance						
115V Ref	120	*	*	kΩ		4
26V Ref	27	*	*	kΩ		4
11.8V Ref	12.3	*	*	kΩ		4
ACCELERATION CONSTANT						
	56000	80000	**	sec ⁻²	Symbol K _a	4
LARGE STEP RESPONSE						
	85 typ 100 max	60 typ 75 max	** **	ms ms	179° Step for Settling to 1 LSB of Error	1, 3
POWER LINES						
+V _S = +15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
-V _S = -15V	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
V _L = +5V	35 typ 56 max	*	*	mA	Quiescent Condition	1, 3
Power Dissipation	1.4 max	*	*	W		
DIGITAL INPUTS (INHIBIT, ENABLE L, ENABLE M)						
V (Input High)	2 min	*	*	V dc	V _L = +5V	1, 3
V (Input Low)	0.7 max	*	*	V dc	V _L = +5V	1, 3
I (Input High)	20 max	*	*	μA	V _{IH} = 2.4V	1, 3
I (Input Low)	-400 max	*	*	μA	V _{IL} = 0.4V	1, 3
ENABLE AND DISABLE TIME						
	80 max	*	*	ns		2, 4
INHIBIT						
Sense	Logic Low to INHIBIT	* *	* *			
Time to Data Stable (after Negative-Going Edge of INHIBIT)	640 max	*	*	ns		4
BUSY OUTPUT						
Sense	Active Logic High when converter position output changing.					
Timing	Positive going edge 50ns before change in position output.					
Width						
	400 typ	*	*	ns		1, 3
	200 min	*	*	ns		1, 3
	600 max	*	*	ns		1, 3
Load	2 min	*	*	TTL		4
DIGITAL OUTPUTS						
Voltage Levels						
Logic High	2.4 min	*	*	V dc	V _L = +5V, I _{OH} = -240μA	1, 3
Logic Low	0.4 max	*	*	V dc	V _L = +5V I _{OL} = 9.6mA	1, 3
Load	6 max	*	*	TTL		

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
OPERATING TEMPERATURE RANGE						
Option 5YZ	0 to +70	*	*	°C		
Option 4YZ	-55 to +125	*	*	°C		
DIMENSIONS	1.74×1.14×0.28 (44.2×28.9×7.1)	*	*	Inch mm	See Package Information	4
WEIGHT	0.86 max 25 max	*	*	oz grams		4

NOTES

¹Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.

²ENABLE M enables most significant 8 bits.

ENABLE L enables least significant 4 bits (or 6 bits for SDC/RDC1740).

³100% tested at nominal values of power supplies, input signal voltages and operating frequency.

⁴Guaranteed by design.

*Specifications same as SDC/RDC1740.

**Specifications same as SDC/RDC1741.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

+V_S¹ to GND +17.25V dc
 -V_S to GND -17.25V dc
 +V_L² to GND +7V dc
 Reference Input HI to GND ±350V dc
 Reference Input LO to GND ±350V dc
 Common Mode Range 175V rms
 S1, S2, S3, S4 to GND ±350V dc
 Any Logical Input to GND -0.4V to +V_L
 Case to GND ±20V dc
 Storage Temperature Range -65°C to +150°C

CAUTION:

¹Correct polarity voltages must be maintained on the +V_S and -V_S pins.

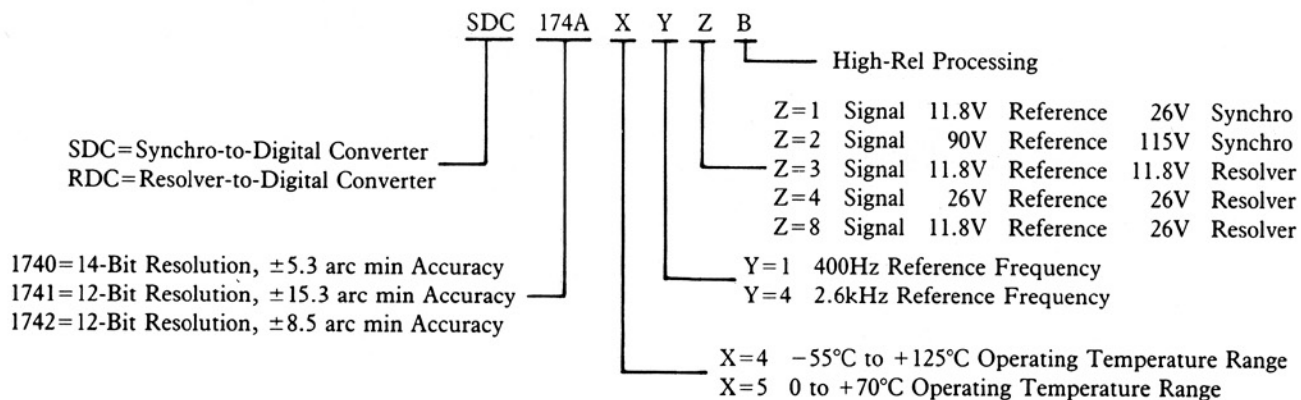
²The +5V power supply must never go below GND potential.

NOTE

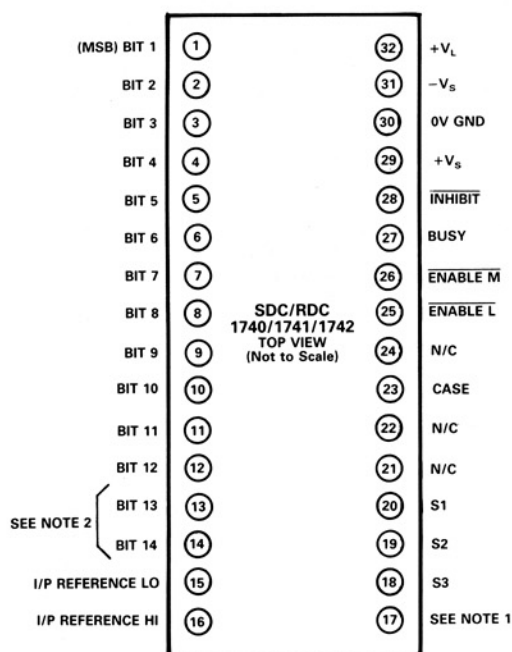
Absolute maximum ratings are those values beyond which damage to the device may occur.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.



PIN CONFIGURATION



NOTE 1. FOR THE RESOLVER OPTION PIN 17 IS S4
FOR THE SYNCHRO OPTION PIN 17 IS
NOT CONNECTED.

NOTE 2. FOR THE 1741 AND 1742 PINS 13 AND 14
ARE NOT CONNECTED.

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for 1741/1742)	0.0879
13	0.0439
14 (LSB for 1740)	0.0220

Table I. Bit Weight Table

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1-14	Bit 1-14 (1740)	Parallel output data bits.
1-12	Bit 1-12 (1741/1742)	
15	REF LO	Input pins for the reference signal.
16	REF HI	
17	S4 OR N/C	S4 signal input for Resolver option. N/C for Synchro option.
18	S3	
19	S2	Synchro/Resolver input signals.
20	S1	
21	N/C	No Connection.
22	N/C	No Connection.
23	CASE	Should be connected to 0V GND.
24	N/C	No Connection.
25	ENABLE L	ENABLE L enables the 6 or 4 least significant bits.
26	ENABLE M	ENABLE M enables the 8 most significant bits. Logic High sets the output data bits to a high impedance state; a Logic Low presents the data in the latches to the output pins.
27	BUSY	Converter busy. A Logic High output indicates that the output latches are being updated and data should not be transferred.
28	INHIBIT	Logic Low inhibits the data transfer from the counter to the output latches.
29	+V _S	Main positive power supply.
30	0V GND	Power supply ground.
31	-V _S	Main negative power supply.
32	+V _L	Logic power supply.

BUSY OUTPUT

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY is initiated each time the input moves by an analog equivalent of an LSB and the internal counter is incremented or decremented or the $\overline{\text{INHIBIT}}$ input is released.

Typically the width of the BUSY pulse is 400ns during the position data output updates. The trailing edge, positive to negative transition, of the BUSY pulse indicates that the position data output has been updated and is ready for transfer (data valid). The maximum load on the BUSY output using the trailing edge of the BUSY pulse is 2 TTL loads.

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm 15V$ and must not be reversed. The digital logic supply V_L is connected to $+5V$.

It is suggested that a parallel combination of a $0.1\mu F$ ceramic and a $6.8\mu F$ electrolytic capacitor is placed from each of the three supply pins to GND.

The pin marked CASE is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin 1 through to Pin 12 for the SDC/RDC1741/1742 and Pin 1 through to Pin 14 for the SDC/RDC1740 where Pin 1 is the MSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$

$$E_{S3-S2} = E_{RLO-RHI} \sin \omega t \sin (\theta + 120^\circ)$$

$$E_{S2-S1} = E_{RLO-RHI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \sin \omega t \sin \theta$$

$$E_{S2-S4} = E_{RHI-RLO} \sin \omega t \cos \theta$$

The BUSY, $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins should be connected as described under the heading Data Transfer.

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any change of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

Note: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling.

To calculate the values of the external scaling resistors in the case of a synchro converter, add $1.11k\Omega$ per extra volt of signal in series with S1, S2 and S3 and $1k\Omega$ per extra volt of reference

in series with RHI. In the case of a resolver-to-digital converter, add $2.22k\Omega$ in series with S1 and S2 per extra volt of signal and $1k\Omega$ per extra volt of reference in series with RHI.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

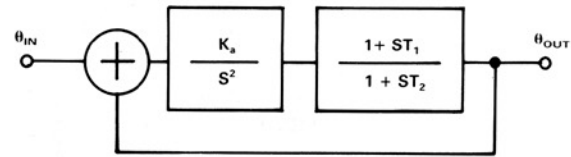


Figure 3. Transfer Function of SDC/RDC1740/1741/1742

Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_a} + \frac{s^3 T_2}{K_a}}$$

Model SDC/RDC1740

Where $K_a = 56,000$

$T_1 = 0.01$

$T_2 = 0.001525$

The gain and phase diagrams are shown in Figures 4 and 5.

Model SDC/RDC1741/1742

Where $K_a = 80,000$

$T_1 = 0.0087$

$T_2 = 0.001569$

The gain and phase diagrams are shown in Figures 6 and 7.

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input Acceleration}}{\text{Error in Output Angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration, only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure. The following is an example using the K_a of the SDC1740.

Acceleration of 50 revolutions sec^{-2} with $K_a = 56000$

$$\text{Error in LSBs} = \frac{50 \times 16384}{56000} = 14.62 \text{ LSBs}$$

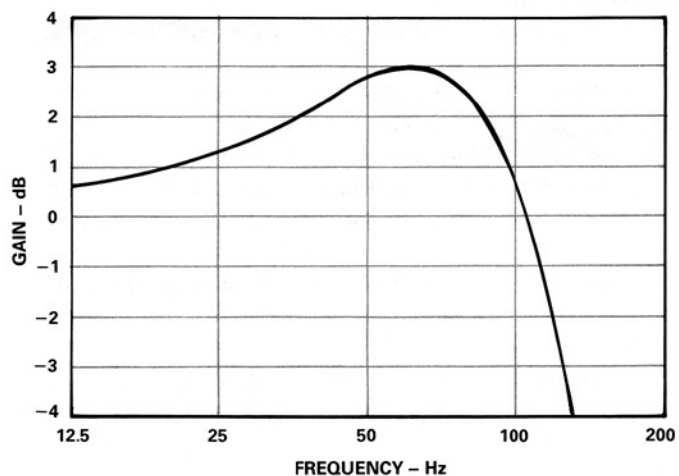


Figure 4. SDC/RDC1740 Gain Plot

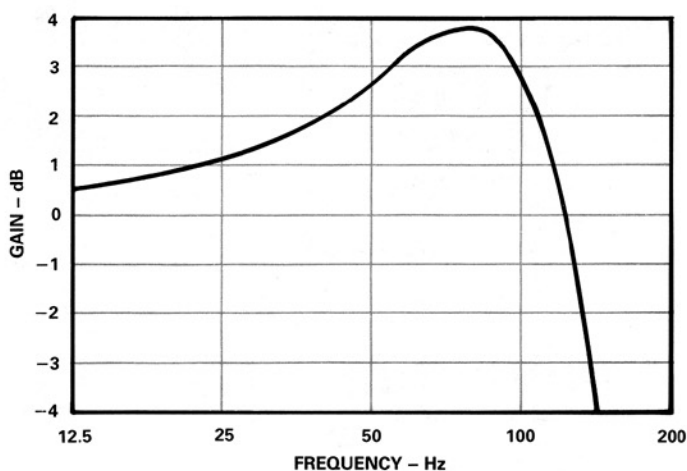


Figure 6. SDC/RDC1741/1742 Gain Plot

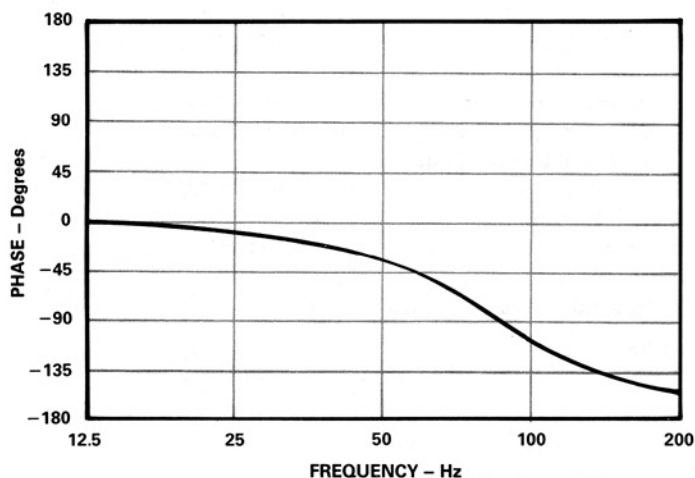


Figure 5. SDC/RDC1740 Phase Plot

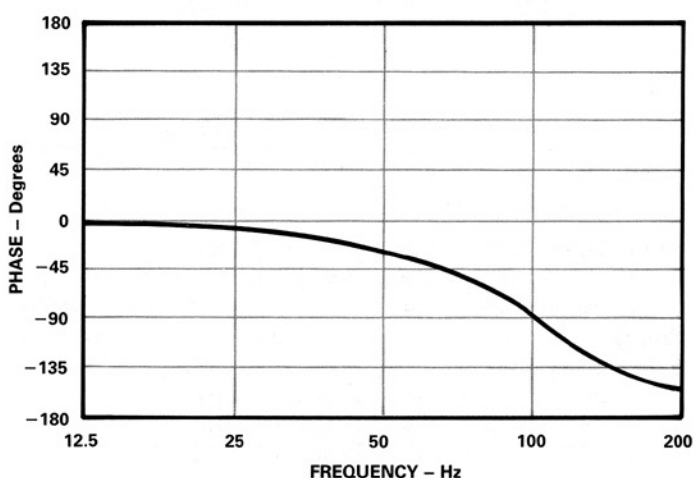


Figure 7. SDC/RDC1741/1742 Phase Plot

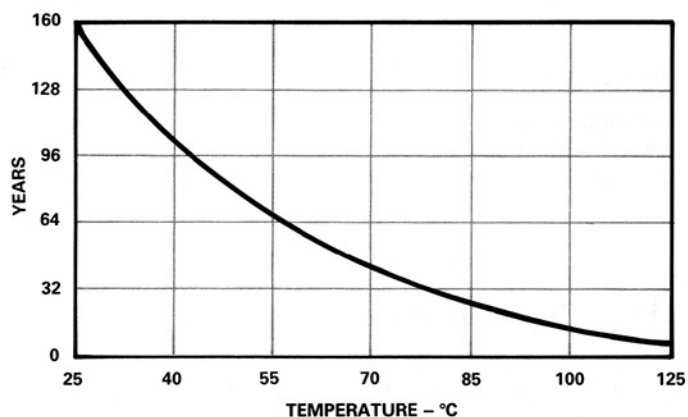


Figure 8. SDC/RDC1740/41/42 MTBF Curve

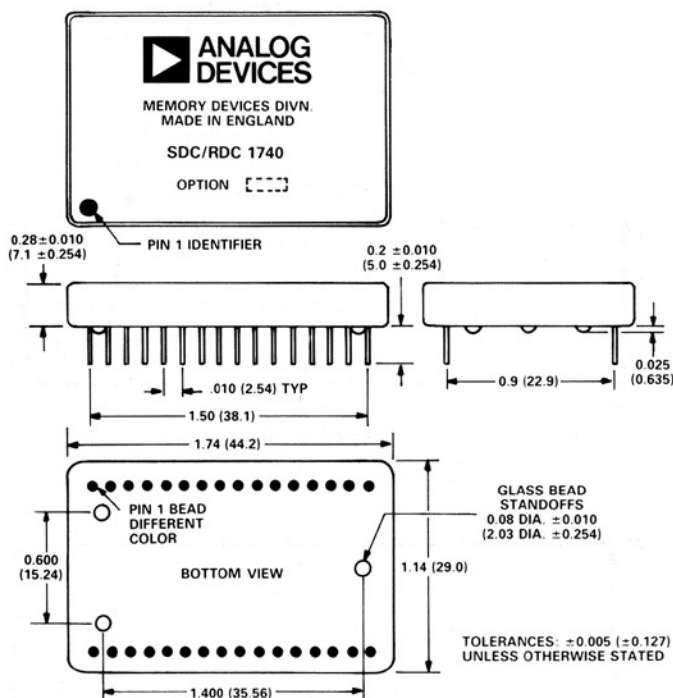
RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217E, Figure 8 shows the MTBF in years versus case temperature in naval sheltered conditions for SDC/RDC1740/41/42.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



STANDARD PROCESSING (5YZ OPTION)

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	In-house criteria
3. Seal Test, Fine and Gross	In-house criteria
4. Final Electrical Test	Performed at +25°C
Extended temperature range versions receive additional processing as follows:	
Final Electrical Test	Performed at max and min operating temperatures

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The SDC/RDC1767 and SDC/RDC1768 are hybrid synchro-to-digital converters with isolating microtransformers similar to the SDC/RDC1740/41/42 described on this data sheet with the additional features of analog velocity output and dc error output.

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over a frequency range of 0 to 10kHz.

The DRC1745 and DRC1746 are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins, and the outputs can supply 2VA at 7V rms.

PROCESSING FOR HIGH RELIABILITY

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	2017
3. Temperature Cycling	10 Cycles, -65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 hours @ +125°C
7. Seal Test, Fine and Gross	1014
8. Final Electrical Testing (Group A)	Performed at T _{min} , T _{ambient} and T _{max}
9. External Visual Inspection	2009

NOTE

Test and screening data can be supplied. Further information on request.