ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, CB_ .....-0.3V to +6.0V
COM_, NC_, NO_ .....-0.3V to (V_{CC} + 0.3V)
Continuous Current NO_, NC_, COM_ .....±300mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 50% duty cycle).....±400mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 10% duty cycle).....±500mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (3mm x 3mm), Single-Layer Board
(derate 15.6mW/°C above +70°C).....1250mW
16-Pin TQFN (3mm x 3mm), Multilayer Board (derate
20.8mW/°C above +70°C) 1667mW
16-Pin Ultra-Thin QFN (2.5mm x 2.5mm), MultiLayer
Board (derate 11.5mW/°C above +70°C) 923.8mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = +3.3V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{CC}			1.6		5.5	V
Supply Current	I_{CC}	V_{CC} = +5.5V, $V_{CB\_}$ = 0V or V_{CC}			0.3	1	µA
		V_{CC} = +5.5V, $V_{CB\_}$ = 0.5V or +1.6V			0.3	5	
		V_{CC} = +2.5V, $V_{CB\_}$ = 0.5V or +1.4V			0.1		
ANALOG SWITCH							
Analog Signal Range	$V_{NC\_}$, $V_{NO\_}$, $V_{COM\_}$,	(Note 2)		0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 3.3V, $I_{COM\_}$ = 100mA; CB_ = low or high	T_A = +25°C		0.61	0.90	Ω
			T_A = T_{MIN} to T_{MAX}			1	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 3.3V, $V_{NC\_}$ or $V_{NO\_}$ = 0.875V; $I_{COM\_}$ = 100mA (Note 3)	T_A = +25°C		0.06		Ω
			T_A = T_{MIN} to T_{MAX}			0.1	
On-Resistance Flatness	$R_{FLAT(NO)}$	V_{CC} = 3.3V, $V_{COM\_}$ = 0 to V_{CC}; $I_{COM\_}$ = 100mA (Note 4)	T_A = +25°C		0.32	0.72	Ω
			T_A = T_{MIN} to T_{MAX}			0.87	
NO_, NC_ Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V_{CC} = 5.5V; $V_{NC\_}$ or $V_{NO\_}$ = 0.3V, 5.5V; $V_{COM\_}$ = 5.5V or 0.3V		-1	0.1	+1	µA
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V_{CC} = 5.5V, $V_{NC\_}$ or $V_{NO\_}$ = 0.3V, 5.5V, or unconnected; $V_{COM\_}$ = 0.3V, 5.5V, or unconnected		-1	0.1	+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 3.3V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	R_L = 32Ω, C_L = 35pF, Figure 2	For NO_, $V_{NO\_}$ = 1V		70		ns
			For NC_, $V_{NC\_}$ = 1V		210		
Turn-Off Time	t_{OFF}	R_L = 32Ω, C_L = 35pF, Figure 2	For NO_, $V_{NO\_}$ = 1V		210		ns
			For NC_, $V_{NC\_}$ = 1V		55		
Charge Injection	Q	$V_{GEN\_}$ = 0V; R_{GEN} = 0Ω; C_L = 1nF; Figure 3			200		pC
Off-Isolation	V_{ISO}	C_L = 5pF; R_L = 32Ω; f = 100kHz; $V_{COM\_}$ = $1V_{RMS}$; Figure 4 (Note 5)			-64		dB
Crosstalk	V_{CT}	C_L = 5pF; R_L = 32Ω; f = 100kHz; $V_{COM\_}$ = $1V_{RMS}$; Figure 4			-68		dB
Power-Supply Rejection Ratio	PSRR	f = 20kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF			-60		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V_{P-P} = 0.5V, R_L = 32Ω			0.08		%
NO_, NC_ Off-Capacitance	$C_{NC\_(OFF)}$, $C_{NO\_(OFF)}$	f = 1MHz, Figure 5			40		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 5			150		pF
DIGITAL INPUTS (CB_)							
Input Logic-High	V_{IH}	V_{CC} = 1.6V to 2.7V		1.4			V
		V_{CC} = 2.7V to 5.5V		1.6			
Input Logic-Low	V_{IL}					0.5	V
Input Leakage Current	I_{IN}			-1	0.1	+1	µA

Note 1: For TQFN (3mm x 3mm) electrical specifications are production tested at T_A = +85°C and guaranteed by design at T_A = +25°C and -40°C. For Ultra-Thin QFN (2.5mm x 2.5mm) electrical specifications are production tested at T_A = +25°C and guaranteed by design at T_A = +85°C and -40°C.

Note 2: Signals on COM_, NO_, or NC_ exceeding V_{CC} are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 3: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

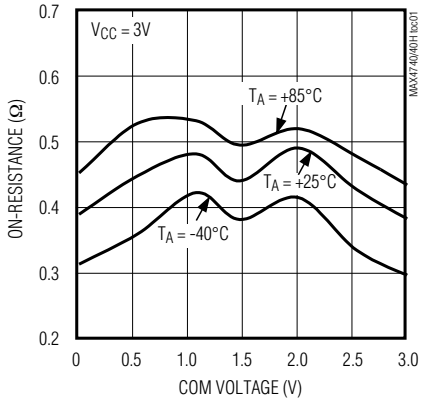
Note 5: Off-isolation = 20log10 [$V_{COM\_}$/ $V_{NO\_}$], $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.

Quad SPDT Audio Switches

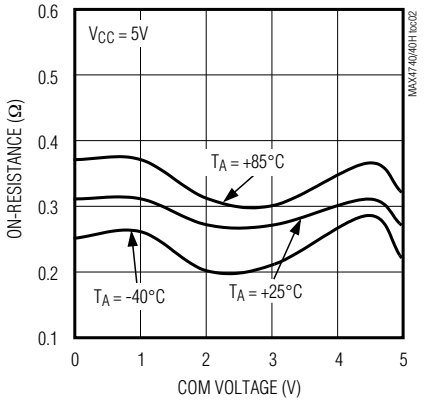
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted)

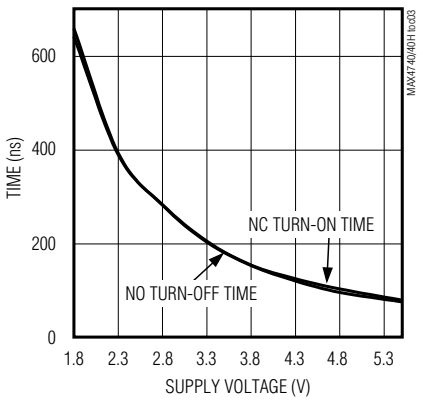
ON-RESISTANCE vs. COM VOLTAGE



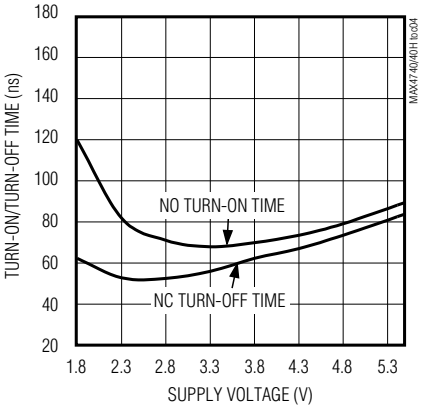
ON-RESISTANCE vs. COM VOLTAGE



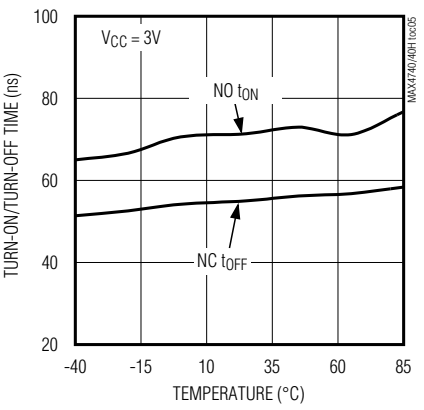
NC TURN-ON/NO TURN-OFF TIME vs. SUPPLY VOLTAGE



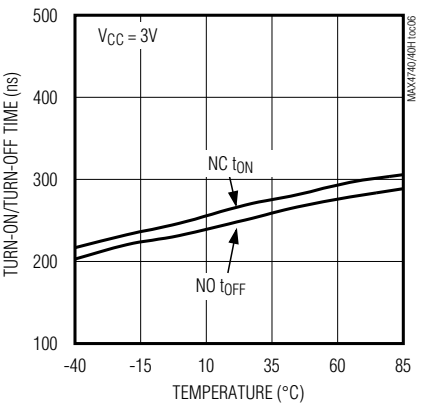
NO TURN-ON/NC TURN-OFF TIME vs. SUPPLY VOLTAGE



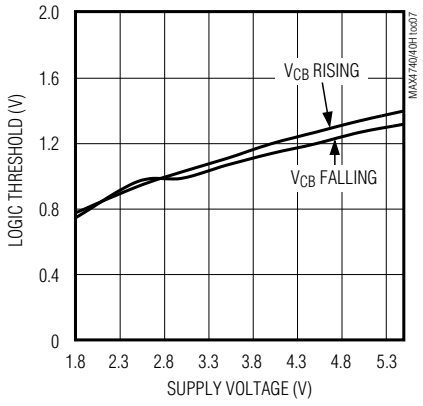
NO TURN-ON/NC TURN-OFF TIME vs. TEMPERATURE



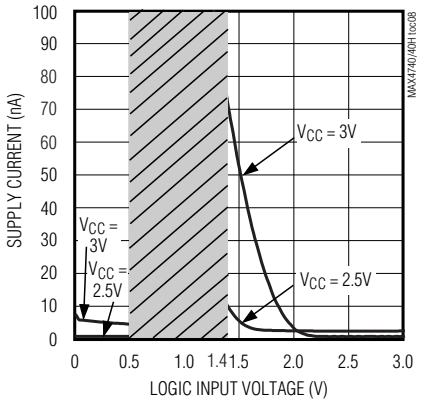
NC TURN-ON/NO TURN-OFF TIME vs. TEMPERATURE



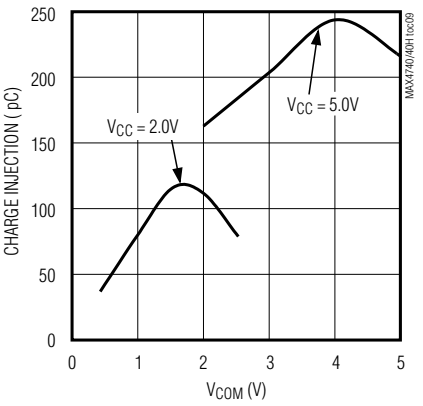
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



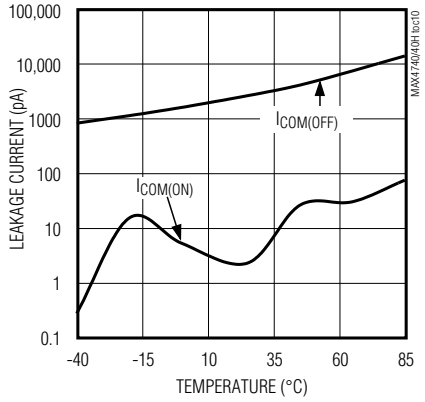
CHARGE INJECTION vs. COM VOLTAGE



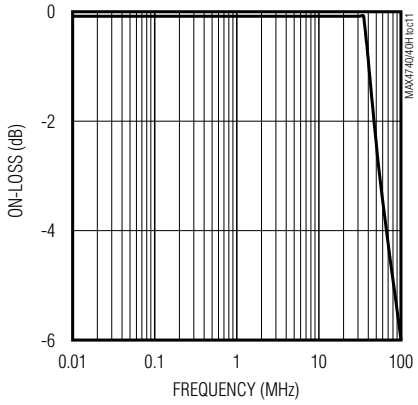
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted)

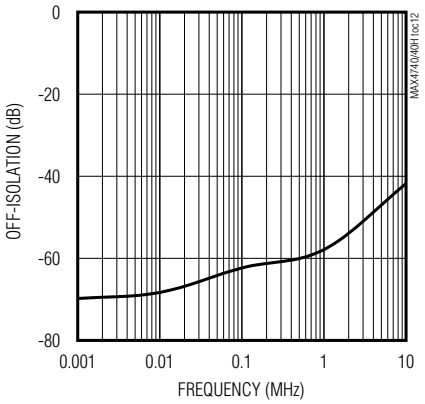
LEAKAGE CURRENT vs. TEMPERATURE



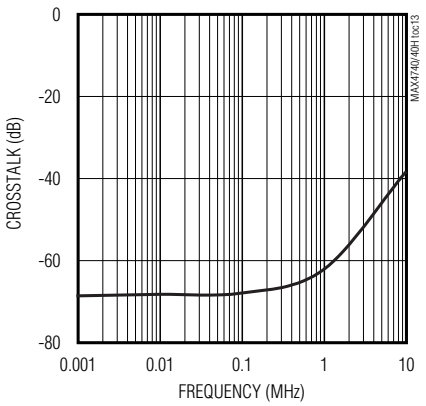
FREQUENCY RESPONSE



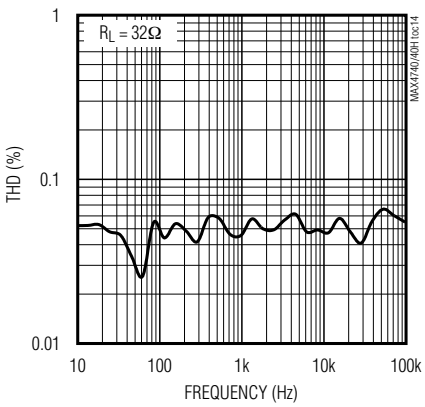
OFF-ISOLATION vs. FREQUENCY



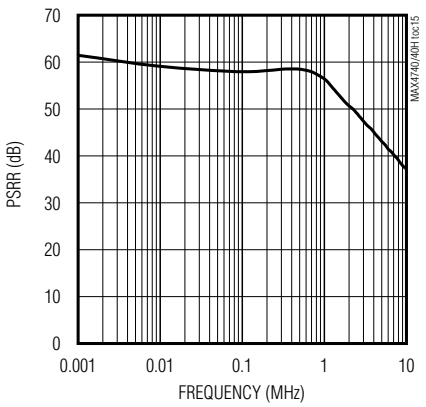
CROSSTALK vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



Quad SPDT Audio Switches

Pin Description

PIN	NAME	FUNCTION
1	NC1	Analog Switch 1—Normally Closed Terminal
2	CB1	Digital Control Input for Analog Switch 1 and Analog Switch 2
3	NO2	Analog Switch 2—Normally Open Terminal
4	COM2	Analog Switch 2—Common Terminal
5	NC2	Analog Switch 2—Normally Closed Terminal
6	GND	Ground
7	NO3	Analog Switch 3—Normally Open Terminal
8	COM3	Analog Switch 3—Common Terminal
9	NC3	Analog Switch 3—Normally Closed Terminal
10	CB2	Digital Control Input for Analog Switch 3 and Analog Switch 4
11	NO4	Analog Switch 4—Normally Open Terminal
12	COM4	Analog Switch 4—Common Terminal
13	NC4	Analog Switch 4—Normally Closed Terminal
14	V_{CC}	Positive Supply Voltage
15	NO1	Analog Switch 1—Normally Open Terminal
16	COM1	Analog Switch 1—Common Terminal
EP	EP	Exposed Pad. Connect to GND or leave unconnected for normal operation.

Detailed Description

The MAX4740/MAX4740H quad SPDT audio switches are low on-resistance, low supply current, high power-supply rejection ratio (PSRR) devices that operate from a +1.6V to +5.5V single supply. The MAX4740/MAX4740H have two digital control inputs, CB1 and CB2, where each bit controls a pair of switches (see Tables 1 and 2).

Applications Information

The MAX4740/MAX4740H logic inputs accept up to +5.5V, regardless of supply voltage. For example with a +3.3V supply, CB1 and CB2 can be driven low to GND and high to +5.5V, allowing for mixed logic levels in a system. Driving CB1 and CB2 rail-to-rail minimizes power consumption. For a 3.3V supply voltage, the logic thresholds are +0.5V (low) and +1.6V (high).

Analog Signal Levels

Analog signals that range over the entire supply voltage range (V_{CC} to GND) can be passed with very little change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ terminals can be used as either inputs or outputs.

Table 1. MAX4740 Truth Table

CONTROL		SWITCH STATE	
CB2	CB1	Switch 3/4	Switch 1/2
0	0	COM = NC	COM = NC
0	1	COM = NC	COM = NO
1	0	COM = NO	COM = NC
1	1	COM = NO	COM = NO

Table 2. MAX4740H Truth Table

CONTROL		SWITCH STATE	
CB2	CB1	Switch 3/4	Switch 1/2
0	0	COM = NC	COM = NC
0	1	High-Z	High-Z
1	0	COM = NO	COM = NC
1	1	COM = NO	COM = NO

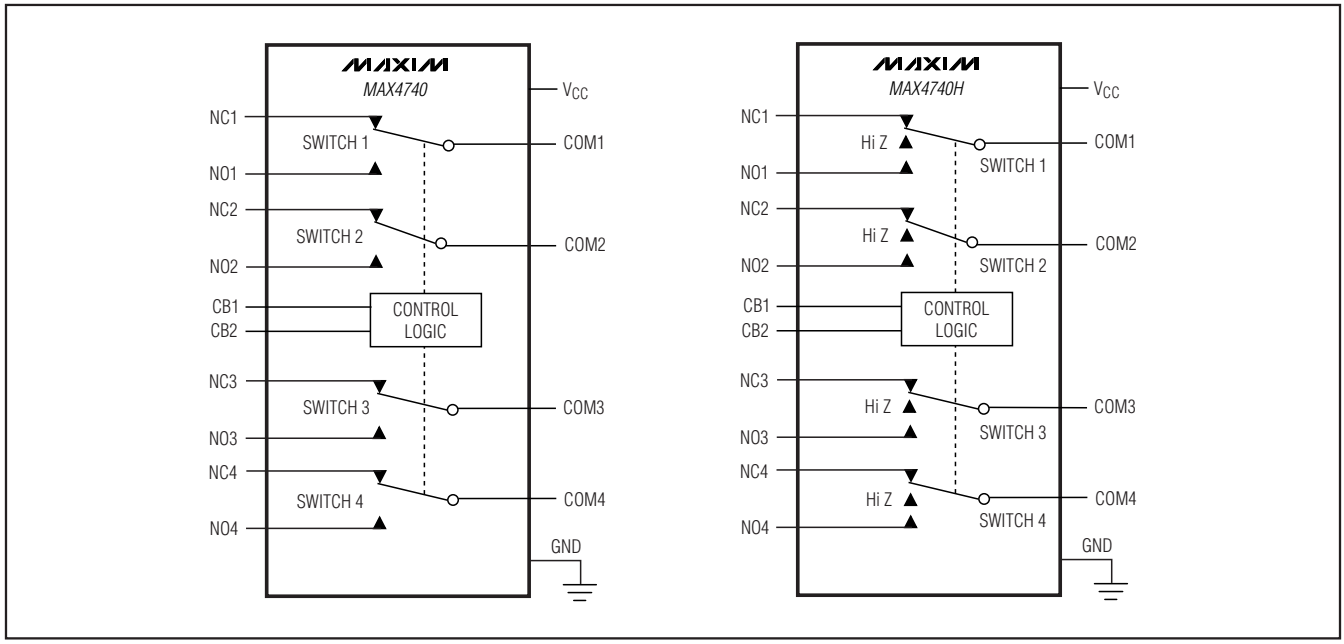


Figure 1. Functional Diagram

Test Circuits/Timing Diagrams

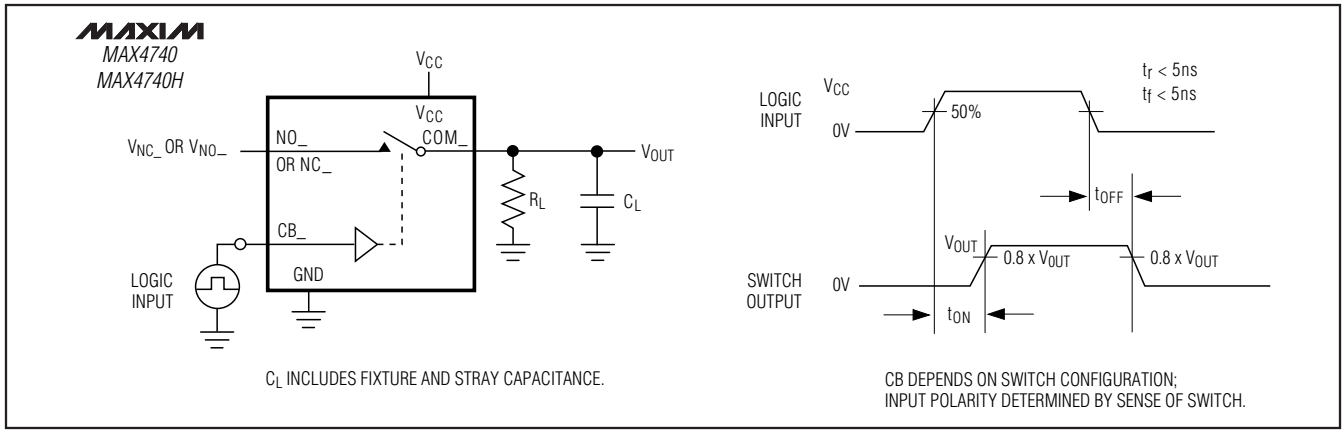


Figure 2. Switching Time

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the Absolute Maximum Ratings since stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Improper supply sequencing can force the switch into latch-up, causing it to draw excessive supply current. The only way out of latch-up is to recycle the power and reapply properly. Connect all ground pins first, then apply power to V_{CC} , and finally apply signals to NO_, NC_, and COM_. Follow the reverse order upon power-down.

Chip Information

PROCESS: BICMOS

Quad SPDT Audio Switches

Test Circuits/Timing Diagrams (continued)

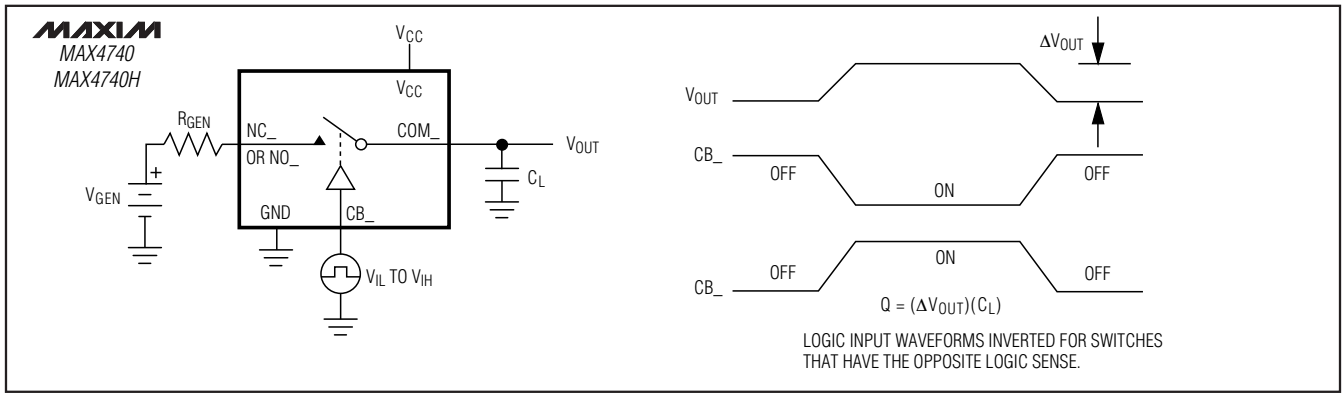


Figure 3. Charge injection

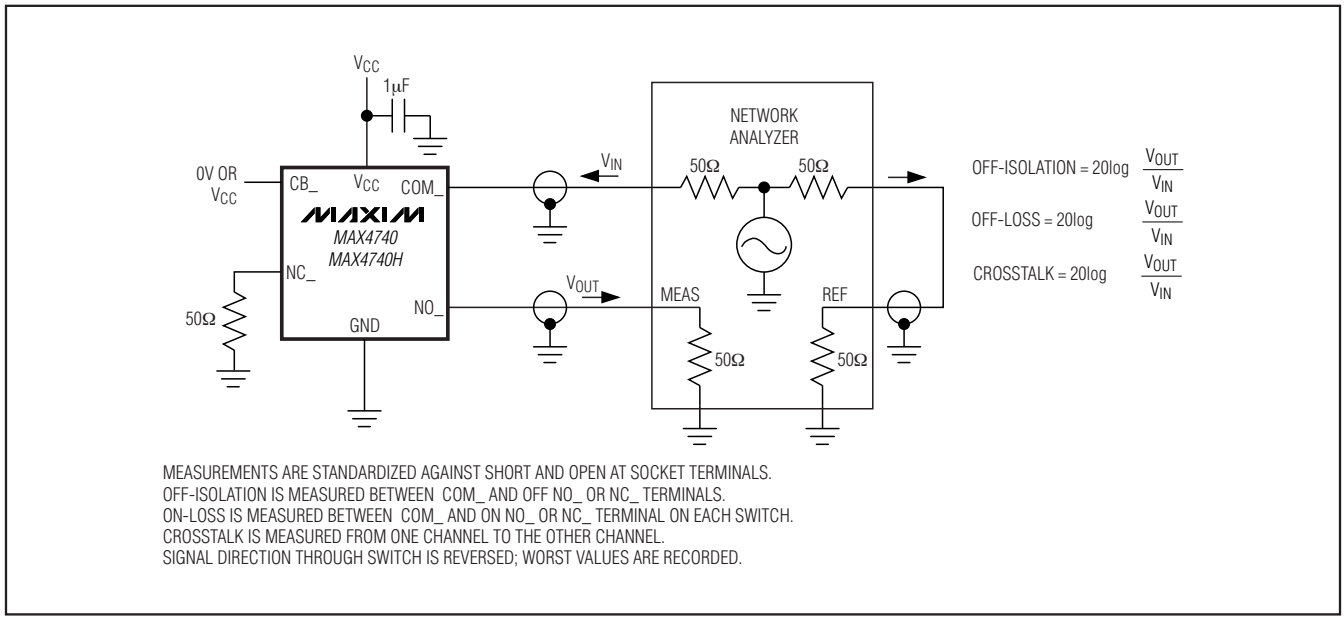


Figure 4. Off-Isolation, On-Loss, and Crosstalk

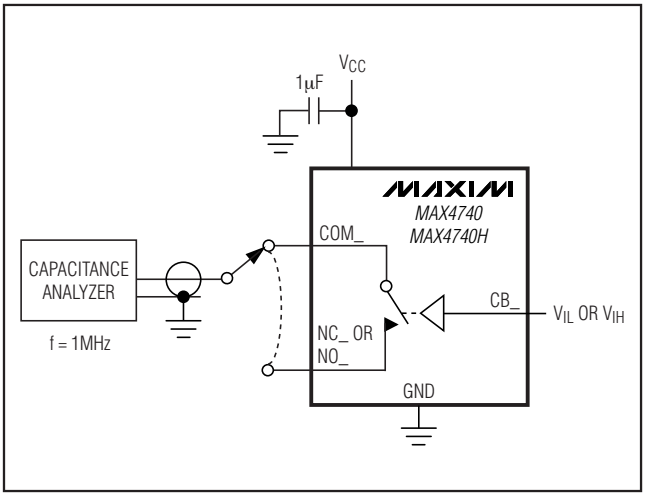


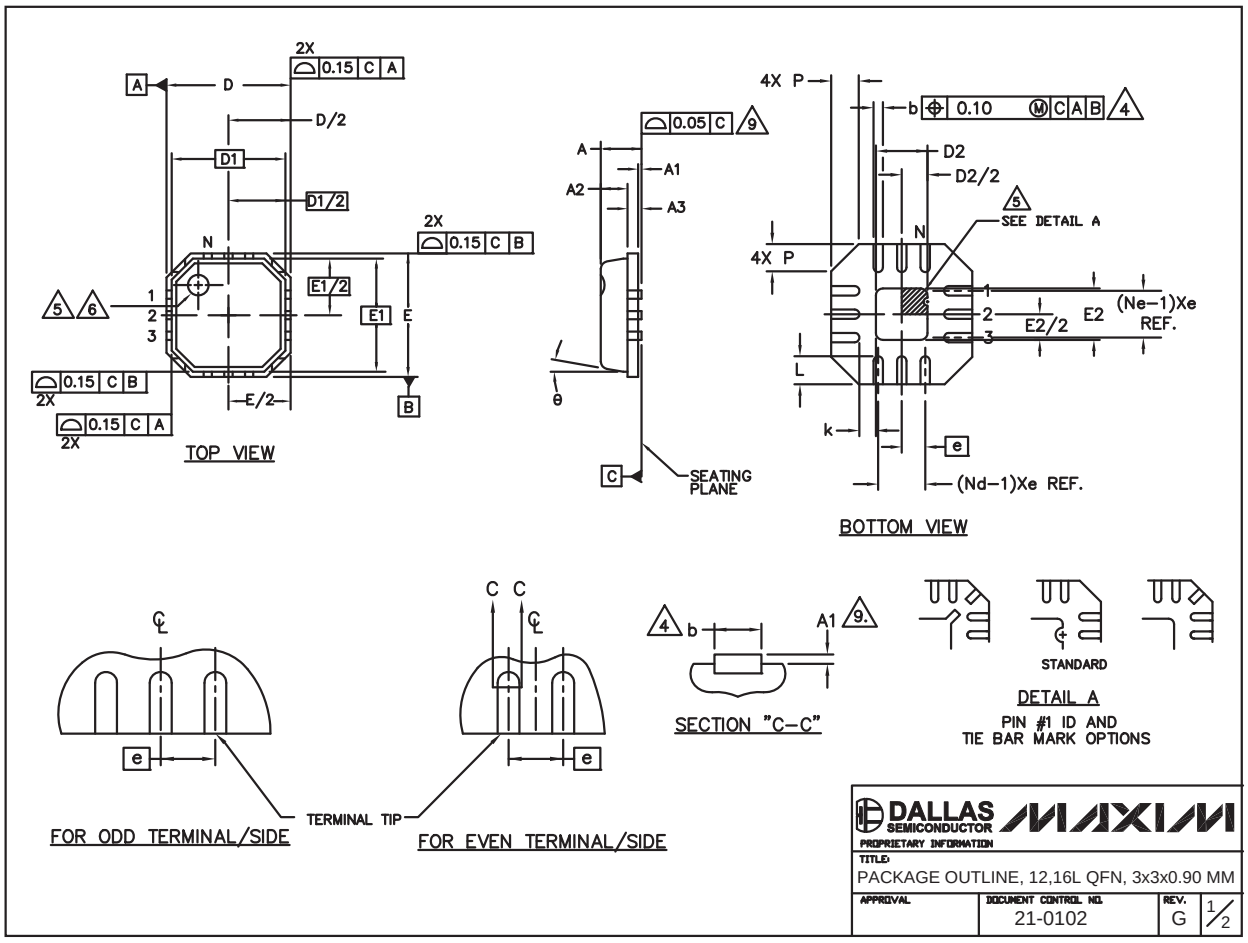
Figure 5. Channel Off/On-Capacitance

Quad SPDT Audio Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12, 16L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS						
PKG	12L 3x3			16L 3x3		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF		
b	0.18	0.23	0.30	0.18	0.23	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
D1	2.75 BSC			2.75 BSC		
E	2.90	3.00	3.10	2.90	3.00	3.10
E1	2.75 BSC			2.75 BSC		
e	0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
P	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1233-1	0.95	1.10	1.25	0.95	1.10	1.25
G1633-2	0.95	1.10	1.25	0.95	1.10	1.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

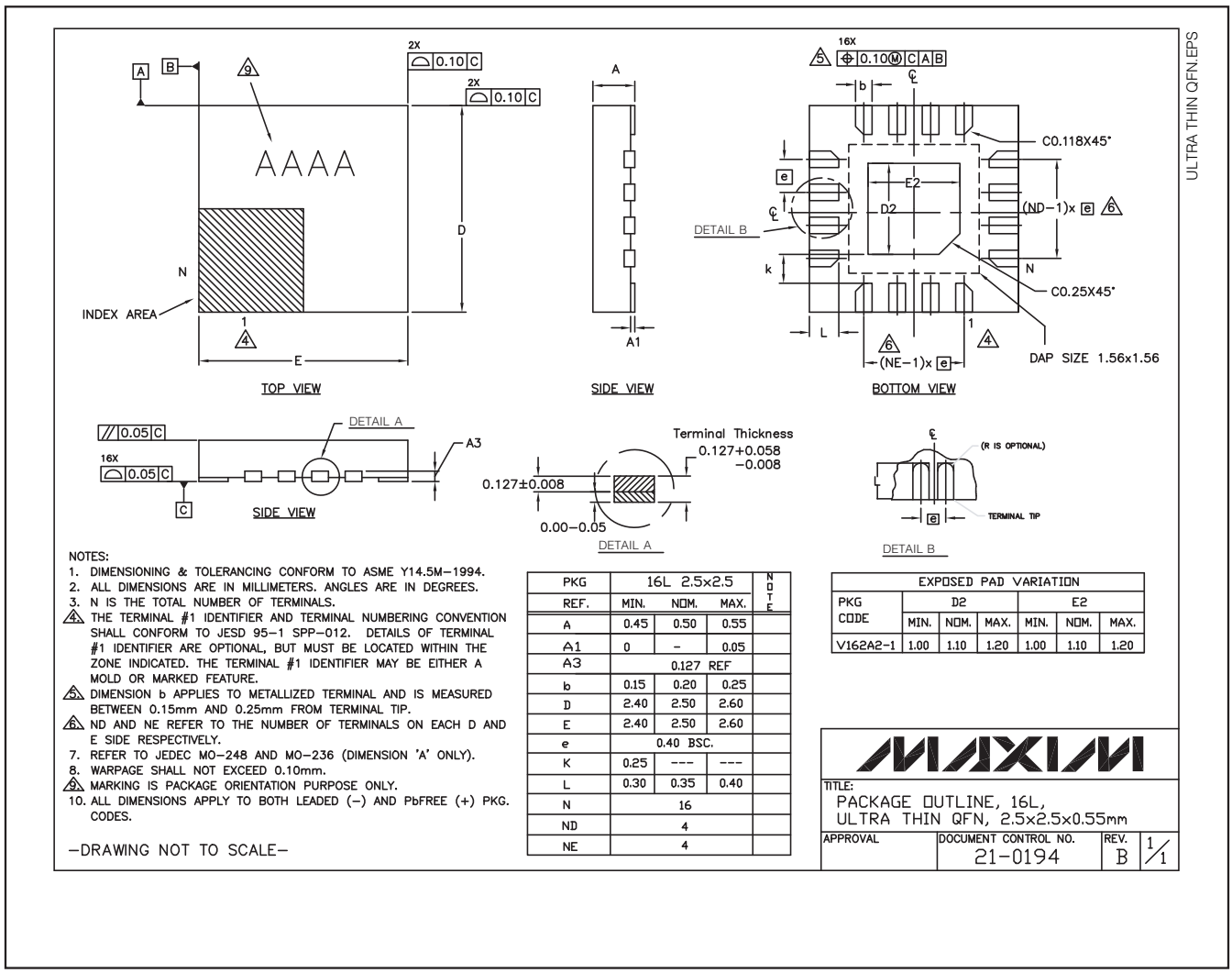
TITLE: PACKAGE OUTLINE, 12,16L QFN, 3x3x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0102	G	1/2

Quad SPDT Audio Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.25mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. REFER TO JEDEC MO-248 AND MO-236 (DIMENSION 'A' ONLY).
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS PACKAGE ORIENTATION PURPOSE ONLY.
10. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

PKG	16L 2.5x2.5			NOTE
REF.	MIN.	NOM.	MAX.	
A	0.45	0.50	0.55	
A1	0	-	0.05	
A3	0.127 REF			
b	0.15	0.20	0.25	
D	2.40	2.50	2.60	
E	2.40	2.50	2.60	
e	0.40 BSC.			
K	0.25	---	---	
L	0.30	0.35	0.40	
N	16			
ND	4			
NE	4			

EXPOSED PAD VARIATION						
PKG CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
V162A2-1	1.00	1.10	1.20	1.00	1.10	1.20

MAXIM

TITLE: PACKAGE OUTLINE, 16L, ULTRA THIN QFN, 2.5x2.5x0.55mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0194	B	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/06	Initial release	—
1	11/07	Adding ultra-thin QFN package	1, 2, 3, 10–13