

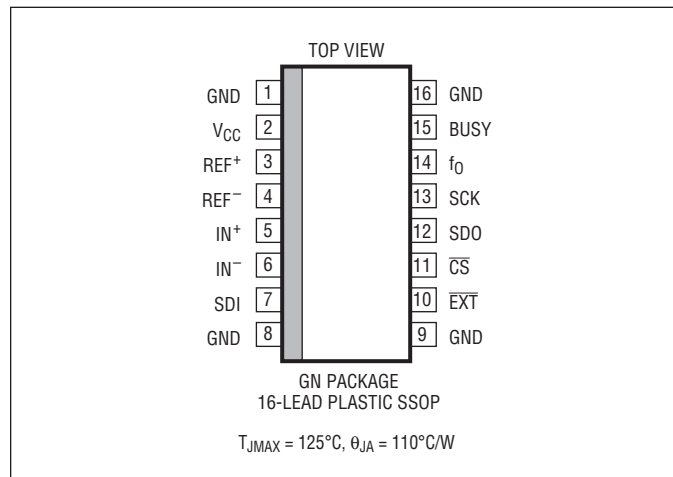
LTC2440

ABSOLUTE MAXIMUM RATINGS

(Notes 1,2)

Supply Voltage (V_{CC}) to GND	–0.3V to 6V
Analog Input Pins Voltage to GND	–0.3V to ($V_{CC} + 0.3V$)
Reference Input Pins Voltage to GND	–0.3V to ($V_{CC} + 0.3V$)
Digital Input Voltage to GND	–0.3V to ($V_{CC} + 0.3V$)
Digital Output Voltage to GND	–0.3V to ($V_{CC} + 0.3V$)
Operating Temperature Range	
LTC2440C	0°C to 70°C
LTC2440I	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



ORDER INFORMATION <http://www.linear.com/product/LTC2440#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2440CGN#PBF	LTC2440CGN#TRPBF	2440	Narrow 16-Lead SSOP	0°C to 70°C
LTC2440IGN#PBF	LTC2440IGN#TRPBF	2440I	Narrow 16-Lead SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	$0.1V \leq V_{REF} \leq V_{CC}$, $-0.5 \cdot V_{REF} \leq V_{IN} \leq 0.5 \cdot V_{REF}$ (Note 5)	●	24		Bits
Integral Nonlinearity	$V_{CC} = 5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$, (Note 6) $REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$, (Note 6)	●	5 3	15	ppm of V_{REF} ppm of V_{REF}
Offset Error	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$ (Note 12)	●	2.5	5	μV
Offset Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$		20		nV/°C
Positive Full-Scale Error	$REF^+ = 5V$, $REF^- = GND$, $IN^+ = 3.75V$, $IN^- = 1.25V$ $REF^+ = 2.5V$, $REF^- = GND$, $IN^+ = 1.875V$, $IN^- = 0.625V$	● ●	10 10	30 50	ppm of V_{REF} ppm of V_{REF}
Positive Full-Scale Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.75REF^+$, $IN^- = 0.25 \cdot REF^+$		0.2		ppm of $V_{REF}/^\circ\text{C}$
Negative Full-Scale Error	$REF^+ = 5V$, $REF^- = GND$, $IN^+ = 1.25V$, $IN^- = 3.75V$ $REF^+ = 2.5V$, $REF^- = GND$, $IN^+ = 0.625V$, $IN^- = 1.875V$	● ●	10 10	30 50	ppm of V_{REF} ppm of V_{REF}
Negative Full-Scale Error Drift	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.25 \cdot REF^+$, $IN^- = 0.75 \cdot REF^+$		0.2		ppm of $V_{REF}/^\circ\text{C}$
Total Unadjusted Error	$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$ $5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$ $REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$, (Note 6)		15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Input Common Mode Rejection DC	$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$		120		dB

2440fe

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN ⁺	Absolute/Common Mode IN ⁺ Voltage		●	GND – 0.3V		V _{CC} + 0.3V	V
IN [–]	Absolute/Common Mode IN [–] Voltage		●	GND – 0.3V		V _{CC} + 0.3V	V
V _{IN}	Input Differential Voltage Range (IN ⁺ – IN [–])		●	–V _{REF} /2		V _{REF} /2	V
REF ⁺	Absolute/Common Mode REF ⁺ Voltage		●	0.1		V _{CC}	V
REF [–]	Absolute/Common Mode REF [–] Voltage		●	GND		V _{CC} – 0.1V	V
V _{REF}	Reference Differential Voltage Range (REF ⁺ – REF [–])		●	0.1		V _{CC}	V
C _{S(IN⁺)}	IN ⁺ Sampling Capacitance				3.5		pF
C _{S(IN[–])}	IN [–] Sampling Capacitance				3.5		pF
C _{S(REF⁺)}	REF ⁺ Sampling Capacitance				3.5		pF
C _{S(REF[–])}	REF [–] Sampling Capacitance				3.5		pF
I _{DC_LEAK(IN⁺, IN[–], REF⁺, REF[–])}	Leakage Current, Inputs and Reference	C _S = V _{CC} , IN ⁺ = GND, IN [–] = GND, REF ⁺ = 5V, REF [–] = GND	●	–100	10	100	nA
I _{SAMPLE(IN⁺, IN[–], REF⁺, REF[–])}	Average Input/Reference Current During Sampling			Varies, See Applications Section			

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	High Level Input Voltage \overline{CS} , f_0 , SDI	$4.5V \leq V_{CC} \leq 5.5V$	●	2.5		V
V_{IL}	Low Level Input Voltage \overline{CS} , f_0 , SDI	$4.5V \leq V_{CC} \leq 5.5V$	●		0.8	V
V_{IN}	High Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●	2.5		V
V_{IL}	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 8)	●		0.8	V
I_{IN}	Digital Input Current \overline{CS} , f_0	$0V \leq V_{IN} \leq V_{CC}$	●	-10	10	μA
I_{IN}	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 8)	●	-10	10	μA
C_{IN}	Digital Input Capacitance \overline{CS} , f_0			10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)		10		pF
V_{OH}	High Level Output Voltage SDO, BUSY	$I_O = -800\mu A$	●	$V_{CC} - 0.5V$		V
V_{OL}	Low Level Output Voltage SDO, BUSY	$I_O = 1.6mA$	●		0.4	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800\mu A$ (Note 9)	●	$V_{CC} - 0.5V$		V
V_{OL}	Low Level Output Voltage SCK	$I_O = 1.6mA$ (Note 9)	●		0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	-10	10	μA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		● 4.5		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	$\overline{CS} = 0V$ (Note 7) $\overline{CS} = V_{CC}$ (Note 7)	●	8 8	11 30	mA μA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	●	0.1		12	MHz
t_{HEO}	External Oscillator High Period	●	25		10000	ns
t_{LEO}	External Oscillator Low Period	●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 (SDI = 0) OSR = 32768 (SDI = 1) External Oscillator (Note 10, 13)	● ● ●	0.99 126 $\frac{40 \cdot OSR + 178}{f_{EOSC}(\text{kHz})}$	1.13 145 1.33 170	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9) External Oscillator (Notes 9, 10)	●	0.8 $f_{EOSC}/10$	1	MHz Hz
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45	55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●		20	MHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	25		ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25		ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	●	30.9 35.3 $320/f_{EOSC}$	41.6	μs s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●	$32/f_{ESCK}$		s
t_1	$\overline{CS} \downarrow$ to SDO Low Z	(Note 12)	●	0	25	ns
t_2	$\overline{CS} \uparrow$ to SDO High Z	(Note 12)	●	0	25	ns
t_3	$\overline{CS} \downarrow$ to SCK \downarrow	(Note 9)	●	5		μs
t_4	$\overline{CS} \downarrow$ to SCK \uparrow	(Notes 8, 12)	●	25		ns
t_{KQMAX}	SCK \downarrow to SDO Valid		●		25	ns
t_{KQMIN}	SDO Hold After SCK \downarrow	(Note 5)	●	15		ns
t_5	SCK Set-Up Before $\overline{CS} \downarrow$		●	50		ns
t_7	SDI Setup Before SCK \uparrow	(Note 5)	●	10		ns
t_8	SDI Hold After SCK \uparrow	(Note 5)	●	10		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: $V_{CC} = 4.5$ to $5.5V$ unless otherwise specified.

$V_{REF} = REF^+ - REF^-$, $V_{REFCM} = (REF^+ + REF^-)/2$;

$V_{IN} = IN^+ - IN^-$, $V_{INCM} = (IN^+ + IN^-)/2$.

Note 4: f_0 pin tied to GND or to external conversion clock source with $f_{EOSC} = 10\text{MHz}$ unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of $C_{LOAD} = 20\text{pF}$.

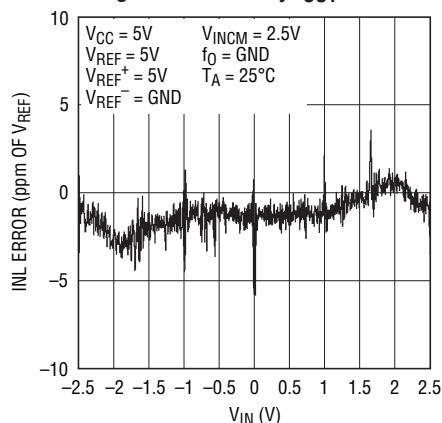
Note 10: The external oscillator is connected to the f_0 pin. The external oscillator frequency, f_{EOSC} , is expressed in kHz.

Note 11: The converter uses the internal oscillator. $f_0 = 0V$.

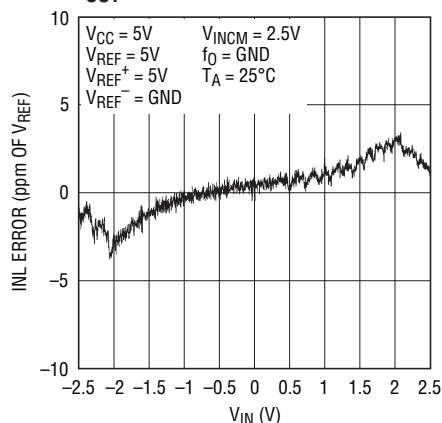
Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional 5 to 15 f_0 cycles to the conversion time.

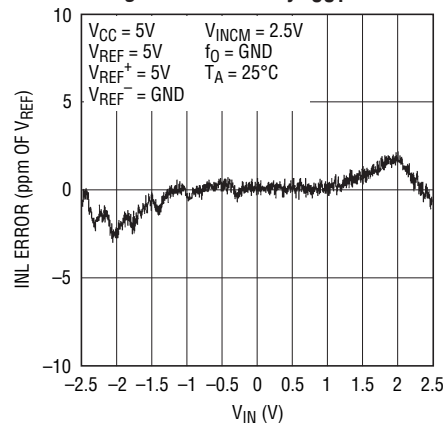
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity $f_{OUT} = 3.5\text{kHz}$ 

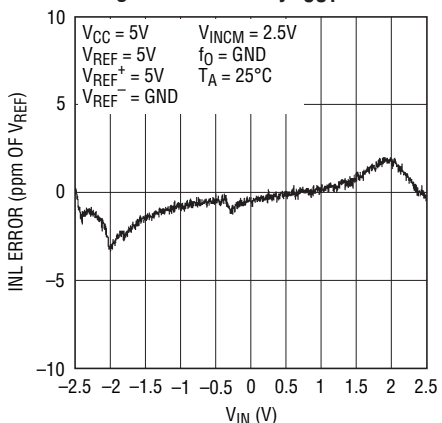
2440 G01

Integral Nonlinearity
 $f_{OUT} = 1.76\text{kHz}$ 

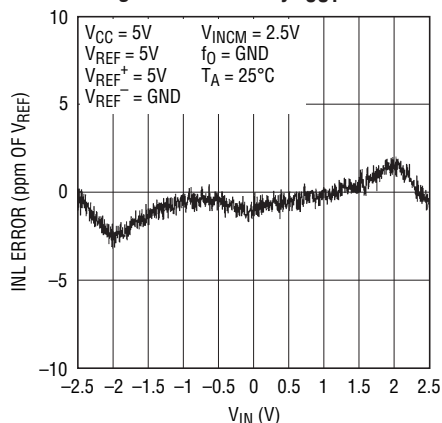
2440 G02

Integral Nonlinearity $f_{OUT} = 880\text{Hz}$ 

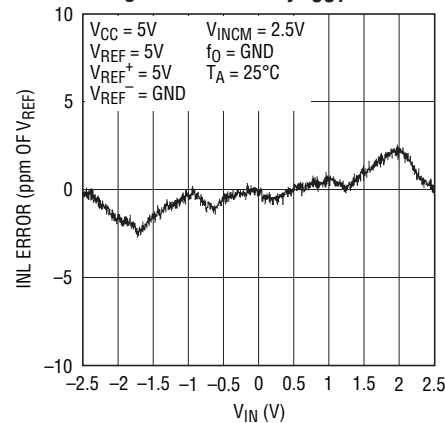
2440 G03

Integral Nonlinearity $f_{OUT} = 440\text{Hz}$ 

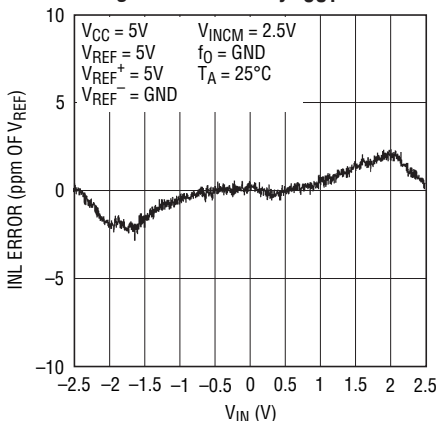
2440 G04

Integral Nonlinearity $f_{OUT} = 220\text{Hz}$ 

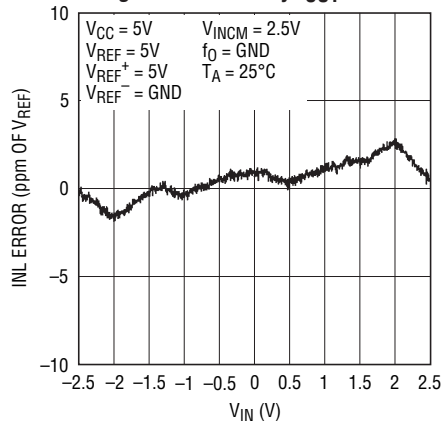
2440 G05

Integral Nonlinearity $f_{OUT} = 110\text{Hz}$ 

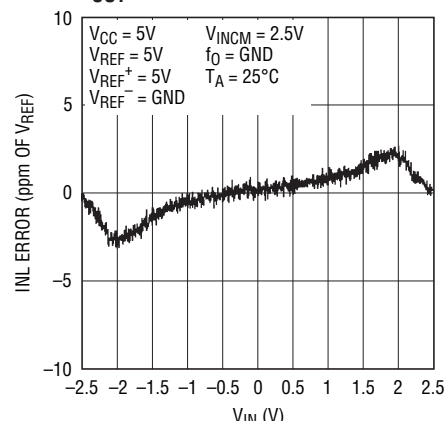
2440 G06

Integral Nonlinearity $f_{OUT} = 55\text{Hz}$ 

2440 G07

Integral Nonlinearity $f_{OUT} = 27.5\text{Hz}$ 

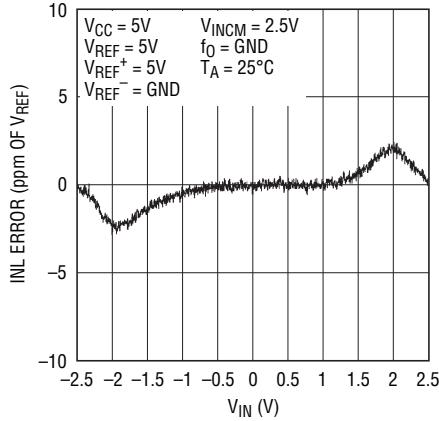
2440 G08

Integral Nonlinearity
 $f_{OUT} = 13.75\text{Hz}$ 

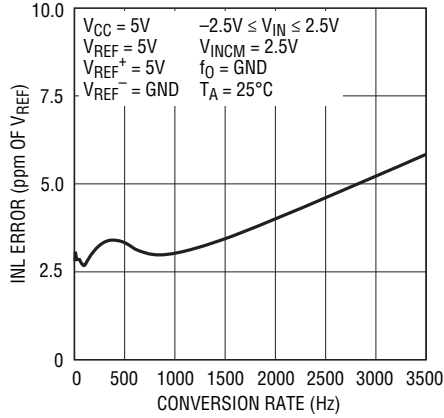
2440 G09

2440fe

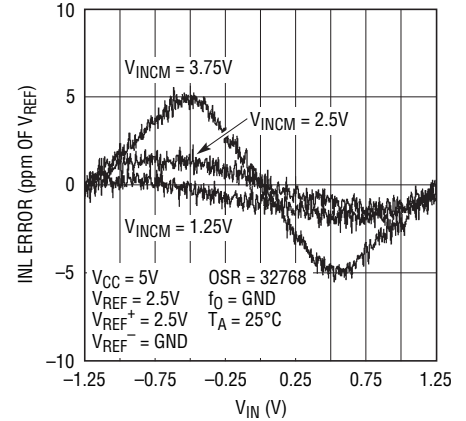
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity
 $f_{OUT} = 6.875\text{Hz}$


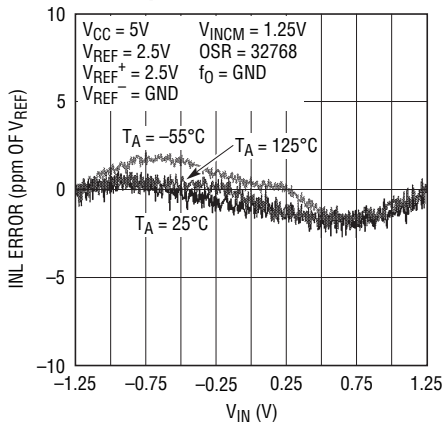
2440 G10

Integral Nonlinearity vs Conversion Rate


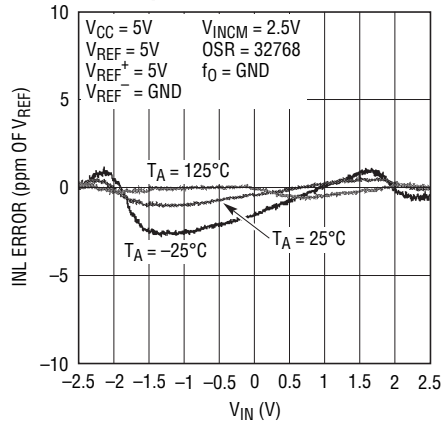
2440 G11

Integral Nonlinearity vs V_{INCM}


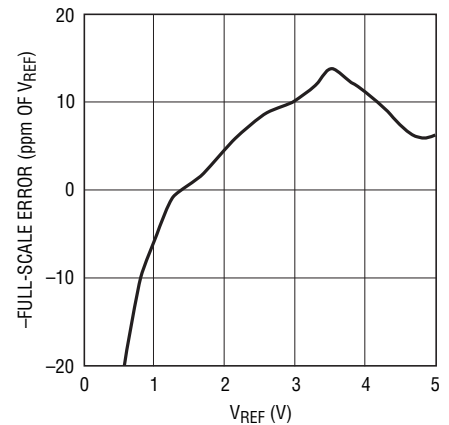
2440 G12

Integral Nonlinearity vs Temperature


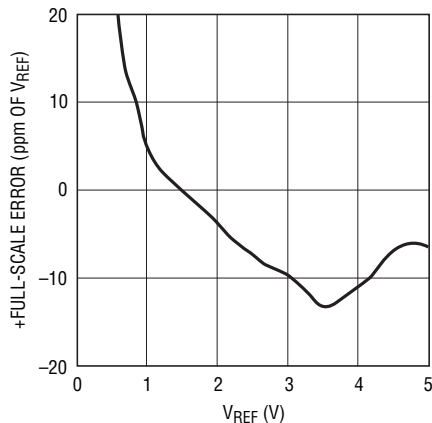
2440 G13

Integral Nonlinearity vs Temperature


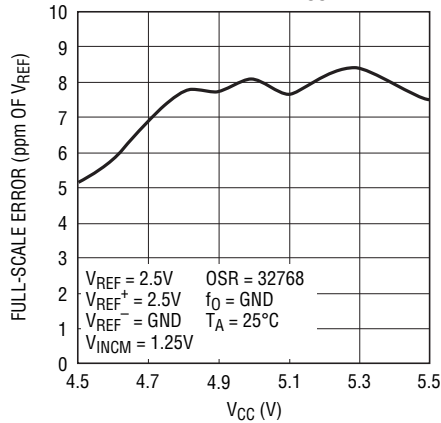
2440 G14

-Full-Scale Error vs V_{REF}


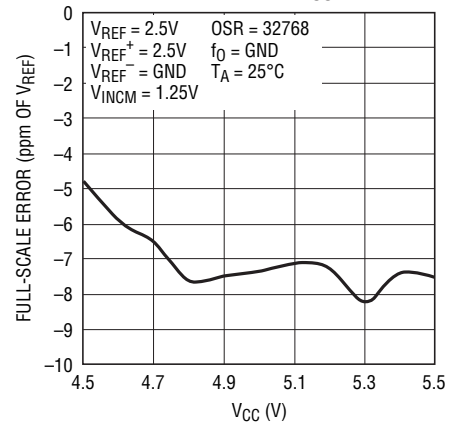
2440 G15

+Full-Scale Error vs V_{REF}


2440 G16

-Full-Scale Error vs V_{CC}


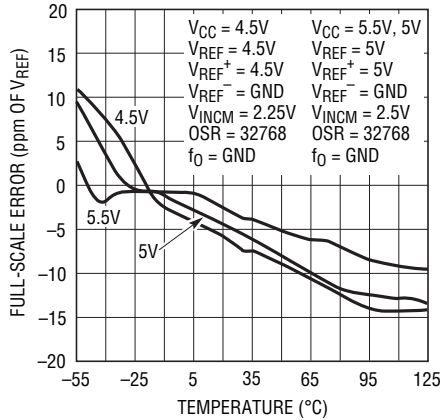
2440 G17

+Full-Scale Error vs V_{CC}


2440 G18

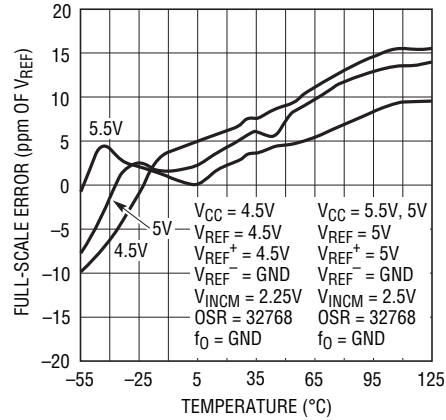
TYPICAL PERFORMANCE CHARACTERISTICS

Negative Full-Scale Error vs Temperature

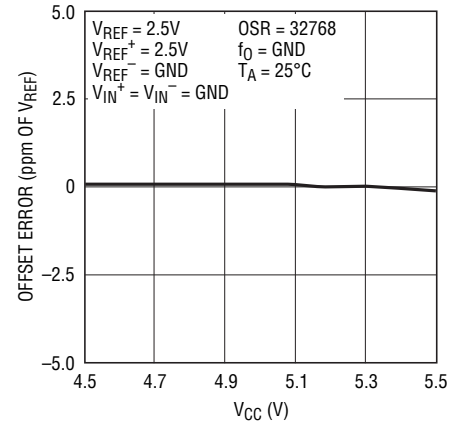


2440 G19

Positive Full-Scale Error vs Temperature

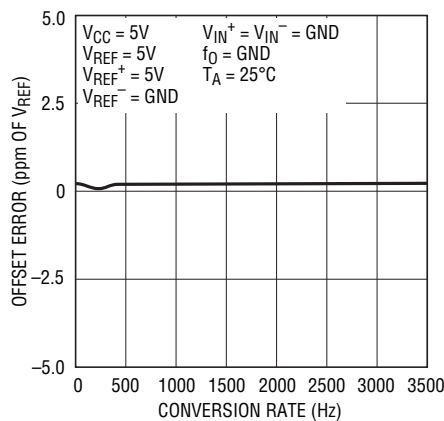


2440 G20

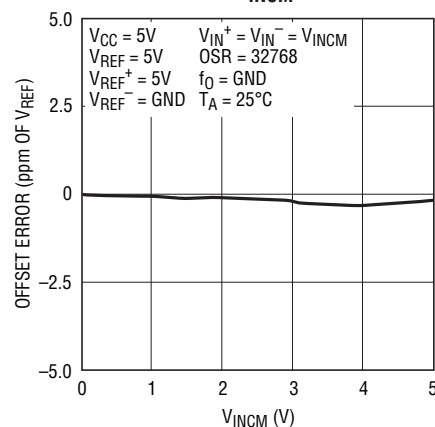
Offset Error vs V_{CC} 

2440 G21

Offset Error vs Conversion Rate

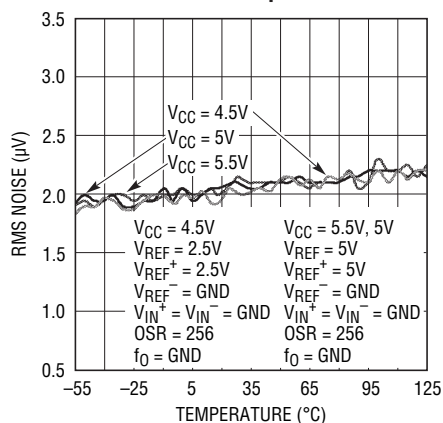


2440 G22

Offset Error vs V_{INCM} 

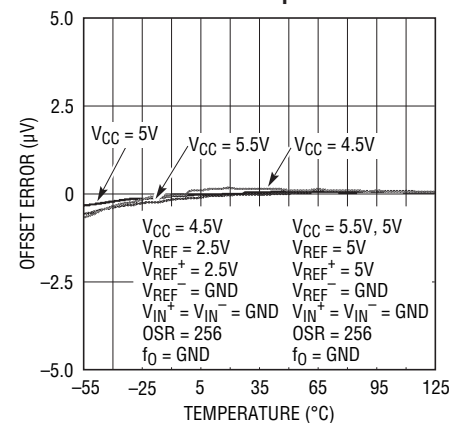
2440 G23

RMS Noise vs Temperature



2440 G24

Offset Error vs Temperature



2440 G25

PIN FUNCTIONS

GND (Pins 1, 8, 9, 16): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a ground plane through a low impedance connection. All four pins must be connected to ground for proper operation.

V_{CC} (Pin 2): Positive Supply Voltage. Bypass to GND (Pin 1) with a 10 μ F tantalum capacitor in parallel with 0.1 μ F ceramic capacitor as close to the part as possible.

REF⁺ (Pin 3), REF⁻ (Pin 4): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF⁺, is maintained more positive than the reference negative input, REF⁻, by at least 0.1V.

IN⁺ (Pin 5), IN⁻ (Pin 6): Differential Analog Input. The voltage on these pins can have any value between GND – 0.3V and V_{CC} + 0.3V. Within these limits the converter bipolar input range ($V_{IN} = IN^+ - IN^-$) extends from $-0.5 \cdot (V_{REF})$ to $0.5 \cdot (V_{REF})$. Outside this input range the converter produces unique overrange and underrange output codes.

SDI (Pin 7): Serial Data Input. This pin is used to select the speed/resolution of the converter. If SDI is grounded (pin compatible with LTC2410) the device outputs data at 880Hz with 21 bits effective resolution. By tying SDI HIGH, the converter enters the ultralow noise mode (200nV_{RMS}) with simultaneous 50/60Hz rejection at 6.9Hz output rate. SDI may be driven logic HIGH or LOW anytime during the conversion or sleep state in order to change the speed/resolution. The conversion immediately following the data output cycle will be valid and performed at the newly selected output rate/resolution. SDI may also be programmed by a serial input data stream under control of SCK during the data output cycle. One of ten speed/resolution ranges (from 6.9Hz/200nV_{RMS} to 3.5kHz/21 μ V_{RMS}) may be selected. The first conversion following a new selection is valid and performed at the newly selected speed/resolution.

EXT (Pin 10): Internal/External SCK Selection Pin. This pin is used to select internal or external SCK for outputting

data. If EXT is tied low (pin compatible with the LTC2410), the device is in the external SCK mode and data is shifted out the device under the control of a user applied serial clock. If EXT is tied high, the internal serial clock mode is selected. The device generates its own SCK signal and outputs this on the SCK pin. A framing signal BUSY (Pin 15) goes low indicating data is being output.

CS (Pin 11): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as CS is HIGH. A LOW-to-HIGH transition on CS during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 12): Three-State Digital Output. During the Data Output period, this pin is used as serial data output. When the chip select CS is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling \overline{CS} LOW.

SCK (Pin 13): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface clock during the Data Output period. The Serial Clock Operation mode is determined by the logic level applied to the EXT pin.

f₀ (Pin 14): Frequency Control Pin. Digital input that controls the internal conversion clock. When f₀ is connected to V_{CC} or GND, the converter uses its internal oscillator.

BUSY (Pin 15): Conversion in Progress Indicator. For compatibility with the LTC2410, this pin should not be tied to ground. This pin is HIGH while the conversion is in progress and goes LOW indicating the conversion is complete and data is ready. It remains low during the sleep and data output states. At the conclusion of the data output state, it goes HIGH indicating a new conversion has begun.

FUNCTIONAL BLOCK DIAGRAM

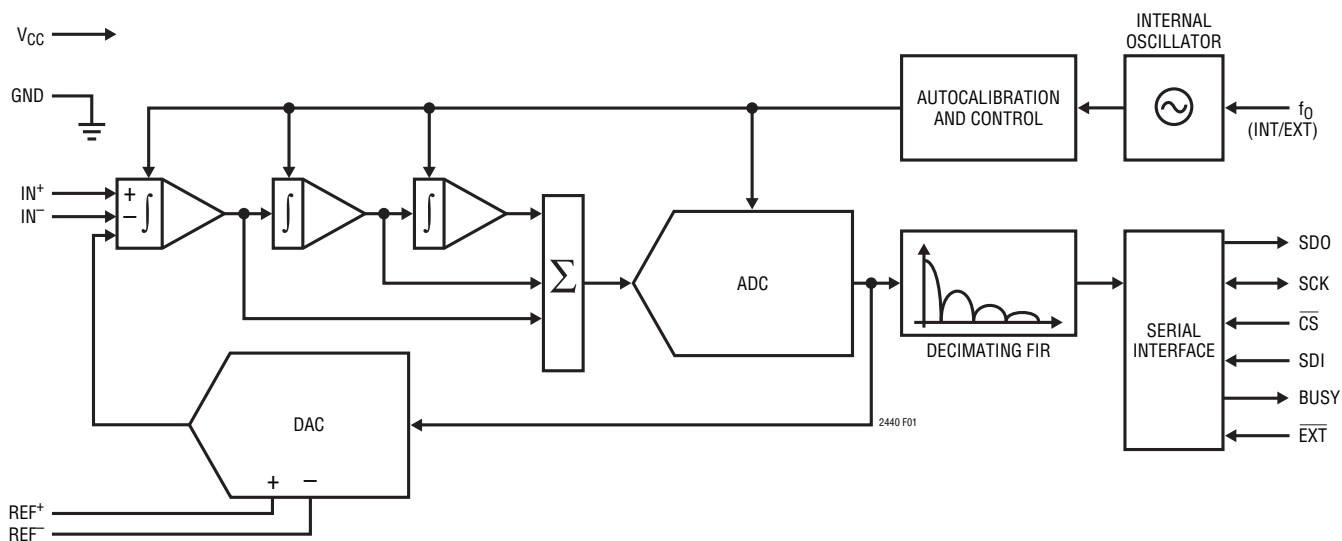


Figure 1. Functional Block Diagram

TEST CIRCUITS



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2440 is a high speed, delta-sigma analog-to-digital converter with an easy to use 4-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 2). The 4-wire interface consists of serial data input (SDI), serial data output (SDO), serial clock (SCK) and chip select (\overline{CS}). The interface, timing, operation cycle and data out format is compatible with the LTC2410.

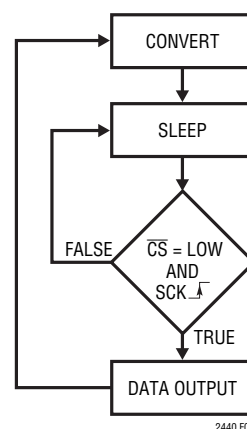


Figure 2. LTC2440 State Transition Diagram

APPLICATIONS INFORMATION

Initially, the LTC2440 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced below $10\mu\text{A}$. The part remains in the sleep state as long as $\overline{\text{CS}}$ is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{\text{CS}}$ is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32-bits are read out of the ADC or when $\overline{\text{CS}}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the $\overline{\text{CS}}$, SCK and $\overline{\text{EXT}}$ pins, the LTC2440 offers several flexible modes of operation (internal or external SCK). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Ease of Use

The LTC2440 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy. Speed/resolution adjustments may be made seamlessly between two conversions without settling errors.

The LTC2440 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2440 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection.

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2440 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (4.5V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF^+ and REF^- pins covers the entire range from GND to V_{CC} . For correct converter operation, the REF^+ pin must always be more positive than the REF^- pin.

The LTC2440 can accept a differential reference voltage from 0.1V to V_{CC} . The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the converter's overall INL performance.

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the IN^+ and IN^- input pins extending from $\text{GND} - 0.3\text{V}$ to $V_{\text{CC}} + 0.3\text{V}$. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2440 converts the bipolar differential input signal, $V_{\text{IN}} = \text{IN}^+ - \text{IN}^-$, from $-\text{FS} = -0.5 \cdot V_{\text{REF}}$ to $+\text{FS} = 0.5 \cdot V_{\text{REF}}$ where $V_{\text{REF}} = \text{REF}^+ - \text{REF}^-$. Outside this range,

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the converter indicates the overrange or the underrange condition using distinct output codes.

Output Data Format

The LTC2440 serial output data stream is 32-bits long. The first 3-bits represent status information indicating the sign and conversion state. The next 24-bits are the conversion result, MSB first. The remaining 5-bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. In the case of ultrahigh resolution modes, more than 24 effective bits of performance are possible (see Table 3). Under these conditions, sub LSBs are included in the conversion result and represent useful information beyond the 24-bit level. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below $-FS$) or an overrange condition (the differential input voltage is above $+FS$). For input conditions in excess of twice full scale ($|V_{IN}| \geq V_{REF}$), the converter may indicate either overrange or underrange. Once the input returns to the normal operating range, the conversion result is immediately accurate within the specifications of the device.

Bit 31 (first output bit) is the end of conversion (\overline{EOC}) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the \overline{CS} pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0 , this bit is HIGH. If V_{IN} is <0 , this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above $+FS$. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below $-FS$.

The function of these bits is summarized in Table 1.

Table 1. LTC2440 Status Bits

Input Range	Bit 31 \overline{EOC}	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0	0	0

Bits ranging from 28 to 5 are the 24-bit conversion result MSB first.

Bit 5 is the Least Significant Bit (LSB).

Bits ranging from 4 to 0 are sub LSBs below the 24-bit level. Bits 4 to bit 0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever \overline{CS} is HIGH, SDO remains high impedance.

In order to shift the conversion result out of the device, \overline{CS} must first be driven LOW. \overline{EOC} is seen at the SDO pin of the device once \overline{CS} is pulled LOW. \overline{EOC} changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (\overline{EOC}) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is

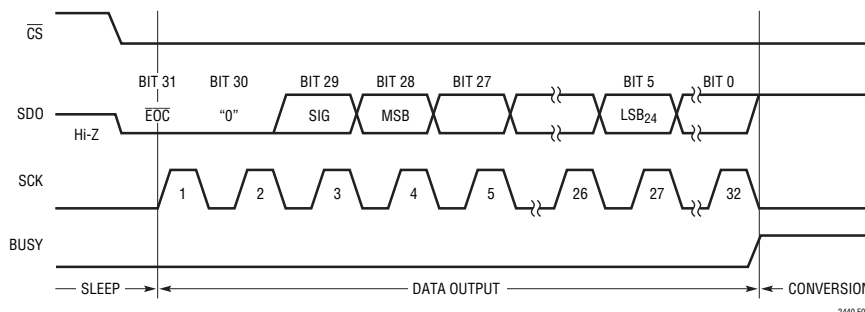


Figure 3. Output Data Timing

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shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{\text{EOC}}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN^+ and IN^- pins is maintained within the -0.3V to $(\text{V}_{\text{CC}} + 0.3\text{V})$ absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from $-\text{FS} = -0.5 \cdot \text{V}_{\text{REF}}$ to $+\text{FS} = 0.5 \cdot \text{V}_{\text{REF}}$. For differential input voltages greater than $+\text{FS}$, the conversion result is clamped to the value corresponding to the $+\text{FS} + 1\text{LSB}$. For differential input voltages below $-\text{FS}$, the conversion result is clamped to the value corresponding to $-\text{FS} - 1\text{LSB}$.

SERIAL INTERFACE PINS

The LTC2440 transmits the conversion results and receives the start of conversion command through a synchronous 2-wire, 3-wire or 4-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result and program the speed/resolution.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 13) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2440 creates its own serial clock. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected by tying $\overline{\text{EXT}}$ (Pin 10) LOW for external SCK and HIGH for internal SCK.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 12), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{\text{CS}}$ (Pin 11) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{\text{CS}}$ is LOW during the convert or sleep state, SDO will output $\overline{\text{EOC}}$. If $\overline{\text{CS}}$ is LOW during the conversion phase, the $\overline{\text{EOC}}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{\text{EOC}}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{\text{CS}} = \text{LOW}$.

Table 2. LTC2440 Output Data Format

Differential Input Voltage V_{IN}^*	Bit 31 $\overline{\text{EOC}}$	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	...	Bit 0
$\text{V}_{\text{IN}}^* \geq 0.5 \cdot \text{V}_{\text{REF}}^{**}$	0	0	1	1	0	0	0	...	0
$0.5 \cdot \text{V}_{\text{REF}}^{**} - 1\text{LSB}$	0	0	1	0	1	1	1	...	1
$0.25 \cdot \text{V}_{\text{REF}}^{**}$	0	0	1	0	1	0	0	...	0
$0.25 \cdot \text{V}_{\text{REF}}^{**} - 1\text{LSB}$	0	0	1	0	0	1	1	...	1
0	0	0	1	0	0	0	0	...	0
-1LSB	0	0	0	1	1	1	1	...	1
$-0.25 \cdot \text{V}_{\text{REF}}^{**}$	0	0	0	1	1	0	0	...	0
$-0.25 \cdot \text{V}_{\text{REF}}^{**} - 1\text{LSB}$	0	0	0	1	0	1	1	...	1
$-0.5 \cdot \text{V}_{\text{REF}}^{**}$	0	0	0	1	0	0	0	...	0
$\text{V}_{\text{IN}}^* < -0.5 \cdot \text{V}_{\text{REF}}^{**}$	0	0	0	0	1	1	1	...	1

*The differential input voltage $\text{V}_{\text{IN}} = \text{IN}^+ - \text{IN}^-$. **The differential reference voltage $\text{V}_{\text{REF}} = \text{REF}^+ - \text{REF}^-$.

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Chip Select Input (\overline{CS})

The active LOW chip select, \overline{CS} (Pin 11), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the \overline{CS} signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2440 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the \overline{CS} pin after the converter has entered the data output state (i.e., after the fifth falling edge of SCK occurs with $\overline{CS} = \text{LOW}$).

Serial Data Input (SDI)—Logic Level Speed Selection

The serial data input (SDI, Pin 7) is used to select the speed/resolution of the LTC2440. A simple 2-speed control is selectable by either driving SDI HIGH or LOW. If SDI is grounded (pin compatible with LTC2410) the device outputs data at 880Hz with 21 bits effective resolution. By tying SDI HIGH, the converter enters the ultralow noise mode ($200\text{nV}_{\text{RMS}}$) with simultaneous 50/60Hz rejection at 6.9Hz output rate. SDI may be driven logic HIGH or LOW anytime during the conversion or sleep state in order to change the speed/resolution. The conversion immediately following the data output cycle will be valid and performed at the newly selected output rate/resolution.

Changing SDI logic state during the data output cycle should be avoided as speed resolution other than 6.9Hz or 880Hz may be selected. For example, if SDI is changed from logic 0 to logic 1 after the second rising edge of SCK, the conversion rate will change from 880Hz to 55Hz (the following values are listed in Table 3: $\text{OSR4} = 0$, $\text{OSR3} = 0$, $\text{OSR2} = 1$, $\text{OSR1} = 1$ and $\text{OSR0} = 1$). If SDI remains HIGH, the conversion rate will switch to the desired 6.9Hz speed immediately following the conversion at 55Hz. The 55Hz rate conversion cycle will be a valid result as well as the first 6.9Hz result. On the other hand, if SDI is changed to a 1 anytime before the first rising edge of SCK, the following conversion rate will become 6.9Hz. If SDI is changed to a 1 after the 5th rising edge of SCK, the next conversion will remain 880Hz while all subsequent conversions will be at 6.9Hz.

Serial Data Input (SDI)—Serial Input Speed Selection

SDI may also be programmed by a serial input data stream under control of SCK during the data output cycle, see Figure 4. One of ten speed/resolution ranges (from 6.9Hz/ $200\text{nV}_{\text{RMS}}$ to 3.5kHz/ $21\mu\text{V}_{\text{RMS}}$) may be selected, see Table 3. The conversion following a new selection is valid and performed at the newly selected speed/resolution.

BUSY

The BUSY output (Pin 15) is used to monitor the state of conversion, data output and sleep cycle. While the part is converting, the BUSY pin is HIGH. Once the conversion is complete, BUSY goes LOW indicating the conversion is complete and data out is ready. The part now enters the LOW power sleep state. BUSY remains LOW while data is shifted out of the device. It goes HIGH at the conclusion of the data output cycle indicating a new conversion has begun. This rising edge may be used to flag the completion of the data read cycle.

SERIAL INTERFACE TIMING MODES

The LTC2440's 2-wire, 3-wire or 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2-wire or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator ($f_0 = \text{LOW}$) or an external oscillator connected to the f_0 pin. See Table 4 for a summary.

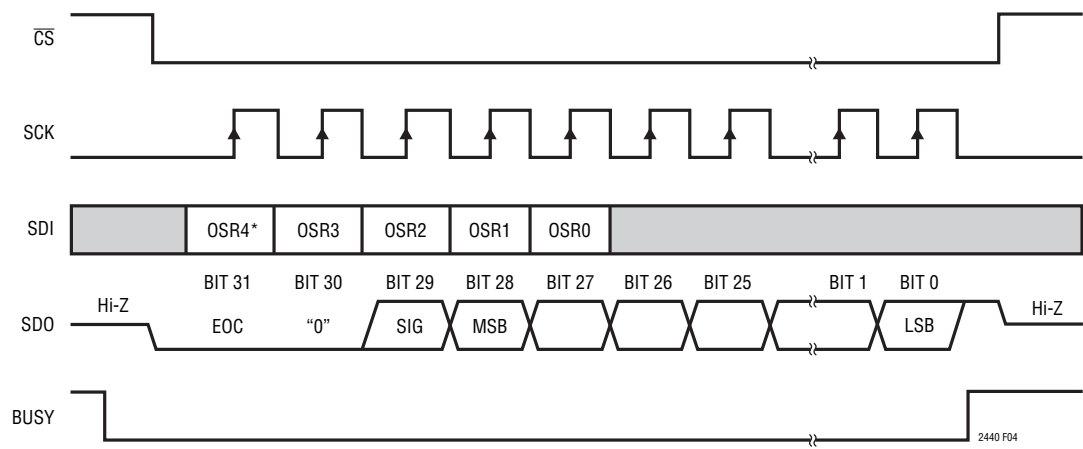
External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected by the \overline{EXT} pin. To select the external serial clock mode, \overline{EXT} must be tied low.

The serial data output pin (SDO) is Hi-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be pulled LOW in order to monitor the state of the converter. While \overline{CS} is pulled LOW, \overline{EOC} is output to the SDO pin.

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*OSR4 BIT MUST BE AT FIRST SCK RISING EDGE DURING SERIAL DATA OUT CYCLE

Figure 4. SDI Speed/Resolution Programming

Table 3. SDI Speed/Resolution Programming

OSR4	OSR3	OSR2	OSR1	OSR0	RMS NOISE	ENOB	OSR
X	0	0	0	1	23μV	17	64
X	0	0	1	0	3.5μV	20	128
0	0	0	0	0	2μV	21.3	256*
X	0	0	1	1	2μV	21.3	256
X	0	1	0	0	1.4μV	21.8	512
X	0	1	0	1	1μV	22.4	1024
X	0	1	1	0	750nV	22.9	2048
X	0	1	1	1	510nV	23.4	4096
X	1	0	0	0	375nV	24	8192
X	1	0	0	1	250nV	24.4	16384
X	1	1	1	1	200nV	24.6	32768**

** Address allows tying SDI HIGH *Additional address to allow tying SDI LOW

Table 4. LTC2440 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	CS and SCK	CS and SCK	Figures 5, 6
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 7
Internal SCK, Single Cycle Conversion	Internal	CS ↓	CS ↓	Figures 8, 9
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 10

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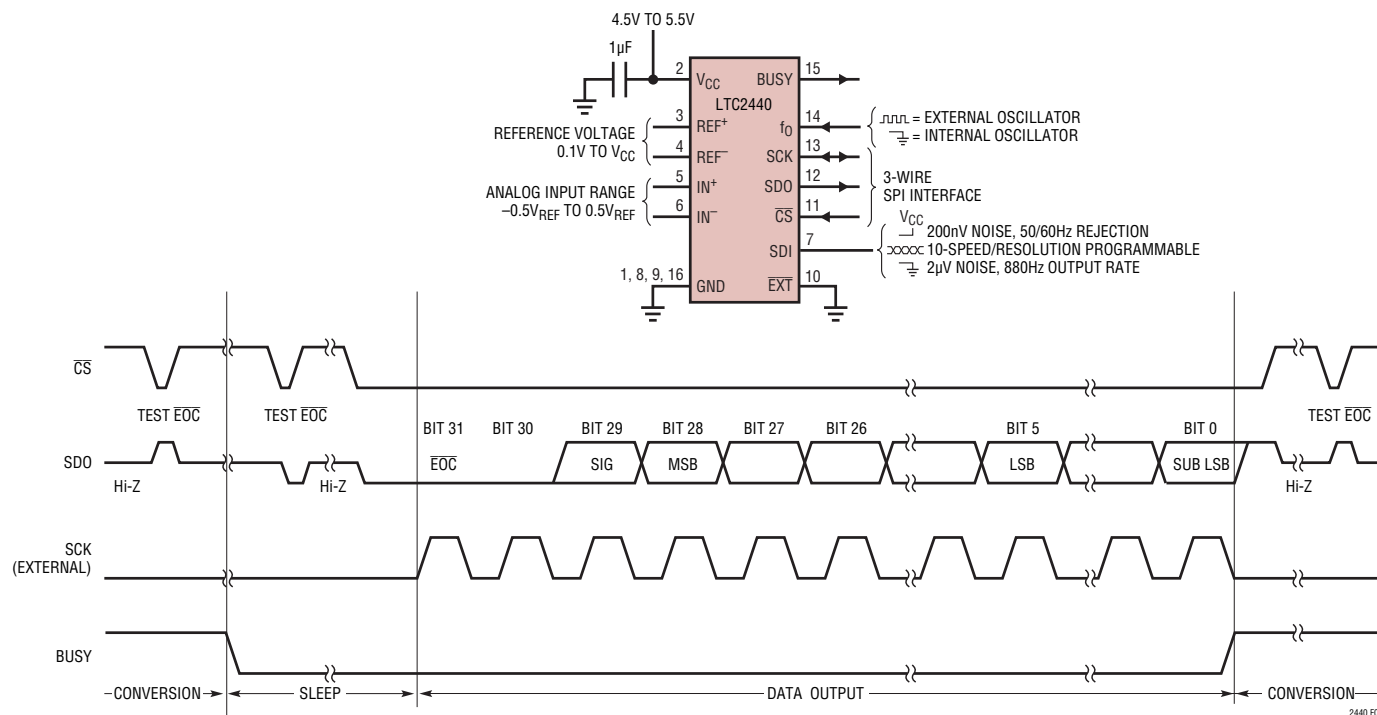


Figure 5. External Serial Clock, Single Cycle Operation

$\overline{EOC} = 1$ ($BUSY = 1$) while a conversion is in progress and $\overline{EOC} = 0$ ($BUSY = 0$) if the device is in the sleep state. Independent of \overline{CS} , the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC} = 0$), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC} = 1$) and BUSY goes HIGH indicating a conversion is in progress.

At the conclusion of the data cycle, \overline{CS} may remain LOW and \overline{EOC} monitored as an end-of-conversion interrupt. Alternatively, \overline{CS} may be driven HIGH setting SDO to Hi-Z and BUSY monitored for the completion of a conversion. As described above, \overline{CS} may be pulled LOW at any time in order to monitor the conversion status on the SDO pin.

Typically, \overline{CS} remains LOW during the data output state. However, the data output state may be aborted by pulling \overline{CS} HIGH anytime between the fifth falling edge (SDI must be properly loaded each cycle) and the 32nd falling edge of SCK, see Figure 6. On the rising edge of \overline{CS} , the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. \overline{CS} may be permanently tied to ground, simplifying the user interface or isolation barrier. The external serial clock mode is selected by tying \overline{EXT} LOW.

Since \overline{CS} is tied LOW, the end-of-conversion (\overline{EOC}) can be continuously monitored at the SDO pin during the convert and sleep states. Conversely, BUSY (Pin 15) may be used to monitor the status of the conversion cycle. \overline{EOC} or BUSY may be used as an interrupt to an external

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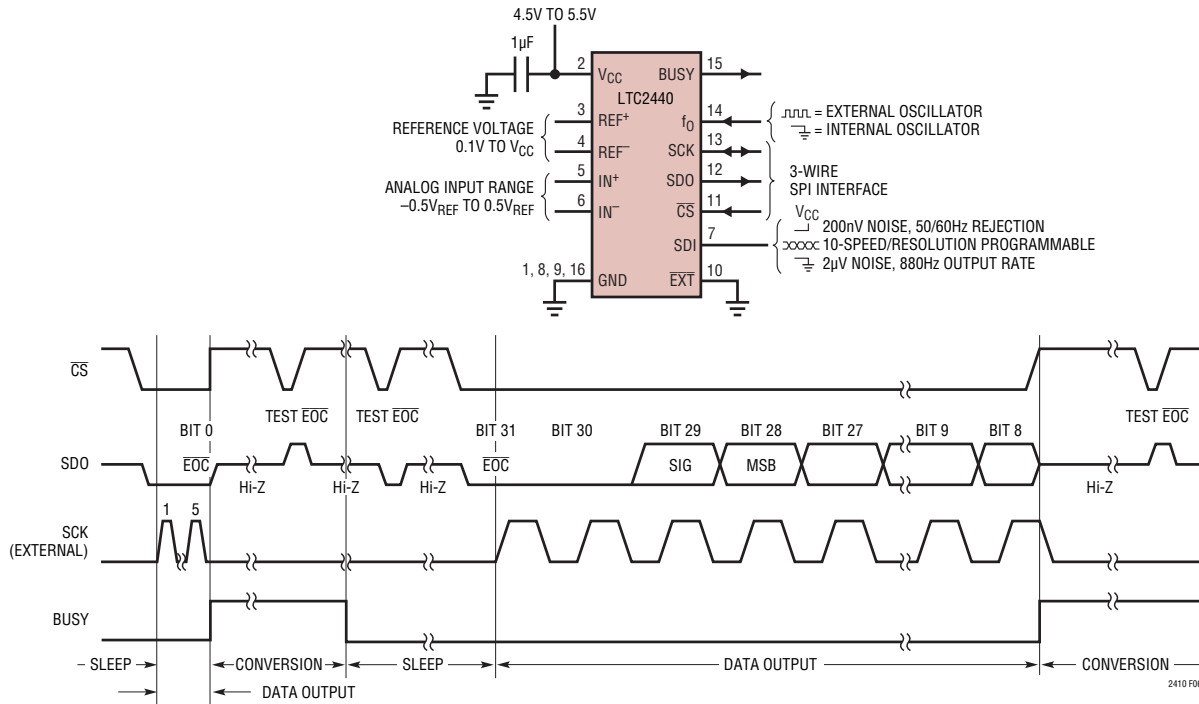


Figure 6. External Serial Clock, Reduced Data Output Length

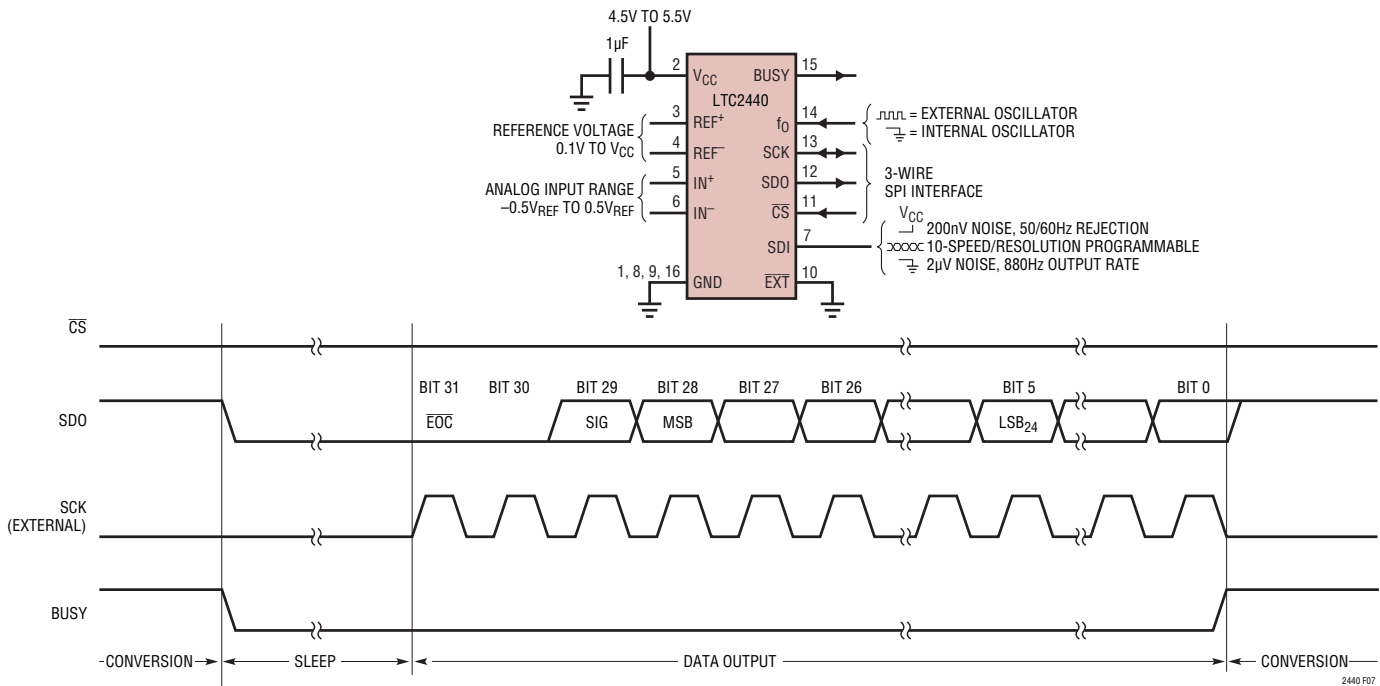


Figure 7. External Serial Clock, $\overline{CS} = 0$ Operation (2-Wire)

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controller indicating the conversion result is ready. \overline{EOC} = 1 (BUSY = 1) while the conversion is in progress and \overline{EOC} = 0 (BUSY = 0) once the conversion enters the low power sleep state. On the falling edge of \overline{EOC} /BUSY, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. \overline{EOC} can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO and BUSY go HIGH (\overline{EOC} = 1) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a \overline{CS} signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the \overline{EXT} pin must be tied HIGH.

The serial data output pin (SDO) is Hi-Z as long as \overline{CS} is HIGH. At any time during the conversion cycle, \overline{CS} may be pulled LOW in order to monitor the state of the converter.

Once \overline{CS} is pulled LOW, SCK goes LOW and \overline{EOC} is output to the SDO pin. \overline{EOC} = 1 while a conversion is in progress and \overline{EOC} = 0 if the device is in the sleep state. Alternatively, BUSY (Pin 15) may be used to monitor the status of the conversion in progress. BUSY is HIGH during the conversion and goes LOW at the conclusion. It remains LOW until the result is read from the device.

When testing \overline{EOC} , if the conversion is complete (\overline{EOC} = 0), the device will exit the sleep state and enter the data output state if \overline{CS} remains LOW. In order to prevent the device from exiting the low power sleep state, \overline{CS} must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of \overline{CS} (if \overline{EOC} = 0) or $t_{EOCtest}$ after \overline{EOC} goes LOW (if \overline{CS} is LOW during the falling edge of \overline{EOC}). The value of $t_{EOCtest}$ is 500ns. If \overline{CS} is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If \overline{CS} remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins

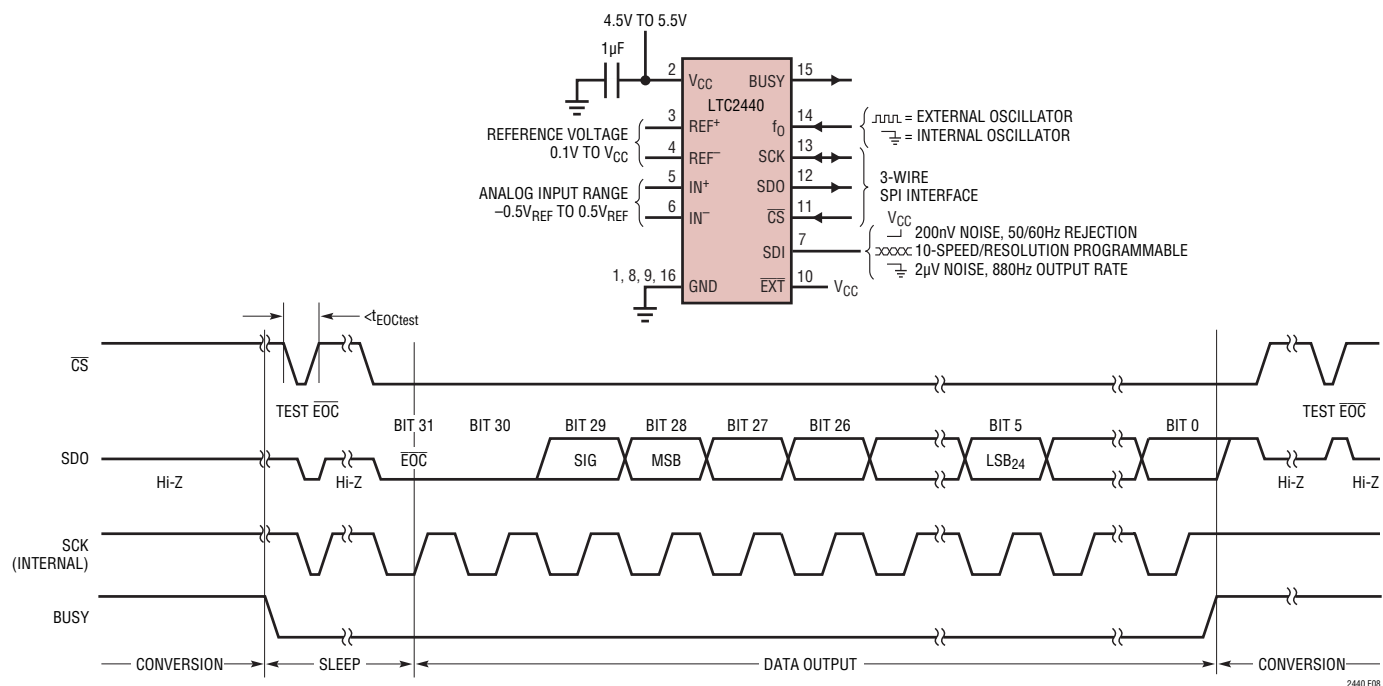


Figure 8. Internal Serial Clock, Single Cycle Operation

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on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{\text{EOC}}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{\text{EOC}} = 1$), SCK stays HIGH and a new conversion starts.

Typically, $\overline{\text{CS}}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{\text{CS}}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. In order to properly select the OSR for the conversion following a data abort, five SCK rising edges must be seen prior to performing a data out abort (pulling $\overline{\text{CS}}$ HIGH). If $\overline{\text{CS}}$ is pulled high prior to the fifth SCK falling edge, the OSR selected depends on the number of SCK signals seen prior to data abort, where subsequent nonaborted conversion cycles return to the programmed OSR. On the rising edge of $\overline{\text{CS}}$, the device aborts the data output state and immediately initiates a

new conversion. This is useful for systems not requiring all 32-bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. $\overline{\text{CS}}$ may be permanently tied to ground, simplifying the user interface or isolation barrier. The internal serial clock mode is selected by tying $\overline{\text{EXT}}$ HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{\text{EOC}} = 1$) and $\text{BUSY} = 1$. Once the conversion is complete, SCK, BUSY and SDO go LOW ($\overline{\text{EOC}} = 0$) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time ($\approx 500\text{ns}$) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each

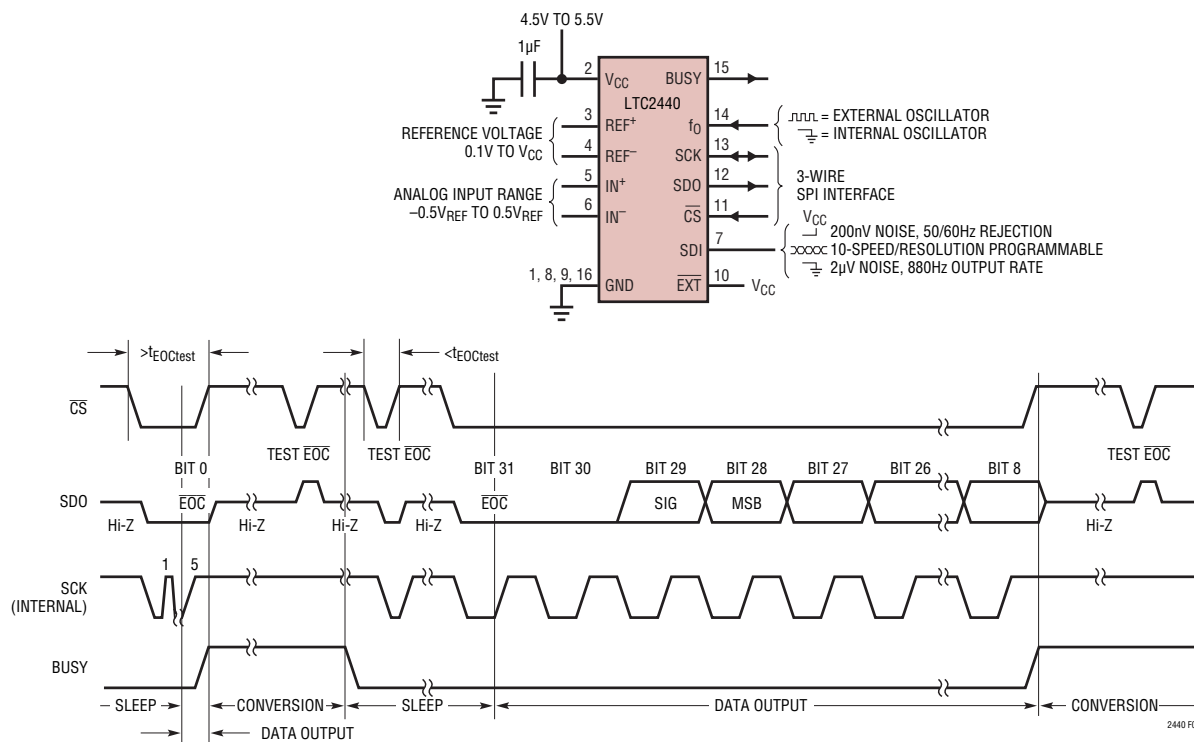


Figure 9. Internal Serial Clock, Reduced Data Output Length

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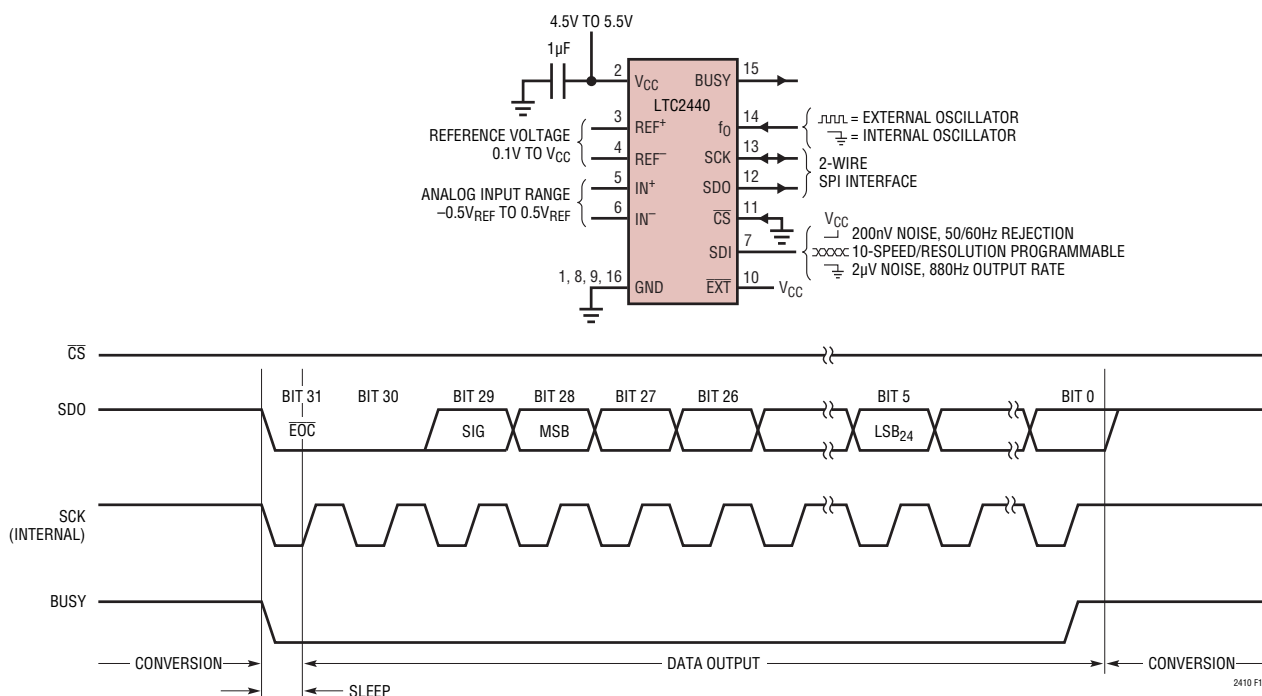


Figure 10. Internal Serial Clock, Continuous Operation

falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. \overline{EOC} can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC} = 1$) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

Normal Mode Rejection and Antialiasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2440 significantly simplifies antialiasing filter requirements.

The LTC2440's speed/resolution is determined by the over sample ratio (OSR) of the on-chip digital filter. The OSR ranges from 64 for 3.5kHz output rate to 32,768 for 6.9Hz output rate. The value of OSR and the sample rate f_s determine the filter characteristics of the device. The first NULL of the digital filter is at f_N and multiples of f_N where

$f_N = f_s / \text{OSR}$, see Figure 11 and Table 5. The rejection at the frequency $f_N \pm 14\%$ is better than 80dB, see Figure 12.

If f_0 is grounded, f_s is set by the on-chip oscillator at 1.8MHz (over supply and temperature variations). At an OSR of 32,768, the first NULL is at $f_N = 55\text{Hz}$ and the no latency output rate is $f_N / 8 = 6.9\text{Hz}$. At the maximum OSR,

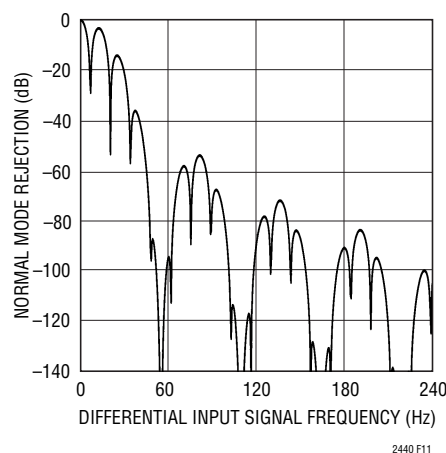


Figure 11. LTC2440 Normal Mode Rejection (Internal Oscillator)

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Table 5. OSR vs Notch Frequency (f_N) with Internal Oscillator

OSR	NOTCH (f _N)
64	28.16kHz
128	14.08kHz
256	7.04kHz
512	3.52kHz
1024	1.76kHz
2048	880Hz
4096	440Hz
8192	220Hz
16384	110Hz
32768*	55Hz

*Simultaneous 50/60 rejection

the noise performance of the device is 200nV_{RMS} with better than 80dB rejection of 50Hz ±2% and 60Hz ±2%. Since the OSR is large (32,768) the wide band rejection is extremely large and the antialiasing requirements are simple. The first multiple of f_S occurs at 55Hz • 32,768 = 1.8MHz, see Figure 13.

The first NULL becomes f_N = 7.04kHz with an OSR of 256 (an output rate of 880Hz) and f_O grounded. While the NULL has shifted, the sample rate remains constant. As a result of constant modulator sampling rate, the linearity, offset and full-scale performance remains unchanged as does the first multiple of f_S.

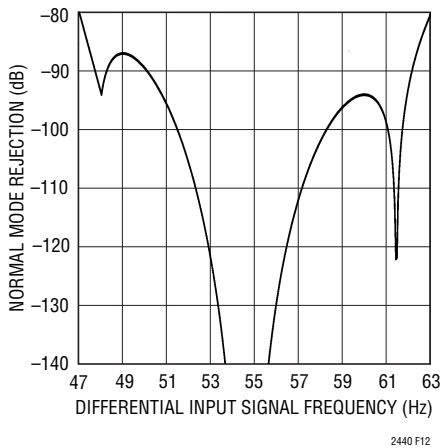


Figure 12. LTC2440 Normal Mode Rejection (Internal Oscillator)

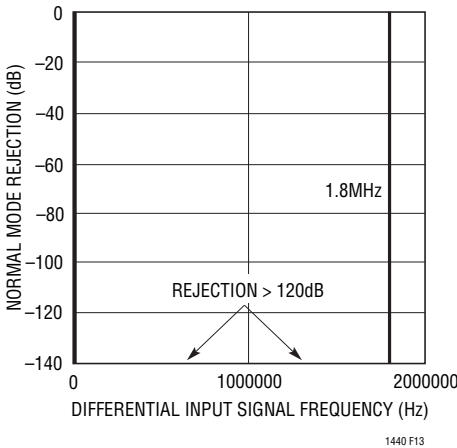


Figure 13. LTC2440 Normal Mode Rejection (Internal Oscillator)

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The sample rate f_S and NULL f_N , may also be adjusted by driving the f_O pin with an external oscillator. The sample rate is $f_S = f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to f_O . Combining a large OSR with a reduced sample rate leads to notch frequencies f_N near DC while maintaining simple antialiasing requirements. A 100kHz clock applied to f_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 14. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

An external oscillator operating from 100kHz to 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 22. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

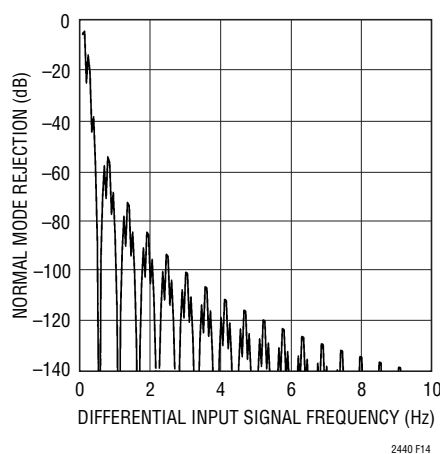
$$f_{OSC} = 10\text{MHz} \cdot \left(\frac{10k}{10 \cdot R_{SET}} \right)$$

The normal mode rejection characteristic shown in Figure 14 is achieved by applying the output of the LTC1799 (with $R_{SET} = 100k$) to the f_O pin on the LTC2440 with SDI tied HIGH (OSR = 32768).

Reduced Power Operation

In addition to adjusting the speed/resolution of the LTC2440, the speed/resolution/power dissipation may also be adjusted using the automatic sleep mode. During the conversion cycle, the LTC2440 draws 8mA supply current independent of the programmed speed. Once the conversion cycle is completed, the device automatically enters a low power sleep state drawing 8 μ A. The device remains in this state as long as \overline{CS} is HIGH and data is not shifted out. By adjusting the duration of the sleep state (hold \overline{CS} HIGH longer) and the duration of the conversion cycle (programming OSR) the DC power dissipation can be reduced, see Figure 16.

For example, if the OSR is programmed at the fastest rate (OSR = 64, $t_{CONV} = 0.285\text{ms}$) and the sleep state is 10ms, the effective output rate is approximately 100Hz while the average supply current is reduced to 240 μ A. By further extending the sleep state to 100ms, the effective output rate of 10Hz draws on average 30 μ A. Noise, power, and speed can be optimized by adjusting the OSR (Noise/Speed) and sleep mode duration (Power).



**Figure 14. LTC2440 Normal Mode Rejection
(External Oscillator at 90kHz)**

APPLICATIONS INFORMATION

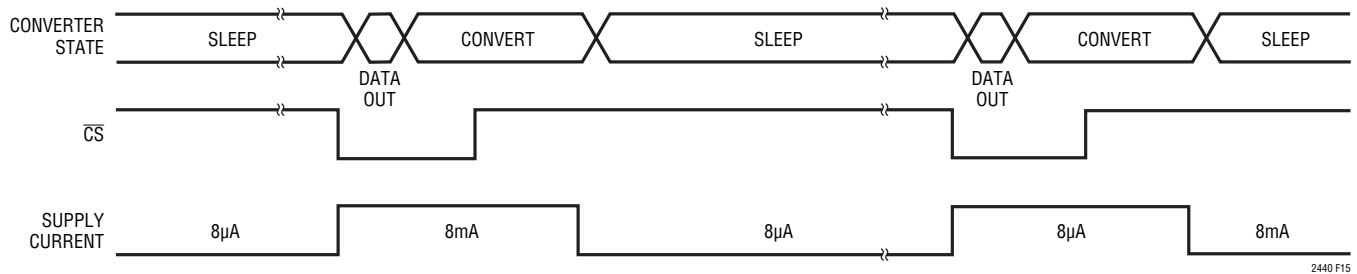


Figure 15. Reduced Power Timing Mode

LTC2440 Input Structure

Modern delta sigma converters have switched capacitor front ends that repeatedly sample the input voltage over some time period. The sampling process produces a small current pulse at the input and reference terminals as the capacitors are charged. The LTC2440 switches the input and reference to a 5pF sample capacitor at a frequency of 1.8MHz. A simplified equivalent circuit is shown in Figure 16.

The average input and reference currents can be expressed in terms of the equivalent input resistance of the sample capacitor, where:

$$R_{eq} = 1/(f_{sw} \cdot C_{eq})$$

When using the internal oscillator, f_{sw} is 1.8MHz and the equivalent resistance is approximately 110k Ω .

Driving the Input and Reference

Because of the small current pulses, excessive lead length at the analog or reference input may allow reflections or ringing to occur, affecting the conversion accuracy. The key to preserving the accuracy of the LTC2440 is complete settling of these sampling glitches at both the input and reference terminals. There are several recommended methods of doing this.

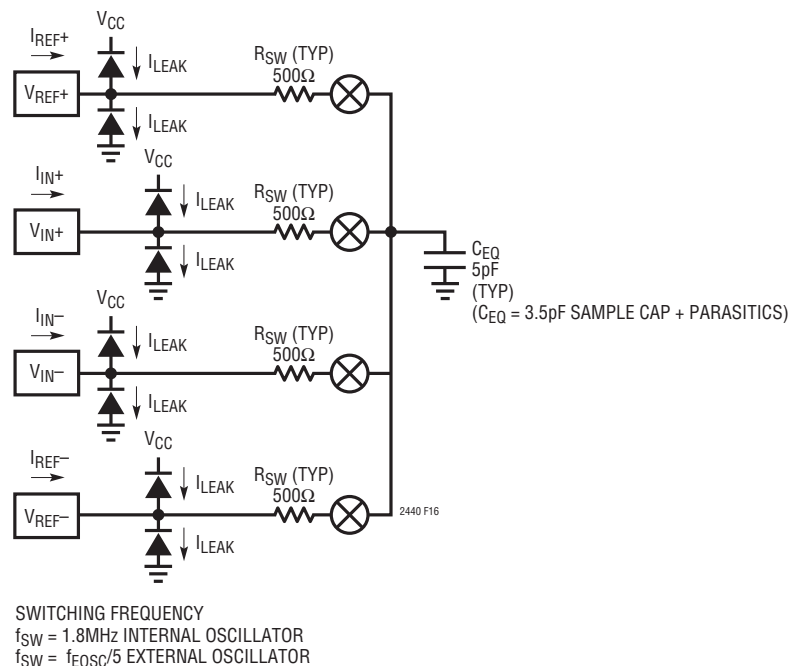


Figure 16. LTC2440 Input Structure

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Direct Connection to Low Impedance Sources

If the ADC can be located physically close to the sensor, it can be directly connected to sensors or other sources with impedances up to 350Ω with no other components required (see Figure 17).

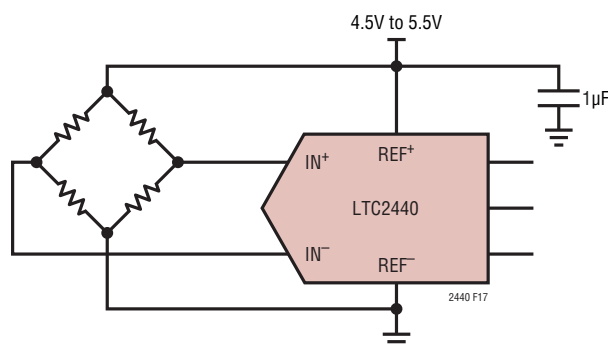


Figure 17. Direct Connection to Low Impedance ($<350\Omega$) Source is Possible if the Sensor is Located Close to the ADC.

Longer Connections to Low Impedance Sources

If longer lead lengths are unavoidable, adding an input capacitor close to the ADC input pins will average the charging pulses and prevent reflections or ringing (see Figure 18). Averaging the current pulses results in a DC input current that should be taken into account. The resulting $110k\Omega$ input impedance will result in a gain error of 0.44% for a 350Ω bridge (within the full scale specs of many bridges) and a very low 12.6ppm error for a 2Ω thermocouple connection.

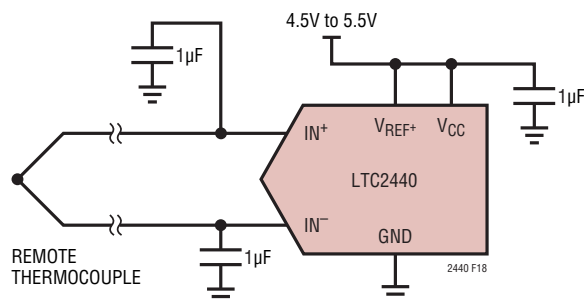


Figure 18. Input Capacitors Allow Longer Connection Between the Low Impedance Source and the ADC.

Buffering the LTC2440

Many applications will require buffering, particularly where high impedance sources are involved or where the device being measured is located some distance from the LTC2440. When buffering the LTC2440 a few simple steps should be followed.

Figure 19 shows a network suitable for coupling the inputs of a LTC2440 to a LTC2051 chopper-stabilized op amp. The $3\mu V$ offset and low noise of the LTC2051 make it a good choice for buffering the LTC2440. Many other op amps will work, with varying performance characteristics.

The LTC2051 is configured to be able to drive the $1\mu F$ capacitors at the inputs of the LTC2440. The $1\mu F$ capacitors should be located close to the ADC input pins.

The measured total unadjusted error of Figure 19 is well within the specifications of the LTC2440 by itself. Most autozero amplifiers will degrade the overall resolution to some degree because of the extremely low input noise of the LTC2440, however the LTC2051 is a good general purpose buffer. The measured input referred noise of two LTC2051s buffering both LTC2440 inputs is approximately double that of the LTC2440 by itself, which reduces the effective resolution by 1 bit for all oversample ratios. Adding gain to the LTC2051 will increase gain and offset errors and will not appreciably increase the overall resolution, so it has limited benefit.

Procedure For Coupling Any Amplifier to the LTC2440

The LTC2051 is suitable for a wide range of DC and low frequency measurement applications. If another amplifier is to be selected, a general procedure for evaluating the suitability of an amplifier for use with the LTC2440 is suggested here:

1. Perform a thorough error and noise analysis on the amplifier and gain setting components to verify that the amplifier will perform as intended.
2. Measure the large signal response of the overall circuit. The capacitive load may affect the maximum slew rate of the amplifier. Verify that the slew rate is adequate for the

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fastest expected input signal. Figure 20 shows the large signal response of the circuit in Figure 19.

3. Measure noise performance of the complete circuit. A good technique is to build one amplifier for each input, even if only one will be used in the end application. Bias both amplifier outputs to midscale, with the inputs tied together. Verify that the noise is as expected, taking into account the bandwidth of the LTC2440 inputs for the OSR being used, the amplifier's broadband voltage noise and 1/f corner (if any) and any additional noise due to the amplifier's current noise and source resistance.

For more information on testing high linearity ADCs, refer to Linear Technology Design Solutions 11.

Input Bandwidth and Frequency Rejection

The combined effect of the internal SINC⁴ digital filter and the digital and analog autocalibration circuits determines the LTC2440 input bandwidth and rejection characteristics. The digital filter's response can be adjusted by setting the oversample ratio (OSR) through the SPI interface or by supplying an external conversion clock to the f_0 pin.

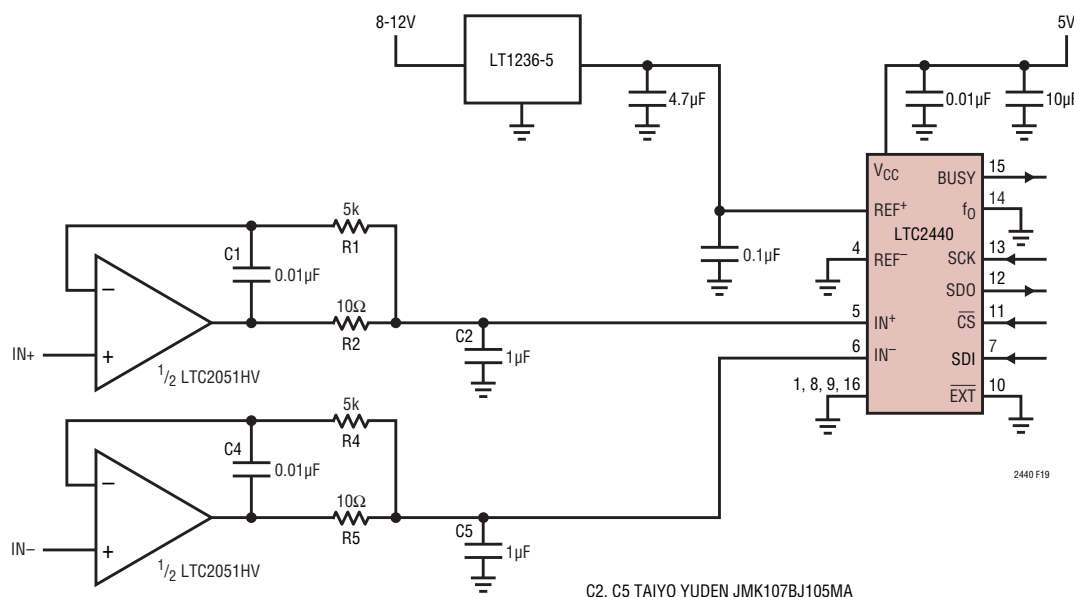


Figure 19. Buffering the LTC2440 from High Impedance Sources Using a Chopper Amplifier

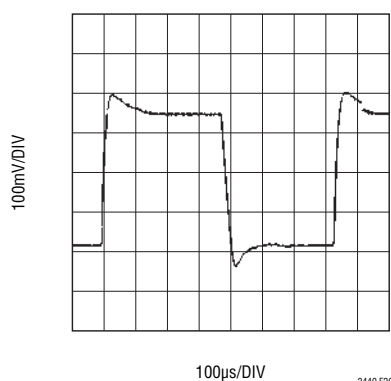


Figure 20. Large Signal Input Settling Time Indicates Completed Settling with Selected Load Capacitance.

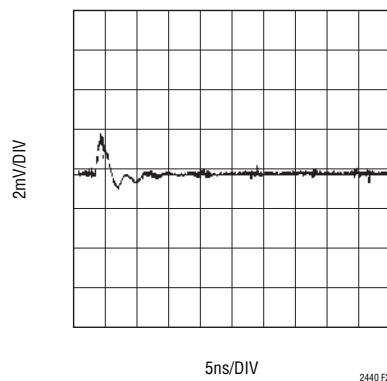


Figure 21. Dynamic Input Current is Attenuated by Load Capacitance and Completely Settled Before the Next Conversion Sample Resulting in No Reduction in Performance.

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Table 6 lists the properties of the LTC2440 with various combinations of oversample ratio and clock frequency. Understanding these properties is the key to fine tuning the characteristics of the LTC2440 to the application.

Maximum Conversion Rate

The maximum conversion rate is the fastest possible rate at which conversions can be performed.

First Notch Frequency

This is the first notch in the SINC^4 portion of the digital filter and depends on the f_0 clock frequency and the oversample ratio. Rejection at this frequency and its multiples (up to

the modulator sample rate of 1.8MHz) exceeds 120dB. This is 8 times the maximum conversion rate.

Effective Noise Bandwidth

The LTC2440 has extremely good input noise rejection from the first notch frequency all the way out to the modulator sample rate (typically 1.8MHz). Effective noise bandwidth is a measure of how the ADC will reject wideband input noise up to the modulator sample rate. The example on the following page shows how the noise rejection of the LTC2440 reduces the effective noise of an amplifier driving its input.

Table 6. Performance vs Oversample Ratio

Oversample Ratio (OSR)	ADC Noise*	ENOB ($V_{\text{REF}} = 5\text{V}$)*	Maximum Conversion Rate (sps)		First Notch Frequency (Hz)		Effective Noise BW (Hz)		-3dB Point (Hz)	
			Internal Clock	External f_0 (f_0/x)	Internal Clock	External f_0 (f_0/x)	Internal 9MHz clock	External (f_0/x)	Internal Clock	External f_0 (f_0/x)
64	23 μV	17	2816.35	$f_0/2738$	28125	$f_0/320$	3148	$f_0/2860$	1696	$f_0/5310$
128	3.5 μV	20	1455.49	$f_0/5298$	14062.5	$f_0/640$	1574	$f_0/5720$	848	$f_0/10600$
256	2 μV	21.3	740.18	$f_0/10418$	7031.3	$f_0/1280$	787	$f_0/11440$	424	$f_0/21200$
512	1.4 μV	21.8	373.28	$f_0/20658$	3515.6	$f_0/2560$	394	$f_0/22840$	212	$f_0/42500$
1024	1 μV	22.4	187.45	$f_0/41138$	1757.8	$f_0/5120$	197	$f_0/45690$	106	$f_0/84900$
2048	750nV	22.9	93.93	$f_0/82098$	878.9	$f_0/10200$	98.4	$f_0/91460$	53	$f_0/170000$
4096	510nV	23.4	47.01	$f_0/164018$	439.5	$f_0/20500$	49.2	$f_0/183000$	26.5	$f_0/340000$
8192	375nV	24	23.52	$f_0/327858$	219.7	$f_0/41000$	24.6	$f_0/366000$	13.2	$f_0/679000$
16384	250nV	24.4	11.76	$f_0/655538$	109.9	$f_0/81900$	12.4	$f_0/731000$	6.6	$f_0/1358000$
32768	200nV	24.6	5.88	$f_0/1310898$	54.9	$f_0/163800$	6.2	$f_0/1463000$	3.3	$f_0/2717000$

*ADC noise increases by approximately $\sqrt{2}$ when OSR is decreased by a factor of 2 for OSR 32768 to OSR 256. The ADC noise at OSR 128 and OSR 64 include effects from internal modulator quantization noise.

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Example:

If an amplifier (e.g. LT1219) driving the input of an LTC2440 has wideband noise of $33\text{nV}/\sqrt{\text{Hz}}$, band-limited to 1.8MHz , the total noise entering the ADC input is:

$$33\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{1.8\text{MHz}} = 44.3\mu\text{V}.$$

When the ADC digitizes the input, its digital filter filters out the wideband noise from the input signal. The noise reduction depends on the oversample ratio which defines the effective bandwidth of the digital filter.

At an oversample of 256, the noise bandwidth of the ADC is 787Hz which reduces the total amplifier noise to:

$$33\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{787\text{Hz}} = 0.93\mu\text{V}.$$

The total noise is the RMS sum of this noise with the $2\mu\text{V}$ noise of the ADC at $\text{OSR}=256$.

$$\sqrt{0.93\mu\text{V}^2 + 2\mu\text{V}^2} = 2.2\mu\text{V}.$$

Increasing the oversampling ratio to 32768 reduces the noise bandwidth of the ADC to 6.2Hz which reduces the total amplifier noise to:

$$33\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{6.2\text{Hz}} = 82\text{nV}.$$

The total noise is the RMS sum of this noise with the 200nV noise of the ADC at $\text{OSR} = 32768$.

$$\sqrt{82\text{nV}^2 + 200\text{nV}^2} = 216\text{nV}.$$

In this way, the digital filter with its variable oversampling ratio can greatly reduce the effects of external noise sources.

Using Non-Autozeroed Amplifiers for Lowest Noise Applications

Ultralow noise applications may require the use of low noise bipolar amplifiers that are not autozeroed. Because the LTC2440 has such exceptionally low offset, offset drift and $1/f$ noise, the offset drift and $1/f$ noise in the amplifiers may need to be compensated for to retain the system performance of which the ADC is capable.

The circuit of Figure 23 uses low noise bipolar amplifiers and correlated double sampling to achieve a resolution of 14nV , or 19 effective bits over a 10mV span. Each measurement is the difference between two ADC readings taken with opposite polarity bridge excitation. This cancels $1/f$ noise below 3.4Hz and eliminates errors due to parasitic thermocouples. Allow $750\mu\text{s}$ settling time after switching excitation polarity.

TYPICAL APPLICATIONS

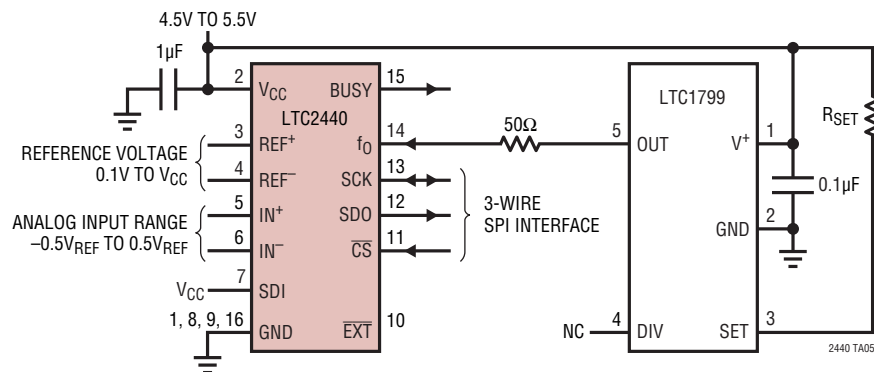
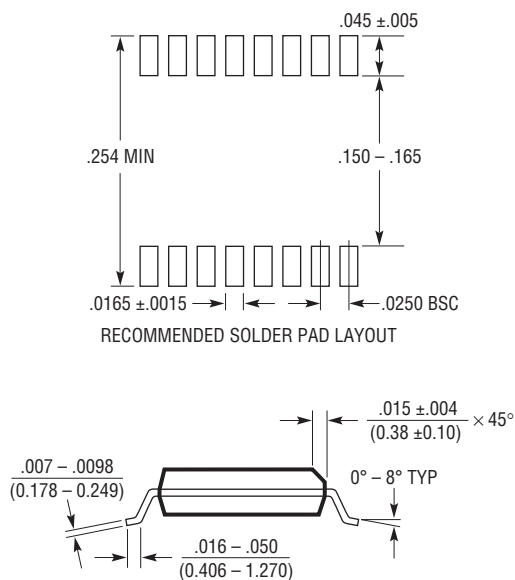


Figure 22. Simple External Clock Source

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2440#packaging> for the most recent package drawings.

GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641 Rev B)

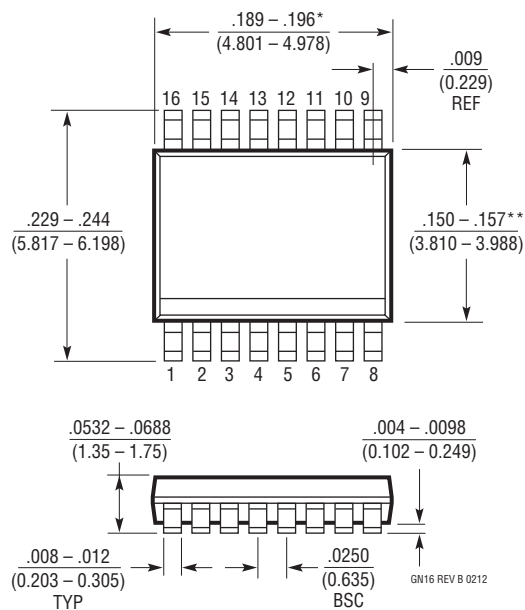


NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED $0.006''$ (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED $0.010''$ (0.254mm) PER SIDE



REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	01/17	Updated Max value for f_{EOSC} .	4
		Updated formula for t_{CONV} .	4
		Updated Note 13.	4
		Revised Table 6. Performance vs Oversample Ratio.	25

TYPICAL APPLICATION

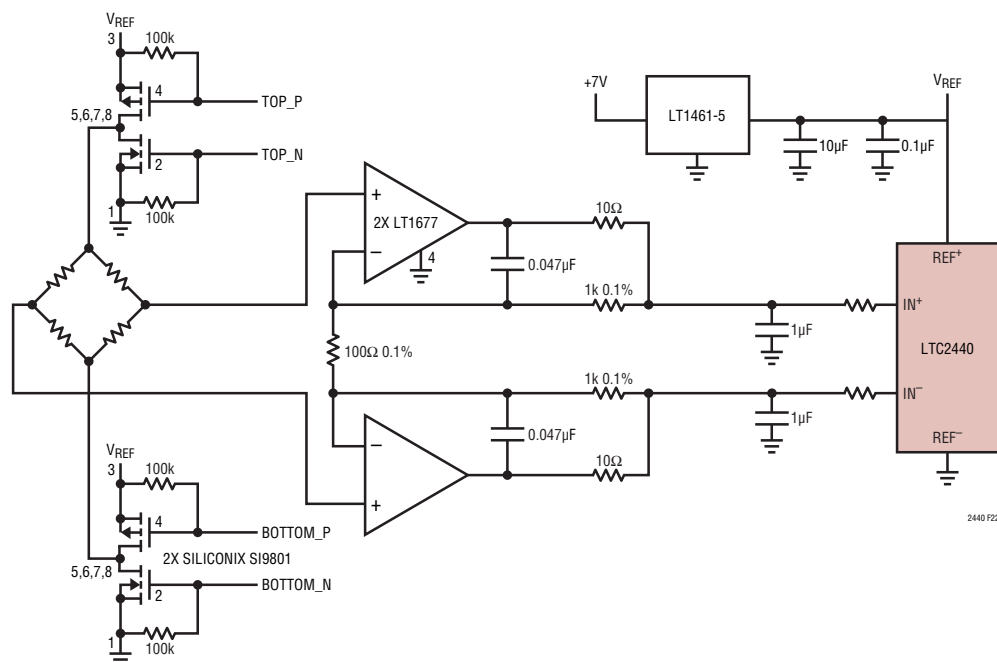


Figure 23. Bridge Reversal Eliminates 1/f Noise and Offset Drift of a Low Noise, Non-Autozeroed, Bipolar Amplifier. Circuit Gives 14nV Noise Level or 19 Effective Bits over a 10mV Span

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1025	Micropower Thermocouple Cold Junction Compensator	80µA Supply Current, 0.5°C Initial Accuracy
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5µV Offset, 1.6µV _{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Series Reference, 2.5V	0.04% Max, 3ppm/°C Max Drift
LTC1592	Ultraprecise 16-Bit SoftSpan™ DAC	Six Programmable Output Ranges
LTC1655	16-Bit Rail-to-Rail Micropower DAC	±1LSB DNL, 600µA, Internal Reference, SO-8
LTC1799	Resistor Set SOT-23 Oscillator	Single Resistor Frequency Set
LTC2053	Rail-to-Rail Instrumentation Amplifier	10µV Offset with 50nV/°C Drift, 2.5µV _{P-P} Noise 0.01Hz to 10Hz
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2401/LTC2402	1-/2-Channel, 24-Bit, No Latency ΔΣ ADC in MSOP	0.6ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2404/LTC2408	4-/8-Channel, 24-Bit, No Latency ΔΣ ADC	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2410/LTC2413	24-Bit, No Latency ΔΣ ADC	800nV _{RMS} Noise, 5ppm INL/Simultaneous 50Hz/60Hz Rejection
LTC2411	24-Bit, No Latency ΔΣ ADC in MSOP	1.45µV _{RMS} Noise, 6ppm INL
LTC2420/LTC2424/LTC2428	1-/4-/8-Channel, 20-Bit, No Latency ΔΣ ADCs	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2400/LTC2404/LTC2408