

# LT1997-3

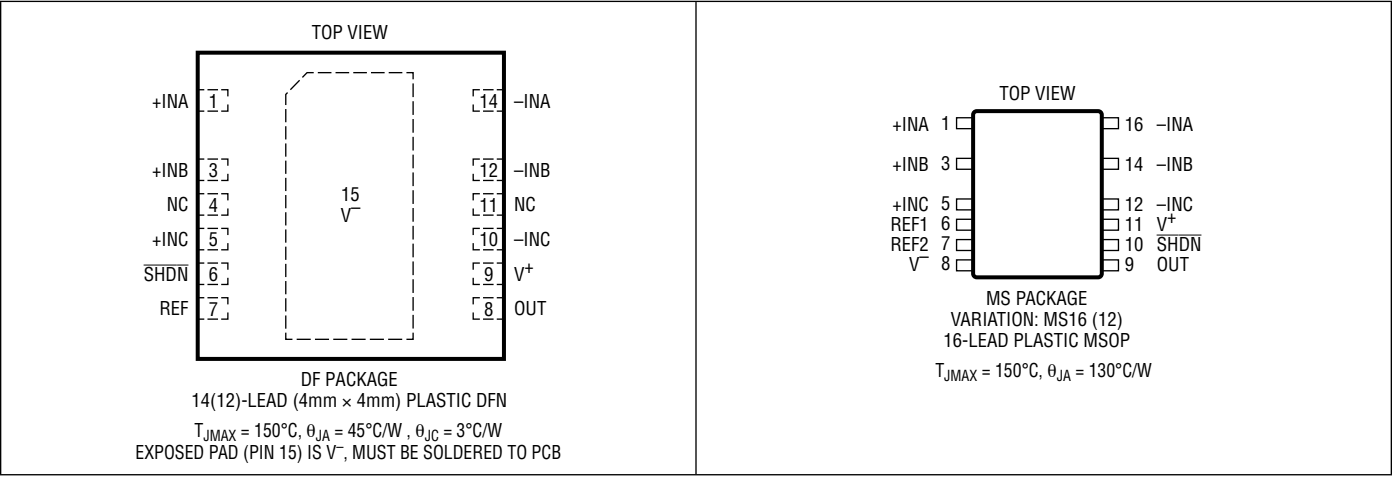
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages ( $V^+$  to  $V^-$ ).....60V  
+INA, -INA (Note 2).....  $V^- \pm 160V$   
+INB, -INB, +INC, -INC  
(Note 2)..... ( $V^- + 80V$ ) to ( $V^- - 0.3V$ )  
REF, REF1, REF2..... ( $V^- + 60V$ ) to ( $V^- - 0.3V$ )  
SHDN..... ( $V^+ + 0.3V$ ) to ( $V^- - 0.3V$ )  
Output Current (Continuous) (Note 6).....50mA

Output Short-Circuit Duration  
(Note 3) .....Thermally Limited  
Temperature Range (Notes 4, 5)  
LT1997I-3 .....-40 to 85°C  
LT1997H-3 .....-40 to 125°C  
Maximum Junction Temperature ..... 150°C  
Storage Temperature Range .....-65 to 150°C  
MSOP Lead Temperature (Soldering, 10 sec)..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LT1997-3#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1997IDF-3#PBF	LT1997IDF-3#TRPBF	19973	14-Lead (4mm × 4mm) Plastic DFN	-40°C to 85°C
LT1997HDF-3#PBF	LT1997HDF-3#TRPBF	19973	14-Lead (4mm × 4mm) Plastic DFN	-40°C to 125°C
LT1997IMS-3#PBF	LT1997IMS-3#TRPBF	19973	16-Lead Plastic MSOP	-40°C to 85°C
LT1997HMS-3#PBF	LT1997HMS-3#TRPBF	19973	16-Lead Plastic MSOP	-40°C to 125°C

\*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges. Parts ending with PBF are RoHS and WEEE compliant.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>  
For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range,  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  for I-grade parts,  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$  for H-grade parts, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ . Difference Amplifier Configuration,  $V^+ = 15\text{V}$ ,  $V^- = -15\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{REF}} = V_{\text{REF1}} = V_{\text{REF2}} = 0\text{V}$ .  $V_{\text{CMOP}}$  is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V <sub>OUT</sub> = ±10V G = 1	●	±0.001	±0.006 ±0.012	% %	
		G = 3	●	±0.001	±0.015 ±0.02	% %	
		G = 9	●	±0.002	±0.03 ±0.04	% %	
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V <sub>OUT</sub> = ±10V	●	±0.2	±1	ppm/°C	
GNL	Gain Nonlinearity	V <sub>OUT</sub> = ±10V	●	±1	±2 ±3	ppm ppm	
V <sub>OS</sub>	Op Amp Offset Voltage (Note 9)	V <sup>−</sup> < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	±20	±60 ±200	μV μV	
ΔV <sub>OS</sub> /ΔT	Op Amp Offset Voltage Drift (Note 6)	V <sup>−</sup> < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	±0.5	±1.5	μV/°C	
I <sub>B</sub>	Op Amp Input Bias Current	V <sup>−</sup> + 0.25V < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	−5 −15	±2 5 15	nA nA	
I <sub>OS</sub>	Op Amp Input Offset Current	V <sup>−</sup> + 0.25V < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	−3 −10	±0.5 3 10	nA nA	
R <sub>IN</sub>	Input Impedance (Note 8)	Common Mode G = 1	●	19	22.5	26	kΩ
		G = 3	●	12.6	15	17.4	kΩ
		G = 9	●	10.5	12.5	14.5	kΩ
		Differential G = 1	●	38	45	52	kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	G = 1, V <sub>CM</sub> = −28V to +26.5V	●	91 87	106		dB dB
		G = 3, V <sub>CM</sub> = −15V to +17.6V	●	90 86	99		dB dB
		G = 9, V <sub>CM</sub> = −15V to +14.7V	●	96 94	112		dB dB
		G = 1, V <sub>CM</sub> = −28V to +26.5V	●	91 87	101		dB dB
		G = 1, V <sub>CM</sub> = −90V to +90V, +INB = −INB = 0V, V <sub>S</sub> = ±25V	●	83 80	94		dB dB
		G = 1, V <sub>CM</sub> = −120V to +120V, +INC = −INC = 0V, V <sub>S</sub> = ±25V, T <sub>A</sub> = −40°C to 125°C	●	81 77	91		dB dB
CMRR	Common Mode Rejection Ratio, DF14 Package	G = 1, V <sub>CM</sub> = −160V to +160V, +INC = −INC = 0V, V <sub>S</sub> = ±25V, T <sub>A</sub> = −40°C to 85°C	●	81 78	91		dB dB
		G = 3, V <sub>CM</sub> = −15V to +17.6V	●	90 86	98		dB dB
		G = 9, V <sub>CM</sub> = −15V to +14.7V	●	96 94	103		dB dB
		+INA/−INA	●	−30	26.5	V	
		+INA/−INA, +INC/−INC Connected to Ground	●	−160	160	V	
		+INB/−INB	●	−15	17.6	V	
V <sub>CM</sub>	Input Voltage Range (Note 7)	+INC/−INC	●	−15	14.7	V	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range,  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  for I-grade parts,  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$  for H-grade parts, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ . Difference Amplifier Configuration,  $V^+ = 15\text{V}$ ,  $V^- = -15\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{REF}} = V_{\text{REF1}} = V_{\text{REF2}} = 0\text{V}$ .  $V_{\text{CMOP}}$  is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\Delta R/R$	Reference Divider Matching Error $\frac{\Delta R}{R} = \frac{R_{\text{REF1}} - R_{\text{REF2}}}{\left(\frac{R_{\text{REF1}} + R_{\text{REF2}}}{2}\right)}$	Available in MS16 Package Only	●	$\pm 0.001$	$\pm 0.006$ $\pm 0.012$	% %
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.65\text{V}$ to $\pm 25\text{V}$ , $V_{\text{CM}} = V_{\text{OUT}} = \text{Mid-Supply}$ (Note 9)	●	114	124	dB
$e_{\text{ni}}$	Input Referred Noise Voltage Density	$f = 1\text{kHz}$ $G = 1$ $G = 3$ $G = 9$		50 30 22		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
	Input Referred Noise Voltage	$f = 0.1\text{Hz}$ to $10\text{Hz}$ $G = 1$ $G = 3$ $G = 9$		1.4 1 0.8		$\mu\text{V}_{\text{P-P}}$ $\mu\text{V}_{\text{P-P}}$ $\mu\text{V}_{\text{P-P}}$
$V_{\text{OL}}$	Output Voltage Swing Low (Referred to $V^-$ )	No Load $I_{\text{SINK}} = 5\text{mA}$	● ●	100 280	150 500	mV mV
$V_{\text{OH}}$	Output Voltage Swing High (Referred to $V^+$ )	No Load $I_{\text{SOURCE}} = 5\text{mA}$	● ●	100 530	180 900	mV mV
$I_{\text{SC}}$	Short-Circuit Output Current	$50\Omega$ to $V^+$ $50\Omega$ to $V^-$	● ●	10 10	28 30	mA mA
SR	Slew Rate	$\Delta V_{\text{OUT}} = \pm 5\text{V}$	●	0.45	0.75	V/ $\mu\text{s}$
BW	Small Signal $-3\text{dB}$ Bandwidth	$G = 1$ $G = 3$ $G = 9$		1100 700 300		kHz kHz kHz
$t_s$	Settling Time	$G = 1$ 0.1%, $\Delta V_{\text{OUT}} = 10\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 10\text{V}$		14.6 95		$\mu\text{s}$ $\mu\text{s}$
		$G = 3$ 0.1%, $\Delta V_{\text{OUT}} = 10\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 10\text{V}$		13.6 29		$\mu\text{s}$ $\mu\text{s}$
		$G = 9$ 0.1%, $\Delta V_{\text{OUT}} = 10\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 10\text{V}$		13.8 29		$\mu\text{s}$ $\mu\text{s}$
$V_S$	Supply Voltage		●	3 3.3	50 50	V V
$t_{\text{ON}}$	Turn-On Time			16		$\mu\text{s}$
$V_{\text{IL}}$	SHDN Input Logic Low (Referred to $V^+$ )		●		-2.5	V
$V_{\text{IH}}$	SHDN Input Logic High (Referred to $V^+$ )		●	-1.2		V
$I_{\text{SHDN}}$	SHDN Pin Current		●	-10	-15	$\mu\text{A}$
$I_S$	Supply Current	Active, $V_{\text{SHDN}} \geq V^+ - 1.2\text{V}$ Active, $V_{\text{SHDN}} \geq V^+ - 1.2\text{V}$ Shutdown, $V_{\text{SHDN}} \leq V^+ - 2.5\text{V}$ Shutdown, $V_{\text{SHDN}} \leq V^+ - 2.5\text{V}$	● ● ●	350 20	400 600 25 70	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range,  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  for I-grade parts,  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$  for H-grade parts, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ . Difference Amplifier Configuration,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{REF}} = V_{\text{REF1}} = V_{\text{REF2}} = \text{Mid-Supply}$ .  $V_{\text{CMOP}}$  is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V <sub>OUT</sub> = 1V to 4V G = 1	●	±0.001	±0.006 ±0.012	% %	
		G = 3	●	±0.001	±0.015 ±0.02	% %	
		G = 9	●	±0.002	±0.03 ±0.04	% %	
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V <sub>OUT</sub> = 1V to 4V	●	±0.2	±1	ppm/°C	
GNL	Gain Nonlinearity	V <sub>OUT</sub> = 1V to 4V		±1		ppm	
V <sub>OS</sub>	Op Amp Offset Voltage (Note 9)	V <sup>−</sup> < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	±20	±60 ±200	μV μV	
ΔV <sub>OS</sub> /ΔT	Op Amp Offset Voltage Drift (Note 6)	V <sup>−</sup> < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	±0.5	±1.5	μV/°C	
I <sub>B</sub>	Op Amp Input Bias Current	V <sup>−</sup> + 0.25V < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	−5 −15	±2 5 15	nA nA	
I <sub>OS</sub>	Op Amp Input Offset Current	V <sup>−</sup> + 0.25V < V <sub>CMOP</sub> < V <sup>+</sup> − 1.75V	●	−3 −10	±0.5 3 10	nA nA	
R <sub>IN</sub>	Input Impedance (Note 8)	Common Mode G = 1	●	19	22.5	26	kΩ
		G = 3	●	12.6	15	17.4	kΩ
		G = 9	●	10.5	12.5	14.5	kΩ
		Differential G = 1	●	38	45	52	kΩ
		G = 3	●	12.6	15	17.4	kΩ
		G = 9	●	4.2	5	5.8	kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	G = 1, V <sub>CM</sub> = −2.5V to +4.0V	●	90 88	100	dB dB	
		G = 3, V <sub>CM</sub> = 0V to +3.5V	●	90 87	103	dB dB	
		G = 9, V <sub>CM</sub> = 0V to +3.3V	●	96 94	108	dB dB	
CMRR	Common Mode Rejection Ratio, DF14 Package	G = 1, V <sub>CM</sub> = −2.5V to +4.0V	●	90 88	96	dB dB	
		G = 3, V <sub>CM</sub> = 0V to +3.5V	●	90 87	101	dB dB	
		G = 9, V <sub>CM</sub> = 0V to +3.3V	●	96 94	107	dB dB	
ΔR/R	Reference Divider Matching Error $\frac{\Delta R}{R} = \frac{R_{REF1} - R_{REF2}}{\left(\frac{R_{REF1} + R_{REF2}}{2}\right)}$	Available in MS16 Package Only	●	±0.001	±0.006 ±0.012	% %	
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> = ±1.65V to ±25V, V <sub>CM</sub> = V <sub>OUT</sub> = Mid-Supply (Note 9)	●	114	124	dB	
e <sub>ni</sub>	Input Referred Noise Voltage Density	f = 1kHz G = 1 G = 3 G = 9			50 30 22	nV/√Hz nV/√Hz nV/√Hz	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range,  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$  for I-grade parts,  $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$  for H-grade parts, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ . Difference Amplifier Configuration,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{REF}} = V_{\text{REF1}} = V_{\text{REF2}} = \text{Mid-Supply}$ .  $V_{\text{CMOP}}$  is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Input Referred Noise Voltage	$f = 0.1\text{Hz to } 10\text{Hz}$ $G = 1$ $G = 3$ $G = 9$		1.4 1 0.8		$\mu\text{V}_{\text{P-P}}$ $\mu\text{V}_{\text{P-P}}$ $\mu\text{V}_{\text{P-P}}$
$V_{\text{OL}}$	Output Voltage Swing Low (Referred to $V^-$ )	No Load $I_{\text{SINK}} = 5\text{mA}$	● ●	15 280	50 500	mV mV
$V_{\text{OH}}$	Output Voltage Swing High (Referred to $V^+$ )	No Load $I_{\text{SOURCE}} = 5\text{mA}$	● ●	15 450	50 800	mV mV
$I_{\text{SC}}$	Short-Circuit Output Current	$50\Omega$ to $V^+$ $50\Omega$ to $V^-$	● ●	10 10	27 25	mA mA
SR	Slew Rate	$\Delta V_{\text{OUT}} = 3\text{V}$	●	0.45	0.75	V/ $\mu\text{s}$
BW	Small signal $-3\text{dB}$ Bandwidth	$G = 1$ $G = 3$ $G = 9$		1100 700 300		kHz kHz kHz
$t_{\text{S}}$	Settling Time	$G = 1$ 0.1%, $\Delta V_{\text{OUT}} = 2\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 2\text{V}$		5.4 91		$\mu\text{s}$ $\mu\text{s}$
		$G = 3$ 0.1%, $\Delta V_{\text{OUT}} = 2\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 2\text{V}$		6 21		$\mu\text{s}$ $\mu\text{s}$
		$G = 9$ 0.1%, $\Delta V_{\text{OUT}} = 2\text{V}$ 0.01%, $\Delta V_{\text{OUT}} = 2\text{V}$		7 36		$\mu\text{s}$ $\mu\text{s}$
$V_{\text{S}}$	Supply Voltage		● 3.3		50 50	V V
$t_{\text{ON}}$	Turn-On Time			22		$\mu\text{s}$
$V_{\text{IL}}$	SHDN Input Logic Low (Referred to $V^+$ )		●		-2.5	V
$V_{\text{IH}}$	SHDN Input Logic High (Referred to $V^+$ )		●	-1.2		V
$I_{\text{SHDN}}$	SHDN Pin Current		●	-10	-15	$\mu\text{A}$
$I_{\text{S}}$	Supply Current	Active, $V_{\text{SHDN}} \geq V^+ - 1.2\text{V}$ Active, $V_{\text{SHDN}} \geq V^+ - 1.2\text{V}$ Shutdown, $V_{\text{SHDN}} \leq V^+ - 2.5\text{V}$ Shutdown, $V_{\text{SHDN}} \leq V^+ - 2.5\text{V}$	● ● ● ●	330 330 15	370 525 20 40	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** See “Common Mode Voltage Range” and “High Common Mode Voltage Difference Amplifiers” in the Applications Information section of this data sheet for other considerations when taking +INA/-INA pins to  $\pm 160\text{V}$  and +INB/-INB/+INC/-INC pins to  $+80\text{V}$ .

**Note 3:** A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply, input voltages and the output current.

**Note 4:** The LT1997I-3 is guaranteed functional over the operating temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The LT1997H-3 is guaranteed functional over the operating temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Note 5:** The LT1997I-3 is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The LT1997H-3 is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Note 6:** This parameter is not 100% tested.

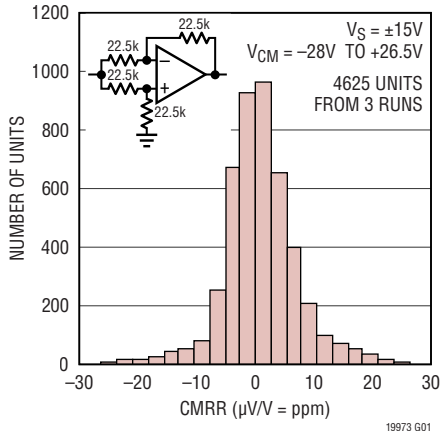
**Note 7:** The Input Voltage Range numbers specified in the table guarantee that the internal op amp operates in its normal operating region. The Input voltage range can be significantly higher if the internal op amp operates in its Over-The-Top® operating region. See “Common Mode Voltage Range” in the Applications Information section to determine the valid input voltage range under various operating conditions.

**Note 8:** Input impedance is tested by a combination of direct measurements and correlation to the CMRR and gain error tests.

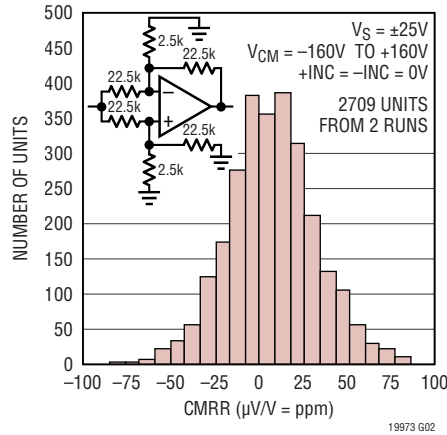
**Note 9:** Offset voltage, offset voltage drift and PSRR are defined as referred to the internal op amp. You can calculate output offset as follows. In the case of balanced source resistance,  $V_{\text{OS,OUT}} = (V_{\text{OS}} \cdot \text{NOISEGAIN}) + (I_{\text{OS}} \cdot 22.5\text{k}) + (I_{\text{B}} \cdot 22.5\text{k} \cdot (1 - R_{\text{P}}/R_{\text{N}}))$  where  $R_{\text{P}}$  and  $R_{\text{N}}$  are the total resistance at the op amp positive and negative terminal, respectively.

# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

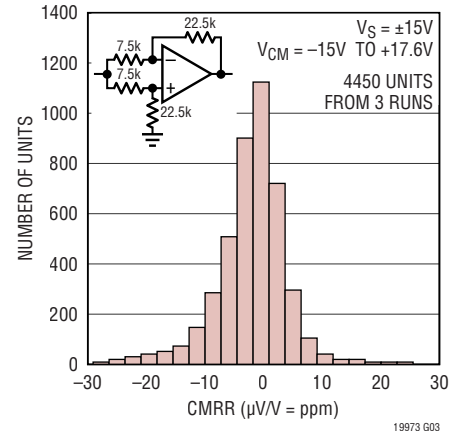
**Typical Distribution of CMRR  
(G = 1)**



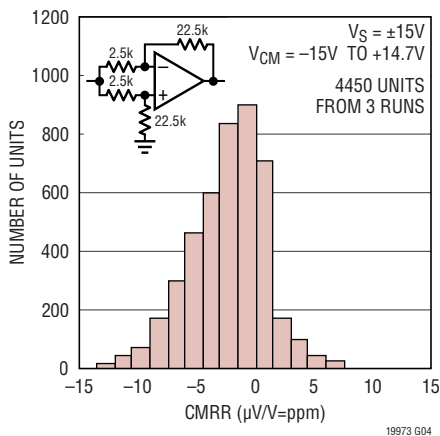
**Typical Distribution of CMRR  
(G = 1)**



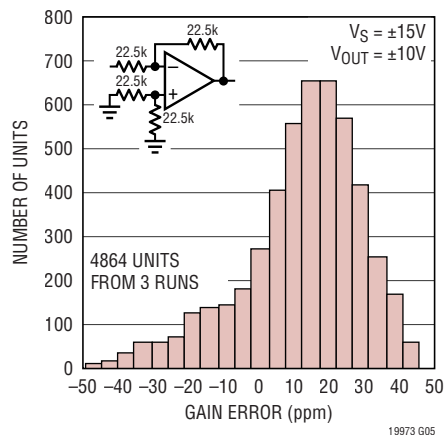
**Typical Distribution of CMRR  
(G = 3)**



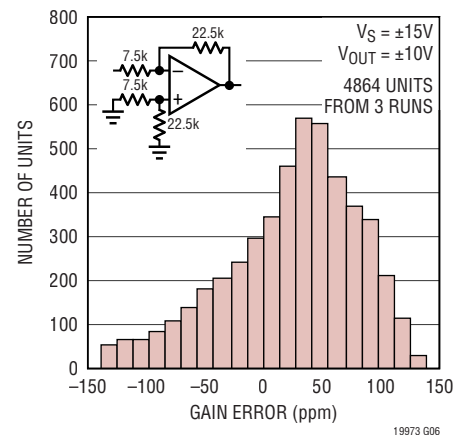
**Typical Distribution of CMRR  
(G = 9)**



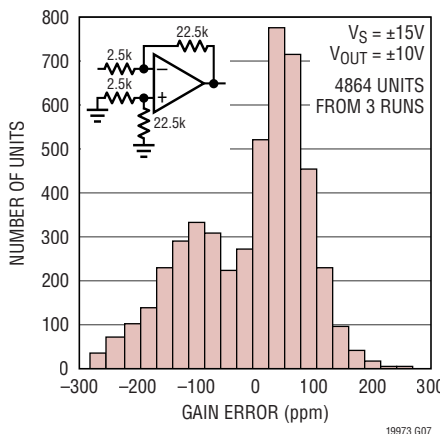
**Typical Distribution of Gain Error  
(G = 1)**



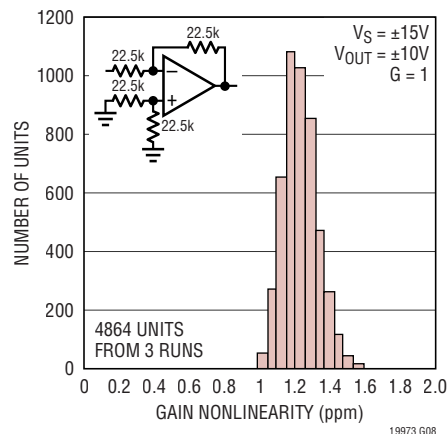
**Typical Distribution of Gain Error  
(G = 3)**



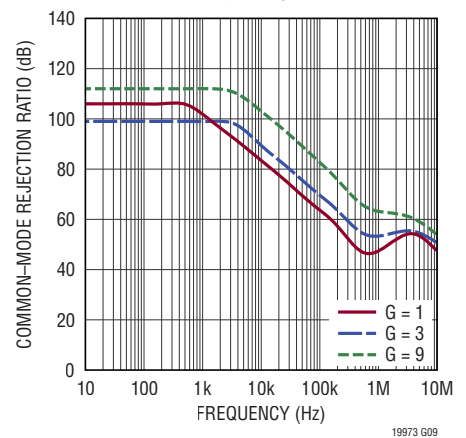
**Typical Distribution of Gain Error  
(G = 9)**



**Typical Distribution of Gain Nonlinearity**

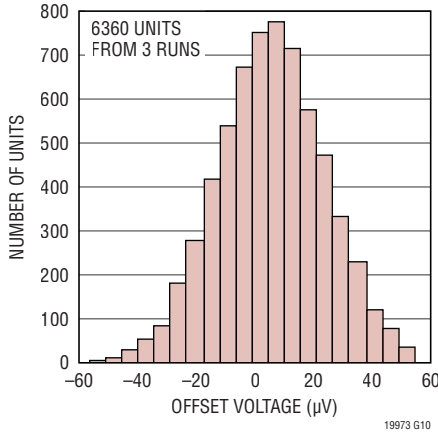


**CMRR vs Frequency**

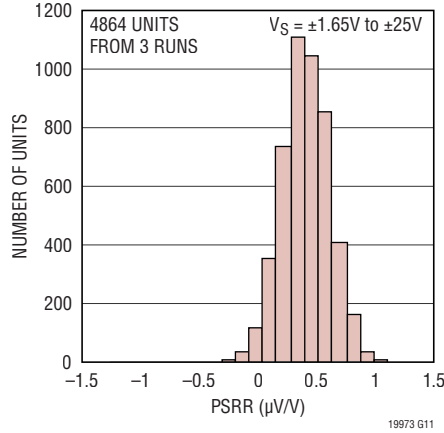


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

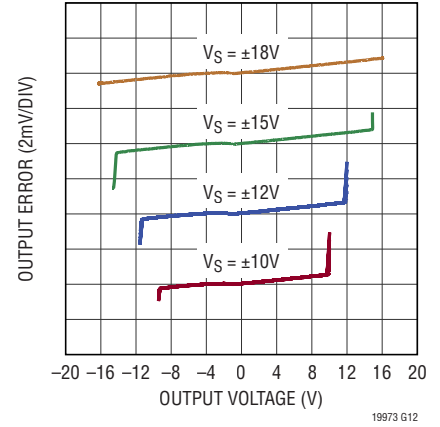
**Typical Distribution of Op Amp Offset Voltage**



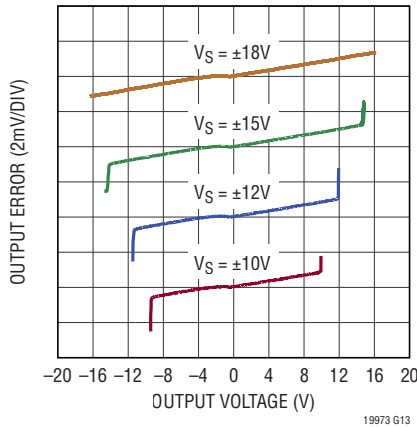
**Typical Distribution of Op Amp PSRR**



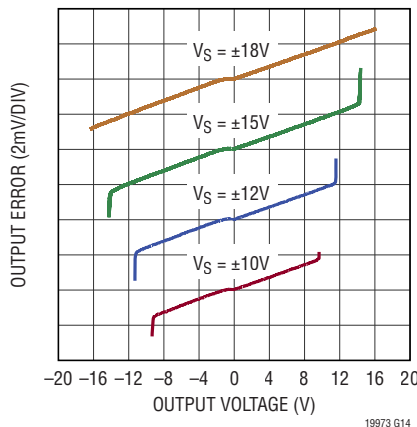
**Typical Gain Error for  $R_L = 10\text{k}\Omega$   $G = 1$  (Curves Offset for Clarity)**



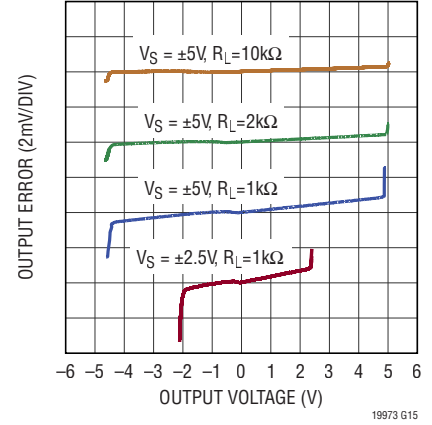
**Typical Gain Error for  $R_L = 5\text{k}\Omega$   $G = 1$  (Curves Offset for Clarity)**



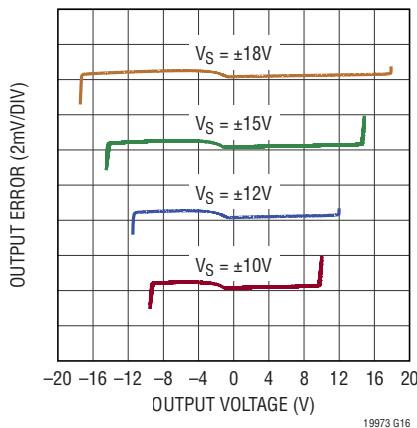
**Typical Gain Error for  $R_L = 2\text{k}\Omega$   $G = 1$  (Curves Offset for Clarity)**



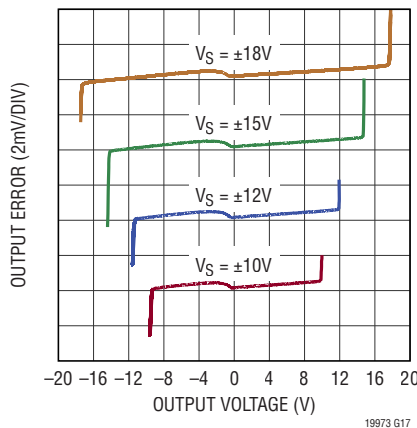
**Typical Gain Error for Low Supply Voltages,  $G = 1$  (Curves Offset for Clarity)**



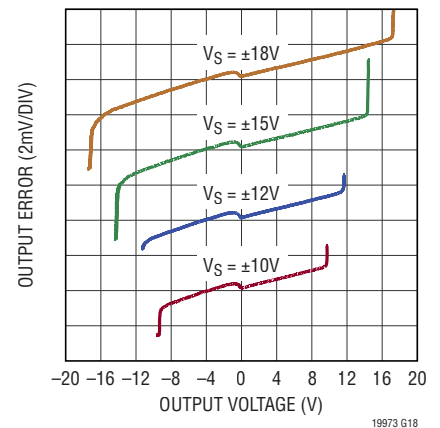
**Typical Gain Error for  $R_L = 10\text{k}\Omega$   $G = 3$  (Curves Offset for Clarity)**



**Typical Gain Error for  $R_L = 5\text{k}\Omega$   $G = 3$  (Curves Offset for Clarity)**

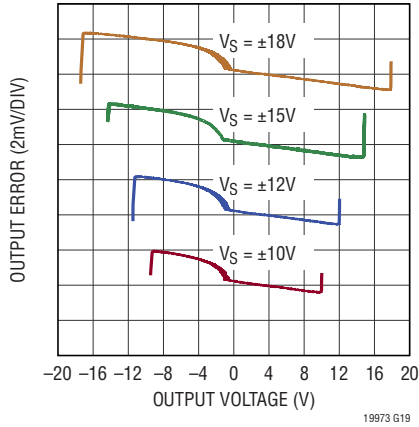


**Typical Gain Error for  $R_L = 2\text{k}\Omega$   $G = 3$  (Curves Offset for Clarity)**

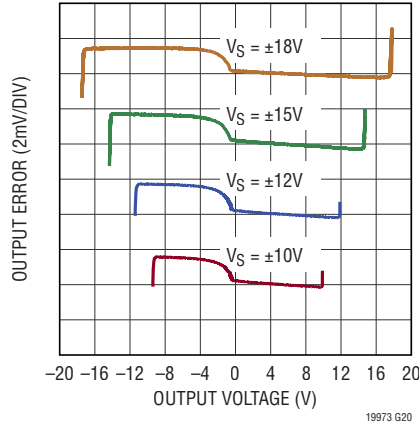


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

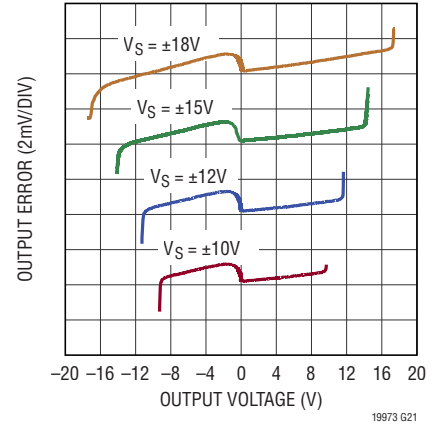
**Typical Gain Error for  $R_L = 10\text{k}\Omega$   
 $G = 9$  (Curves Offset for Clarity)**



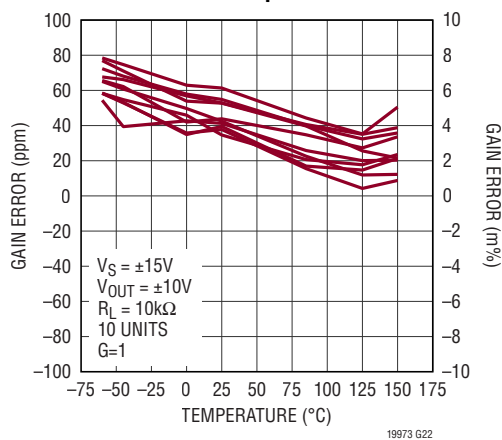
**Typical Gain Error for  $R_L = 5\text{k}\Omega$   
 $G = 9$  (Curves Offset for Clarity)**



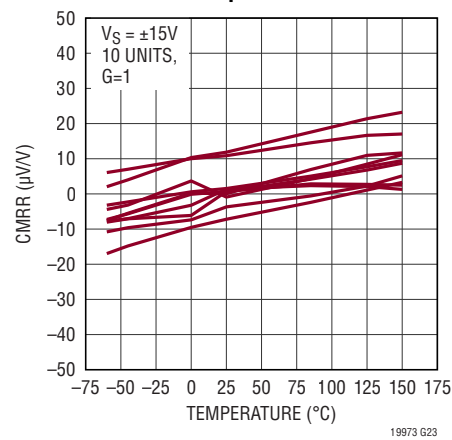
**Typical Gain Error for  $R_L = 2\text{k}\Omega$   
 $G = 9$  (Curves Offset for Clarity)**



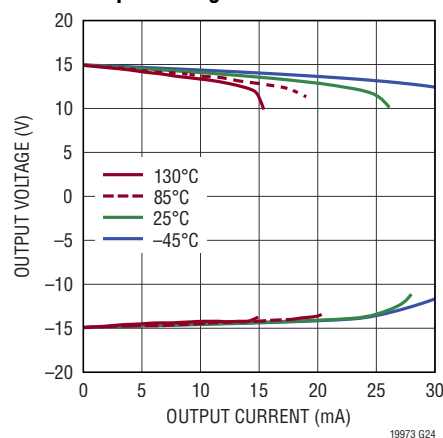
**Gain Error vs Temperature**



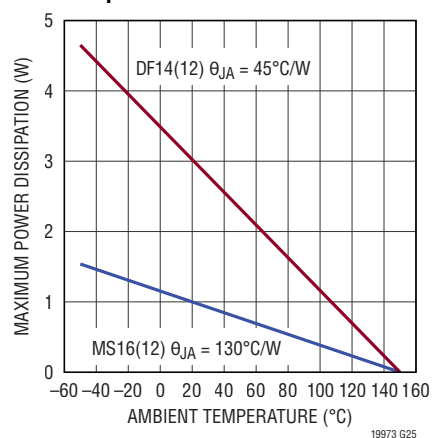
**CMRR vs Temperature**



**Output Voltage vs Load Current**



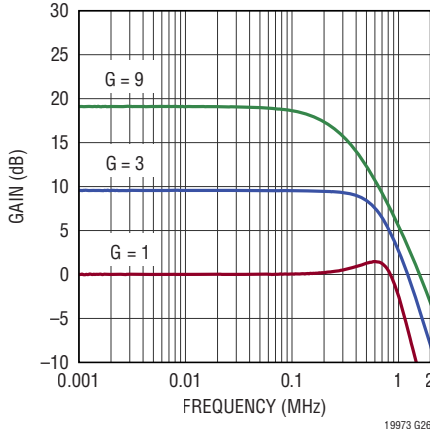
**Maximum Power Dissipation vs Temperature**



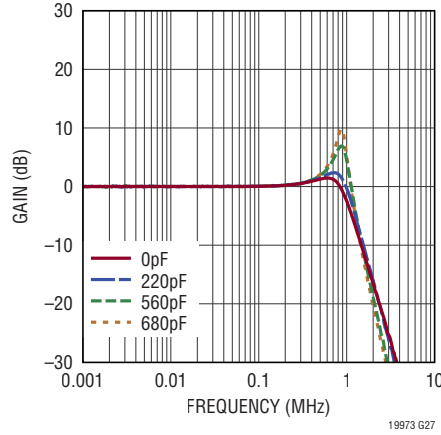


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

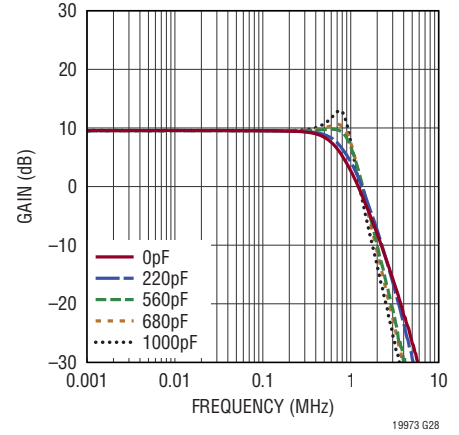
**Gain vs Frequency**



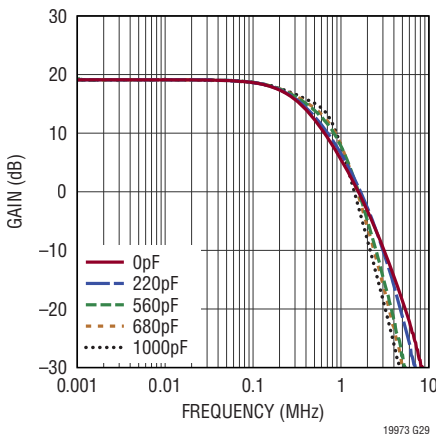
**Frequency Response vs Capacitive Load ( $G = 1$ )**



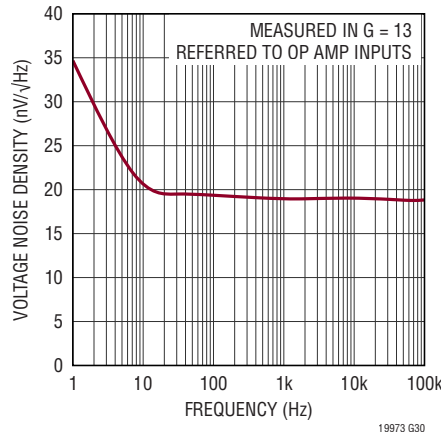
**Frequency Response vs Capacitive Load ( $G = 3$ )**



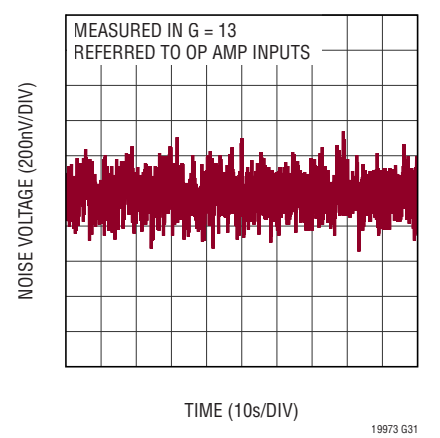
**Frequency Response vs Capacitive Load ( $G = 9$ )**



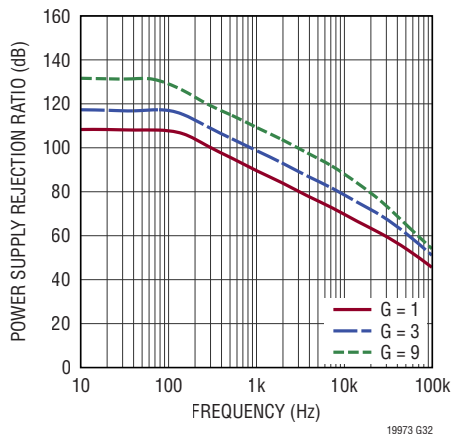
**Op Amp Noise Density vs Frequency**



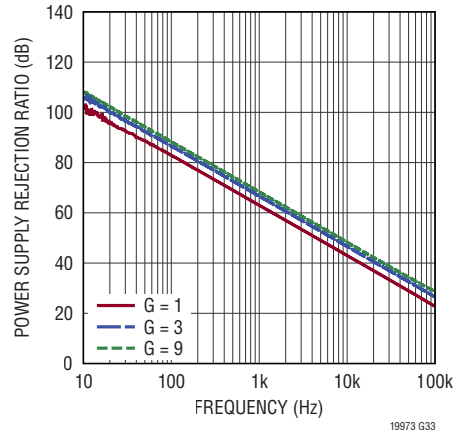
**0.1Hz to 10Hz Noise**



**Positive PSRR vs Frequency**

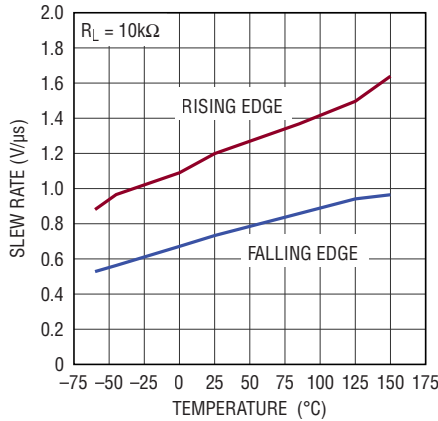


**Negative PSRR vs Frequency**

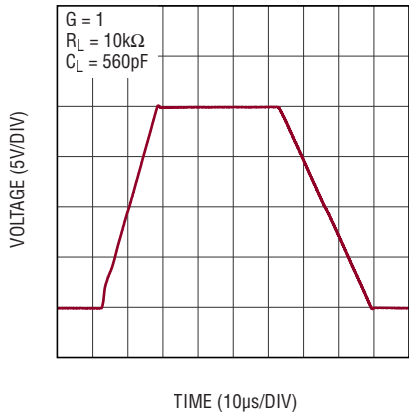


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

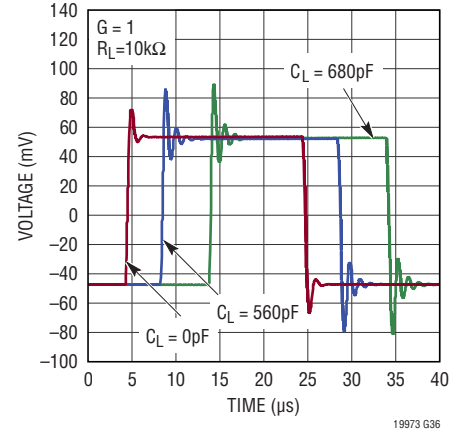
**Slew Rate vs Temperature**



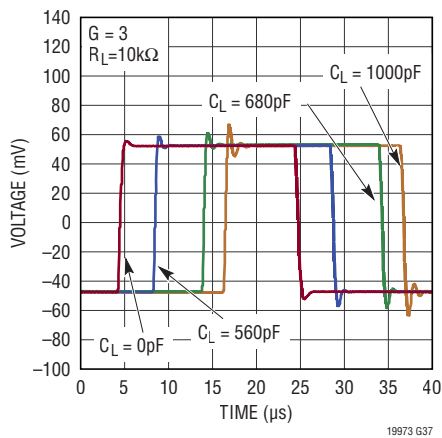
**Large-Signal Step Response**



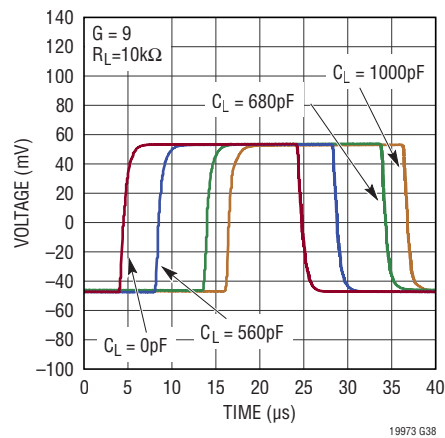
**Small-Signal Step Response**



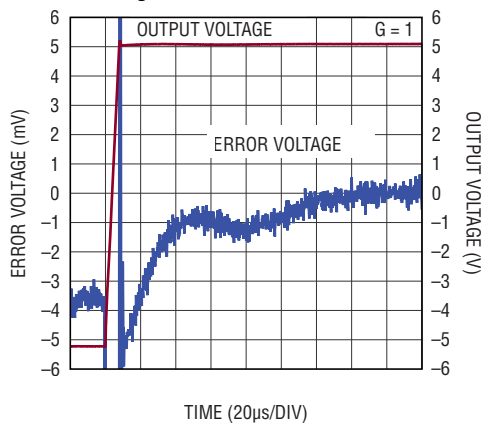
**Small-Signal Step Response**



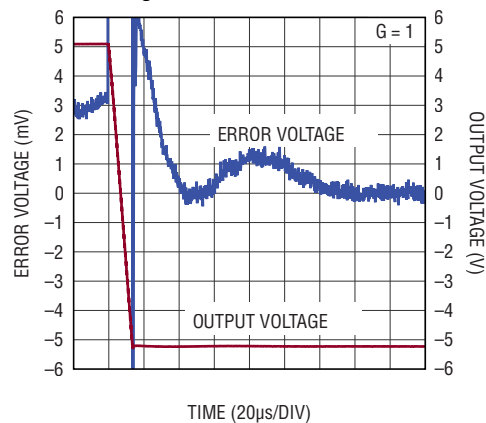
**Small-Signal Step Response**



**Settling Time**

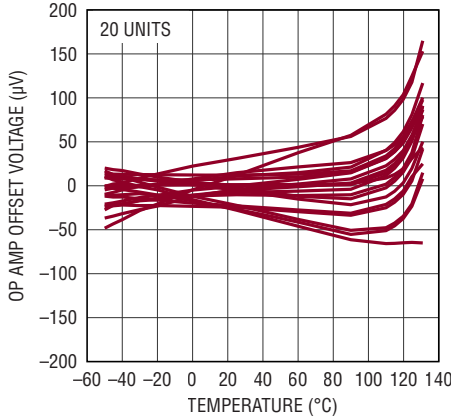


**Settling Time**

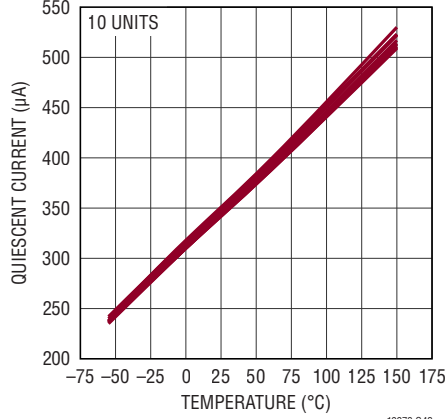


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , Difference Amplifier configuration, unless otherwise noted.

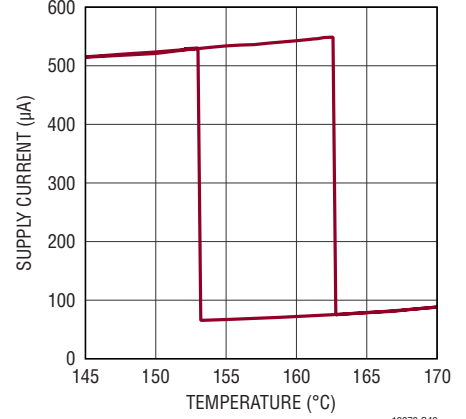
**Op Amp Offset Voltage vs Temperature**



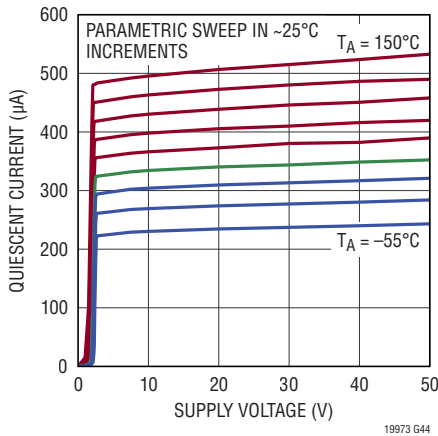
**Quiescent Current vs Temperature**



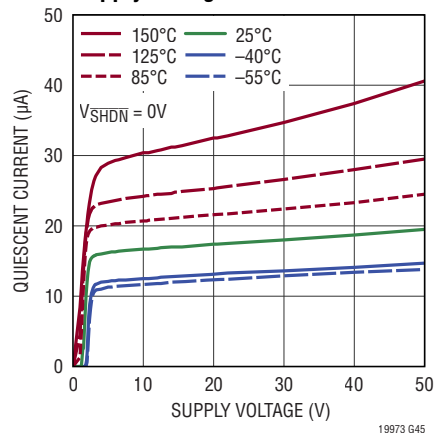
**Thermal Shutdown vs Hysteresis**



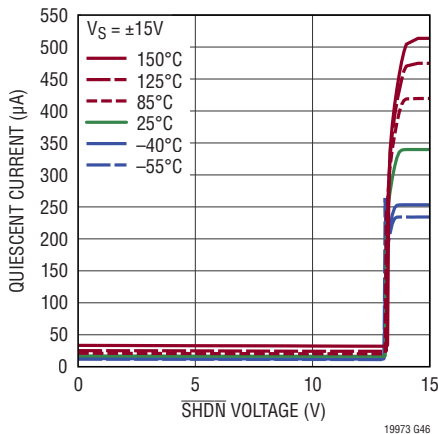
**Quiescent Current vs Supply Voltage**



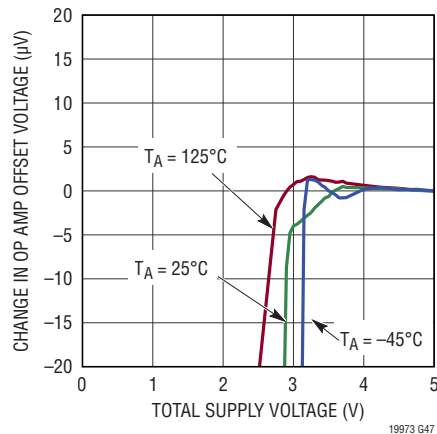
**Shutdown Quiescent Current vs Supply Voltage**



**Quiescent Current vs SHDN Voltage**



**Minimum Supply Voltage**



## PIN FUNCTIONS (DFN/MSOP)

**V<sup>+</sup> (Pin 9/Pin 11):** Positive Supply Pin.

**V<sup>-</sup> (EXPOSED PAD Pin 15/Pin 8):** Negative Supply Pin.

**OUT (Pin 8/Pin 9):** Output Pin.

**+INA (Pin 1/Pin 1):** Noninverting Gain-of-1 Input Pin. Connects a 22.5k internal resistor to the internal op amp's noninverting input.

**+INB (Pin 3/Pin 3):** Noninverting Gain-of-3 Input Pin. Connects a 7.5k internal resistor to the internal op amp's noninverting input.

**+INC (Pin 5/Pin 5):** Noninverting Gain-of-9 Input Pin. Connects a 2.5k internal resistor to the internal op amp's noninverting input.

**-INA (Pin 14/Pin 16):** Inverting Gain-of-1 input Pin. Connects a 22.5k internal resistor to the internal op amp's inverting input.

**-INB (Pin 12/Pin 14):** Inverting Gain-of-3 input Pin. Connects a 7.5k internal resistor to the internal op amp's inverting input.

**-INC (Pin 10/Pin 12):** Inverting Gain-of-9 input Pin. Connects a 2.5k internal resistor to the internal op amp's inverting input.

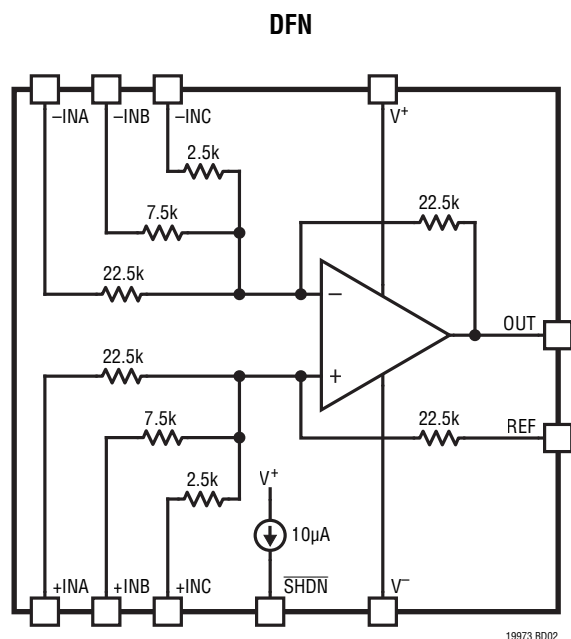
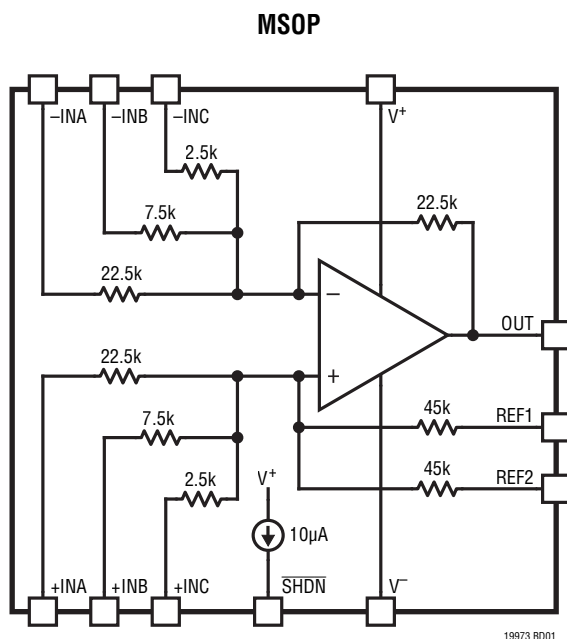
**REF (Pin 7/NA):** Reference Input Pin. Sets the output level when the difference between the inputs is zero.

**REF1 (NA/Pin 6):** Reference 1 Input Pin. With REF2, sets the output level when the difference between the inputs is zero.

**REF2 (NA/Pin 7):** Reference 2 Input. Pin. With REF1, sets the output level when the difference between the inputs is zero.

**SHDN (Pin 6/Pin 10):** Shutdown Pin. Amplifier is active when this pin is tied to V<sup>+</sup> or left floating. Pulling the pin >2.5V below V<sup>+</sup> causes the amplifier to enter a low power state.

## BLOCK DIAGRAM





## APPLICATIONS INFORMATION

By superposition we can write:

$$V_{CMOP} = V_{EXT} \cdot \frac{R_F}{R_F + R_G} + V_{REF} \cdot \frac{R_G}{R_F + R_G}$$

Or, solving for  $V_{EXT}$ :

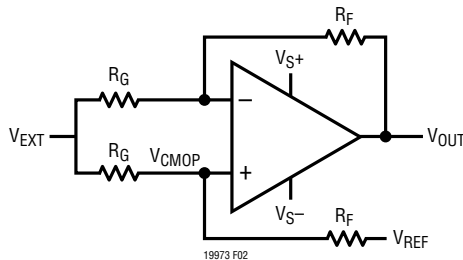
$$V_{EXT} = V_{CMOP} \cdot \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \cdot \frac{R_G}{R_F}$$

But valid  $V_{CMOP}$  voltages are limited to  $V_{S+} - 1.75V$  ( $V_{S-} + 76V$  OTT) on the high side and  $V_{S-}$  on the low side, so:

$$MAX V_{EXT} = (V_{S+} - 1.75) \cdot \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \cdot \frac{R_G}{R_F}$$

and:

$$MIN V_{EXT} = (V_{S-}) \cdot \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \cdot \frac{R_G}{R_F}$$



**Figure 2. Calculating the Common Mode Input Voltage Range**

Exceeding the  $MAX V_{EXT}$  limit will cause the amplifier to transition into the Over-The-Top region. The maximum input voltage for the Over-The-Top region is:

$$MAX V_{EXTOTT} = (V_{S-} + 76) \cdot \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \cdot \frac{R_G}{R_F}$$

Keep in mind that the above  $MAX$  and  $MIN$  values for input voltage range should not exceed the allowed voltage range specified earlier for LT1997-3's input pins.

The negative inputs are not limited by the internal op amp common mode range ( $V_{CMOP}$ ) because they do not affect it.

They are limited by the output swing of the amplifier (and obviously by the allowed voltage range for the input pins).

### Over-The-Top Operation

When the input common mode voltage of the internal op amp ( $V_{CMOP}$ ) in the LT1997-3 is biased near or above the  $V^+$  supply, the op amp is operating in the Over-The-Top (OTT) region. The op amp continues to operate with an input common mode voltage of up to 76V above  $V^-$  (regardless of the positive power supply voltage  $V^+$ ), but its performance is degraded. The op amp's input bias currents change from under  $\pm 2nA$  to  $14\mu A$ . The op amp's input offset current rises to  $\pm 50nA$ , which adds  $\pm 1.1mV$  to the output offset voltage.

In addition, when operating in the Over-The-Top region, the differential input impedance decreases from  $1M\Omega$  in normal operation to approximately  $3.7k\Omega$  in Over-The-Top operation. This resistance appears across the summing nodes of the internal op amp and boosts noise and offset while decreasing speed. Noise and offset will increase by between 75% and 450% depending on the gain setting. The bandwidth will be reduced by 2X to 5.5X. For more detail on Over-The-Top operation, consult the LT6015 data sheet.

### The Classical Noninverting Amplifier: High Input Z

A common op amp configuration enabled by the LT1997-3 is the noninverting amplifier. Figure 3 shows the textbook representation of the circuit on the top. The LT1997-3 is shown on the bottom configured in a precision gain of 5.5. One of the benefits of the noninverting op amp configuration is that the input impedance is extremely high. The LT1997-3 maintains this benefit. A large number of gains can be achieved with the LT1997-3 in the noninverting configuration. The complete list of such Hi-Z input noninverting gain configuration is shown in Table 1. Many of these are also represented in Figure 4 in schematic form. Note that the positive inputs are connected such that the source impedance seen by the positive and negative inputs of the internal op amp are equal. This minimizes the offset voltage due to the input bias current of the op amp. The noise gain and amplifier's gain in the noninverting configuration are identical.

APPLICATIONS INFORMATION

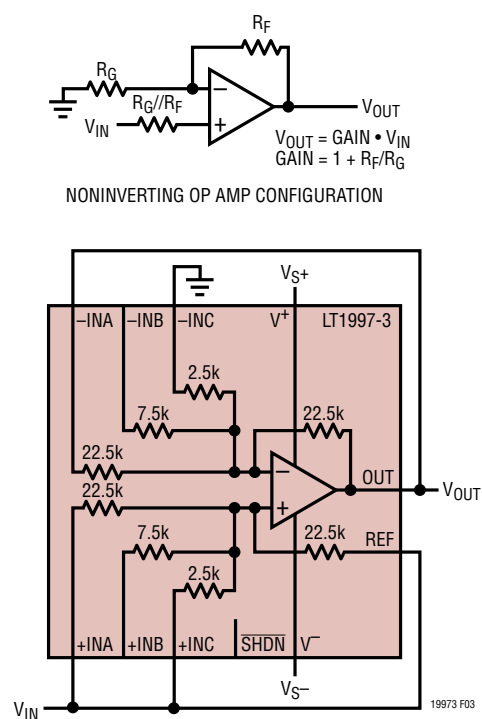


Figure 3. The LT1997-3 Configured as a Noninverting Op Amp

Table 1. Configuring the Negative Pins for Noninverting Gains. The Positive Inputs Are Driven as Shown in the Examples in Figure 4

Gain	Negative Input Connections		
	-INA	-INB	-INC
1	$V_{OUT}$	$V_{OUT}$	$V_{OUT}$
1.077	GND	$V_{OUT}$	$V_{OUT}$
1.1	GND	OPEN	$V_{OUT}$
1.25	GND	$V_{OUT}$	OPEN
1.273	$V_{OUT}$	GND	$V_{OUT}$
1.3	OPEN	GND	$V_{OUT}$
1.4	GND	GND	$V_{OUT}$
2	GND	OPEN	OPEN
2.5	$V_{OUT}$	GND	OPEN
2.8	$V_{OUT}$	$V_{OUT}$	GND
3.25	OPEN	$V_{OUT}$	GND
3.5	GND	$V_{OUT}$	GND
4	OPEN	GND	OPEN
5	GND	GND	OPEN
5.5	$V_{OUT}$	OPEN	GND
7	$V_{OUT}$	GND	GND
10	OPEN	OPEN	GND
11	GND	OPEN	GND
13	OPEN	GND	GND
14	GND	GND	GND

# APPLICATIONS INFORMATION

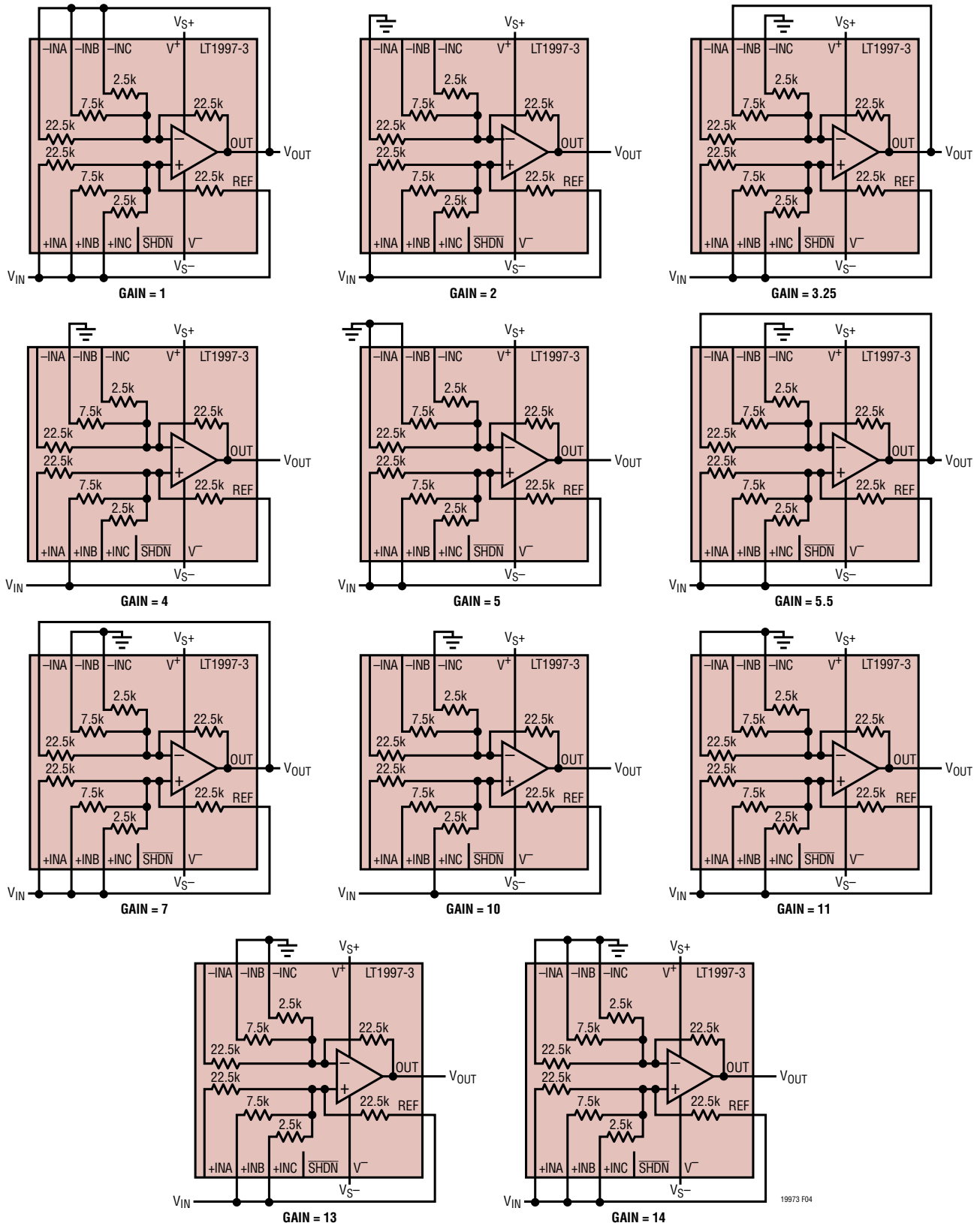


Figure 4. Some Implementations of Classical Noninverting Gains Using the LT1997-3. High Input Z is Maintained



APPLICATIONS INFORMATION

Attenuation

The positive input resistors can be configured to attenuate the input signal (Figure 5). This allows a trade-off to be made between input range and precision. Attenuating the input can prevent the op amp from entering the less precise Over-the-Top operating region at the cost of decreasing the output signal. The four positive resistors ( $R_{+INA}$ ,  $R_{+INB}$ ,  $R_{+INC}$ ,  $R_{REF}$ ) can be arranged to make many precise input attenuators. These are shown in Table 2.

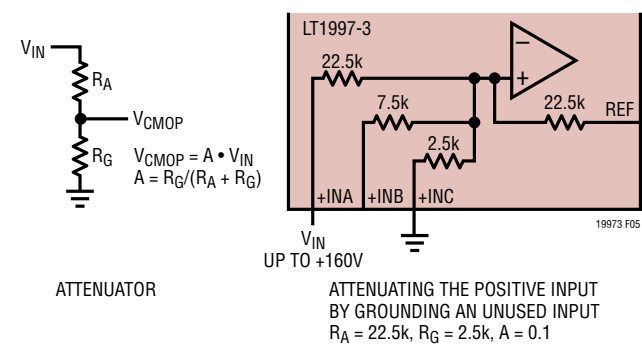


Figure 5. The Input of the LT1997-3 Can Be Attenuated to Increase the Usable Input Range. The +INA Input Can Be Taken to ±160V.

The attenuations and noninverting gains are set independently and can be combined to produce even more gain options. 346 unique gains between 0.0714 and 14 (Figure 6) can be realized. When using the positive side resistors as an attenuator, the benefit of canceling input bias current effects on offset voltage reduces. The impedance seen by the two op amp input nodes will not be identical.

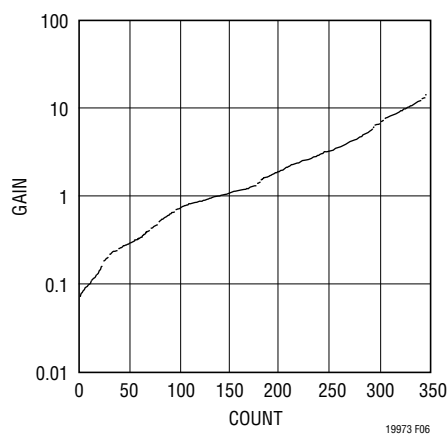


Figure 6. Many Unique Gains Can Be Achieved by Combining Attenuation with Noninverting Gain

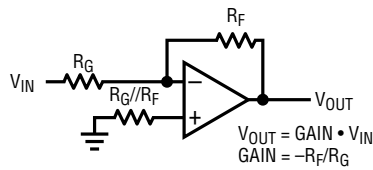
Table 2. Configuring the Positive Pins for Various Attenuations

Gain	Positive Input Connections			
	+INA	+INB	+INC	REF
0.0714	$V_{IN}$	GND	GND	GND
0.0769	$V_{IN}$	GND	GND	OPEN
0.0909	$V_{IN}$	OPEN	GND	GND
0.1	$V_{IN}$	OPEN	GND	OPEN
0.143	$V_{IN}$	GND	GND	$V_{IN}$
0.182	$V_{IN}$	OPEN	GND	$V_{IN}$
0.2	$V_{IN}$	GND	OPEN	GND
0.214	GND	$V_{IN}$	GND	GND
0.231	OPEN	$V_{IN}$	GND	GND
0.25	$V_{IN}$	GND	OPEN	OPEN
0.286	$V_{IN}$	$V_{IN}$	GND	GND
0.308	$V_{IN}$	$V_{IN}$	GND	OPEN
0.357	$V_{IN}$	$V_{IN}$	GND	$V_{IN}$
0.4	$V_{IN}$	GND	OPEN	$V_{IN}$
0.5	$V_{IN}$	OPEN	OPEN	GND
0.6	GND	$V_{IN}$	OPEN	GND
0.643	GND	GND	$V_{IN}$	GND
0.692	OPEN	GND	$V_{IN}$	GND
0.714	$V_{IN}$	GND	$V_{IN}$	GND
0.75	OPEN	$V_{IN}$	OPEN	GND
0.769	$V_{IN}$	GND	$V_{IN}$	OPEN
0.786	$V_{IN}$	GND	$V_{IN}$	$V_{IN}$
0.8	$V_{IN}$	$V_{IN}$	OPEN	GND
0.818	GND	OPEN	$V_{IN}$	GND
0.857	GND	$V_{IN}$	$V_{IN}$	GND
0.9	OPEN	OPEN	$V_{IN}$	GND
0.909	$V_{IN}$	OPEN	$V_{IN}$	GND
0.923	OPEN	$V_{IN}$	$V_{IN}$	GND
0.929	$V_{IN}$	$V_{IN}$	$V_{IN}$	GND
1	$V_{IN}$	$V_{IN}$	$V_{IN}$	$V_{IN}$

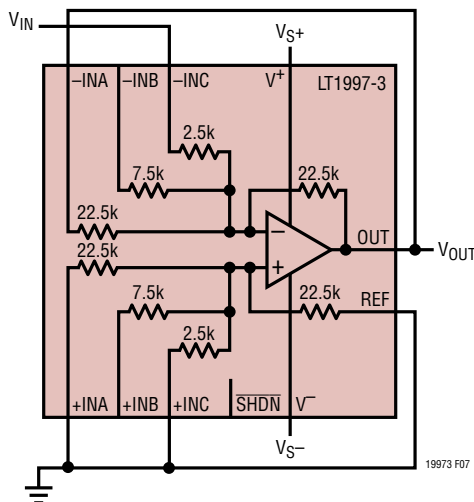
## APPLICATIONS INFORMATION

### The Inverting Configuration

The inverting amplifier, shown in Figure 7, is another classical op amp configuration. The circuit is actually identical to the noninverting amplifier of Figure 3, except that  $V_{IN}$  and GND have been swapped. The list of available gains is shown in Table 3, and some of the circuits are shown in Figure 8. Noise gain is  $1+|Gain|$ , as is the usual case for inverting amplifiers. For the best DC precision, match the source impedances seen by the op amp inputs.



INVERTING OP AMP CONFIGURATION



INVERTING OP AMP CONFIGURATION  
IMPLEMENTED WITH THE LT1997-3,  $R_F = 11.25k$ ,  $R_G = 2.5k$ ,  $GAIN = -4.5$

GAIN IS ACHIEVED BY GROUNDING, FLOATING OR FEEDING BACK  
THE AVAILABLE RESISTORS TO ARRIVE AT THE DESIRED  $R_F$  AND  $R_G$

Table 3. Configuring the Negative Pins for Inverting Gains

Gain	Negative Input Connections		
	-INA	-INB	-INC
-0.077	$V_{IN}$	$V_{OUT}$	$V_{OUT}$
-0.1	$V_{IN}$	OPEN	$V_{OUT}$
-0.25	$V_{IN}$	$V_{OUT}$	OPEN
-0.273	$V_{OUT}$	$V_{IN}$	$V_{OUT}$
-0.3	OPEN	$V_{IN}$	$V_{OUT}$
-0.4	$V_{IN}$	$V_{IN}$	$V_{OUT}$
-1	$V_{IN}$	OPEN	OPEN
-1.5	$V_{OUT}$	$V_{IN}$	OPEN
-1.8	$V_{OUT}$	$V_{OUT}$	$V_{IN}$
-2.25	OPEN	$V_{OUT}$	$V_{IN}$
-2.5	$V_{IN}$	$V_{OUT}$	$V_{IN}$
-3	OPEN	$V_{IN}$	OPEN
-4	$V_{IN}$	$V_{IN}$	OPEN
-4.5	$V_{OUT}$	OPEN	$V_{IN}$
-6	$V_{OUT}$	$V_{IN}$	$V_{IN}$
-9	OPEN	OPEN	$V_{IN}$
-10	$V_{IN}$	OPEN	$V_{IN}$
-12	OPEN	$V_{IN}$	$V_{IN}$
-13	$V_{IN}$	$V_{IN}$	$V_{IN}$

Figure 7. The LT1997-3 Configured as an Inverting Op Amp

# APPLICATIONS INFORMATION

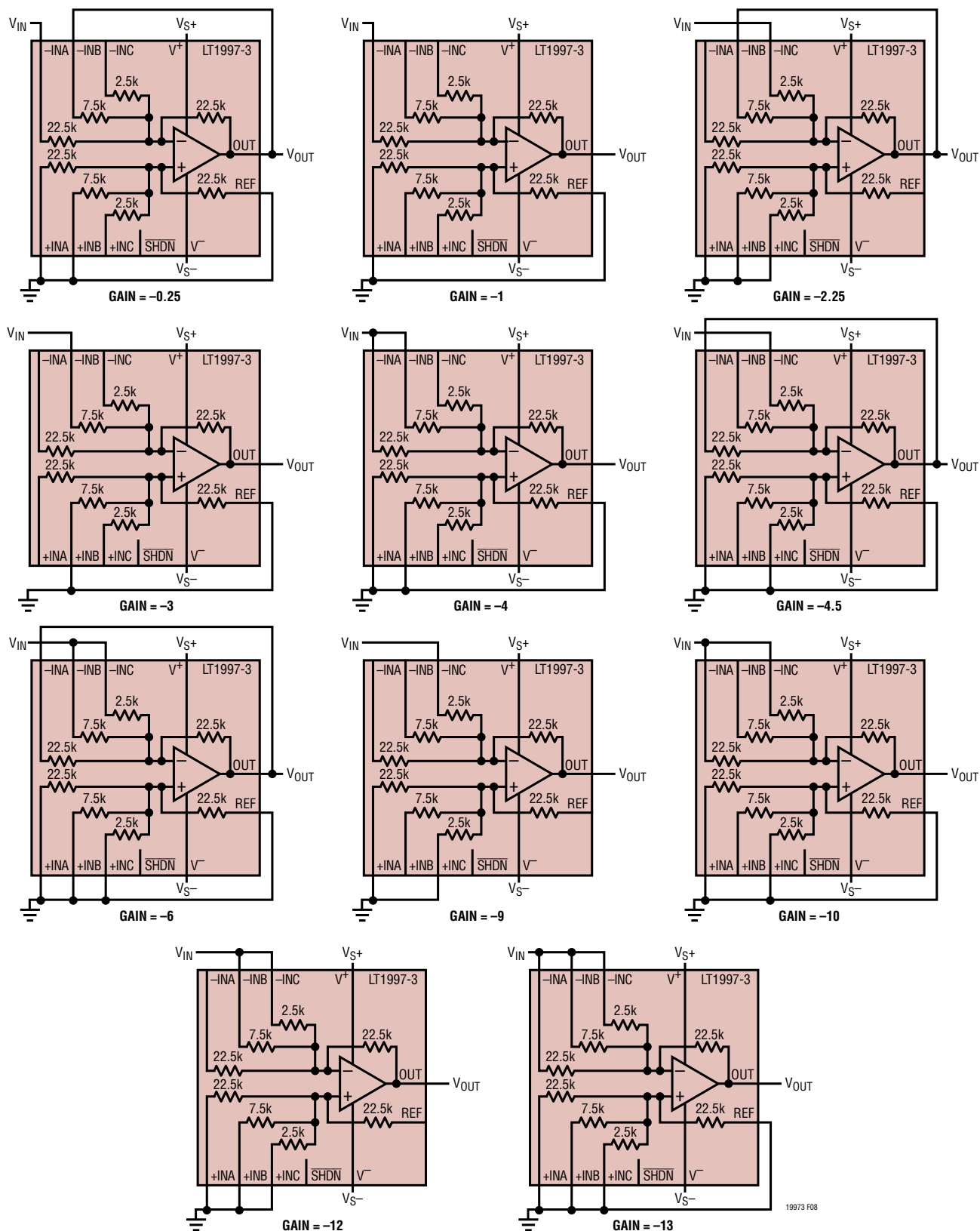
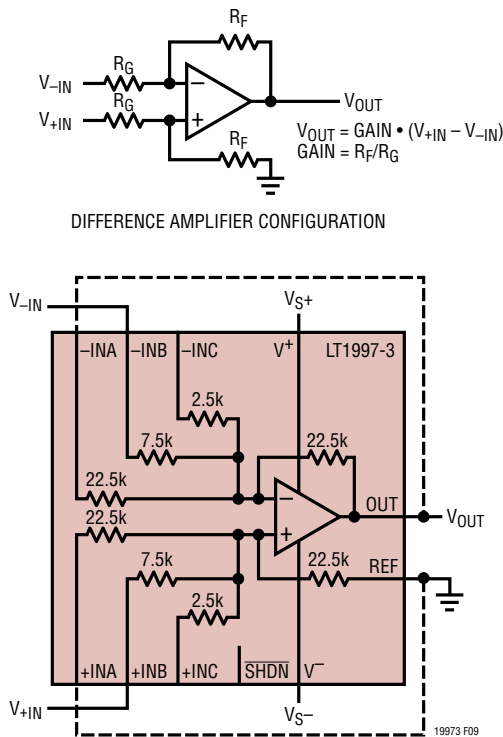


Figure 8. Inverting Gains with Input Impedance that Varies from 1.73kΩ (Gain = -13) to 22.5kΩ (Gain = -1)

# APPLICATIONS INFORMATION

## Difference Amplifiers

The LT1997-3 is ideally suited to be used as a difference amplifier. Figure 9 shows the basic 4-resistor difference amplifier and the LT1997-3. A difference gain of 3 is shown, but can be altered by additional dashed connections. By connecting the 22.5k resistors in parallel, the gain is reduced by a factor of 2. Of course there are many possible gains. Table 4 shows the difference gains and how they are achieved. Note that, as for inverting amplifiers, the noise gain is equal to the signal gain plus 1.



DIFFERENCE AMPLIFIER CONFIGURATION  
 IMPLEMENTED WITH THE LT1997-3,  $R_F = 22.5k$ ,  $R_G = 7.5k$ , GAIN = 3  
 ADDING THE DASHED CONNECTIONS CONNECT THE  
 TWO 22.5k RESISTORS IN PARALLEL, SO  $R_F$  IS REDUCED TO 11.25k.  
 THE GAIN BECOMES  $11.25k/7.5k = 1.5$

**Figure 9. The LT1997-3 Configured as a Difference Amplifier. Gain Is Set by Connecting the Correct Resistors or Combinations of Resistors. Gain of 3 Is Shown, with Dashed Lines Modifying It to a Gain of 1.5**

The Common Mode Voltage at the inputs of the internal op amp ( $V_{CMOP}$ ) is set by the voltages at pins +INA, +INB, +INC and REF.

**Table 4. Difference Amplifier Gains**

Gain	$V_{+IN}$	$V_{-IN}$	OUT	GND (REF)
0.077	+INA	-INA	-INB, -INC	+INB, +INC
0.1	+INA	-INA	-INC	+INC
0.25	+INA	-INA	-INB	+INB
0.273	+INB	-INB	-INA, -INC	+INA, +INC
0.3	+INB	-INB	-INC	+INC
0.4	+INA, +INB	-INA, -INB	-INC	+INC
1	+INA	-INA		
1.5	+INB	-INB	-INA	+INA
1.8	+INC	-INC	-INA, -INB	+INA, +INB
2.25	+INC	-INC	-INB	+INB
2.5	+INA, +INC	-INA, -INC	-INB	+INB
3	+INB	-INB		
4	+INA, +INB	-INA, -INB		
4.5	+INC	-INC	-INA	+INA
6	+INB, +INC	-INB, -INC	-INA	+INA
9	+INC	-INC		
10	+INA, +INC	-INA, -INC		
12	+INB, +INC	-INB, -INC		
13	+INA, +INB, +INC	-INA, -INB, -INC		

## APPLICATIONS INFORMATION

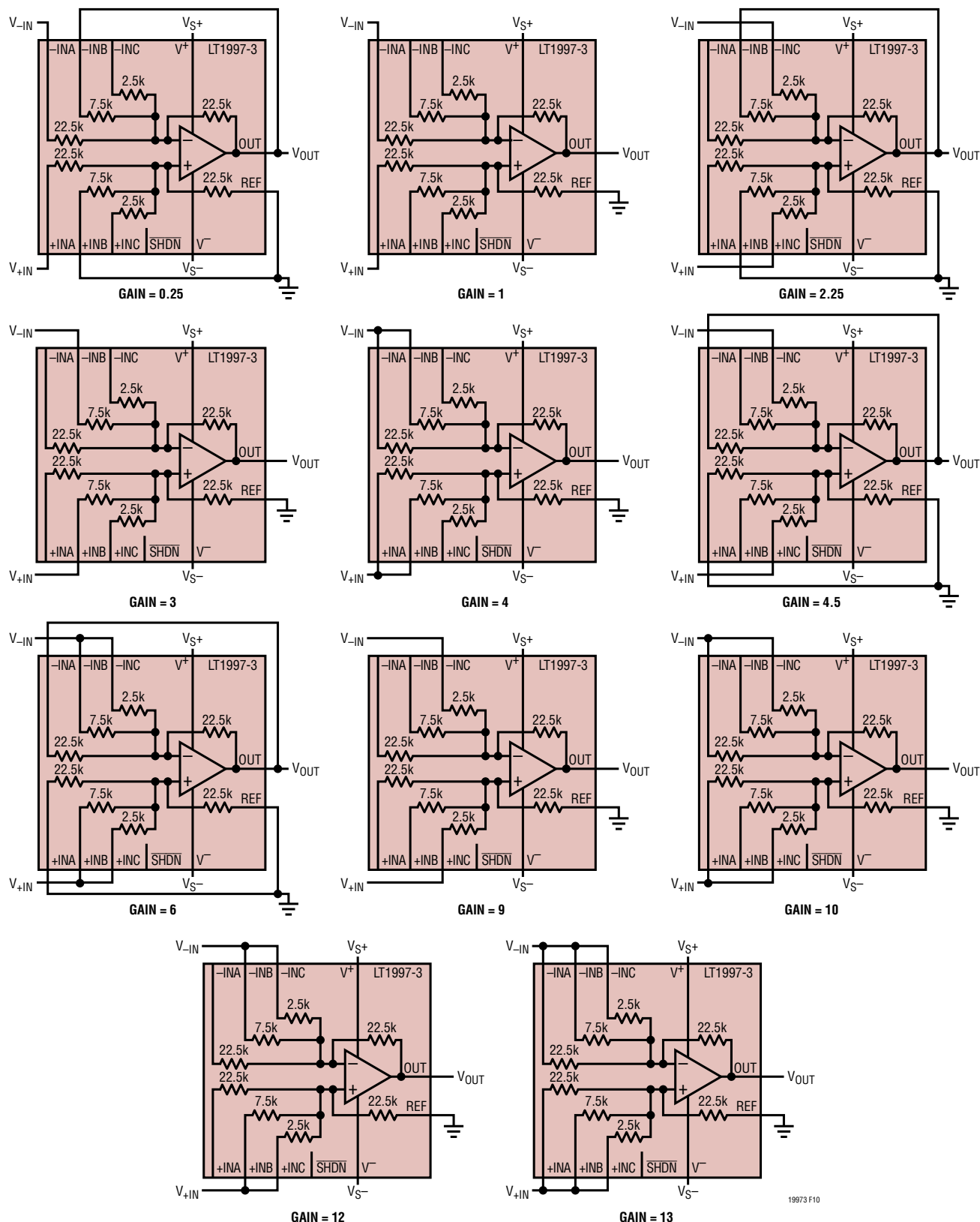


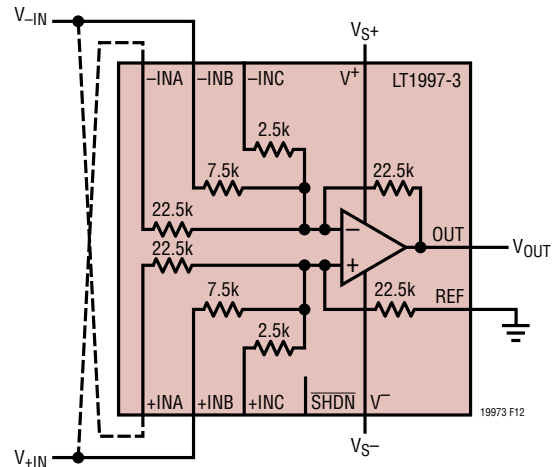
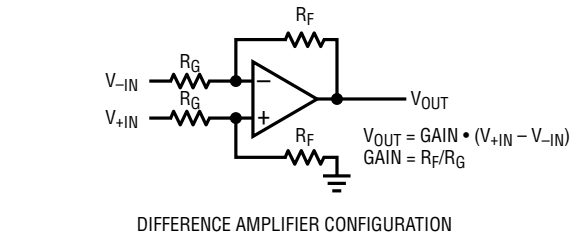
Figure 10. Many Difference Amplifier Gains Can Be Achieved by Strapping Pins

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## APPLICATIONS INFORMATION

### Difference Amplifier: Additional Integer Gains Using Cross-Coupling

Figure 11 shows the basic difference amplifier as well as the LT1997-3 with cross-coupled inputs. The additional dashed connections reduce the differential gain from 3 to 2. Using this method, additional integer gains are achievable, as shown in Table 5, so that all integer gains from 1 to 13 are achieved with the LT1997-3. Note that the equations can be written by inspection from the  $V_{+IN}$  connections, and that the  $V_{-IN}$  connections are simply the opposite (swap + for – and – for +). Noise gain, bandwidth, and input impedance specifications for the various cases are also shown. Schematics of the difference amplifiers using cross-coupling are shown in Figure 12. Additional non-integer gains produced with cross-coupling are listed in Table 6.



**Figure 11. Cross-Coupling the Inputs of the LT1997-3 Allows Additional Integer Gains to Be Constructed. The LT1997-3 Provides All Integer Gains from 1 to 13**

**Table 5. Connections Using Cross-Coupling. Note that Equations Can Be Written by Inspection of the  $V_{+IN}$  Column**

Gain	$V_{+IN}$	$V_{-IN}$	Equation	Noise Gain	–3dB BW (kHz)	Differential Input Impedance (k $\Omega$ )	Common Mode Input Impedance (k $\Omega$ )
2	+INB, –INA	–INB, +INA	$3 - 1$	5	540	11.25	14.1
5	+INC, –INB, –INA	–INC, +INB, +INA	$9 - 3 - 1$	14	222	3.5	12.1
7	+INC, +INA, –INB	–INC, –INA, +INB	$9 + 1 - 3$	14	222	3.5	12.1
8	+INC, –INA	–INC, +INA	$9 - 1$	11	277	4.5	12.4
11	+INC, +INB, –INA	–INC, –INB, +INA	$9 + 3 - 1$	14	222	3.5	12.1

**Table 6. Additional Non-Integer Gains that Can Be Achieved Using Cross-Coupling**

Gain	$V_{+IN}$	$V_{-IN}$	OUT	GND (REF)
0.143	+INA	–INA	+INB, –INC	–INB, +INC
0.2	–INA, +INB	+INA, –INB	–INC	+INC
0.333	+INB	–INB	+INA, –INC	–INA, +INC

# APPLICATIONS INFORMATION

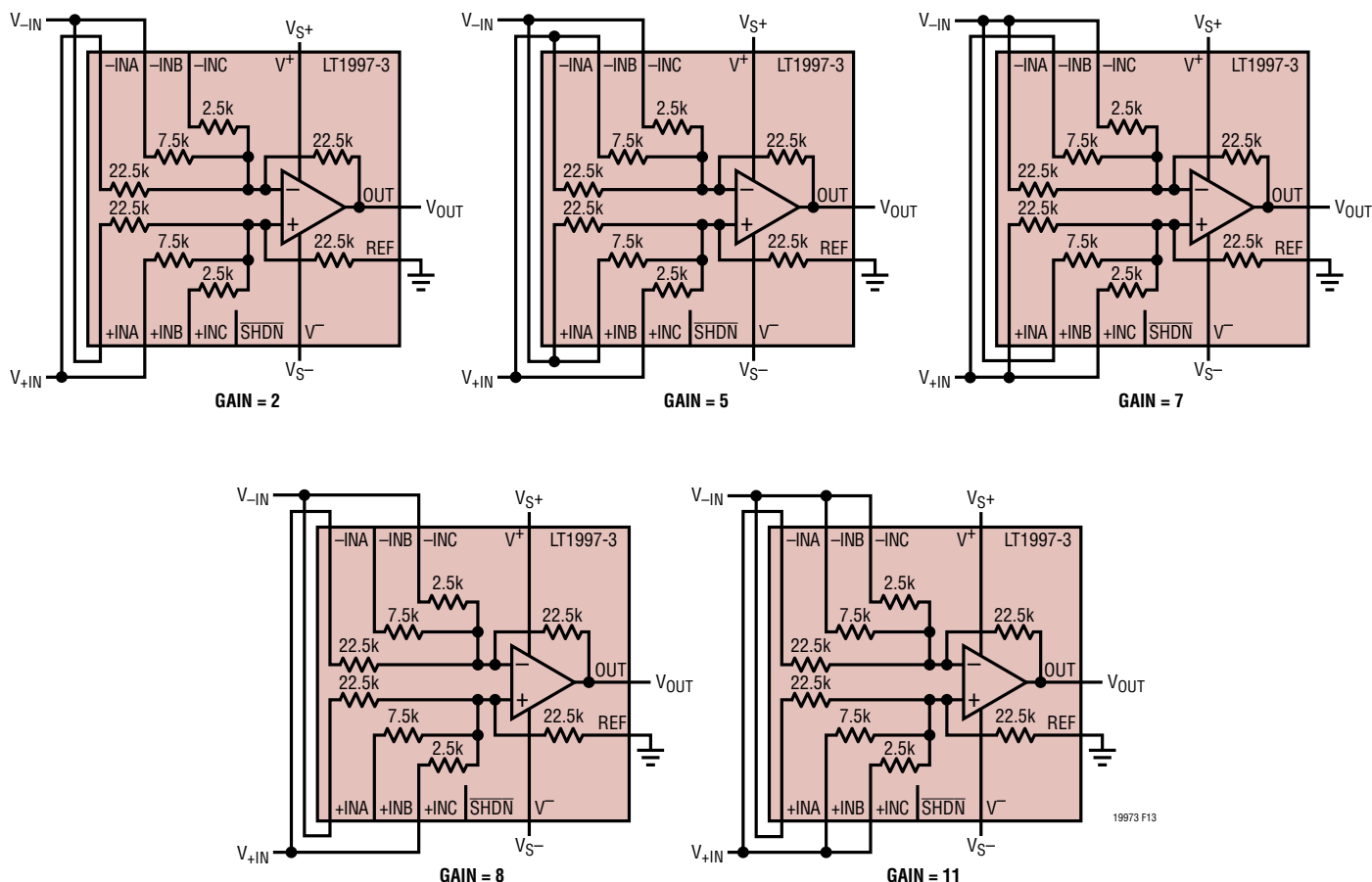


Figure 12. Integer Gain Difference Amplifiers Using Cross-Coupling

## High Common Mode Voltage Difference Amplifiers

The input range of a difference amplifier can be extended by configuring the amplifier to divide the input common mode voltage. Figure 13 shows the basic circuit on the top. The effective input voltage range of the circuit is extended by the fact that resistors  $R_T$  attenuate the common mode (CM) voltage seen by the internal op amp inputs ( $V_{CMOP}$ ). For the LT1997-3, the most useful resistors for  $R_G$  are the +INA and -INA 22.5k $\Omega$  resistors, because they do not have diode clamps to the  $V_{S-}$  supply and therefore can be taken beyond both rails. +INB, -INB, +INC and -INC pins can be taken 80V above  $V_{S-}$ , but not below  $V_{S-}$ . As before, the input common mode of the internal op amp is the limiting

factor and is set by the voltage at the op amp's positive input ( $V_{CMOP}$ ). By superposition we can write:

$$V_{CMOP} = V_{EXT} \cdot \frac{R_F \parallel R_T}{R_G + R_F \parallel R_T} + V_{REF} \cdot \frac{R_G \parallel R_T}{R_F + R_G \parallel R_T} + V_{TERM} \cdot \frac{R_F \parallel R_G}{R_T + R_F \parallel R_G}$$

Solving for  $V_{EXT}$ :

$$V_{EXT} = \left( 1 + \frac{R_G}{R_F \parallel R_T} \right) \cdot \left( \frac{V_{CMOP} - V_{REF} \cdot \frac{R_G \parallel R_T}{R_F + R_G \parallel R_T}}{-V_{TERM} \cdot \frac{R_F \parallel R_G}{R_T + R_F \parallel R_G}} \right)$$

## APPLICATIONS INFORMATION

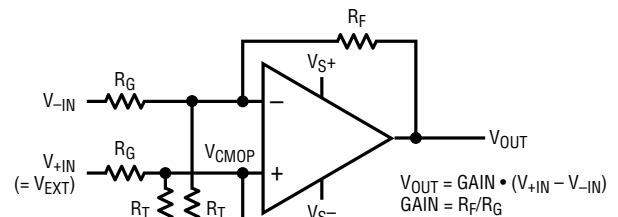
Given the values of the resistors in the LT1997-3, this equation has been simplified and evaluated, and the resulting equations are provided in Table 7. Substituting  $V_{S+} - 1.75V$  and  $V_{S-}$  for  $V_{LIM}$  will give the valid upper and lower common mode extremes respectively for the normal operating region of the op amp. Substituting  $V_{S-} + 76V$  and  $V_{S-}$  for  $V_{LIM}$  will give the valid upper and lower common mode extremes respectively for the Over-The-Top region of the op amp (see Over-The-Top Operation section of this data sheet for more detail). Following are sample calculations for the case shown in Figure 13. Note that +INC and -INC are terminated so row 3 of Table 7 provides the equation:

$$\begin{aligned} \text{MAX } V_{EXT} &= 11 \cdot (V_{S+} - 1.75) - V_{REF} - 9 \cdot V_{TERM} \\ &= 11 \cdot (10.25V) - 2.5 - 9 \cdot 12 \\ &= 2.25V \end{aligned}$$

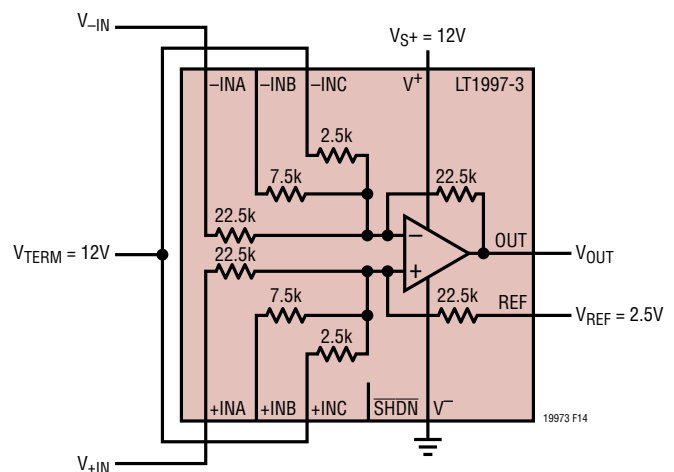
and:

$$\begin{aligned} \text{MIN } V_{EXT} &= 11 \cdot (V_{S-}) - V_{REF} - 9 \cdot V_{TERM} \\ &= 11 \cdot (0) - 2.5 - 9 \cdot 12 \\ &= -110.5V \end{aligned}$$

If the calculated  $V_{EXT}$  voltage exceeds the 160V absolute maximum rating of the +INA, -INA pins, 160V or -160V would become the de facto common mode limit. Several more examples of high CM circuits are shown in Figure 14, Figure 15 and Figure 16 for various supplies.



HIGH COMMON MODE VOLTAGE DIFFERENCE AMPLIFIER  
INPUT COMMON MODE VOLTAGE TO OP AMP IS  
ATTENUATED BY RESISTORS  $R_T$  CONNECTED TO  $V_{TERM}$



HIGH NEGATIVE COMMON MODE VOLTAGE DIFFERENCE AMPLIFIER  
IMPLEMENTED WITH THE LT1997-3,  $R_F = 22.5k$ ,  $R_G = 22.5k$ ,  $R_T = 2.5k$ ,  $GAIN = 1$   
 $V_{TERM} = V_{S+} = 12V$ ,  $V_{REF} = 2.5V$ ,  $V_{S-} = 0V$

**Figure 13. Extending Common Mode Input Range**

**Table 7. Input Common Mode Voltage Ranges for the LT1997-3 when Configured as a High Common Mode Voltage Difference Amplifier**

Gain	$V_{+IN}$	$V_{-IN}$	$R_T$	Noise Gain	Max, Min $V_{EXT}$ (Substitute $V_{S+} - 1.75$ (Normal Region) or $V_{S-} + 76$ (OTT), and $V_{S-}$ for $V_{LIM}$ )
1	+INA	-INA		2	$2 \cdot V_{LIM} - V_{REF}$
1	+INA	-INA	$R_{+INB}, R_{-INB}$	5	$5 \cdot V_{LIM} - V_{REF} - 3 \cdot V_{TERM}$
1	+INA	-INA	$R_{+INC}, R_{-INC}$	11	$11 \cdot V_{LIM} - V_{REF} - 9 \cdot V_{TERM}$
1	+INA	-INA	$R_{+INB}    R_{+INC}, R_{-INB}    R_{-INC}$	14	$14 \cdot V_{LIM} - V_{REF} - 12 \cdot V_{TERM}$



# APPLICATIONS INFORMATION

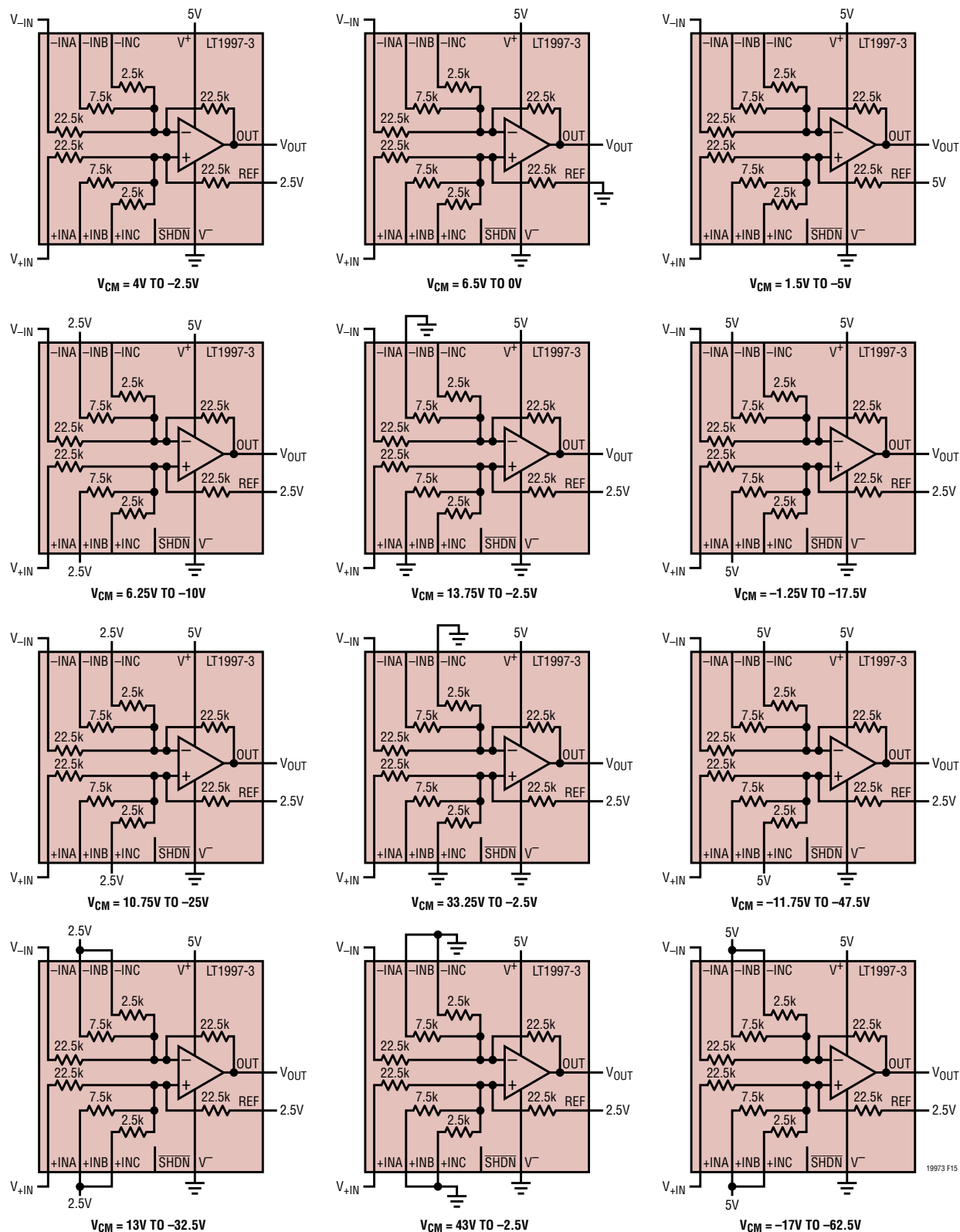


Figure 14. Common Mode Ranges for Various LT1997-3 Configurations on  $V_S = 5V, 0V$ , with Gain = 1. These Ranges Guarantee that the Internal Op Amp Operates in Its Normal Operating Region

# APPLICATIONS INFORMATION

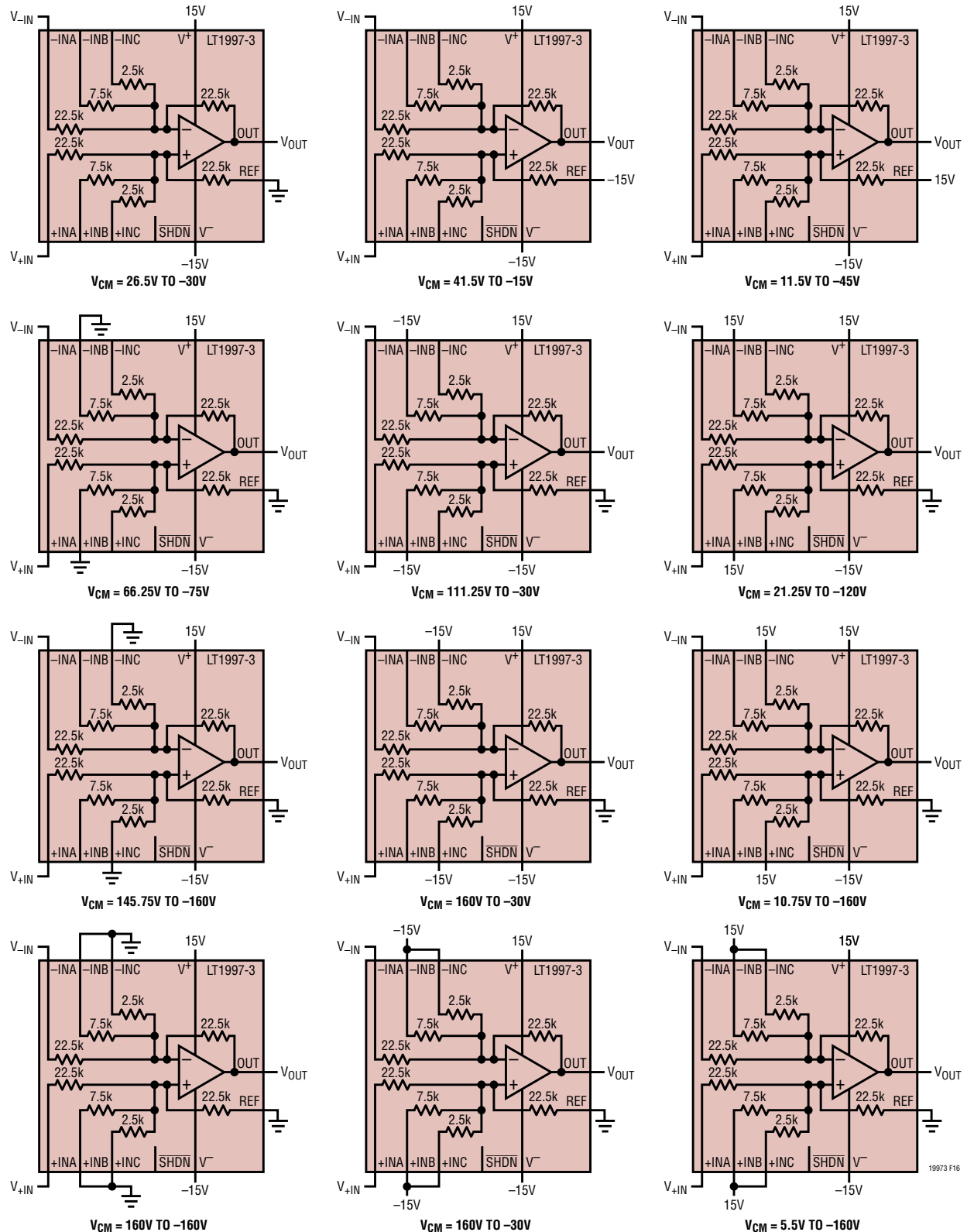


Figure 15. Common Mode Ranges for Various LT1997-3 Configurations on  $V_S = \pm 15V$ , with Gain = 1. These Ranges Guarantee that the Internal Op Amp Operates in Its Normal Operating Region

## APPLICATIONS INFORMATION

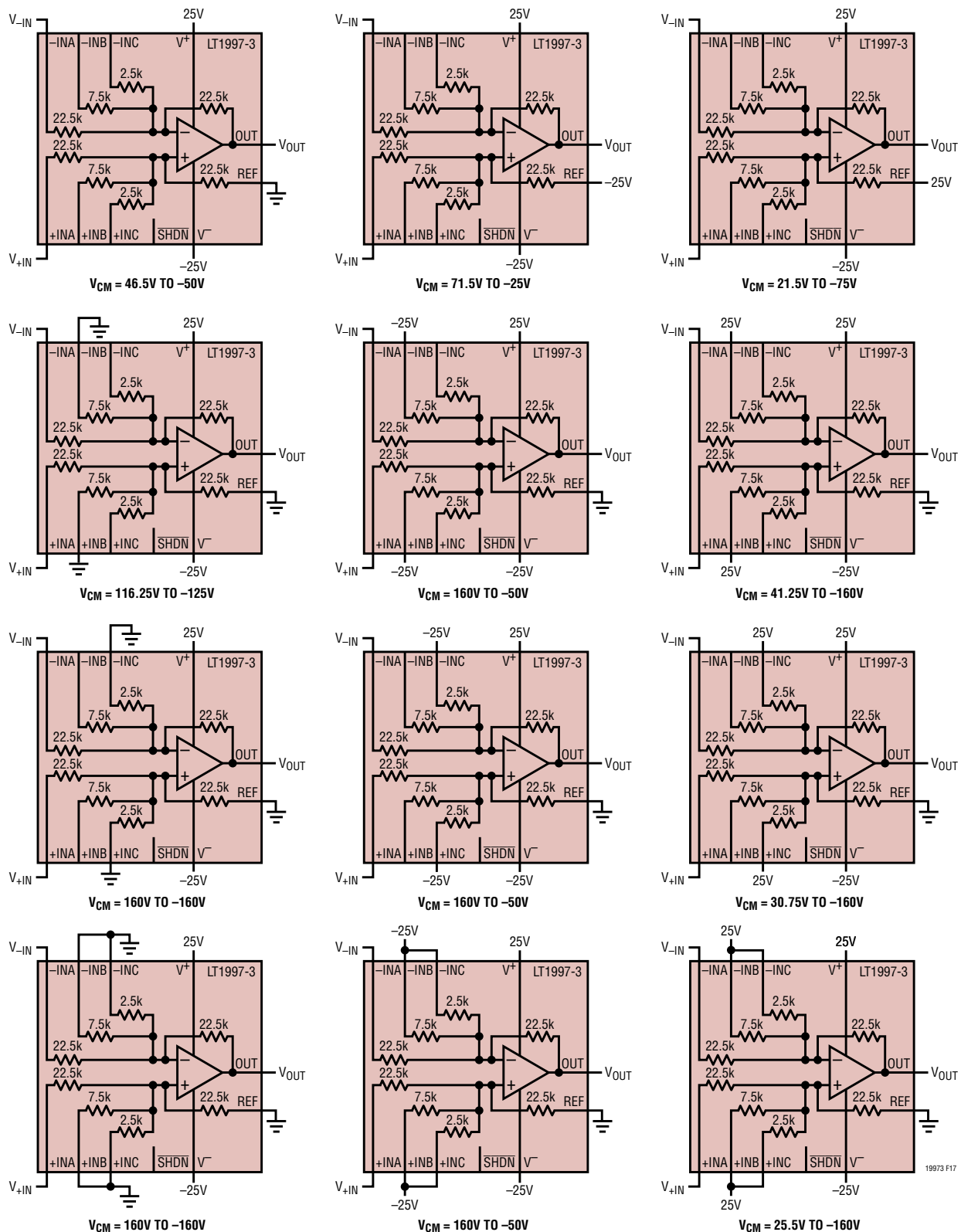


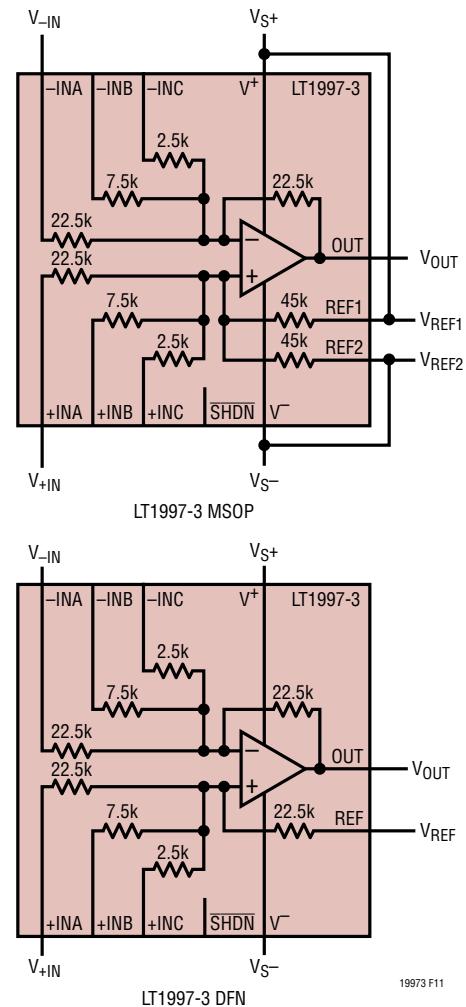
Figure 16. Common Mode Ranges for Various LT1997-3 Configurations on  $V_S = \pm 25V$ , with Gain = 1. These Ranges Guarantee that the Internal Op Amp Operates in Its Normal Operating Region

## APPLICATIONS INFORMATION

### Reference Resistors

In the preceding discussions, the Reference resistor is shown as a single 22.5k resistor. This is true in the DFN package. In the MSOP package the reference resistor is split into two 45k resistors (Figure 17). Tying the REF1 and REF2 pins to the same voltage produces the same reference voltage as tying the  $V_{REF}$  pin in the DFN package to that voltage. Connecting REF1 and REF2 to different voltages produces an effective reference voltage that is the average of  $V_{REF1}$  and  $V_{REF2}$ . This is especially useful when the desired reference voltage is half way between the supplies. Tying REF1 to  $V_{S+}$  and REF2 to  $V_{S-}$  produces the desired mid-supply voltage without the help of another external reference voltage (Figure 17). The ratio of  $R_{REF1}$  to  $R_{REF2}$  is very precise:

$$\frac{\Delta R}{R} = \left| \frac{R_{REF1} - R_{REF2}}{\left( \frac{R_{REF1} + R_{REF2}}{2} \right)} \right| < 60\text{ppm}$$



**Figure 17. The LT1997-3 Reference Resistors: Split Resistors in the MSOP Package Above, Single Resistor in the DFN Package Below**

## APPLICATIONS INFORMATION

### Shutdown

The LT1997-3 has a shutdown pin ( $\overline{\text{SHDN}}$ ). Under normal operation this pin should be tied to  $V^+$  or allowed to float. Tying this pin 2.5V or more below  $V^+$  will cause the part to enter a low power state. The supply current is reduced to less than 25 $\mu\text{A}$  and the op amp output becomes high impedance. The voltages at the input pins can be still be present even in shutdown mode.

### Supply Voltage

The positive supply pin of the LT1997-3 should be bypassed with a small capacitor (typically 0.1 $\mu\text{F}$ ) as close to the supply pins as possible. When driving heavy loads, an additional 4.7 $\mu\text{F}$  electrolytic capacitor should be added. When using split supplies, the same is true for the  $V^-$  supply pin.

### Output

The output of the LT1997-3 can typically swing to within 100mV of either rail with no load and is capable of sourcing and sinking approximately 25mA at 25°C. The LT1997-3 is internally compensated to drive at least 1nF of capacitance under any output loading conditions. For larger capacitive loads, a 0.22 $\mu\text{F}$  capacitor in series with a 150 $\Omega$  resistor between the output and ground will compensate the amplifier to drive capacitive loads greater than 1nF. Additionally, the LT1997-3 has more gain and phase margin as its gain is increased.

### Distortion

The LT1997-3 features excellent distortion performance when the internal op amp is operating in the normal operating region. Operating the LT1997-3 with the internal op amp in the over the top region will increase distortion due to the lower loop gain of the op amp. Operating the LT1997-3 with input common mode voltages that go from the normal to Over-The-Top operation will significantly degrade the LT1997-3's linearity as the op amp must transition between two different input stages. Driving resistive loads significantly smaller than the 22.5k internal feedback resistor will also degrade the amplifier's linearity performance.

### Power Dissipation Considerations

Because of the ability of the LT1997-3 to operate on power supplies up to  $\pm 25\text{V}$ , to withstand very high input voltages and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed 150°C. The LT1997-3 is housed in DF14 ( $\theta_{\text{JA}} = 45^\circ\text{C/W}$ ,  $\theta_{\text{JC}} = 3^\circ\text{C/W}$ ) and MS16 ( $\theta_{\text{JA}} = 130^\circ\text{C/W}$ ) packages.

In general, the die junction temperature ( $T_{\text{J}}$ ) can be estimated from the ambient temperature ( $T_{\text{A}}$ ), the device's power dissipation ( $P_{\text{D}}$ ) and the thermal resistance of the device and board ( $\theta_{\text{JA}}$ ).

$$T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \cdot \theta_{\text{JA}}$$

The thermal resistance from the junction to the ambient environment ( $\theta_{\text{JA}}$ ) is the sum of the thermal resistance from the junction to the exposed pad ( $\theta_{\text{JC}}$ ) and the thermal resistance from the exposed pad to the ambient environment ( $\theta_{\text{CA}}$ ). The  $\theta_{\text{CA}}$  value depends on how much PCB metal is connected to the exposed pad in the board. The more PCB metal that is used, the lower  $\theta_{\text{CA}}$  and  $\theta_{\text{JA}}$  will be.

Power is dissipated by the amplifier's quiescent current, by the output current driving a resistive load, and by the input current driving the LT1997-3's internal resistor network.

$$P_{\text{D}} = ((V_{\text{S}+} - V_{\text{S}-}) \cdot I_{\text{S}}) + P_{\text{OD}} + P_{\text{RESD}}$$

For a given supply voltage, the worst-case output power dissipation  $P_{\text{OD(MAX)}}$  occurs with the output voltage at half of either supply voltage.  $P_{\text{OD(MAX)}}$  is given by:

$$P_{\text{OD(MAX)}} = \frac{(V_{\text{S}}/2)^2}{R_{\text{LOAD}}}$$

The power dissipated in the internal resistors ( $P_{\text{RESD}}$ ) depends on the manner the input resistors have been configured as well as the input voltage, the output voltage and the voltage on the REF pin. The following equations and Figure 18 show the different components of  $P_{\text{RESD}}$  corresponding to the different groups of the LT1997-3's internal resistors, assuming that the LT1997-3 is used with a dual supply configuration with +INC, -INC, and REF pins

## APPLICATIONS INFORMATION

at ground (refer to Figure 13 for resistor terminologies used in equations below).

$$P_{RESDA} = \frac{(V_{+IN})^2}{R_G + R_F \parallel R_T}$$

$$P_{RESDB} = \frac{\left( V_{-IN} - V_{+IN} \cdot \frac{(R_F \parallel R_T)}{R_G + R_F \parallel R_T} \right)^2}{R_G}$$

$$P_{RESDC} = \frac{\left( V_{+IN} \cdot \frac{(R_F \parallel R_T)}{R_G + R_F \parallel R_T} \right)^2}{R_T}$$

$$P_{RESDD} = \frac{\left( V_{+IN} \cdot \frac{(R_F \parallel R_T)}{R_G + R_F \parallel R_T} - V_{OUT} \right)^2}{R_F}$$

$$P_{RES D} = P_{RESDA} + P_{RESDB} + P_{RESDC} + P_{RESDD}$$

In general,  $P_{RES D}$  increases with higher input voltage and lower output and REF pin voltages.

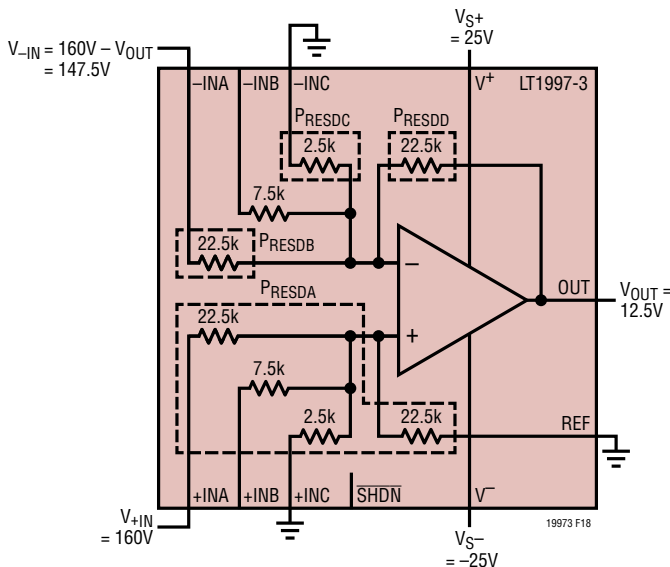


Figure 18. Power Dissipation Example

Example: For an LT1997-3 in a DFN package mounted on a PC board with a thermal resistance of 45°C/W, operating on ±25V supplies and driving a 2.5kΩ load to 12.5V with  $V_{+IN} = 160V$  and  $+INC = -INC = REF = 0V$ , the total power dissipation is given by:

$$\begin{aligned} P_D &= (50 \cdot 0.6mA) + \frac{12.5^2}{2.5k} + \frac{160^2}{24.75k} \\ &+ \frac{\left( 147.5 - \frac{160}{11} \right)^2}{22.5k} + \frac{\left( \frac{160}{11} \right)^2}{2.5k} + \frac{\left( \frac{160}{11} - 12.5 \right)^2}{22.5k} \\ &= 2W \end{aligned}$$

Assuming a thermal resistance of 45°C/W, the die temperature will experience an 90°C rise above ambient. This implies that the maximum ambient temperature the LT1997-3 should operate under the above conditions is:

$$T_A = 150^\circ C - 90^\circ C = 60^\circ C$$

It is recommended that the exposed pad of the DFN package have as much PCB metal connected to it as reasonably available. The more PCB metal connected to the exposed pad, the lower the thermal resistance. Connecting a large amount of PCB metal to the exposed pad can reduce the  $\theta_{JA}$  to even less than 45°C/W. Use multiple vias from the exposed pad to the  $V^-$  plane. The exposed pad is electrically connected to the  $V^-$  pin. In addition, a heat sink may be necessary if operating near maximum junction temperature.

The MSOP package has no exposed pad and a higher thermal resistance ( $\theta_{JA} = 130^\circ C/W$ ). It should not be used in applications which have a high ambient temperature, require driving a heavy load, or require an extreme input voltage.

### Thermal Shutdown

For safety, the LT1997-3 will enter shutdown mode when the die temperature rises to approximately 163°C. This thermal shutdown has approximately 9°C of hysteresis requiring the die temperature to cool 9°C before enabling the amplifier again.

## ESD Protection

The LT1997-3 is protected by a number of ESD structures. The structures are shown in Figure 19.

The ESD structures serve to protect the internal circuitry but also limit signal swing on certain nodes. The structures on the +INB, -INB, +INC, -INC pins and on the internal op amp inputs limit the voltage on these nodes to 0.3V below  $V^-$  and 80V above  $V^-$ . The voltage on the REF (DFN), REF1 (MSOP) and REF2 (MSOP) pins are limited to 0.3V below  $V^-$  and 60V above  $V^-$ . The voltage on the  $\overline{\text{SHDN}}$  pin is limited to 0.3V below  $V^-$  and 0.3V above  $V^+$ .

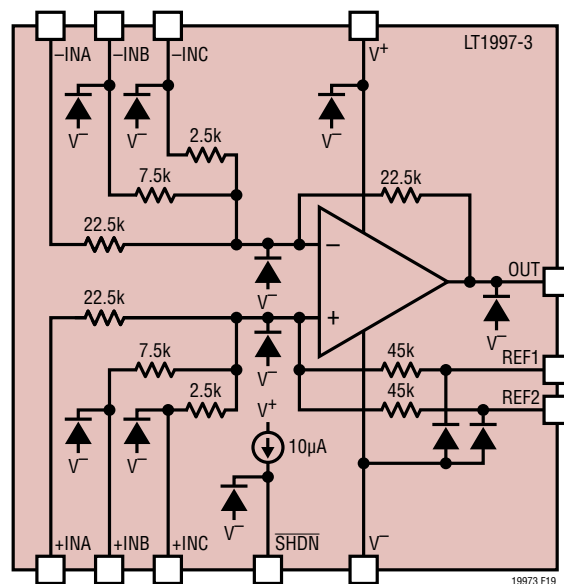
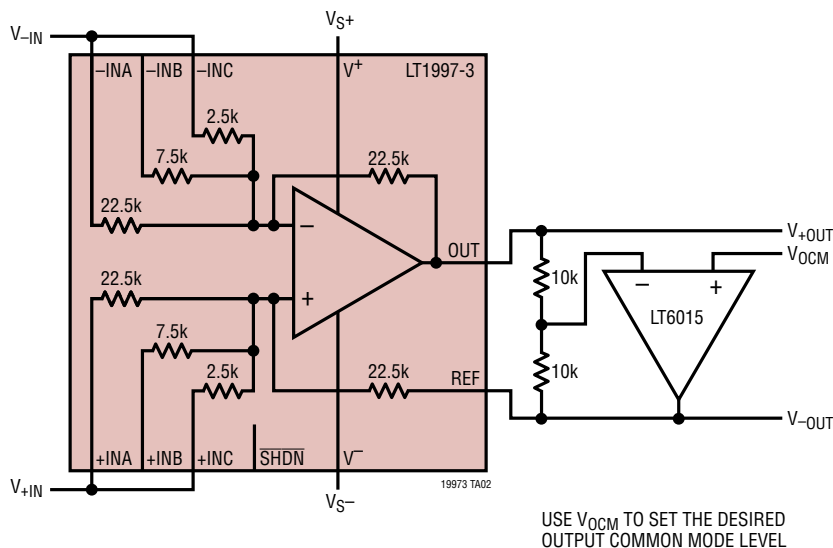


Figure 19. ESD Protection

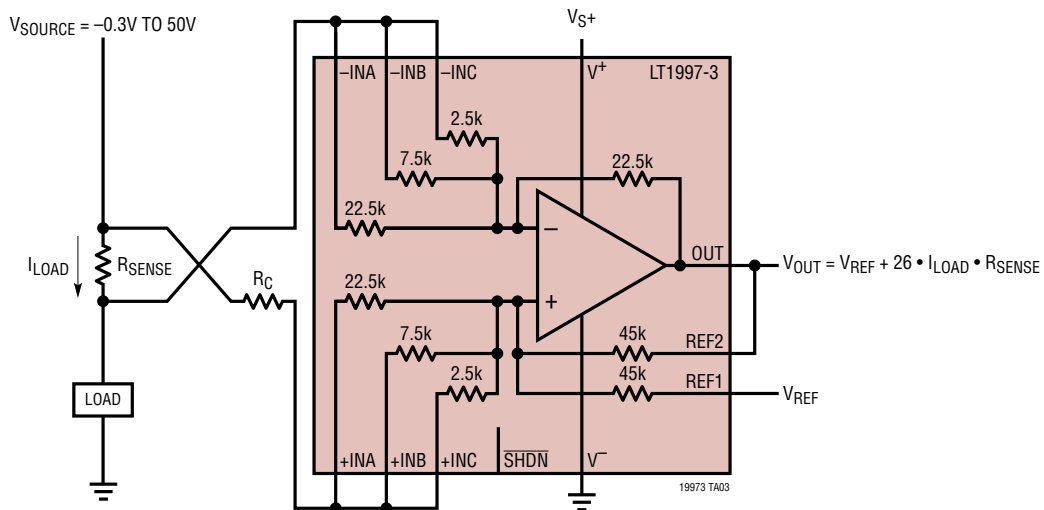
## TYPICAL APPLICATIONS

### Differential Input/Output Gain of 10 Amplifier

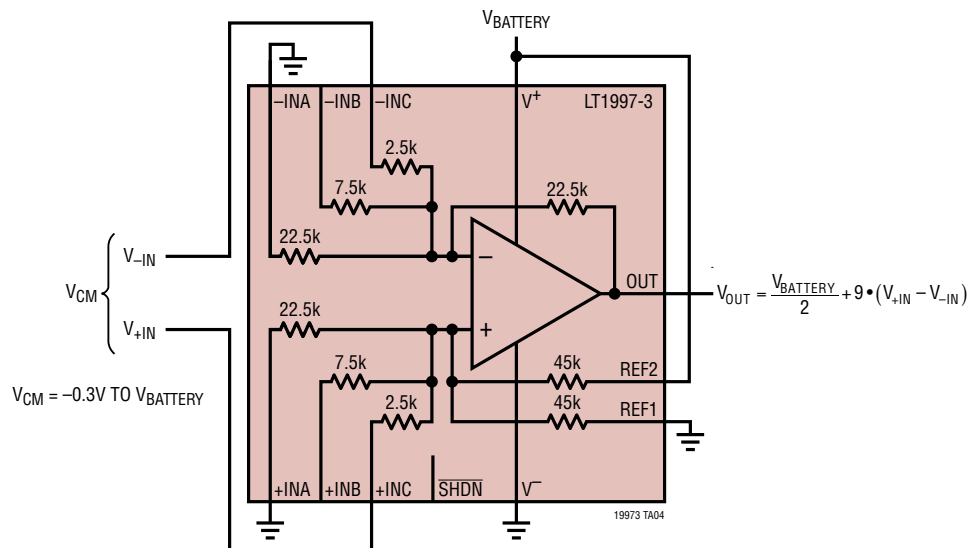


## TYPICAL APPLICATIONS

### Bidirectional Current Sense Amplifier



### Precision RRIO Single-Supply Difference Amplifier



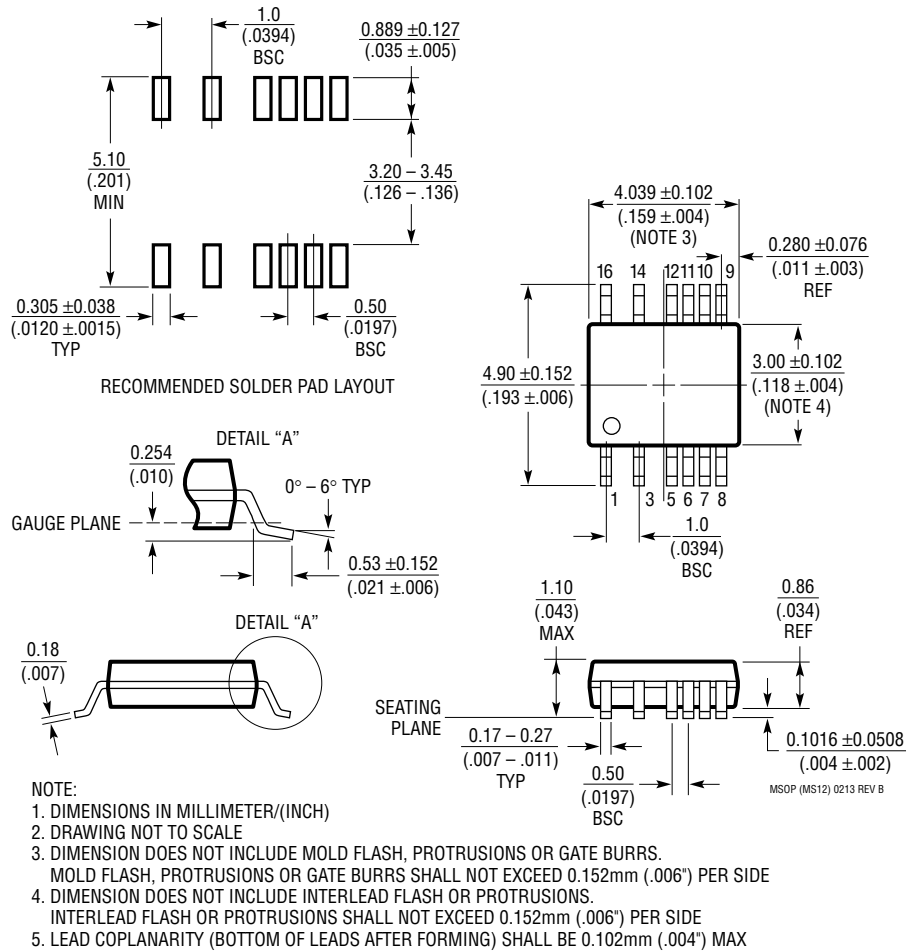




# PACKAGE DESCRIPTION

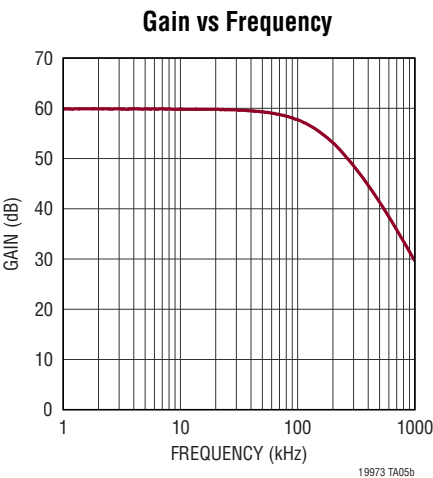
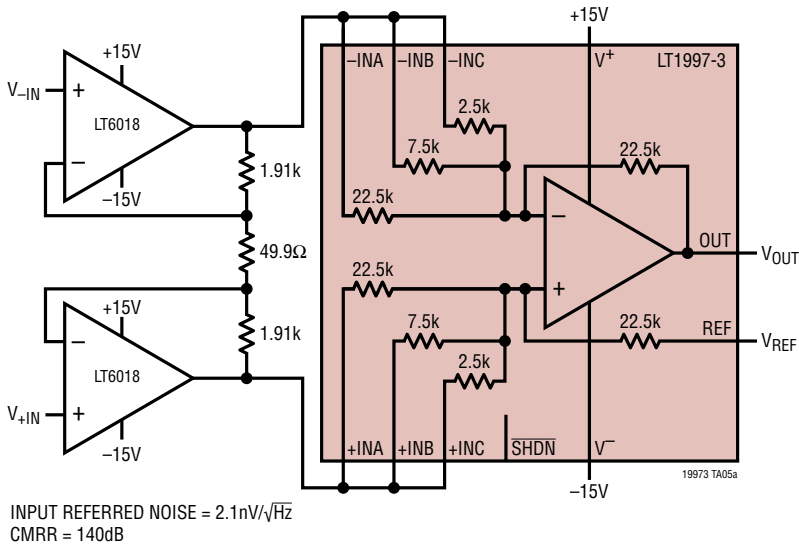
Please refer to <http://www.linear.com/product/LT1997-3#packaging> for the most recent package drawings.

## MS Package 16 (12)-Lead Plastic MSOP with 4 Pins Removed (Reference LTC DWG # 05-08-1847 Rev B)



TYPICAL APPLICATION

Low Noise, High CMRR Instrumentation Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LT6375</a>	$\pm 270V$ Common Mode Voltage Difference Amplifier	3.3V to 50V Operation, CMRR > 97dB, Input Voltage = $\pm 270V$
<a href="#">LT1990</a>	$\pm 250V$ Input Range Difference Amplifier	2.7V to 36V Operation, CMRR > 70dB, Input Voltage = $\pm 250V$
<a href="#">LT1991</a>	Precision, 100 $\mu A$ Gain Selectable Amplifier	2.7V to 36V Operation, 50 $\mu V$ Offset, CMRR > 75dB, Input Voltage = $\pm 60V$
<a href="#">LT1996</a>	Precision, 100 $\mu A$ Gain Selectable Amplifier	Micropower, Pin Selectable Up to Gain = 118
<a href="#">LT1999</a>	High Voltage, Bidirectional Current Sense Amplifier	-5V to 80V, 750 $\mu V$ , CMRR 80dB at 100kHz, Gain: 10V/V, 20V/V, 50V/V
<a href="#">LT6015/LT6016/LT6017</a>	Single, Dual, and Quad Over-The-Top Precision Op Amp	3.2MHz, 0.8V/ $\mu s$ , 50 $\mu V$ $V_{OS}$ , 3V to 50V $V_S$ , 0.335mA $I_S$ , RRIO
<a href="#">LT6018</a>	33V, Ultralow Noise, Precision Op Amp	$V_{OS}$ : 50 $\mu V$ , GBW: 15MHz, SR: 30V/ $\mu s$ , en: 1.2nV/ $\sqrt{Hz}$ , $I_S$ : 7.2mA
<a href="#">LTC6090</a>	140V Operational Amplifier	50pA $I_B$ , 1.6mV $V_{OS}$ , 9.5V to 140V $V_S$ , 4.5mA $I_S$ , RR Output
<a href="#">LT6108</a>	High Side Current Sense Amplifier with Reference and Comparator with Shutdown	2.7V to 60V, 125 $\mu V$ , Resistor Set Gain, $\pm 1.25\%$ Threshold Error
<a href="#">LT1787/LT1787HV</a>	Precision, Bidirectional High Side Current Sense Amplifier	2.7V to 60V Operation, 75 $\mu V$ Offset, 60 $\mu A$ Current Draw
<a href="#">LT6100</a>	Gain-Selectable High Side Current Sense Amplifier	4.1V to 48V Operation, Pin-Selectable Gain: 10V/V, 12.5V/V, 20V/V, 25V/V, 40V/V, 50V/V
<a href="#">LTC6101/LTC6101HV</a>	High Voltage High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, External Resistor Set Gain, SOT23
<a href="#">LTC6102/LTC6102HV</a>	Zero Drift High Side Current Sense Amplifier	4V to 60V/5V to 100V Operation, $\pm 10\mu V$ Offset, 1 $\mu s$ Step Response, MSOP8/DFN Packages
<a href="#">LTC6104</a>	Bidirectional, High Side Current Sense	4V to 60V, Gain Configurable, 8-Pin MSOP Package