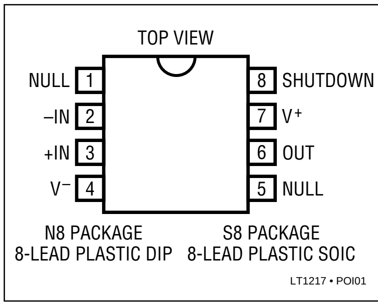
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Input Current .... ±10mA
Input Voltage .... Equal to Supply Voltage
Output Short Circuit Duration (Note 1) .... Continuous
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Junction Temperature .... 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1217CN8 LT1217CS8
S8 PART MARKING
1217

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 0°C$ to 70°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$	●		±1	±3	mV
I_{IN+}	Non-Inverting Input Current	$V_{CM} = 0V$	●		±100	±500	nA
I_{IN-}	Inverting Input Current	$V_{CM} = 0V$	●		±100	±500	nA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, R_G = 10Ω			6.5		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz, R_F = 1k, R_G = 10Ω			0.7		pA/√Hz
R_{IN}	Input Resistance	$V_{IN} = \pm10V$	●	20	100		MΩ
C_{IN}	Input Capacitance				1.5		pF
	Input Voltage Range		●	±10	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm10V$	●	60	66		dB
	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm10V$	●		5	20	nA/V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	●	68	76		dB
	Non-Inverting Input Current Power Supply Rejection	V_S = ±4.5V to ±18V	●		2	20	nA/V
	Inverting Input Current Power Supply Rejection	V_S = ±4.5V to ±18V	●		10	50	nA/V
A_V	Large Signal Voltage Gain	R_{LOAD} = 2k, V_{OUT} = ±10V R_{LOAD} = 400Ω, V_{OUT} = ±10V	● ●	90 70	105		dB dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN-}$	R_{LOAD} = 2k, V_{OUT} = ±10V R_{LOAD} = 400Ω, V_{OUT} = ±10V	● ●	5 1.5	45		MΩ MΩ
V_{OUT}	Output Swing	R_{LOAD} = 2k R_{LOAD} = 200Ω	● ●	±12 ±10	±13		V V
I_{OUT}	Output Current	R_{LOAD} = 0Ω	●	50	100		mA
SR	Slew Rate (Note 2, 3)	R_F = 3k, R_G = 3k	●	100	500		V/µs
BW	Bandwidth	R_F = 3k, R_G = 3k, V_{OUT} = 100mV			10		MHz
t_r	Rise Time, Fall Time (Note 3)	R_F = 3k, R_G = 3k, V_{OUT} = 1V	●		30	40	ns
t_{PD}	Propagation Delay	R_F = 3k, R_G = 3k, V_{OUT} = 1V			25		ns
	Overshoot	R_F = 3k, R_G = 3k, V_{OUT} = 1V			5		%
t_s	Settling Time, 0.1%	R_F = 3k, R_G = 3k, V_{OUT} = 10V			280		ns
I_S	Supply Current	$V_{IN} = 0V$	●		1	2	mA
	Supply Current, Shutdown	Pin 8 Current = 50µA	●		350	1000	µA

The ● denotes specifications which apply over the operating temperature range.

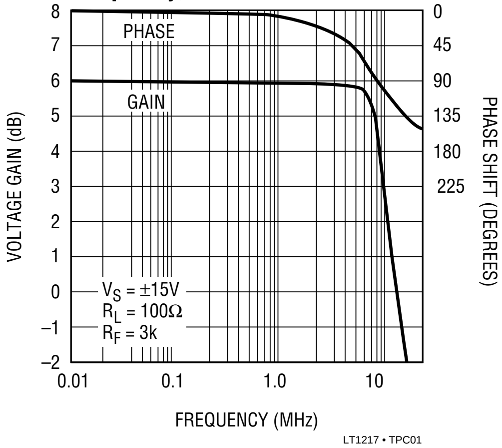
Note 1: A heat sink may be required.

Note 2: Non-Inverting operation, V_{OUT} = ±10V, measured at ±5V.

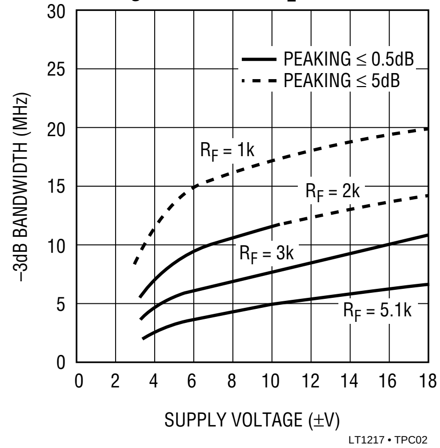
Note 3: AC parameters are 100% tested on the plastic DIP packaged parts (N suffix), and are sample tested on every lot of the SO packaged parts (S suffix).

TYPICAL PERFORMANCE CHARACTERISTICS

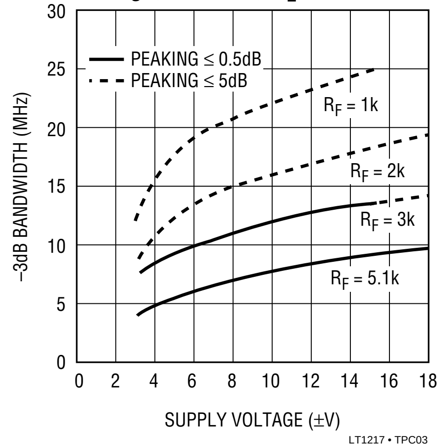
Voltage Gain and Phase vs Frequency, Gain = 6dB



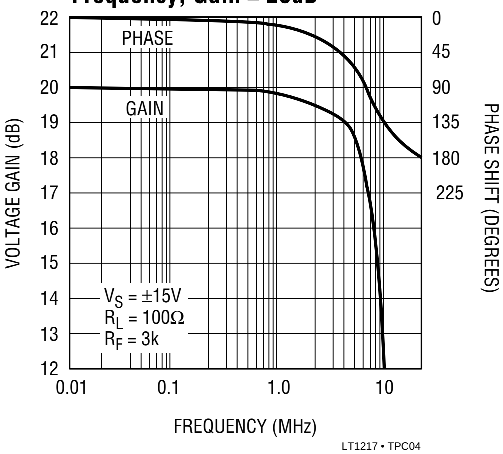
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 100Ω



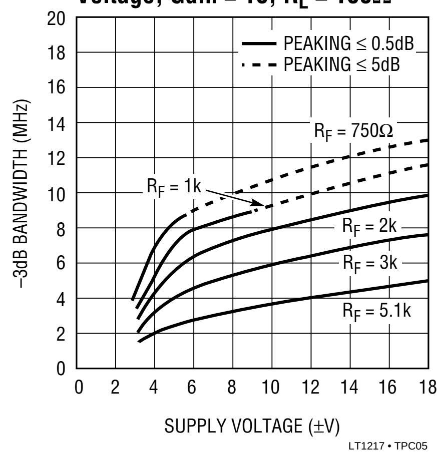
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 1kΩ



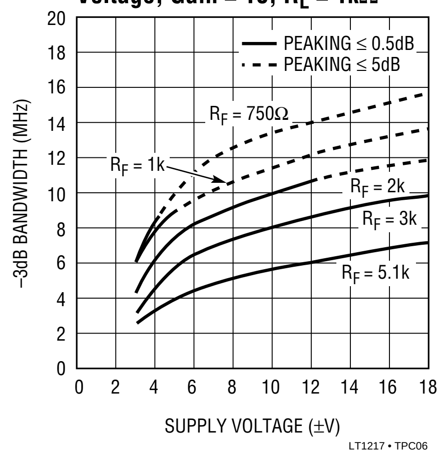
Voltage Gain and Phase vs Frequency, Gain = 20dB



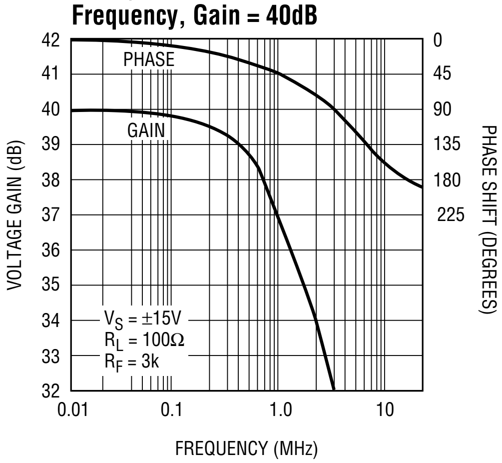
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 100Ω



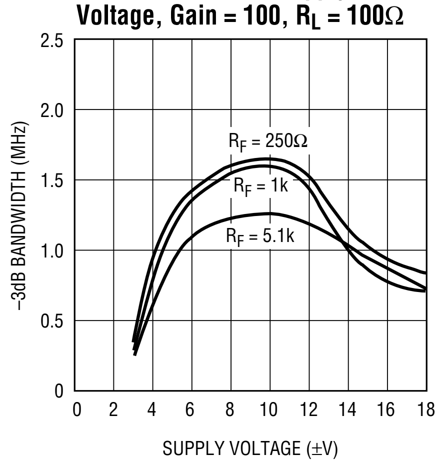
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 1kΩ



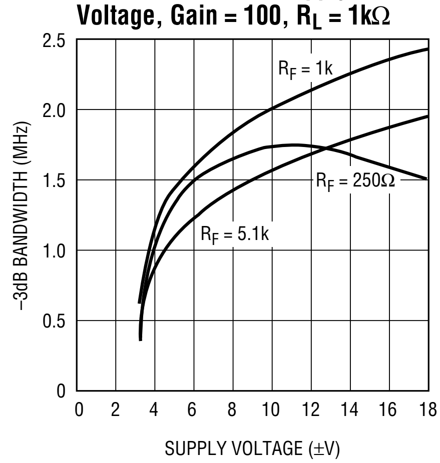
Voltage Gain and Phase vs Frequency, Gain = 40dB



–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 100Ω

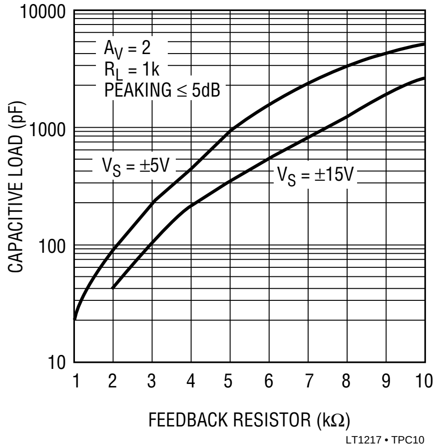


–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 1kΩ

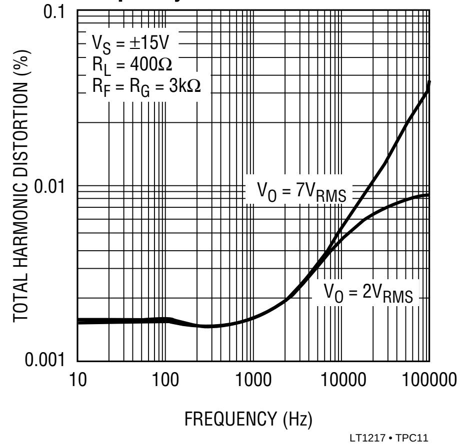


TYPICAL PERFORMANCE CHARACTERISTICS

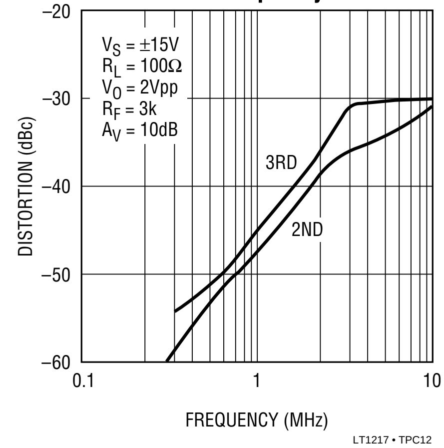
Maximum Capacitive Load vs Feedback Resistor



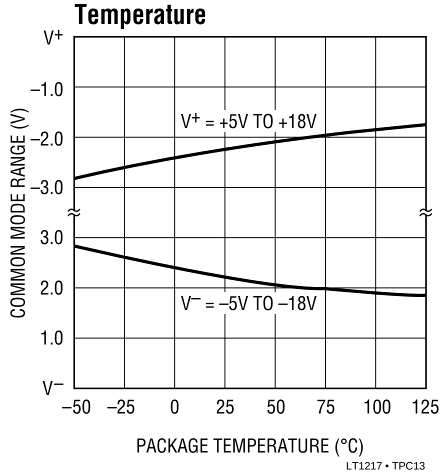
Total Harmonic Distortion vs Frequency



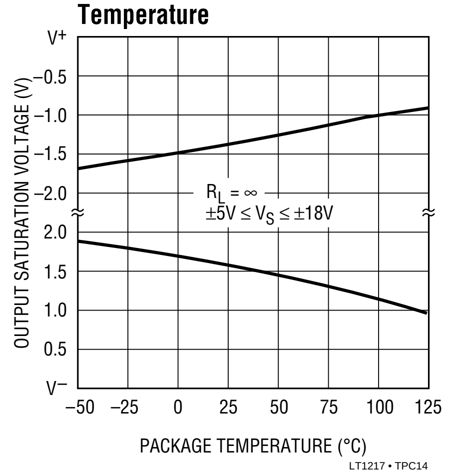
2nd and 3rd Harmonic Distortion vs Frequency



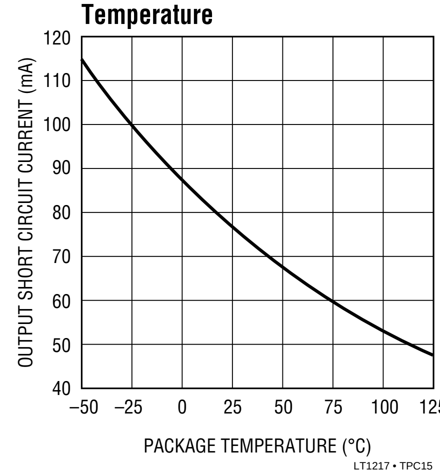
Input Common Mode Limit vs Temperature



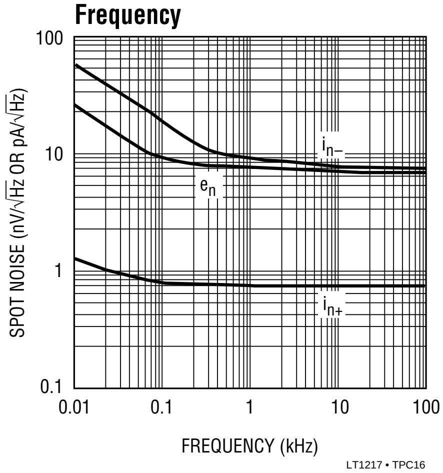
Output Saturation Voltage vs Temperature



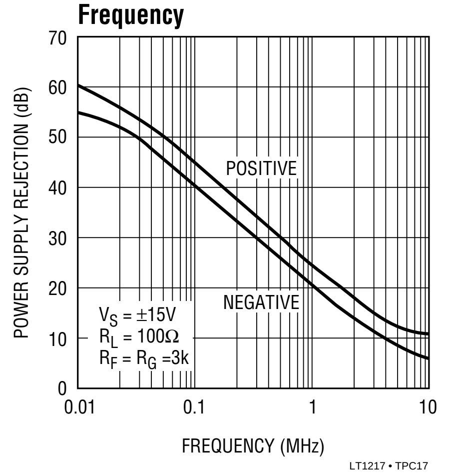
Output Short Circuit Current vs Temperature



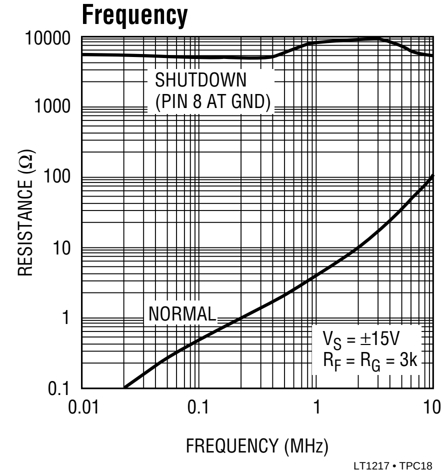
Spot Noise Voltage and Current vs Frequency



Power Supply Rejection vs Frequency

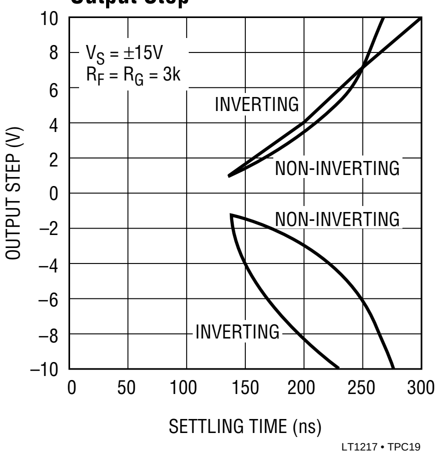


Output Impedance vs Frequency

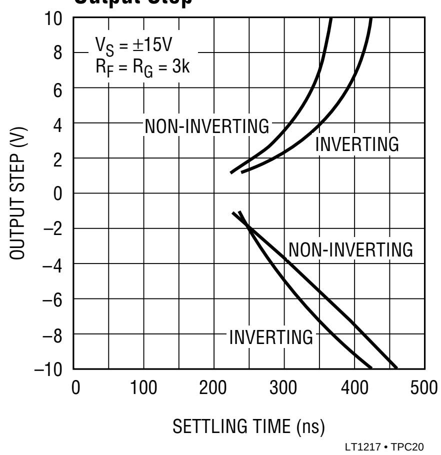


TYPICAL PERFORMANCE CHARACTERISTICS

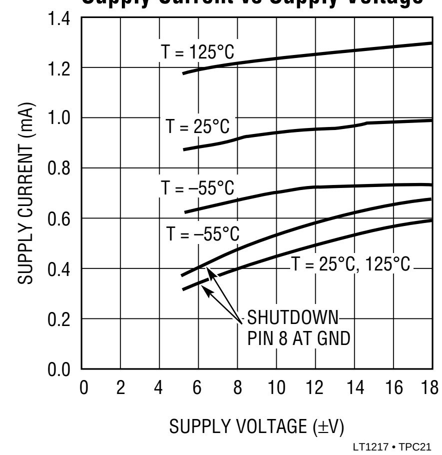
Settling Time to 10mV vs Output Step



Settling Time to 1mV vs Output Step



Supply Current vs Supply Voltage



APPLICATIONS INFORMATION

Current Feedback Basics

The small signal bandwidth of the LT1217, like all current feedback amplifiers, isn't a straight inverse function of the closed loop gain. This is because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_F) from output to inverting input works with internal junction capacitances of the LT1217 to set the closed loop bandwidth.

Even though the gain set resistor (R_G) from inverting input to ground works with R_F to set the voltage gain just like it does in a voltage feedback op amp, the closed loop bandwidth does not change. This is because the equivalent gain bandwidth product of the current feedback amplifier is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. By keeping R_F constant and changing the gain with R_G, the Thevenin resistance changes by the same amount as the change in gain. As a result, the net closed loop bandwidth of the LT1217 remains the same for various closed loop gains.

The curve on the first page shows the LT1217 voltage gain versus frequency while driving 100Ω, for five gain settings from 1 to 100. The feedback resistor is a constant 3k and the gain resistor is varied from infinity to 30Ω. Second order effects reduce the bandwidth somewhat at the higher gain settings.

Feedback Resistor Selection

The small signal bandwidth of the LT1217 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed loop gain and load resistor. The characteristic curves of bandwidth versus supply voltage are done with a heavy load (100Ω) and a light load (1kΩ) to show the effect of loading. These graphs also show the family of curves that result from various values of the feedback resistor. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

At a gain of two, on ±15V supplies with a 3kΩ feedback resistor, the bandwidth into a light load is 13.5MHz with a little peaking, but into a heavy load the bandwidth is 10MHz with no peaking. At very high closed loop gains, the bandwidth is limited by the gain bandwidth product of about 100MHz. The curves show that the bandwidth at a closed loop gain of 100 is about 1MHz.

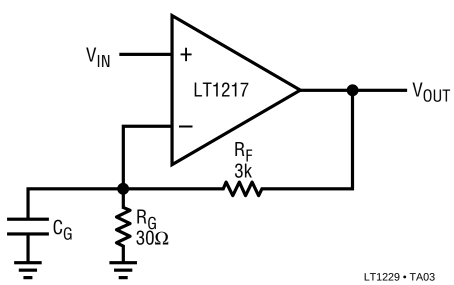
Capacitance on the Inverting Input

Current feedback amplifiers want resistive feedback from the output to the inverting input for stable operation. Take

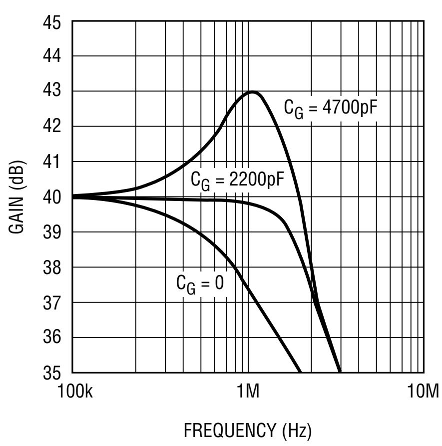
APPLICATIONS INFORMATION

care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier. The amount of capacitance that is necessary to cause peaking is a function of the closed loop gain taken.

The higher the gain, the more capacitance is required to cause peaking. We can add capacitance from the inverting input to ground to increase the bandwidth in high gain applications. For example, in this gain of 100 application, the bandwidth can be increased from 1MHz to 2MHz by adding a 2200pF capacitor.



Boosting Bandwidth of High Gain Amplifier with Capacitance on Inverting Input



Capacitive Loads

The LT1217 can be isolated from capacitive loads with a small resistor (10Ω to 20Ω) or it can drive the capacitive load directly if the feedback resistor is increased. Both techniques lower the amplifier's bandwidth about the same amount. The advantage of resistive isolation is that the bandwidth is only reduced when the capacitive load is present. The disadvantage of resistor isolation is that resistive loading causes gain errors. Because the DC accuracy is not degraded with resistive loading, the desired way of driving capacitive loads, such as flash converters, is to increase the feedback resistor. The Maximum Capacitive Load versus Feedback Resistor curve shows the value of feedback resistor and capacitive load that gives 5dB of peaking. For less peaking, use a larger feedback resistor.

Power Supplies

The LT1217 may be operated with single or split supplies as low as ±4.5V (9V total) to as high as ±18V (36V total). It is not necessary to use equal value split supplies, however, the offset voltage will degrade about 350µV per volt of mismatch. The internal compensation capacitor decreases with increasing supply voltage. The –3dB Bandwidth versus Supply Voltage curves show how this affects the bandwidth for various feedback resistors. Generally, the bandwidth at ±5V supplies is about half the value it is at ±15V supplies for a given feedback resistor.

The LT1217 is very stable even with minimal supply bypassing, however, the transient response will suffer if the supply rings. It is recommended for good slew rate and settling time that 4.7µF tantalum capacitors be placed within 0.5 inches of the supply pins.

Input Range

The non-inverting input of the LT1217 looks like a 100MΩ resistor in parallel with a 3pF capacitor until the common mode range is exceeded. The input impedance drops somewhat and the input current rises to about 10µA when the input comes too close to the supplies. Eventually, when the input exceeds the supply by one diode drop, the base collector junction of the input transistor forward biases and the input current rises dramatically. The input current should be limited to 10mA when exceeding the supplies. The amplifier will recover quickly when the input is returned to its normal common mode range unless the input was over 500mV beyond the supplies, then it will take an extra 100ns.

APPLICATIONS INFORMATION

Offset Adjust

Output offset voltage is equal to the input offset voltage times the gain plus the inverting input bias current times the feedback resistor. The LT1217 output offset voltage can be nulled by pulling approximately 30µA from pin 1 or 5. The easy way to do this is to use a 100kΩ pot between pin 1 and 5 with a 430kΩ resistor from the wiper to ground for 15V supply applications. Use a 110k resistor when operating on a 5V supply.

Shutdown

Pin 8 activates a shutdown control function. Pulling more than 50µA from pin 8 drops the supply current to less than 350µA, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8, using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1217 operates normally.

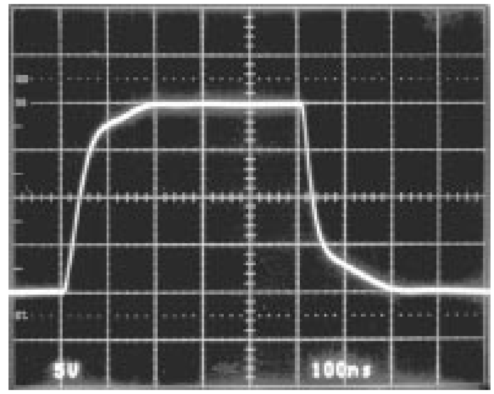
Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way it is in a traditional op amp. This is because the input stage and the output stage both have slew rate limitations. Inverting amplifiers do not slew the input and are therefore limited only by the output stage. High gain, non-inverting amplifiers are similar. The input stage slew rate of the LT1217 is about 50V/µs before it becomes non-linear and is enhanced by the normally reverse biased emitters on the input transistors. The output slew rate depends on the size of the feedback resistors. The output slew rate is about 850V/µs with a 3k feedback resistor and drops proportionally for larger values. The photos show the LT1217 with a 20V peak-to-peak output swing for three different gain configurations.

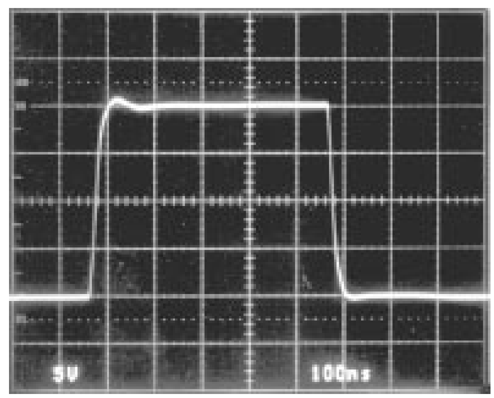
Settling Time

The characteristic curves show that the LT1217 settles to within 10mV of final value in less than 300ns for any output step up to 10V. Settling to 1mV of final value takes less than 500ns.

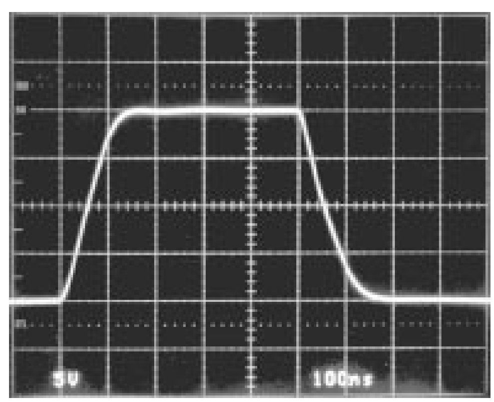
Large Signal Response, $A_V = 2$, $R_F = R_G = 3k$, Slew Rate ≃ 500V/µs



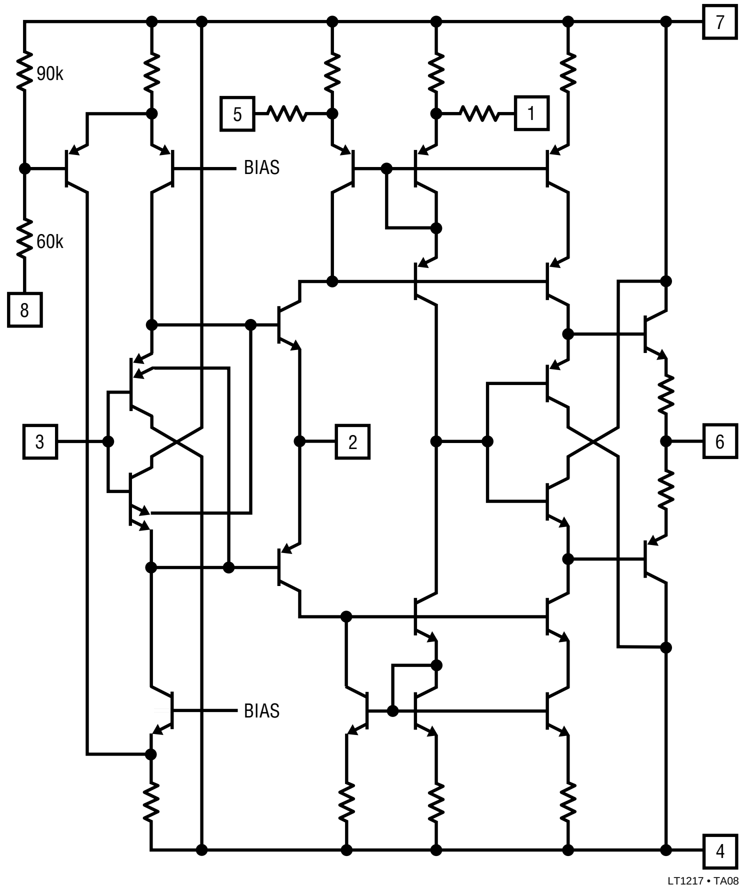
Large Signal Response, $A_V = -2$, $R_F = 3k$, $R_G = 1.5k$, Slew Rate ≃ 850V/µs



Large Signal Response, $A_V = 10$, $R_F = 3k$, $R_G = 330Ω$, Slew Rate ≃ 150V/µs



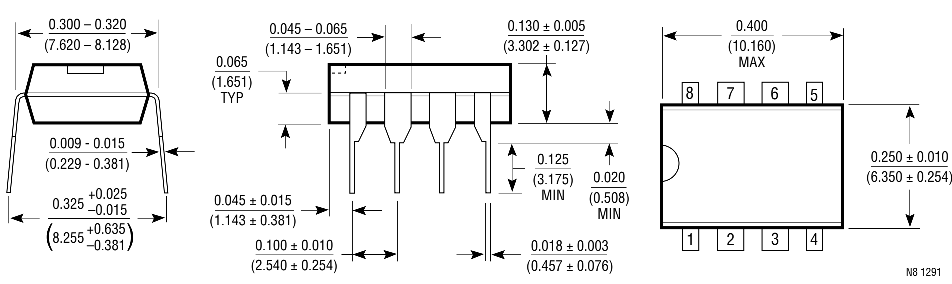
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

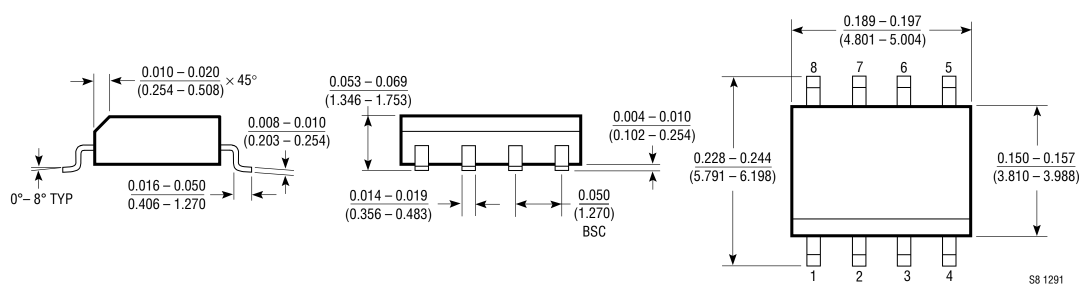
N8 Package
8-Lead Plastic DIP

$T_{J\,MAX}$	θ_{JA}
150°C	100°C/W



S8 Package
8-Lead Plastic SOIC

$T_{J\,MAX}$	θ_{JA}
150°C	150°C/W



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BA/GP 0192 10K REV 0