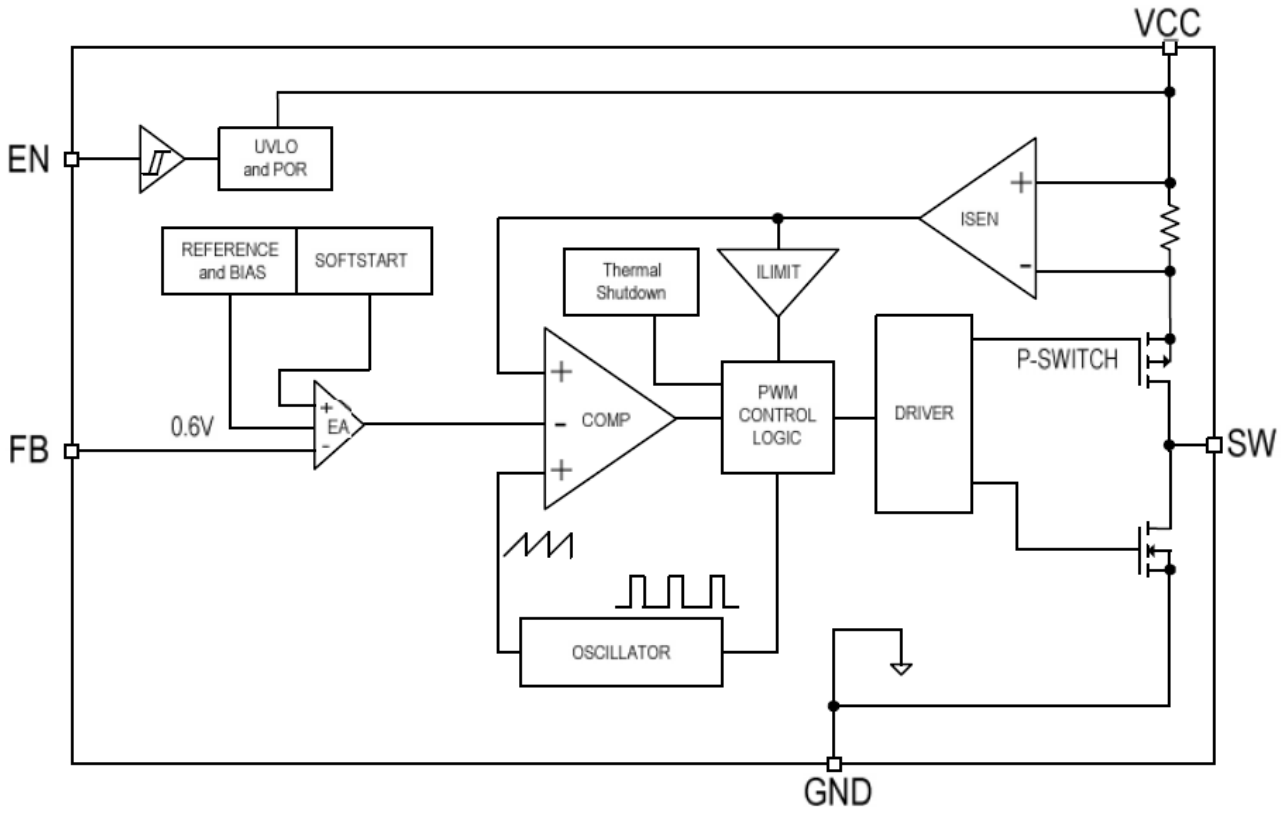
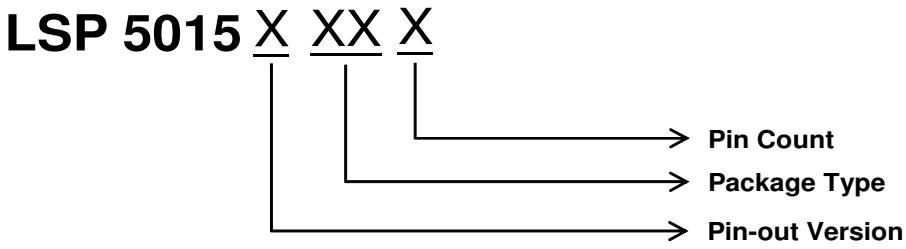
Block Diagram



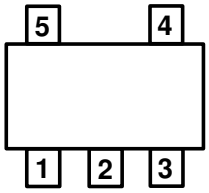
Ordering Information



Pin-out Version	Package Type	Pin Count
A (SOT23-5L) 1. EN 2. GND 3. SW 4. VCC 5. FB	AA: SOT23 AB: TSOT23 DG: TDFN2020	D: 5 E: 6
B (SOT23-5L) 1. VCC 2. GND 3. EN 4. FB 5. SW		
A (TDFN2020-6L) 1. NC 2. EN 3. VCC 4. SW 5. GND 6. FB		

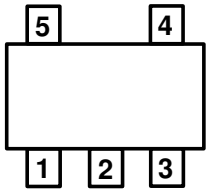
Pin Assignment

SOT23-5L / TSOT23-5L
Top View



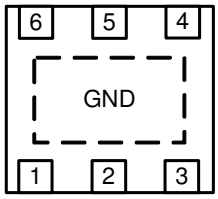
LSP5015AAAD
LSP5015AABD
1. EN
2. GND
3. SW
4. VCC
5. FB

SOT23-5L / TSOT23-5L
Top View



LSP5015BAAD
LSP5015BABD
1. VCC
2. GND
3. EN
4. VFB
5. SW

TDFN2020-6L
Top View



LSP5015ADGE
1. NC
2. EN
3. VCC
4. SW
5. GND
6. FB

Pin Descriptions

Pin Name	Pin Description
NC	No connection.
EN	Chip Enable pin. Active high.
VCC	VCC Input Pin
SW	Switching Pin
GND	Ground Pin.
FB	Feedback Pin

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
VCC pin voltage SW pin voltage		VIN	-0.3 to 7	V
SW pin voltage		VSW	-0.7 to VIN+0.3	V
EN, FB pins voltage			-0.3 to VIN+0.3	V
Operating Junction Temperature		Top	-40 to 125	℃
Storage Temperature Range			-65 to 150	℃
Thermal Resistance (Junction to Case)	SOT23-5L	θjc	81	℃/W
	TSOT23-5L		81	
	TDFN2020-6		85	
Thermal Resistance (Junction to Ambient)	SOT23-5L	θja	260	℃/W
	TSOT23-5L		230	
	TDFN2020-6		160	
Power dissipation	SOT23-5L	P_D	400	mW
	TSOT23-5L		455	
	TDFN2020-6		625	
Moisture Sensitivity		MSL	Please refer the MSL label on the IC package bag/carton for detail	

Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Recommended Operating Conditions

Characteristics	Min	Max	Unit
Supply Voltage	2.5	5.5	V
Operating Ambient Temperature Range, T_A	-40	85	℃

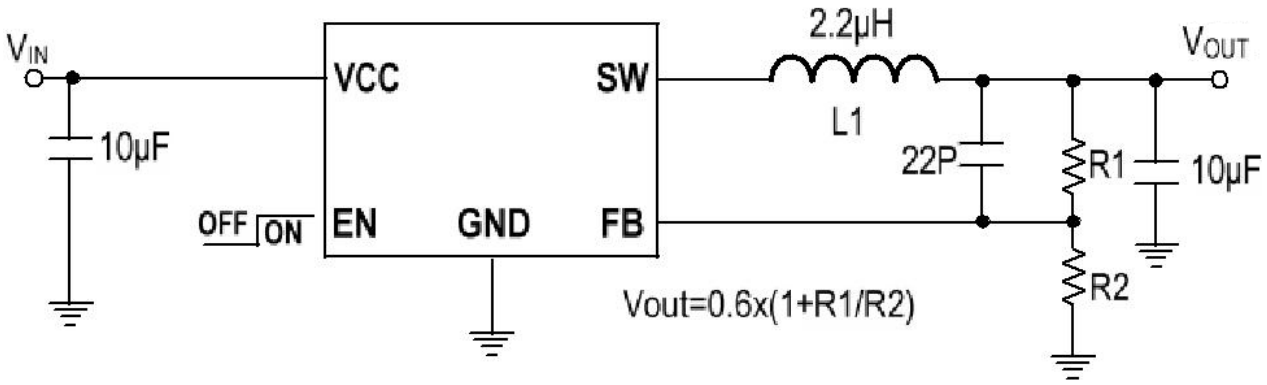
Electrical Characteristics

(VIN = 5V, VEN = 5V, VOUT = 3.3V, TA = 25℃ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage Range	VIN		2.8	-	5.5	V
Input UVLO	UVLO	IOUT=0A	1.8	2.2	2.5	V
Input OVLO	OVLO	IOUT=0A	-	6	-	V
Quiescent Current	ICCQ	VFB = 1V	-	250	350	μA
Shutdown Current	ISD	VEN = 0V	-	0.1	1	μA
FB Pin Voltage	VFB		0.588	0.6	0.612	V
FB Pin Current(Note1)	IFB		-	-	±50	nA
Load Regulation		0A < IOUT<1.0A	-	0.6	-	%
Line Regulation		2.8V<VIN<5.5V	-	0.3	-	%/V
EN Pin Voltage High	VENH		1.5	-	-	V
EN Pin Voltage Low	VENL		-	-	0.4	V
EN Pin Leakage Current		VEN = 3V	-	0.1	1	μA
Switching Frequency	FOSC		1.1	1.5	1.9	MHz
Current Limit	CL		1.7	2.2	-	A
Switching Maximum Duty	Dmax		-	-	100	%
Minimum Duty	Dmin		0	-	-	%
P-Switch RDS(ON)	RDS(ON)-P		-	170	-	mΩ
N-Switch RDS(ON)(Note1)	RDS(ON)-N		-	130	-	mΩ
Low Side Discharger			-	60	-	Ω
Thermal Shutdown	TSD		-	155	-	℃
Thermal Shutdown Protection hysteresis	TSH		-	30	-	℃

Note1: Guaranteed by design.

Application Circuit



Application Description

(1) Normal Operation

The LSP5015 uses a user adjustable frequency, current mode, synchronous step-down architecture with internal paver switch. During normal operation, the internal power switch is turned on each cycle when the oscillator sets the SR latch, and turned off when the comparator resets the SR latch. The peak inductor current at which comparator resets the SR latch is controlled by the output of error amplifier EA. While the high-side switch is off, the external schottky diode turns on until either the inductor current starts to reverse or the beginning of the next switching cycle.

(2) Setting the Output Voltage

Application circuit item shows the basic application circuit with adjustable output version. The external resistor sets the output voltage according to the following
equation:

$$VOUT=VFB \times (1+R1/R2), VFB = 0.6V$$

R2 suggest 60k~300kΩ

Table 1 Resistor select for output voltage setting

VOUT	R2	R1
1.0V	150K	100K
1.2V	100K	100K
1.5V	100K	150K
1.8V	100K	200K
2.5V	150K	470K
3.3V	100K	450K

(3) Dropout Operation

A As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the high-side switch to remain on for more than one cycle until it reaches 100% duty cycle.

The output voltage is dropped from the input supply for the voltage which across the high-side switch.

(4) Over Temperature Protection

In most applications the LSP5015 does not dissipate much heat due to high efficiency. But, in applications where the LSP5015 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 155℃, the internal high-side power switch will be turned off and the LX node will become high impedance.

(5) Over Temperature Protection

The LSP5015 cycle-by -cycle limits the peak inductor current to protect embedded switch from damage. Hence the maximum output current (the average of inductor current) is also limited. In case the load increases, the inductor current is also increase. Whenever the current limit level is reached, the output voltage cannot be regulated and starting to drop.

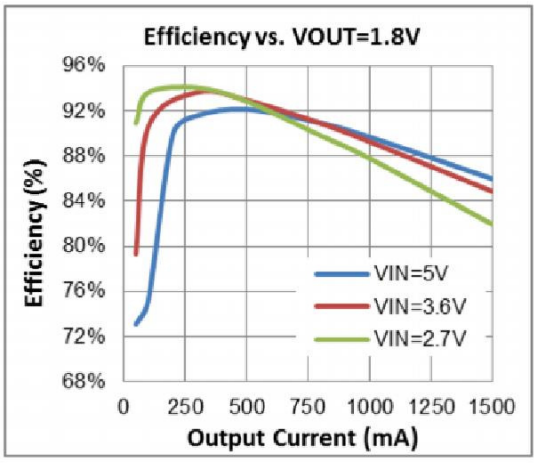
(6) Soft-Start

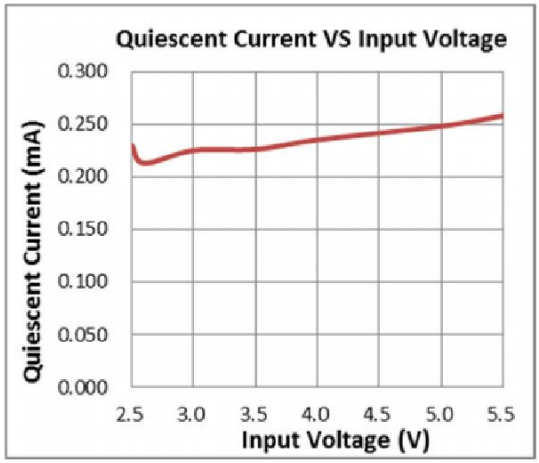
The LSP5015 employs internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under -voltage lockout or shut-down mode, the soft-start circuitry will slowly ramp up the output voltage.

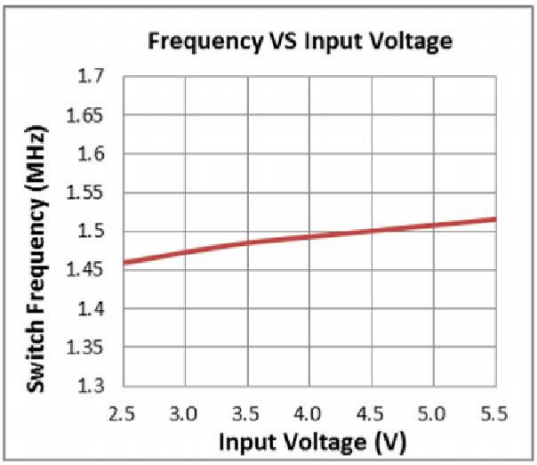
(7) Short-circuit Protection

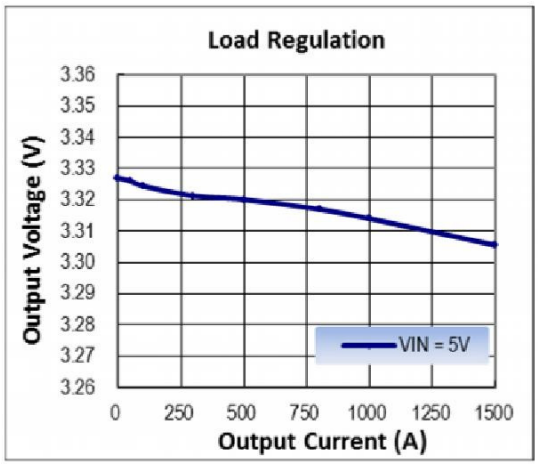
Short-circuit protection will activate once the feedback voltage falls below, and the operating frequency will be reducing normal switching frequency to reduce power delivered from input to output.

Typical Characteristics

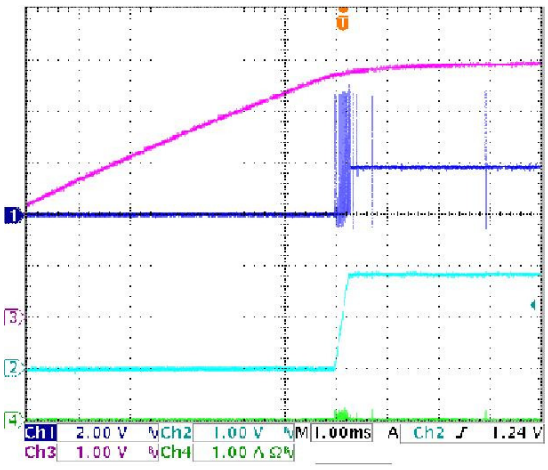




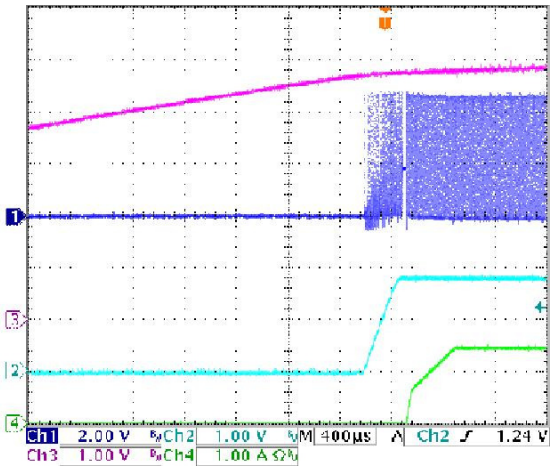




V_{IN} = 5V, V_{OUT} =1.8V,I_{LOAD} = No Load

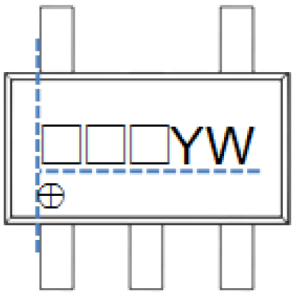


V_{IN} = 5V, V_{OUT} = 1.8V,I_{LOAD} =1.5A



Marking Information

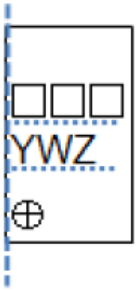
(1) SOT23-5L/TSOT23-5L



1) □□□ = Marking Name
AB = LSP5015AAAD
AY = LSP5015AABD

2) YW = Date Code
Y = Year
W = Week

(2) TDFN-6L

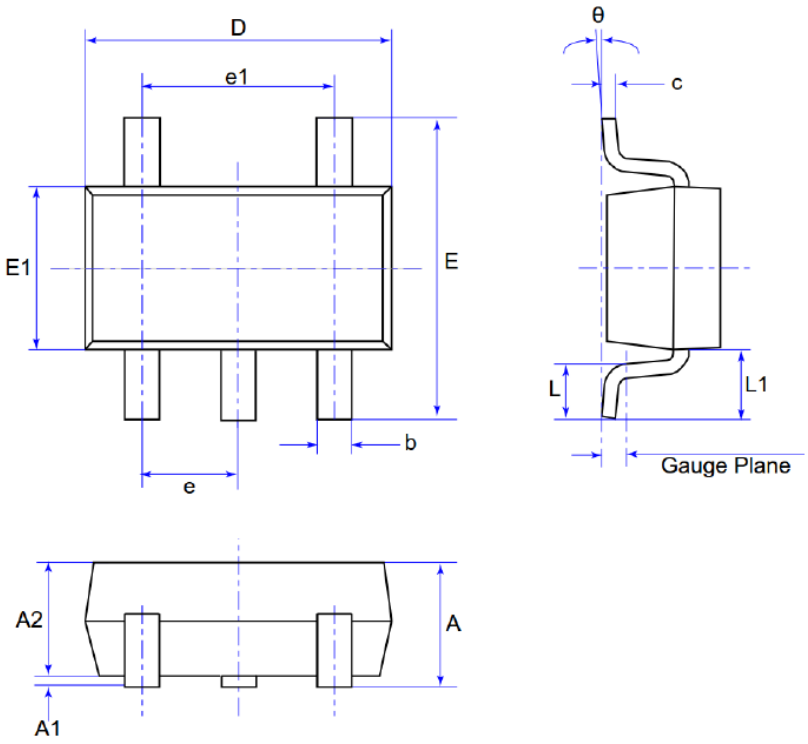


1) □□□ = Marking Name
AAC = LSP5015ADGE

2) YW = Date Code
Y = Year
W = Week
Z = Internal Code

Mechanical Information

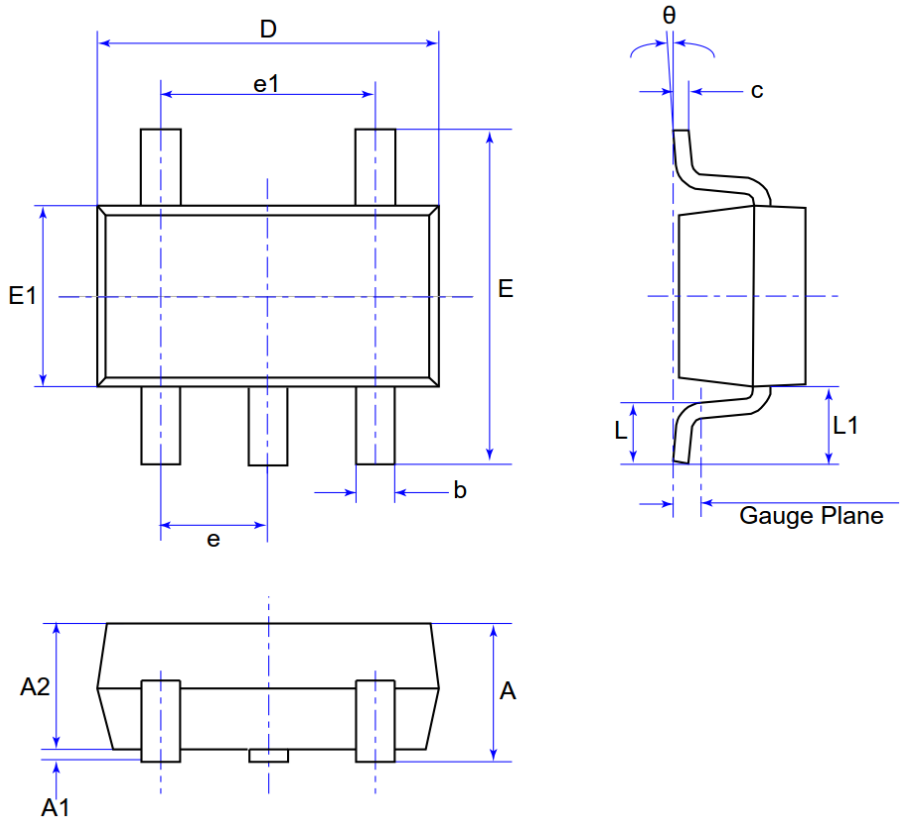
(1) SOT23-5L Package Dimensions



Unit: mm

Symbol	Min	Max
A	-	1.35
A1	-	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.21
D	2.72	3.12
E	2.60	3.00
E1	1.40	1.80
e	0.95 BSC	
e1	1.80	2.00
L	0.30	0.60
L1	0.60 REF	
Gauge Plane	0.25 REF	
θ	0^{o}	8^{o}

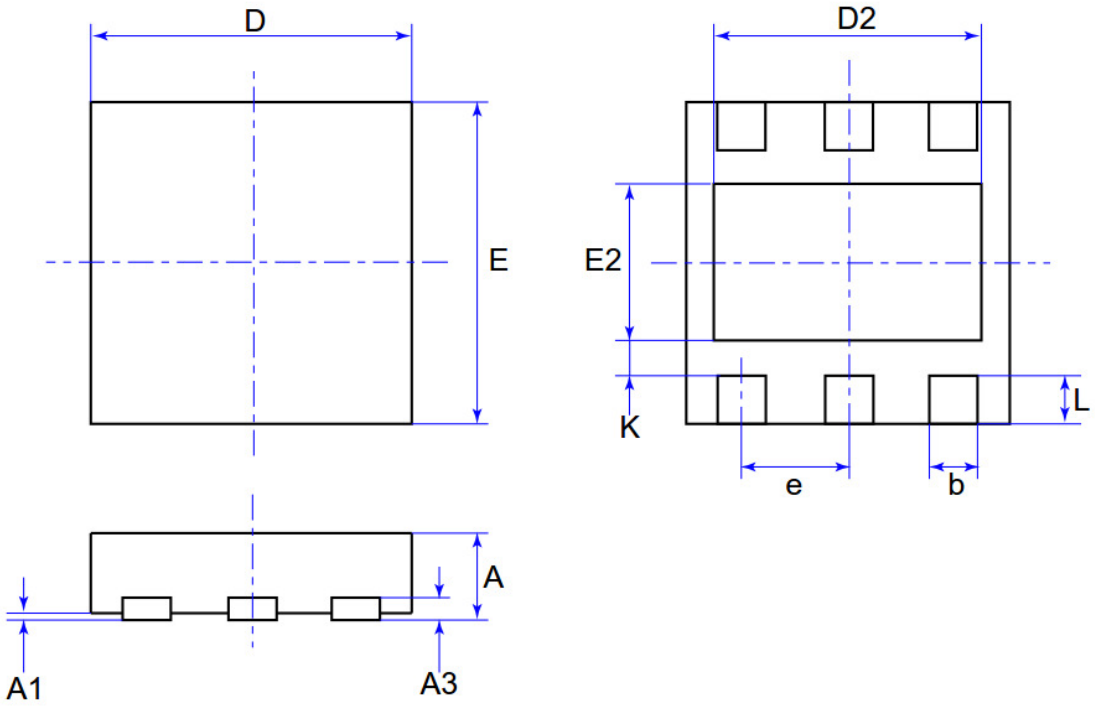
(2) TSOT23-5L Package Dimensions



Unit: mm

Symbol	Min	Max
A	-	1.10
A1	-	0.10
A2	1.00	1.00
b	0.30	0.50
c	0.08	0.20
D	2.72	3.10
E	2.60	3.00
E1	1.40	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
Gauge Plane	0.25 BSC	
θ	0°	8°

(3) TDFN2020-6L Package Dimensions



Unit: mm

Symbol	Min	Max
A	0.50	0.65
A1	-	0.05
A3	0.15 REF	
b	0.25	0.35
D	1.92	2.08
D2	1.50	1.80
E	1.90	2.08
E2	0.85	1.07
e	0.65 TYP	
L	0.20	0.45
K	0.20	-

MSL (Moisture Sensitive Level) Information

IPC/JEDEC J-STD-020D.1 Moisture Sensitivity Levels Table

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			Standard		Accelerated Equivalent [1]		
					eV 0.40-0.48	eV 0.30-0.39	CONDITION
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	
1	Unlimited	≤30 ℃ /85% RH	168 +5/-0	85 ℃ /85% RH	NA	NA	NA
2	1 year	≤30 ℃ /60% RH	168 +5/-0	85 ℃ /60% RH	NA	NA	NA
2a	4 weeks	≤30 ℃ /60% RH	696[2] +5/-0	30 ℃ /60% RH	120 -1/+0	168 -1/+0	60 ℃/ 60% RH
3	168 hours	≤30 ℃ /60% RH	192[2] +5/-0	30 ℃ /60% RH	40 -1/+0	52 -1/+0	60 ℃/ 60% RH
4	72 hours	≤30 ℃ /60% RH	96[2] +2/-0	30 ℃ /60% RH	20 +0.5/-0	24 +0.5/-0	60 ℃/ 60% RH
5	48 hours	≤30 ℃ /60% RH	72[2] +2/-0	30 ℃ /60% RH	15 +0.5/-0	20 +0.5/-0	60 ℃/ 60% RH
a	24 hours	≤30 ℃ /60% RH	48[2] +2/-0	30 ℃ /60% RH	10 +0.5/-0	13 +0.5/-0	60 ℃/ 60% RH
6	Time on Label (TOL)	≤30 ℃ /60% RH	TOL	30 ℃ /60% RH	NA	NA	NA

Note 1: CAUTION - To use the "accelerated equivalent" soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the "standard" soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the "accelerated equivalent" may be used. Accelerated soak times may vary due to material properties (e.g .mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility. If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 ℃/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 ℃/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours. If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 ℃/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 ℃/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.