■Ports

- I/O ports
  Ports whose input/output can be specified in 1-bit units: 34 (P00 to P07, P10 to P17, P20 to P25, P30 to P34, P70 to P73, PWM0, PWM1, XT2)
- USB ports 4 (UHAD+, UHAD–, UHBD+, UHBD–)
- Dedicated oscillator ports 2 (CF1, CF2)
- Input-only port (also used for the oscillator) 1 (XT1)
- Reset pin 1 ($\overline{\text{RES}}$)
- Power supply pins 6 (V_{SS}1 to 3, V_{DD}1 to 3)

■Timers

- Timer 0: 16-bit timer/counter with 2 capture registers
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter that supports PWM/toggle output
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter with an 8-bit prescaler (with toggle output)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle output) (Toggle output also possible from low-order 8 bits.)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle output) (Low-order 8 bits can be used as a PWM output.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  1) The clock can be selected from among a subclock (32.768kHz crystal oscillator), low-speed RC oscillator clock, system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes.

■Serial Interfaces

- SIO0: Synchronous serial interface
  1) LSB first/MSB first selectable
  2) Transfer clock cycle: 4/3 to 512/3 tCYC
  3) Continuous automatic data transmission (1 to 256 bits can be specified in 1-bit units) (Suspension and resumption of data transfer possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clock)
  Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clock)
  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO4: Synchronous serial interface
  1) LSB first/MSB first selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Continuous automatic data transmission (1 to 8192 bytes can be specified in 1-byte units) (Suspension and resumption of data transmission possible in 1-byte units or in word units)
  4) Clock polarity can be selected.
  5) CRC16 calculator circuit built- in
- SMIIC0: Single-master I^2C/8-bit synchronous SIO
  Mode 0: Communication in single-master mode.
  Mode 1: 8-bit synchronous serial I/O (data MSB first)

■Full Duplex UART
1) Data length: 7/8/9 bits selectable
2) Stop bits: 1 bit (2 bits in continuous transmission mode)
3) Parity bits: None/even/odd selectable (for 8-bit data only)
4) Baudrate: 16/3 to 8192/3 tCYC

■AD Converter: 12 bits × 12 channels

■PWM: Variable frequency 12-bit PWM × 2 channels

■Infrared Remote Control Receiver Circuit
1) Noise rejection function (noise filter time constant: Approx. 120µs when the 32.768kHz crystal oscillator is selected as the reference clock)
2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding.
3) X'tal HOLD mode release function

■USB Interface (host control function) × 2 ports
1) Supports full-speed (12Mbps) and low-speed (1.5Mbps) specifications.
2) Supports four transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer).

■Audio Interface
1) Sampling frequencies (fs): 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
2) Master clock: 256fs/384fs
3) Bit clock: 48fs/64fs
4) Data bit length: 16bits/18bits/20bits/24bits
5) LSB first/MSB first selectable.
6) Left justified/right justified/I2S format selectable

■Watchdog Timer
- External RC time constant type
  1) Interrupt generation/reset generation selectable
  2) Operation in HALT/HOLD mode can be selected from “continue operation” and “suspend operation.”
- Internal timer type
  1) Capable of generating a internal reset signal on an overflow of the timer running on the low-speed RC oscillator clock, or subclock.
  2) Operation in HALT/HOLD mode can be selected from among “continue count operation,” “suspend operation,” and “retain the count value.”

■Clock Output Function
1) Can output a clock with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.
2) Can output the source oscillator clock for the subclock.

■Interrupts

- 44 sources, 10 vectors

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt level is not accepted.

2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address is given priority.

No.	Vector	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/UHC-A bus active/UHC-B bus active/remote control receive
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/INT6/UHC-A device connected, disconnected, resumed
6	0002BH	H or L	T1L/T1H/INT7/AIF start/SMIIC0/UHC-B device connected, disconnected, resumed
7	00033H	H or L	SIO0/UART1 reception completed
8	0003BH	H or L	SIO1/SIO4/UART1 buffer empty/UART1 transmission completed/AIF end
9	00043H	H or L	ADC/T6/T7/UHC-ACK/UHC-NAK/UHC error/UHC-STALL
10	0004BH	H or L	Port 0/PWM0/PWM1/T4/T5/UHC-SOF

- Priority levels X > H > L
- When interrupts of the same level occur at the same time, the interrupt with the lowest vector address is given priority.

■Subroutine Stack Levels: Up to 4096 levels (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillator Circuit and PLL

- Medium-speed RC oscillator circuit (internal): For system clock (approx. 1MHz)
- Low-speed RC oscillator circuit (internal): For system clock, timer, and watchdog timer (approx. 30kHz)
- CF oscillator circuit: For system clock
- Crystal oscillator circuit: For system clock and time-of-day clock
- PLL circuit (internal): For USB interface (see Fig. 5) and audio interface (see Fig. 6)

■Internal Reset Functions

- Power-on reset (POR) function

1) POR is activated at power-on.

2) POR release voltage can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) by setting options.

- Low voltage detection reset (LVD) function

1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a threshold level.

2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, and 4.28V) can be selected by setting options.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillators do not stop automatically.
  2) There are three ways of releasing HOLD mode.
     (1) Setting the reset pin to a low level.
     (2) Generating a reset signal by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and operation of the peripheral circuits.
  1) The PLL, CF, RC and crystal oscillators automatically stop operation.
     Note: Low-speed RC oscillator is controlled directly by the watchdog timer and its oscillation in standby mode is also controlled.
  2) There are five ways of releasing HOLD mode.
     (1) Setting the reset pin to a low level
     (2) Generating a reset signal by the watchdog timer or low-voltage detection
     (3) Establishing an interrupt source at one of INT0, INT1, INT2, INT4, and INT5 pins
         * INT0 and INT1 HOLD mode release is available only when level detection is configured.
     (4) Establishing an interrupt source at port 0
     (5) Establishing an bus active interrupt source in the USB host control circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote control receiver circuit.
  1) The PLL, CF and RC oscillators automatically stop operation.
     Note: Low-speed RC oscillator is controlled directly by the watchdog timer and its oscillation in standby mode is also controlled.
     Note: The low-speed RC oscillator retains the state that is established on entry into X'tal HOLD mode if the base timer is running with the low-speed RC oscillator selected as the base timer input clock source.
  2) The state of crystal oscillator established when the X'tal HOLD mode is entered is retained.
  3) There are seven ways of releasing X'tal HOLD mode.
     (1) Setting the reset pin to a low level
     (2) Generating a reset signal by the watchdog timer or low-voltage detection
     (3) Establishing an interrupt source at one of INT0, INT1, INT2, INT4, and INT5 pins
         * INT0 and INT1 X'tal HOLD mode release is available only when level detection is configured.
     (4) Establishing an interrupt source at port 0
     (5) Establishing an interrupt source in the base timer circuit
     (6) Establishing an interrupt source in the infrared remote control receiver circuit
     (7) Establishing an bus active interrupt source in the USB host control circuit

■Development Tools

- On-chip debugger: TCB87–Type B + LC87F1K64A or
  TCB87–Type C (3-wire communication cable) + LC87F1K64A

■Flash ROM Programming Board

Package	Programming Board
SQFP48 (7×7)	W87F55256SQ

■Flash ROM Programmer

Maker		Model	Supported Version	Device
Flash Support Group Company (FSG)	Single	AF9709C	Rev.03.32 and later	87F064JU
Flash Support Group Company (FSG) + Our company (Note 1)	Onboard single/ganged	AF9101/AF9103 (main unit) (FSG model)	(Note 2)	LC87F1K64A
		SIB87 Type C (interface driver) (Our company model)		
Our company	Single/ganged	SKK/SKK Type C (SANYO FWS)	Application version 1.07 and later Chip data version 2.39 and later	LC87F1K64
	Onboard single/ganged	SKK-DBG Type C (SANYO FWS)		

(Further information on the AF series)

Flash Support Group Company (TOA ELECTRONICS, Inc.)
Phone: 053-459-1050
E-mail: sales@j- fsg.co.jp

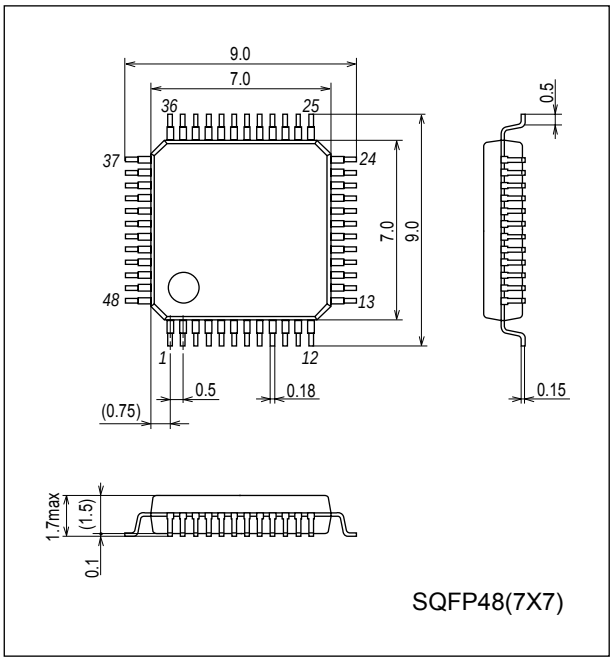
Note 1: PC-less standalone onboard programming is possible using the FSG onboard programmer (AF9101/AF9103) and the serial interface driver (SIB87 Type C) provided by Our company in pair.

Note 2: Dedicated programming device and program are required depending on the programming conditions. Contact Our company or FSG if you have any questions or difficulties regarding this matter.

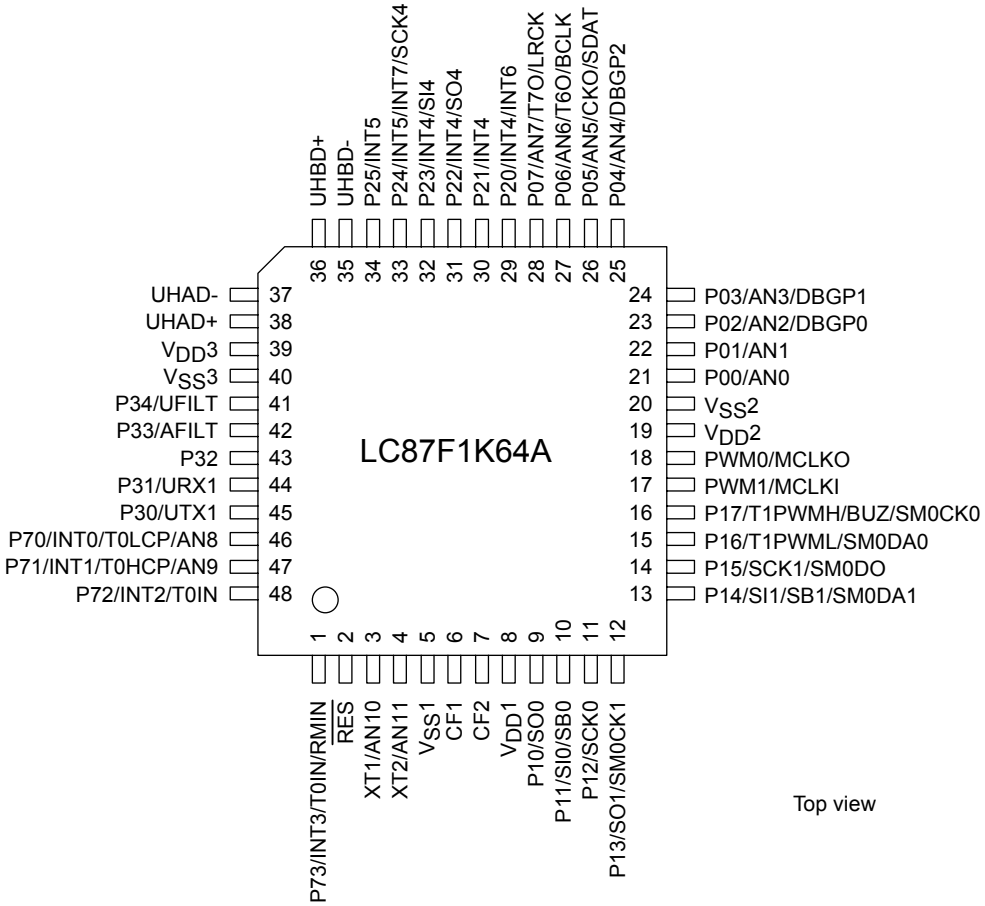
Package Dimensions

unit : mm (typ)

3163B



Pin Assignment

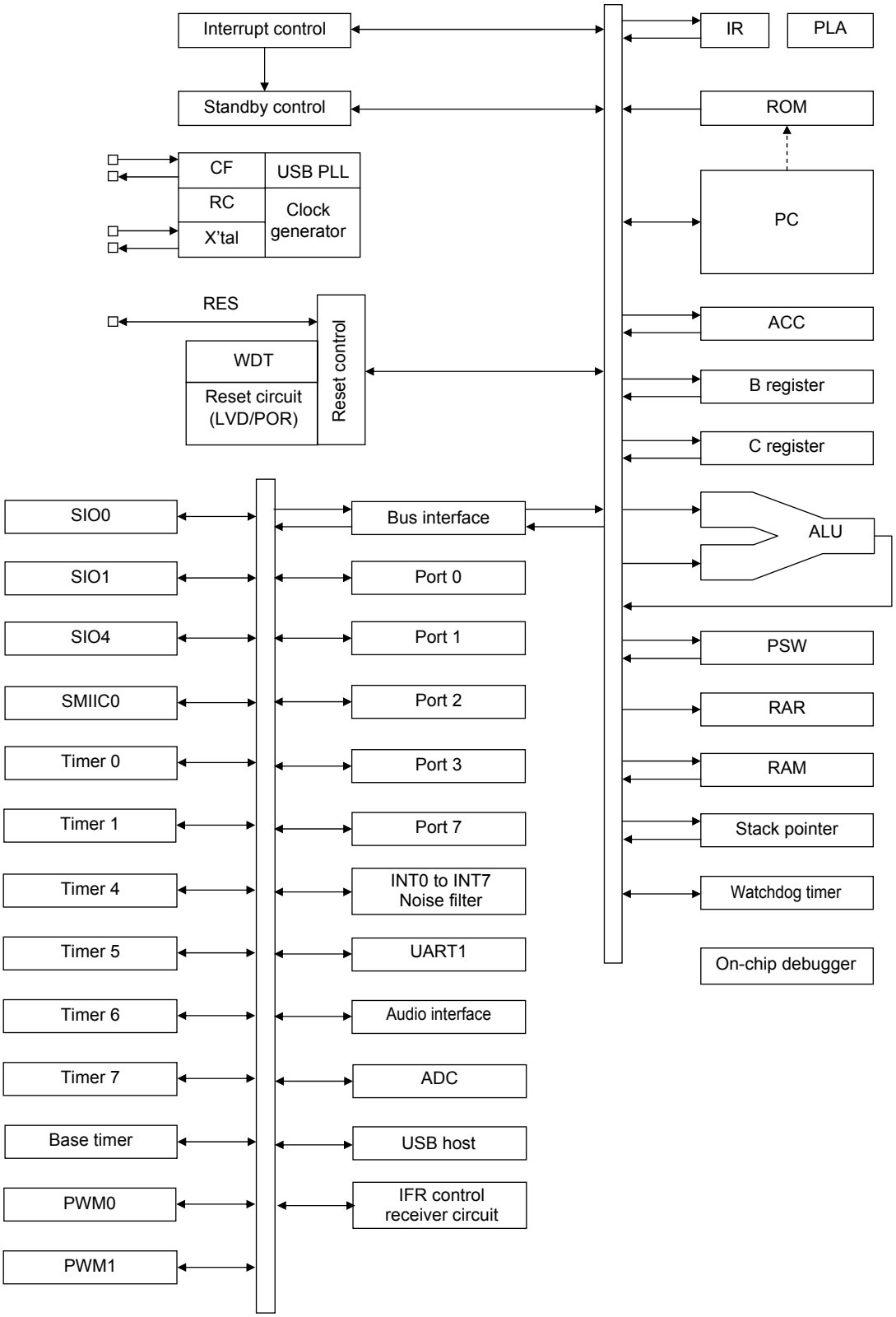


SQFP48 (7×7) (Lead-/halogen-free product)

SQFP48	NAME
1	P73/INT3/T0IN/RMIN
2	$\overline{RES}$
3	XT1/AN10
4	XT2/AN11
5	$V_{SS}1$
6	CF1
7	CF2
8	$V_{DD}1$
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1/SM0CK1
13	P14/SI1/SB1/SM0DA1
14	P15/SCK1/SM0DO
15	P16/T1PWML/SM0DA0
16	P17/T1PWMH/BUZ/SM0CK0
17	PWM1/MCLKI
18	PWM0/MCLKO
19	$V_{DD}2$
20	$V_{SS}2$
21	P00/AN0
22	P01/AN1
23	P02/AN2/DBGP0
24	P03/AN3/DBGP1

SQFP48	NAME
25	P04/AN4/DBGP2
26	P05/AN5/CKO/SDAT
27	P06/AN6/T6O/BCLK
28	P07/AN7/T7O/LRCK
29	P20/INT4/INT6
30	P21/INT4
31	P22/INT4/SO4
32	P23/INT4/SI4
33	P24/INT5/INT7/SCK4
34	P25/INT5
35	UHBD-
36	UHBD+
37	UHAD-
38	UHAD+
39	$V_{DD}3$
40	$V_{SS}3$
41	P34/UFILT
42	P33/AFILT
43	P32
44	P31/URX1
45	P30/UTX1
46	P70/INT0/T0LCP/AN8
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$, $V_{SS}3$</td><td>-</td><td>-power supply</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$</td><td>-</td><td>+power supply</td><td>No</td></tr>
<tr><td>$V_{DD}3$</td><td>-</td><td>USB reference voltage</td><td>Yes</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• HOLD release input
• Port 0 interrupt input
• Pin functions
AD converter input port: AN0 to AN7 (P00 to P07)
On-chip debugger pins: DBGP0 to DBGP2 (P02 to P04)
P05: System clock output / audio interface SDAT I/O
P06: Timer 6 toggle output / audio interface BCLK I/O
P07: Timer 7 toggle output / audio interface LRCK I/O</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input / bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output / SMIIC0 clock I/O
P14: SIO1 data input / bus I/O / SMIIC0 bus I/O / data input
P15: SIO1 clock I/O / SMIIC0 data output (used in 3-wire SIO mode)
P16: Timer 1 PWML output / SMIIC0 bus I/O / data input
P17: Timer 1 PWMH output / buzzer output / SMIIC0 clock I/O</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P25</td><td>I/O</td><td>• 6-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P20 to P23: INT4 input / HOLD release input / timer 1 event input / timer 0L capture input / timer 0H capture input
P24 to P25: INT5 input / HOLD release input / timer 1 event input / timer 0L capture input / timer 0H capture input
P20: INT6 input / timer 0L capture 1 input
P22: SIO4 data I/O
P23: SIO4 data I/O
P24: INT7 input / timer 0H capture 1 input / SIO4 clock I/O
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT4</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT5</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT6</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT7</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P34</td><td>I/O</td><td>• 5-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30: UART1 transmit
P31: UART1 receive
P33: Connected to audio interface PLL filter circuit (see Fig. 6).
P34: Connected to USB interface PLL filter circuit (see Fig. 5).</td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P70: INT0 input / HOLD release input / timer 0L capture input /
watchdog timer output
P71: INT1 input / HOLD release input / timer 0H capture input
P72: INT2 input / HOLD release input / timer 0 event input /
timer 0L capture input / high-speed clock counter input
P73: INT3 input (input with noise filter) / timer 0 event input /
timer 0H capture input / infrared remote control receiver input
AD converter input port: AN8 (P70), AN9 (P71)
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising &
Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT2</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0
PWM1</td><td>I/O</td><td>PWM0 and PWM1 output port
General-purpose input port
• Pin functions
PWM0: Audio interface master clock output
PWM1: Audio interface master clock input</td><td>No</td></tr>
<tr><td>UHAD-
UHAD+</td><td>I/O</td><td>USB-A port data I/O pin / general-purpose I/O port</td><td>No</td></tr>
<tr><td>UHBD-
UHBD+</td><td>I/O</td><td>USB-B port data I/O pin / general-purpose I/O port</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input / internal reset output</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>• 32.768kHz crystal resonator input
• Pin functions
General-purpose input port
AD converter input port: AN10</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal resonator output
• Pin functions
General-purpose I/O port
AD converter input port: AN11</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>Ceramic/crystal resonator input</td><td>No</td></tr>
<tr><td>CF2</td><td>O</td><td>Ceramic/crystal resonator output</td><td>No</td></tr>
</table>

On-chip Debugger Pin Treatment

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation Manual."

Recommended Unused Pin Treatment

Pin Name	Recommended Unused Pin Treatment	
	Board	Software
P00 to P03, P05 to P07	Open	Set output low.
P04	Pull-down with a 100kΩ resistor.	-
P10 to P17	Open	Set output low.
P20 to P25	Open	Set output low.
P30 to P34	Open	Set output low.
P70 to P73	Open	Set output low.
PWM0, PWM1	Open	Set output low.
UHAD+, UHAD-	Open	Set output low.
UHBD+, UHBD-	Open	Set output low.
XT1	Pull-down with a resistor of 100kΩ or lower.	-
XT2	Open	Set output low.

Note: Since P34 is multiplexed with UFILT, it must be configured for input when the USB function is to be used.
Since P33 is multiplexed with AFILT, it must be configured for input when the audio interface PLL circuit is to be used.

Port Output Types

The table below lists the type of port output and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07 P10 to P17 P20 to P25 P30 to P34	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	-	No	N-channel open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
UHAD+, UHAD- UHBD+, UHBD-	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal resonator output (N-channel open drain when in general-purpose output mode)	No

User Option Table

Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	○	1 bit	CMOS
				N-channel open drain
	P10 to P17	○	1 bit	CMOS
				N-channel open drain
	P20 to P25	○	1 bit	CMOS
				N-channel open drain
	P30 to P34	○	1 bit	CMOS
				N-channel open drain
Program start address	-	○	-	00000h
				0FE00h
USB regulator	USB regulator	○	-	Use
				Non-use
	USB regulator (HOLD mode)	○	-	Use
				Non-use
	USB regulator (HALT mode)	○	-	Use
				Non-use
Main clock 8MHz selection	-	○	-	Enable
				Disable
Low-voltage detection reset function	Detection function	○	-	Enable: Use
				Disable: Non-use
	Detection level	○	-	7 levels
Power-on reset function	Power-on reset level	○	-	8 levels

USB Reference Power Option

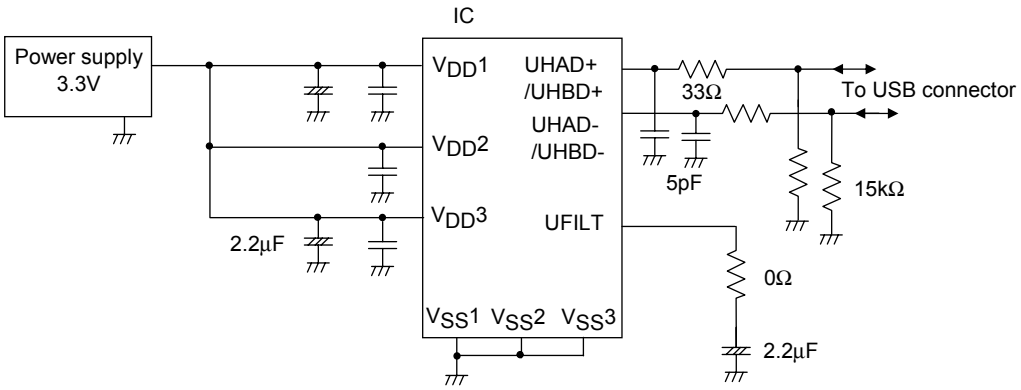
When a voltage 4.5 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by selecting an option. The procedure for making the option selection is described below.

		(1)	(2)	(3)	(4)
Option settings	USB regulator	Use	Use	Use	Non-use
	USB regulator at HOLD mode	Use	Non-use	Non-use	Non-use
	USB regulator at HALT mode	Use	Non-use	Use	Non-use
Reference voltage circuit state	Normal mode	Active	Active	Active	Inactive
	HOLD mode	Active	Inactive	Inactive	Inactive
	HALT mode	Active	Inactive	Active	Inactive

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for the USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100µA compared with when the reference voltage circuit is inactive.

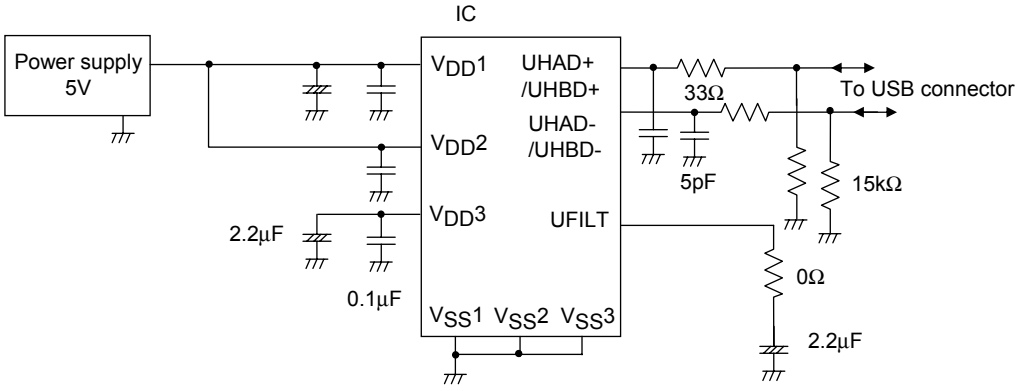
Example 1: $V_{DD}1=V_{DD}2=3.3V$

- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.



Example 2: $V_{DD}1=V_{DD}2=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and V_{SS}.



(Note: Do not apply the voltage of more than 3.6V to UHAD+, UHAD-, UHBD+ and UHBD- when the reference voltage circuit is active.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, CF1, $\overline{RES}$			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2, 3, 7 PWM0, PWM1 XT2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-10			mA
		IOPH(2)	PWM0, PWM1	• Per 1 applicable pin		-20			
		IOPH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-7.5			
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15			
		IOMH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total current of all applicable pins		-25			
		ΣIOAH(2)	Port 1 PWM0, PWM1	Total current of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 1, 2 PWM0, PWM1	Total current of all applicable pins		-45			
		ΣIOAH(4)	Port 3 P71 to P73	Total current of all applicable pins		-10			
		ΣIOAH(5)	UHAD+, UHAD- UHBD+, UHBD-	Total current of all applicable pins		-50			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 3, 7 XT2	Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Ports 3, 7 XT2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total current of all applicable pins				45	
		ΣIOAL(2)	Port 1 PWM0, PWM1	Total current of all applicable pins				45	
		ΣIOAL(3)	Ports 0, 1, 2 PWM0, PWM1	Total current of all applicable pins				80	
		ΣIOAL(4)	Ports 3, 7 XT2	Total current of all applicable pins				15	
		ΣIOAL(5)	UHAD+, UHAD- UHBD+, UHBD-	Total current of all applicable pins				50	
Allowable power dissipation		Pd max	SQFP48(7×7)	Ta=-40 to +85°C				140	mW
Operating ambient Temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245µs ≤ tCYC ≤ 200µs		3.0		5.5	V
			0.245µs ≤ tCYC ≤ 0.383µs USB circuit active.		3.0		5.5	
			0.490µs ≤ tCYC ≤ 200µs Except for onboard programming mode		2.7		5.5	
Memory retention supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents are retained in HOLD mode		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 2, 3, 7 PWM0, PWM1		2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3, 7		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(2)$			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 0 PWM0, PWM1		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(4)$			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(5)$	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.245		200	µs
			USB circuit active.	3.0 to 5.5	0.245		0.383	
			Except for onboard programming mode	2.7 to 5.5	0.490		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio =1/1 • External system clock duty =50±5%	3.0 to 5.5	0.1		12	MHz
			• CF2 pin open • System clock frequency division ratio =1/1 • External system clock duty =50±5%	2.7 to 5.5	0.1		6	
Oscillation frequency range (Note 2-3)	FmCF	CF1, CF2	12MHz ceramic oscillation mode See Fig. 1.	3.0 to 5.5		12		MHz
	FmRC		Internal medium-speed RC oscillation	2.7 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	2.7 to 5.5	15	30	60	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation mode See Fig. 2.	2.7 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3, 7 $\overline{RES}$ PWM0, PWM1	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.7 to 5.5			1	µA
	$I_{IH}(2)$	XT1, XT2	Input port configuration $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3, 7 $\overline{RES}$ PWM0, PWM1	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.7 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2	Input port configuration $V_{IN}=V_{SS}$	2.7 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.7 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 P71 to P73	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	PWM0, PWM1 P05 to P07 (Note 3-1)	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(5)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-1mA	2.7 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=2.5mA	2.7 to 5.5			0.4	
	$V_{OL}(4)$	Ports 0, 1, 2 PWM0, PWM1 XT2	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(5)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$		I_{OL}=1mA	2.7 to 5.5			0.4	
	$V_{OL}(7)$	Ports 3, 7	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(8)$		I_{OL}=1mA	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3, 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 4.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 3, 7		2.7 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than those under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.7 to 5.5		10		pF

Note 3-1: When the CKO system clock output function (P05) or the audio interface output function (P05 to P07) is used.

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 9.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transmission/ reception mode • USB, AIF, SIO4 not used at the same time. • See Fig. 9. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transmission/ reception mode • USB used at the same time • AIF, SIO4 not used at the same time. • See Fig. 9. • (Note 4-1-2)		7			
			tSCKHA(1c)		• Continuous data transmission/ reception mode • USB, AIF, SIO4 used at the same time. • See Fig. 9. • (Note 4-1-2)		9			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• When CMOS output type is selected. • See Fig. 9.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transmission/ reception mode • USB, AIF, SIO4 not used at the same time. • When CMOS output type is selected. • See Fig. 9.		tSCKH(2) +2tCYC		tSCKH(2) + (10/3)tCYC	tCYC
			tSCKHA(2b)		• Continuous data transmission/ reception mode • USB used at the same time • AIF, SIO4 not used at the same time. • When CMOS output type is selected. • See Fig. 9.		tSCKH(2) +2tCYC		tSCKH(2) + (19/3)tCYC	
			tSCKHA(2c)		• Continuous data transmission/ reception mode • USB, AIF, SIO4 used at the same time • When CMOS output type is selected. • See Fig. 9.		tSCKH(2) +2tCYC		tSCKH(2) + (25/3)tCYC	

Note 4-1-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-1-2: In an application where the serial clock input is to be used in continuous data transmission/reception mode, the time from SI0RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.

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Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK • See Fig. 9.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdDO(1)	SO0(P10), SB0(P11)	• Continuous data transmission/ reception mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	
			tdDO(2)		• Synchronous 8-bit mode • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdDO(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be defined as the time up to the beginning of output state change in open drain output mode. See Fig. 9.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pins/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 9.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• When CMOS output type is selected. • See Fig. 9.	2.7 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 9.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time up to the beginning of output state change in open drain output mode. • See Fig. 9.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

3. SIO4 Serial I/O Characteristics (Note 4-3-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK4(P24)	See Fig. 9.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• USB, SIO0 continuous transfer mode, AIF not used at the same time. • See Fig. 9. • (Note 4-3-2)		4			
			tSCKHA(5b)		• USB used at the same time. • SIO0 continuous transfer mode, AIF not used at the same time. • See Fig. 9. • (Note 4-3-2)		7			
			tSCKHA(5c)		• USB, SIO0 continuous transfer mode used at the same time. • AIF not used at the same time. • See Fig. 9. • (Note 4-3-2)		10			
	Output clock	Frequency	tSCK(6)	SCK4(P24)	• When CMOS output type is selected. • See Fig. 9.	2.7 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(6)				1/2			
		High level pulse width	tSCKH(6)				1/2			
			tSCKHA(6a)		• USB, SIO0 continuous transfer mode AIF not used at the same time. • When CMOS output type is selected. • See Fig. 9.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (10/3)tCYC	tCYC
			tSCKHA(6b)		• USB used at the same time. • SIO0 continuous transfer mode AIF not used at the same time. • When CMOS output type is selected. • See Fig. 9.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (19/3)tCYC	
			tSCKHA(6c)		• USB, SIO0 continuous transfer mode used at the same time • AIF not used at the same time. • When CMOS output type is selected. • See Fig. 9.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (28/3)tCYC	
Serial input	Data setup time		tsDI(3)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 9.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Output delay time		tdDO(5)	SO4(P22), SI4(P23)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time up to the beginning of output state change in open drain output mode • See Fig. 9.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-3-2: In an application where the serial clock input is to be used, the time from SI4RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA when continuous data transmission/reception is started.

4-1. SMIIC0 Simple SIO Mode I/O Characteristics (Note 4-4-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(7)	SM0CK0(P17), SM0CK1(P13)	See Fig. 9.	2.7 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(7)				2/3			
		High level pulse width	tSCKH(7)				2/3			
	Output clock	Frequency	tSCK(8)	SM0CK0(P17), SM0CK1(P13)	• When CMOS output type is selected. • See Fig. 9.	2.7 to 5.5	4/3			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(4)	SM0DA0(P16), SM0DA1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 9.	2.7 to 5.5	0.03			µs
	Data hold time		thDI(4)				0.03			
Serial output	Output delay time		tdDO(6)	SM0DO(P15), SM0DA0(P16), SM0DA1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change. • See Fig. 9.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

4-2. SMIIC0 I²C Mode I/O Characteristics (Note 4-5-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCL	SM0CK0(P17), SM0CK1(P13)	See Fig. 11.	2.7 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Frequency	tSCLx	SM0CK0(P17), SM0CK1(P13)	Must be specified as the time up to the beginning of output state change.	2.7 to 5.5	10			tSCL
		Low level pulse width	tSCLLx				1/2			
		HIghlevel pulse width	tSCLHx				1/2			
SM0CK, SM0DA pin input spike suppression time			tsp	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5			1	Tfilt
Bus relinquish time between start and stop	input		tBUF	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5	2.5			Tfilt
	Output		tBUFx		• Standard clock mode • Must be specified as the time up to the beginning of output state change.		5.5			µs
					• High-speed clock mode • Must be specified as the time up to the beginning of output state change.		1.6			
Start, restart condition hold time	input		tHD; STA	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	• When SMIIC register control bit SHDS=0 • See Fig. 11.	2.7 to 5.5	2.0			Tfilt
					• When SMIIC register control bit SHDS=1 • See Fig. 11.		2.5			
	Output		tHD; STAx		• Standard clock mode • Must be specified as the time up to the beginning of output state change.		4.1			µs
					• High-speed clock mode • Must be specified as the time up to the beginning of output state change.		1.0			
Restart condition setup time	input		tSU; STA	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5	1.0			Tfilt
	Output		tSU; STAx		• Standard clock mode • Must be specified as the time up to the beginning of output state change.		5.5			µs
					• High-speed clock mode • Must be specified as the time up to the beginning of output state change.		1.6			

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Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Stop condition setup time	input	tSU; STO	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5	1.0			Tfilt
	Output	tSU; STOx		• Standard clock mode • Must be specified as the time up to the beginning of output state change.		4.9			µs
				• High-speed clock mode • Must be specified as the time up to the beginning of output state change.		1.1			
Data hold time	Input	tHD; DAT	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5	0			Tfilt
	Output	tHD; DATx		Must be specified as the time up to the beginning of output state change.		1		1.5	
Data setup time	Input	tSU; DAT	SM0CK0(P17), SM0CK1(P13), SM0DA0(P16), SM0DA1(P14)	See Fig. 11.	2.7 to 5.5	1			Tfilt
	Output	tSU; DATx		Must be specified as the time up to the beginning of output state change.		1tSCL-1.5Tfilt			

Note 4-5-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-5-2: The value of Tfilt is determined by bits 7 and 6 (BRP1 and BRP0) of the SMIC0BRG register and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	(1/3) tCYC×1
0	1	(1/3) tCYC×2
1	0	(1/3) tCYC×3
1	1	(1/3) tCYC×4

Set the value of the BRP1 and BRP0 bits so that the value of Tfilt falls within the following value range:

250ns ≥ Tfilt > 140ns

Note 4-5-3: For standard clock mode operation, set up the SMIC0BRG register so that the following conditions are satisfied:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 1

SCL frequency value ≤ 100kHz

For high-speed clock mode operation, set up the SMIC0BRG register so that the following conditions are satisfied:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 1

SCL frequency value ≤ 400kHz

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P25), INT6(P20), INT7(P24)	• Interrupt source flag can be set. • Event inputs for timer 0/1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noisefilter time constant is 1/1.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noisefilter time constant is 1/32.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noisefilter time constant is 1/128.	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIL(5)	RMIN(P73)	Recognized as a signal by infrared remote control receiver circuit	2.7 to 5.5	4			RMCK (Note 5-1)
	tPIL(6)	$\overline{RES}$	Resetting is enabled.	2.7 to 5.5	200			μs

Note 5-1: Denotes the reference frequency of the infrared remote control receiver circuit (1tCYC to 128tCYC or source oscillation frequency of the subclock)

AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12-bit AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	32		115	µs
				3.0 to 5.5	64		115	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

<8-bit AD Converter Mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		See conversion time calculation formulas. (Note 6-2)	4.0 to 5.5	20		90	µs
				3.0 to 5.5	40		90	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
A Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Conversion time calculation formulas :

12-bits AD Converter Mode : TCAD (Conversion time) = ((52/(AD division ratio))+2) × (1/3) × tCYC

8-bits AD Converter Mode : TCAD (Conversion time) = ((32/(AD division ratio))+2) × (1/3) × tCYC

<Recommended Operating Conditions>

External Oscillator FmCF[MHz]	Supply Voltage Range V_{DD}[V]	System Clock Division (SYSDIV)	Cycle Time tCYC [ns]	AD Frequency Division Ratio (ADDIV)	Conversion Time (TCAD)[µs]	
					12-bit AD	8-bit AD
12	4.0 to 5.5	1/1	250	1/8	34.8	21.5
	3.0 to 5.5	1/1	250	1/16	69.5	42.8

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process until the time the conversion result register is loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is doubled in the following cases:

- The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.
- The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Conditions	Option selected voltage	Specification min	typ	max	unit
POR release voltage	PORRL	Select from option (Note 7-1)	1.67V	1.55	1.67	1.79	V
			1.97V	1.85	1.97	2.09	
			2.07V	1.95	2.07	2.19	
			2.37V	2.25	2.37	2.49	
			2.57V	2.45	2.57	2.69	
			2.87V	2.75	2.87	2.99	
			3.86V	3.73	3.86	3.99	
			4.35V	4.21	4.35	4.49	
Detection voltage unknown state	POUKS	See Fig. 13 (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS	Power supply rise time from V_{DD}=0V to 1.6V				100	ms

Note 7-1: The POR release level can be selected out of 8 levels only when LDV reset function is disabled.
Note 7-2: POR is in unknown state before transistors start operation.

Low Voltage Detection (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Conditions	Option selected voltage	Specification min	typ	max	unit
LVD reset voltage (Note 8-2)	LVDET	Select from option. See Fig. 14. (Note 8-1) (Note 8-3)	1.91V	1.81	1.91	2.01	V
			2.01V	1.91	2.01	2.11	
			2.31V	2.21	2.31	2.41	
			2.51V	2.41	2.51	2.61	
			2.81V	2.71	2.81	2.91	
			3.79V	3.69	3.79	3.89	
			4.28V	4.18	4.28	4.38	
LVD hysteresis width	LVHYS		1.91V		55		mV
			2.01V		55		
			2.31V		55		
			2.51V		55		
			2.81V		55		
			3.79V		60		
			4.28V		65		
Detection voltage unknown state	LVUKS	See Fig. 14. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW	LVDET-0.5V See Fig. 15.		0.2			ms

Note 8-1: The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.
Note 8-2: LVD reset voltage specification values do not include hysteresis voltage.
Note 8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.
Note 8-4: LVD is in an unknown state before transistors start operation.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal low-/medium-speed RC oscillation stopped • USB circuit stopped • 1/1 frequency division ratio	4.5 to 5.5		9.8	18	mA
				3.0 to 3.6		5.7	11	
	IDDOP(2)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode active • Internal low-/medium-speed RC oscillation stopped • USB circuit active • 1/1 frequency division ratio	4.5 to 5.5		15	28	
				3.0 to 3.6		8.1	15	
	IDDOP(3)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal low-/medium-speed RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		6.7	12	
				3.0 to 3.6		4.2	7.1	
				2.7 to 3.0		3.5	5.8	
	IDDOP(4)		• External oscillation FmCF stopped • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal medium-speed RC oscillation • Internal low-speed RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		0.77	2.8	
				3.0 to 3.6		0.46	1.5	
				2.7 to 3.0		0.39	1.3	
	IDDOP(5)		• External oscillation FsX'tal /FmCF stopped • System clock set to internal low-speed RC oscillation • Internal medium-speed RC oscillation stopped • 1/1 frequency division ratio	4.5 to 5.5		28	170	µA
				3.0 to 3.6		18	100	
				2.7 to 3.0		16	87	
	IDDOP(6)		• External oscillation FmCF stopped • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low-/medium-speed RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		45	124	
				3.0 to 3.6		18	60	
				2.7 to 3.0		14	48	
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal low-/medium-speed RC oscillation stopped • USB circuit stopped • 1/1 frequency division ratio	4.5 to 5.5		4.0	7.0	mA
				3.0 to 3.6		2.2	3.8	

Note 9-1: The consumption current value do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2: The consumption current values do not include operational current of LVD (Low Voltage Detection) function if not specified.

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Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(2)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation active • Internal low-/medium-speed RC oscillation stopped • USB circuit active •1/1 frequency division ratio	4.5 to 5.5		9.2	18	mA
				3.0 to 3.6		4.7	8.6	
	IDDHALT(3)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal low-/medium-speed RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		2.5	4.5	
				3.0 to 3.6		1.3	2.3	
				2.7 to 3.0		1.1	1.8	
	IDDHALT(4)		• HALT mode • External oscillation FmCF stopped • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal medium-speed RC oscillation • Internal low-speed RC oscillation stopped •1/2 frequency division ratio	4.5 to 5.5		0.41	1.5	
				3.0 to 3.6		0.20	0.72	
				2.7 to 3.0		0.17	0.53	
	IDDHALT(5)		• HALT mode • External oscillation FsX'tal /FmCF stopped • System clock set to internal low-speed RC oscillation • Internal medium-speed RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		7.2	95	µA
				3.0 to 3.6		4.0	51	
				2.7 to 3.0		3.4	43	
	IDDHALT(6)		• HALT mode • External oscillation FmCF stopped • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal low-/medium-speed RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		30	112	
				3.0 to 3.6		8.4	51	
				2.7 to 3.0		5.8	40	
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)		• HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.28	67	
				3.0 to 3.6		0.22	35	
				2.7 to 3.0		0.21	30	
	IDDHOLD(2)		• HOLD mode • LVD option selected • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		2.8	70	
				3.0 to 3.6		2.3	38	
				2.7 to 3.0		2.1	33	
	IDDHOLD(3)		• HOLD mode • Internal timer type watchdog timer active (Internal low-speed RC oscillation circuit active) • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.98	68	
				3.0 to 3.6		0.62	36	
				2.7 to 3.0		0.51	31	
X'tal HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(4)		• X'tal HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		26	106	
				3.0 to 3.6		6.1	49	
				2.7 to 3.0		3.8	38	
	IDDHOLD(5)		• X'tal HOLD mode • CF1=V_{DD} or open (External clock mode) • FmSRC=30kHz internal low-speed RC oscillation mode	4.5 to 5.5		1.0	68	
				3.0 to 3.6		0.64	36	
				2.7 to 3.0		0.53	31	

Note 9-1: The consumption current value do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2: The consumption current values do not include operational current of LVD (Low Voltage Detection) function if not specified.

USB Characteristics and Timing at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			
			min	typ	max	unit
High level output	$V_{OH(USB)}$	• 15kΩ±5% to GND	2.8		3.6	V
Low level output	VOL(USB)	• 1.5kΩ±5% to 3.6V	0.0		0.3	V
Output signal crossover voltage	V_{CRS}		1.3		2.0	V
Differential input sensitivity	V_{DI}	• |(UHAD+) – (UHAD–)| • |(UHBD+) – (UHBD–)|	0.2			V
Differential input common mode range	V_{CM}		0.8		2.5	V
High level input	$V_{IH(USB)}$		2.0		3.6	V
Low level input	$V_{IL(USB)}$		0.0		0.8	V
Rise time (full-speed)	t_{FR}	R_S=33Ω, C_L=50pF	4		20	ns
Fall time (full-speed)	t_{FF}	R_S=33Ω, C_L=50pF	4		20	ns
Rise time (low-speed)	t_{LR}	R_S=33Ω, C_L=200 to 600pF	75		300	ns
Fall time (low-speed)	t_{LF}	R_S=33Ω, C_L=200 to 600pF	75		300	ns

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erase operation	3.0 to 5.5		20	30	ms
	tFW(2)		• Write operation			40	60	μs

Main System Clock Oscillation

The characteristics of a sample main system clock oscillator circuit shown in Table 1 are measured using a Our specification oscillation characteristics evaluation board and external components with circuit constant values with which the resonator vendor confirmed normal and stable oscillation.
Table 1 shows the characteristics of a oscillator circuit when USB host function is not used. If USB host function is to be used, it is absolutely recommended to use a resonator that satisfies the precision and stability according to the USB standards (±500ppm)

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0GH5L**-R0	(33)	(33)	470	3.0 to 5.5	0.1	0.5	C1 and C2 integrated SMD type

The oscillation stabilization time is required for the oscillator to get stabilized in the following cases (see Figure 4):

- Until oscillation is stabilized after V_{DD} goes above the operating voltage lower limit
- Until oscillation is stabilized after the instruction for starting the main clock oscillator circuit is executed
- Until oscillation is stabilized after HOLD mode is released.
- Until oscillation is stabilized after X'tal HOLD mode is released with CFSTOP (OCR register, bit 0) set to 0 and oscillation is started.

Subsystem Clock Oscillation

Table 2 shows the characteristics of a sample subsystem clock oscillator circuit that are measured using a Our specification oscillation characteristics evaluation board and external components with circuit constant values with which the resonator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Resonator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	680k	2.7 to 5.5	1.1	3.0	Applicable CL value=12.5pF SMD type

The oscillation stabilization time is required for the oscillator to get stabilized in the following cases (see Figure 4):

- Until oscillation is stabilized after the instruction for starting the subclock oscillator circuit is executed
- Until oscillation is stabilized after HOLD mode is released with EXTOSC (OCR register, bit 6) set to 1 and oscillation is started.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

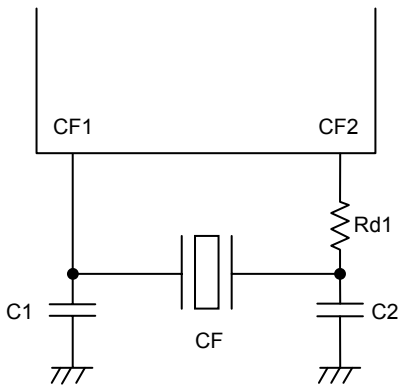


Figure 1 CF Oscillator Circuit

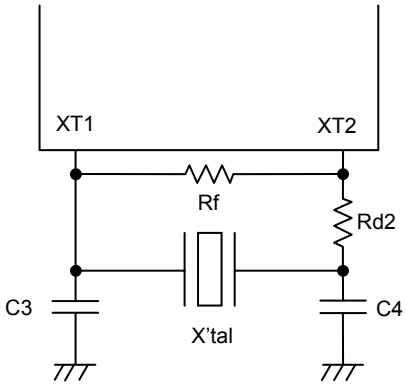


Figure 2 Crystal Oscillator Circuit

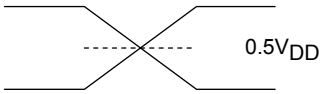
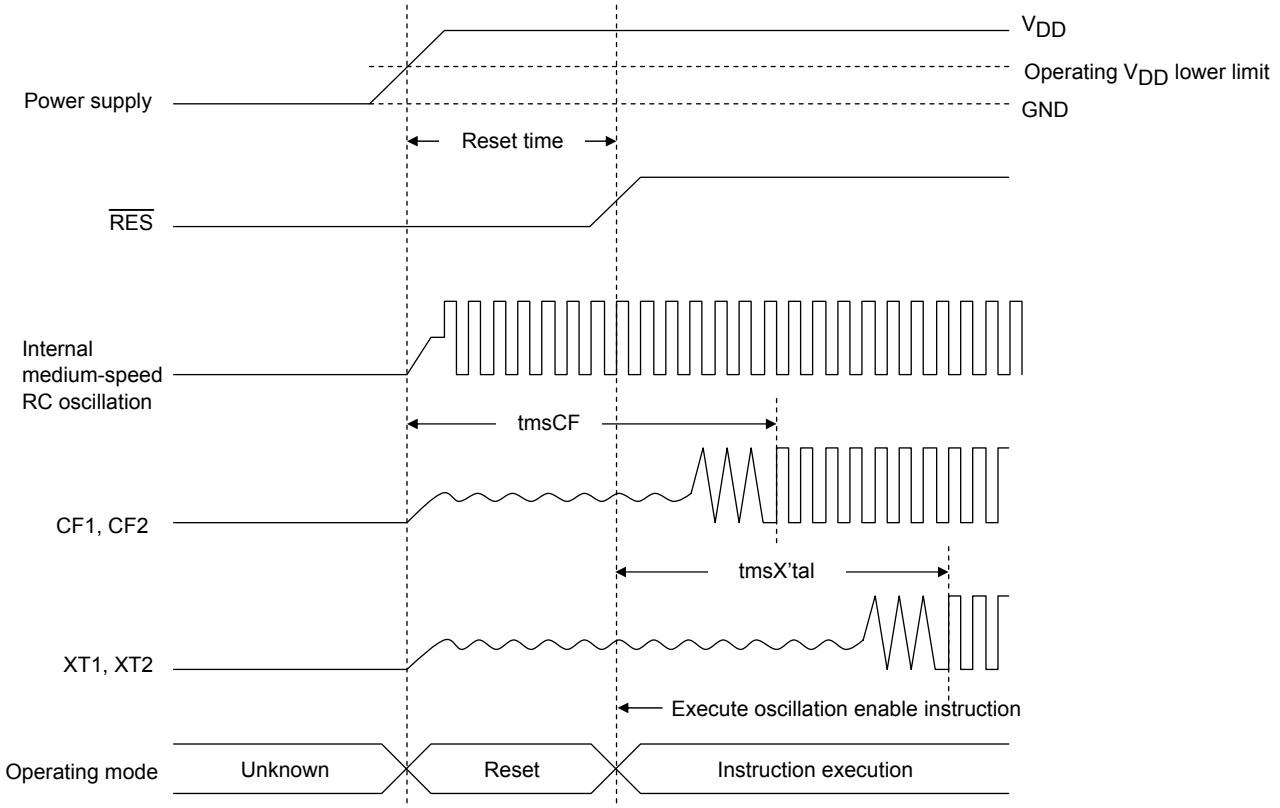
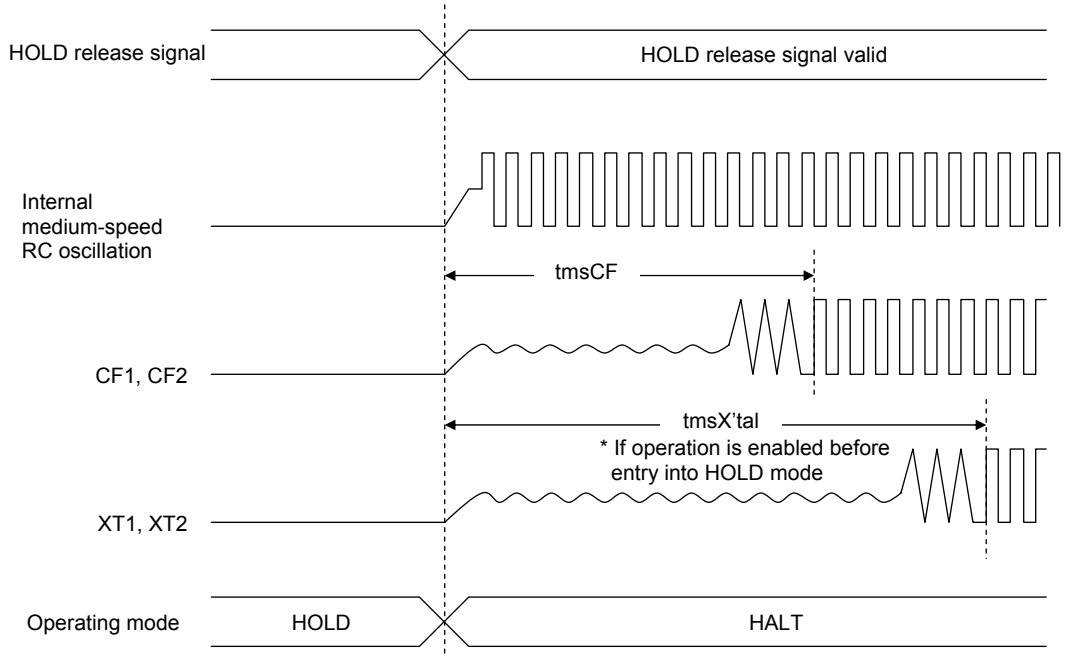


Figure 3 AC Timing Measurement Point

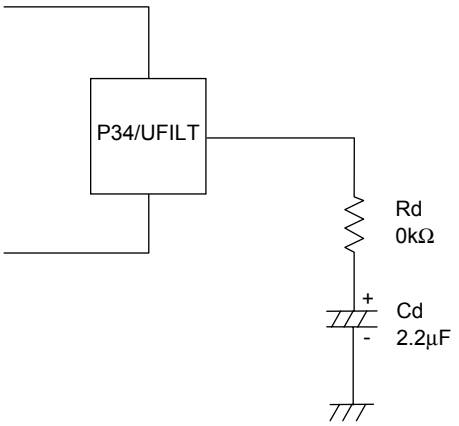


Reset Time and Oscillation Stabilization Time



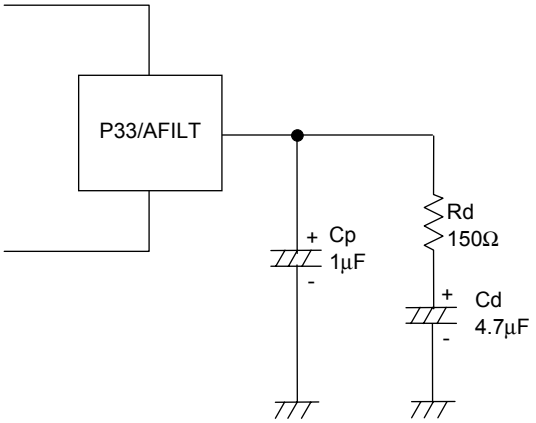
HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



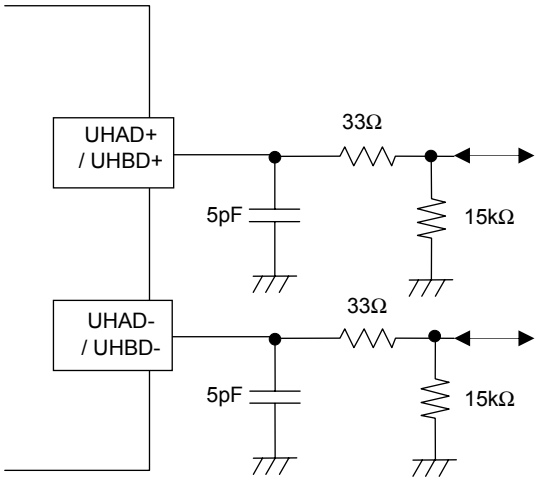
When using the internal PLL circuit to generate the 48MHz clock for USB, it is necessary to connect a filter circuit as shown in the left figure to the P34/UFILT pin.
After PLL is set, stabilization time of 20ms or longer must be secured.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit



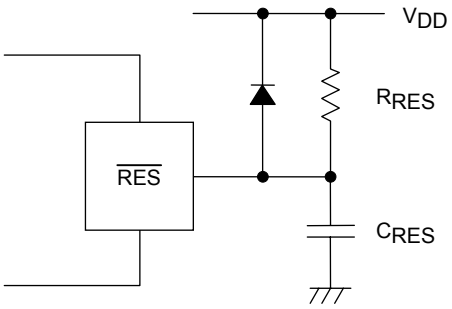
To generate the master clock for the audio interface using the internal PLL circuit, it is necessary to connect a filter circuit as shown in the left figure to the P33 pin.

Figure 6 External Filter Circuit for Audio Interface (Used with Internal PLL Circuit)



It is necessary to adjust the circuit constant of the USB port peripheral circuit for each mounting board.

Figure 7 USB Port Peripheral Circuit



Note:
The external circuit differs depending on which of the power-on reset and low-voltage reset functions is to be used. Refer to the section on the reset functions in the user's manual.

Figure 8 Sample Reset Circuit

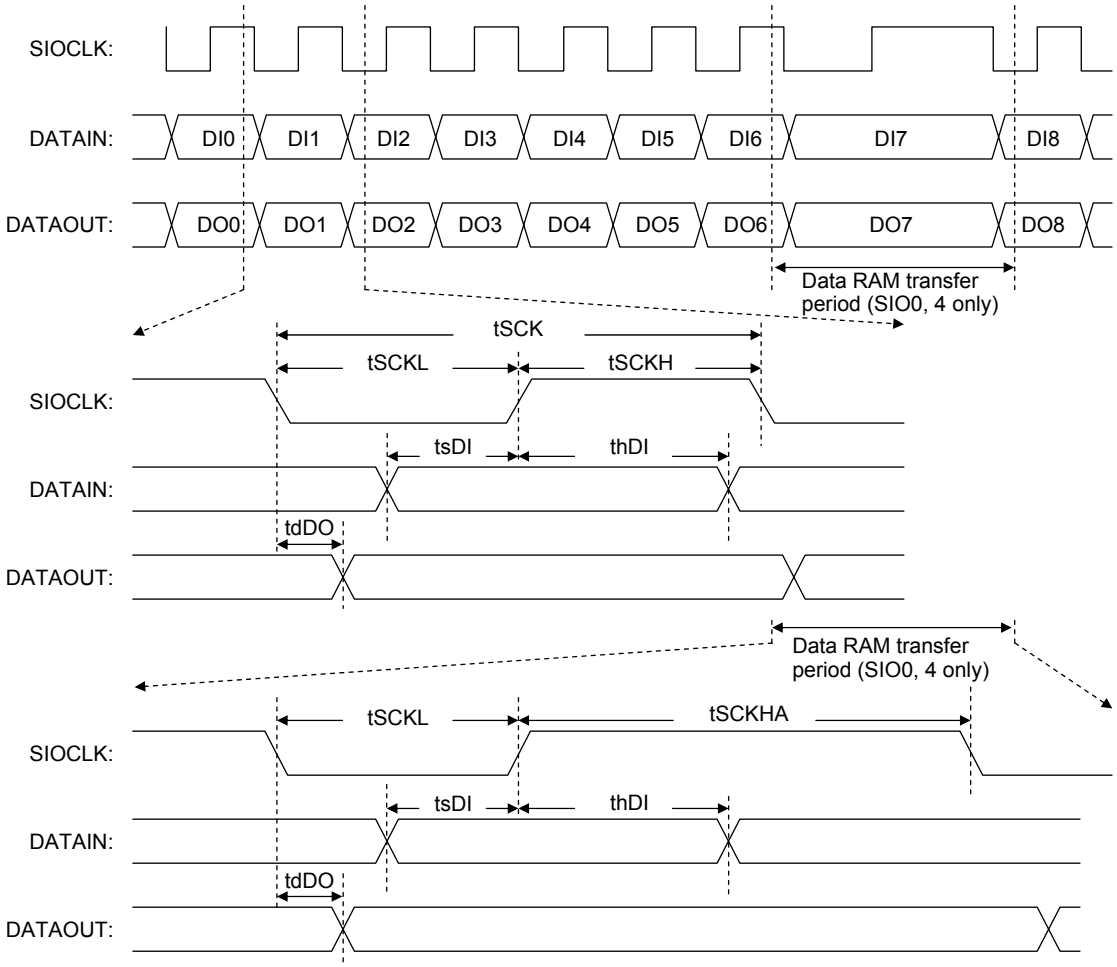


Figure 9 Serial I/O Waveform

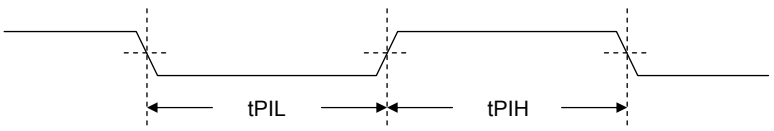
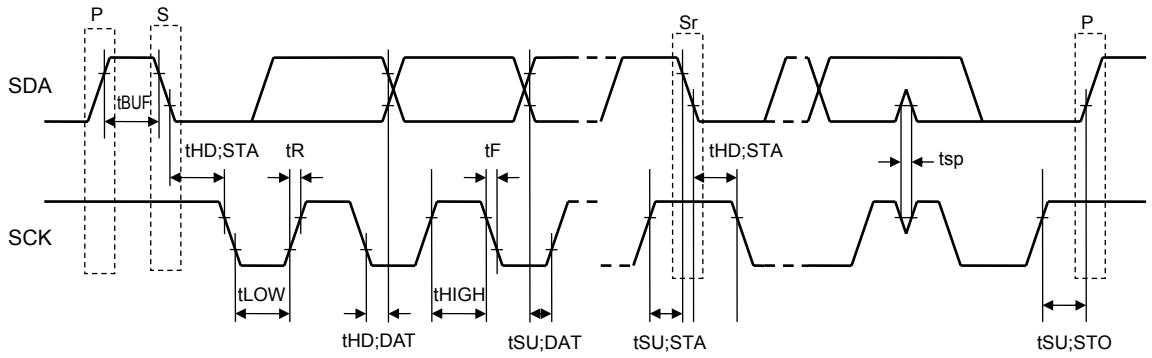


Figure 10 Pulse Input Timing Waveform



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 11 I^2C Timing

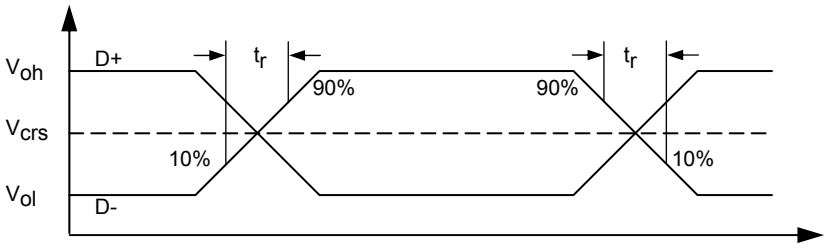


Figure 12 USB Data Signal Timing and Voltage Levels

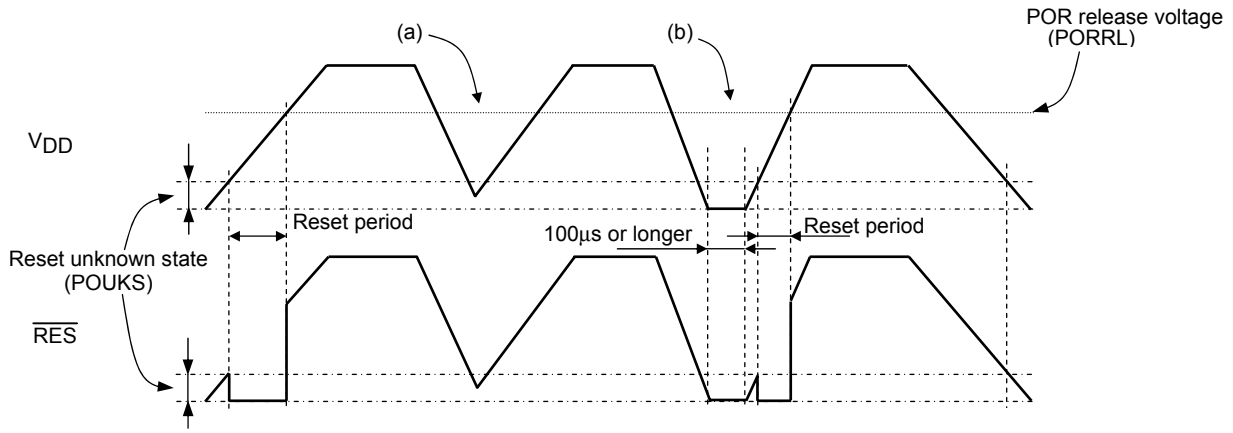


Figure 13 Sample Waveforms for POR-only (LVD deselected) Operation (Reset pin: Pull-up resistor P_{RES} only)

- The POR function generates a reset only when the power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again if the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function as explained below or implement an external reset circuit.
- A reset is generated only when power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

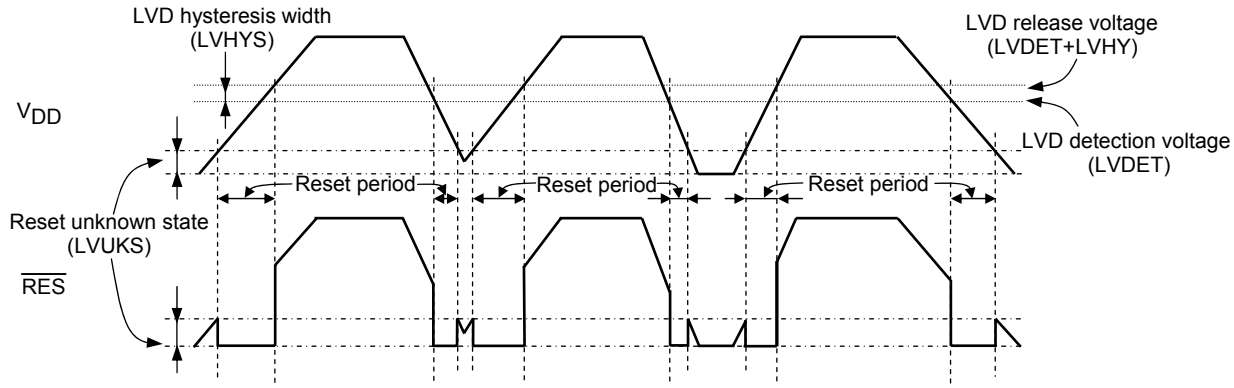


Figure 14 Sample Waveforms for POR+LVD Operation (Reset pin: Pull-up Resistor P_{RES} Only)

- A reset is generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent repetitions of reset release and entry cycles near the detection level.

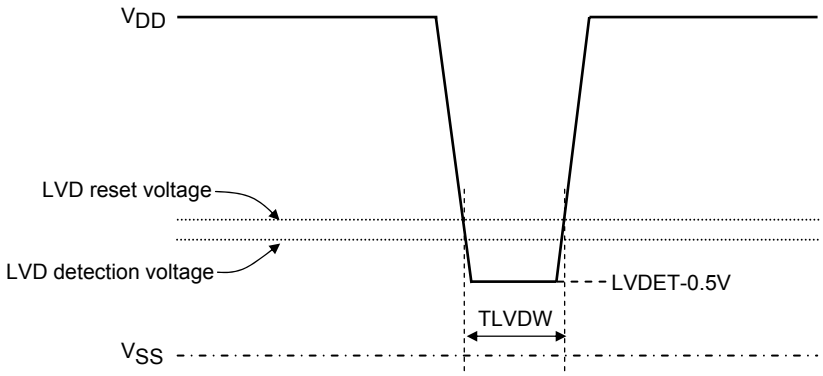


Figure 15 Minimum Low Voltage Detection Width (Sample Temporary Power Interruption/Fluctuation Waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F1K64AUWA-2H	SQFP48(7X7) (Pb-Free / Halogen Free)	250 / Tray Foam