Contents L6395

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L6395 Block diagram

# 1 Block diagram

BOOTSTRAP DRIVER FLOATING STRUCTURE 8 BOOT

UV DETECTION PRIVER FLOATING STRUCTURE 8 BOOT

LEVEL SHIFTER R PRIVER 7 HVG

GND 4 SAM16532V1

Figure 1. Block diagram

Pin connection L6395

## 2 Pin connection

Figure 2. Pin connection

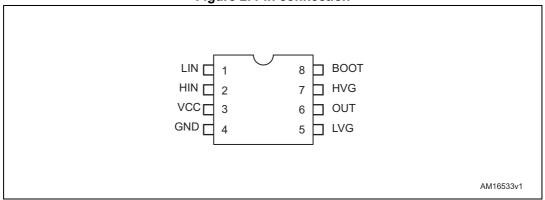


Table 1. Pin description

Pin	Pin name	Type Function	
1	LIN	I	Low-side driver logic input (active high)
2	HIN	I	High-side driver logic input (active high)
3	VCC	Р	Lower section supply voltage
4	GND	Р	Ground
5	LVG <sup>(1)</sup>	0	Low-side driver output
6	OUT	Р	High-side (floating) common voltage
7	HVG <sup>(1)</sup>	0	High-side driver output
8	воот	Р	Bootstrapped supply voltage

The circuit guarantees less than 1 V on the LVG and HVG pins (at I<sub>sink</sub> = 10 mA), with V<sub>CC</sub> > 3 V. In this manner, the "bleeder", resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low, is omitted.

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L6395 Truth table

# 3 Truth table

Table 2. Truth table

Inj	out	Out	put
LIN	HIN	LVG	HVG
L	L	L	L
L	Н	L	Н
Н	L	Н	L
Н	Н	Н	Н

Electrical data L6395

### 4 Electrical data

### 4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Va	Unit	
Symbol	Farameter	Min.	Max.	Onn
V <sub>CC</sub>	Supply voltage	- 0.3	21	V
V <sub>OUT</sub>	Output voltage	V <sub>BOOT</sub> - 21	V <sub>BOOT</sub> + 0.3	V
V <sub>BOOT</sub>	Bootstrap voltage	- 0.3	620	V
$V_{hvg}$	High-side gate output voltage	V <sub>OUT</sub> - 0.3	V <sub>BOOT</sub> + 0.3	V
V <sub>Ivg</sub>	Low-side gate output voltage	- 0.3	V <sub>CC</sub> + 0.3	V
V <sub>i</sub>	Logic input voltage	- 0.3	15	V
dV <sub>OUT</sub> /dt	Allowed output slew rate		50	V/ns
P <sub>tot</sub>	Total power dissipation (T <sub>A</sub> = 25 °C)		800	mW
TJ	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-50	150	°C
ESD	Human body model	:	2	kV

### 4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-8	Unit
R <sub>th(JA)</sub>	Thermal resistance junction to ambient	150	°C/W

## 4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Va	Unit	
Symbol	FIII	raiailletei	rest condition	Min.	Max.	Oille
V <sub>CC</sub>	3	Supply voltage		10	20	V
V <sub>BO</sub> <sup>(1)</sup>	8 - 6	Floating supply voltage		9.4	20	V
V <sub>OUT</sub>	6	Output voltage <sup>(1)</sup>		-11 <sup>(2)</sup>	580	V
f <sub>SW</sub>		Switching frequency	HVG, LVG load C <sub>L</sub> = 1 nF		800	kHz
T <sub>J</sub>		Junction temperature		-40	125	°C

<sup>1.</sup>  $V_{BO} = V_{BOOT} - V_{OUT}$ 

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<sup>2.</sup> LVG off.  $V_{CC}$  = 10 V. Logic is operational if  $V_{BOOT}$  > 5 V.

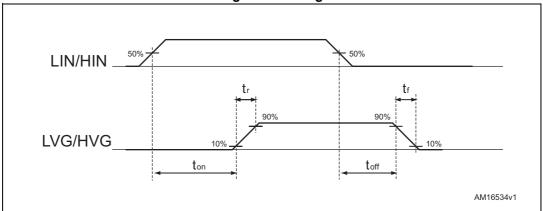
## 5 Electrical characteristics

## 5.1 AC operation

Table 6. AC operation electrical characteristics ( $V_{CC}$  = 15 V;  $T_j$  = +25 °C)

Symbol	Pin	Parameter	Test condition	Value			Unit
Symbol	FIII	Farameter	rest condition	Min.	Тур.	Max.	Oilit
t <sub>on</sub>	1,2 vs. 5, 7	High/low-side driver turn-on propagation delay	$V_{OUT} = 0 V$ $V_{BOOT} = V_{CC}$ $C_L = 1 nF$ $V_{IN} = 0 \text{ to } 3.3 V$ See Figure 3	50	125	200	ns
t <sub>off</sub>	1,2 vs. 5, 7	High/low-side driver turn-off propagation delay	$V_{OUT} = 0 V$ $V_{BOOT} = V_{CC}$ $C_L = 1 nF$ $V_{IN} = 3.3 V to 0$ See Figure 3	50	125	200	ns
t <sub>r</sub>	5, 7	Rise time	C <sub>L</sub> = 1 nF		75	120	ns
t <sub>f</sub>	5, 7	Fall time	C <sub>L</sub> = 1 nF		35	70	ns

Figure 3. Timing



**Electrical characteristics** L6395

#### 5.2 **DC** operation

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 $(V_{cc} = 15 \text{ V}; T_j = +25 ^{\circ}\text{C})$ 

Table 7. DC operation electrical characteristics

Crunch al	D!	Para series	Took oan diking	Value			
Symbol	Pin	Parameter	Test condition	Min.	Тур.	Max.	Unit
Low suppl	y volt	age section			•	•	
V <sub>CC_hys</sub>	3	V <sub>CC</sub> UV hysteresis		0.6	0.7	0.8	V
V <sub>CC_thON</sub>	3	V <sub>CC</sub> UV turn ON threshold		9	9.5	10	V
V <sub>CC_thOFF</sub>	3	V <sub>CC</sub> UV turn OFF threshold		8.3	8.8	9.3	V
I <sub>qccu</sub>	3	Undervoltage quiescent supply current	V <sub>CC</sub> = 7 V LIN = 5V; HIN = GND;	40	90	150	μА
I <sub>qcc</sub>	3	Quiescent current	V <sub>CC</sub> = 15 V LIN = 5 V; HIN = GND;	100	220	350	μА
Bootstrap	oed s	upply voltage section <sup>(1)</sup>			•	•	
V <sub>BO_hys</sub>	8	V <sub>BO</sub> UV hysteresis		0.5	0.6	0.7	V
V <sub>BO_thON</sub>	8	V <sub>BO</sub> UV turn ON threshold		7.9	8.6	9.4	V
V <sub>BO_thOFF</sub>	8	V <sub>BO</sub> UV turn OFF threshold		7.3	8	8.7	V
I <sub>QBOU</sub>	8	Undervoltage V <sub>BO</sub> quiescent current	V <sub>BO</sub> = 7 V LIN = GND; HIN = 5 V	10	30	60	μА
I <sub>QBO</sub>	8	V <sub>BO</sub> quiescent current	V <sub>BO</sub> = 15 V LIN = GND; HIN = 5 V;		190	220	μА
I <sub>LK</sub>	8	High voltage leakage current	V <sub>hvg</sub> = V <sub>OUT</sub> = V <sub>BOOT</sub> = 600 V			10	μА
R <sub>DS(on)</sub>		Bootstrap driver on- resistance <sup>(2)</sup>	LVG on		120		Ω
Driving bu							
I <sub>so</sub>	5, 7	High/low-side source short-circuit current	$V_{IN} = V_{ih} (t_p < 10 \ \mu s)$	200	290		mA
I <sub>si</sub>	5, 7	High/low-side sink short- circuit current	$V_{IN} = V_{il} (t_p < 10 \ \mu s)$	250	430		mA
Logic inpu	Logic inputs						
V <sub>il</sub>	1, 2	Low level logic threshold voltage		0.8		1.1	V
V <sub>ih</sub>	1, 2	High level logic threshold voltage		1.9		2.25	V

L6395 Electrical characteristics

Table 7. DC operation electrical characteristics (continued)

Counch of	Symbol Pin Parameter		Took oon diki on	Value			Unit
Symbol	Pin	Parameter	Test condition	Min.	Тур.	Max.	Unit
I <sub>HINh</sub>	2	HIN logic "1" input bias current	HIN = 15 V	10	40	100	μА
I <sub>HINI</sub>	2	HIN logic "0" input bias current	HIN = 0 V			1	μА
I <sub>LINh</sub>	1	LIN logic "1" input bias current	LIN = 15 V	10	40	100	μА
I <sub>LINI</sub>	1	LIN logic "0" input bias current	LIN = 0 V			1	μА

<sup>1.</sup>  $V_{BO} = V_{BOOT} - V_{OUT}$ 



<sup>2.</sup>  $R_{DS(on)}$  is tested in the following way:  $R_{DS(on)} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})]$  where  $I_1$  is the pin 8 current when  $V_{BOOT} = V_{BOOT1}$ ,  $I_2$  when  $V_{BOOT} = V_{BOOT2}$ .

# 6 Typical application diagram

Figure 4. Application diagram

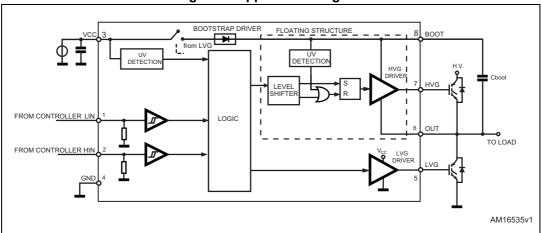
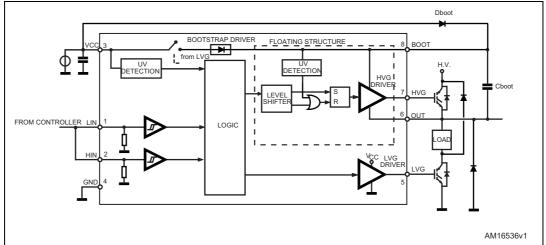


Figure 5. Application diagram for asymmetrical load driving



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L6395 Bootstrap driver

### 7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished using a high voltage fast recovery diode (*Figure 6*). In the L6395 device a patented integrated structure replaces the external diode. It is implemented using a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 7*. An internal charge pump provides the DMOS driving voltage.

### **C**BOOT selection and charging

To select the proper  $C_{BOOT}$  value the external MOS can be seen as an equivalent capacitor. This capacitor  $C_{EXT}$  is related to the MOS total gate charge:

#### **Equation 1**

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors  $C_{\text{EXT}}$  and  $C_{\text{BOOT}}$  is proportional to the cyclical voltage loss.

It must be:

#### **Equation 2**

$$C_{BOOT} \gg C_{EXT}$$

E.g.: if  $Q_{gate}$  is 30 nC and  $V_{gate}$  is 10 V,  $C_{EXT}$  is 3 nF. With  $C_{BOOT}$  = 100 nF the drop is 300 mV.

If HVG needs to be supplied for an extended period, the  $C_{BOOT}$  selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady state consumption is lower than 220  $\mu$ A, so if HVG T<sub>ON</sub> is 5 ms, C<sub>BOOT</sub> must supply 1.1  $\mu$ C to C<sub>EXT</sub>. This charge on a 1  $\mu$ F capacitor means a voltage drop of 1.1 V.

The internal bootstrap driver offers some important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if  $V_{OUT}$  is close to GND (or lower) and, at the same time, the LVG is on. The charging time ( $T_{charge}$ ) of the  $C_{BOOT}$  is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS  $R_{DS(on)}$  (typical value: 120  $\Omega$ ). At low switching frequency, this drop can be neglected but, operating at high switching frequency, it should be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

#### **Equation 3**

$$V_{drop} = I_{charge} \cdot R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} \cdot R_{DS(on)}$$

where  $Q_{gate}$  is the gate charge of the external power MOSFET,  $R_{DS(on)}$  is the on-resistance of the bootstrap DMOS and  $T_{charge}$  is the charging time of the bootstrap capacitor.



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Bootstrap driver L6395

For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the  $T_{charge}$  is 5  $\mu s$ .

#### **Equation 4**

$$V_{drop} = \frac{30_{nc}}{5_{\mu s}} \cdot 120\Omega \cong 0.7V$$

 $V_{drop}$  must be taken into account when the voltage drop on  $C_{BOOT}$  is calculated: whether this drop is too high, or the circuit topology does not allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode

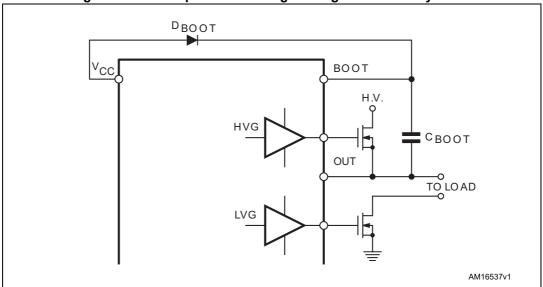
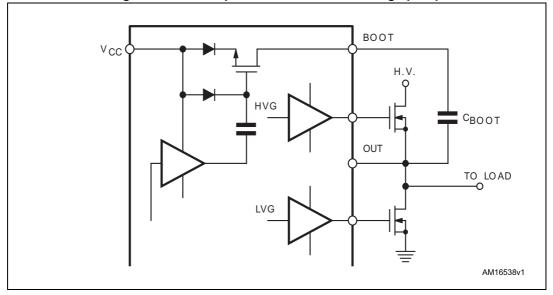


Figure 7. Bootstrap driver with internal charge pump



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L6395 Package information

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: <a href="www.st.com">www.st.com</a>. ECOPACK is an ST trademark.

### **SO-8** package information

SEATING PLANE

B
SECTION B-B

SECTION B-B

B
SECTION B-B

OU16023 G-FU

OU16023 G-FU

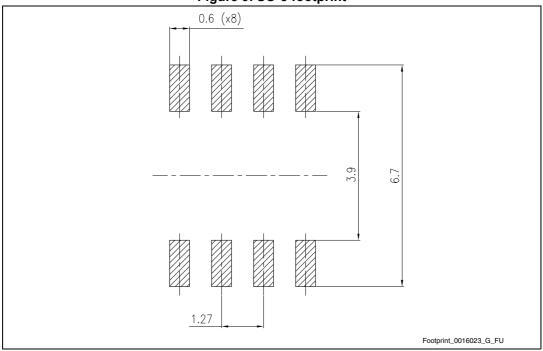
Figure 8. SO-8 package outline

Package information L6395

Table 8. SO-8 package mechanical data

Complete		Dimensions (mm)	
Symbol	Min.	Тур.	Max.
А			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
С	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
е		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 9. SO-8 footprint



L6395 Order codes

## 9 Order codes

Table 9. Order codes

Order codes	Package	Packaging
L6395D	SO-8	Tube
L6395DTR	SO-8	Tape and reel

# 10 Revision history

**Table 10. Document revision history** 

Date	Revision	Changes
20-Mar-2013	1	Initial release.
11-Sep-2015	2	Updated <i>Table 4 on page 6</i> (added ESD parameter and value). Updated note 2. below <i>Table 7 on page 8</i> (replaced V <sub>CBOOTx</sub> by V <sub>BOOTx</sub> ). Updated <i>Section 8 on page 13</i> . Moved <i>Table 9 on page 15</i> (moved from page 1 to page 15, updated/added titles). Minor modifications throughout document.

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