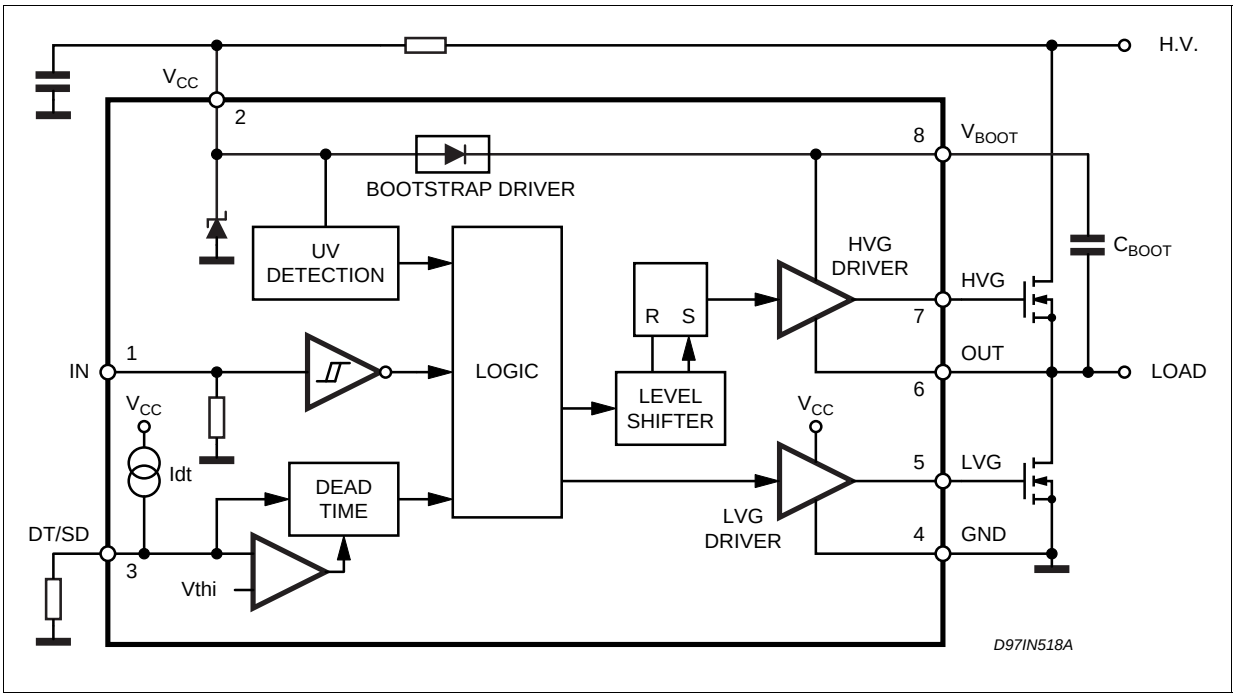
Contents

1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage	-3 to V_{BOOT} -18	V
V_{CC}	Supply voltage(1)	- 0.3 to 14.6	V
I_s	Supply current(1)	25	mA
V_{BOOT}	Floating supply voltage	-1 to 618	V
V_{hvg}	High-side gate output voltage	-1 to V_{BOOT}	V
V_{lvg}	Low-side gate output voltage	-0.3 to V_{CC} +0.3	V
V_i	Logic input voltage	-0.3 to V_{CC} +0.3	V
V_{SD}	Shutdown/deadtime voltage	-0.3 to V_{CC} +0.3	V
dV_{out}/dt	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_j = 85 °C)	750	mW
T_J	Junction temperature	150	°C
T_s	Storage temperature	-50 to 150	°C
ESD	Human body model	2	kV

1. The device has an internal clamping Zener between GND and the V_{CC} pin, it must not be supplied by a low impedance voltage source.

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	100	°C/W

2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OUT}	6	Output voltage		(1)		580	V
V_{BS}(2)	8	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF			400	kHz
V_{CC}	2	Supply voltage				V_{clamp}	V
T_j		Junction temperature		-45		125	°C

1. If the condition V_{BOOT} - V_{OUT} < 18 V is guaranteed, V_{OUT} can range from -3 to 580 V.
2. V_{BS} = V_{BOOT} - V_{OUT}.

3 Pin connection

Figure 2. Pin connection (top view)

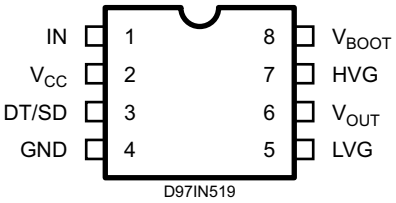


Table 4. Pin description

No.	Pin	Type	Function
1	IN	I	Logic input: it is in phase with HVG and in opposition of phase with LVG. It is compatible to V_{CC} voltage. ($V_{il\ Max}$ = 1.5 V, $V_{ih\ Min}$ = 3.6 V).
2	V_{CC}	P	Supply input voltage: there is an internal clamp [typ. 15.6 V].
3	DT/SD	I	High impedance pin with two functionalities. When pulled lower than V_{dt} (typ. 0.5 V), the device is shut down. A voltage higher than V_{dt} sets the deadtime between the high-side gate driver and low-side gate driver. The deadtime value can be set forcing a certain voltage level on the pin or connecting a resistor between the pin 3 and ground. Care must be taken to avoid below threshold spikes on the pin 3 that can cause undesired shutdown of the IC. For this reason the connection of the components between the pin 3 and ground has to be as short as possible. This pin can not be left floating for the same reason. The pin has not be pulled through a low impedance to V_{CC}, because of the drop on the current source that feeds R_{dt}. The operative range is: V_{dt} … 270 KΩ· I_{dt}, that allows a dt range of 0.4 - 3.1 µs.
4	GND	P	Ground
5	LVG	O	Low-side driver output: the output stage can deliver 400 mA source and 650 mA sink (typ. values). The circuit guarantees 0.3 V max. on the pin (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
6	V_{OUT}	P	High-side driver floating reference: layout care has to be taken to avoid below ground spikes on this pin.
7	HVG	O	High-side driver output: the output stage can deliver 400 mA source and 650 mA sink (typ. values). The circuit guarantees 0.3 V max. between this pin and V_{OUT} (at I_{sink} = 10 mA) with V_{CC} > 3 V and lower than the turn-on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
8	V_{BOOT}	P	Bootstrap supply voltage: it is the high-side driver floating supply. The bootstrap capacitor connected between this pin and the pin 6 can be fed by an internal structure named “bootstrap driver” (a patented structure). This structure can replace the external bootstrap diode.

4 Electrical characteristics

4.1 AC operation

Table 5. AC operation electrical characteristics (V_{CC} = 14.4 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 5, 7	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V R_{dt}= 47 kΩ		200+ dt		ns
t_{onsd}	3 vs. 5, 7	Shutdown input propagation delay			220	280	ns
t_{off}	1 vs. 5, 7	High/low-side driver turn-off propagation delay	V_{OUT} = 0 V R_{dt} = 47 kΩ		250	300	ns
			V_{OUT} = 0 V R_{dt} = 146 kΩ		200	250	ns
			V_{OUT} = 0 V R_{dt} = 270 kΩ		170	200	ns
t_r	5, 7	Rise time	C_L = 1000 pF		50		ns
t_f	5, 7	Fall time	C_L = 1000 pF		30		ns

4.2 DC operation

Table 6. DC operation electrical characteristics (V_{CC} = 14.4 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage section							
V_{clamp}	2	Supply voltage clamping	I_s = 5 mA	14.6	15.6	16.6	V
V_{CCth1}	2	V_{CC} UV turn-on threshold		11.5	12	12.5	V
V_{CCth2}	2	V_{CC} UV turn-off threshold		9.5	10	10.5	V
V_{CChys}		V_{CC} UV hysteresis			2		V
I_{QCCU}		Undervoltage quiescent supply current	$V_{CC} \leq$ 11 V		150		µA
I_{QCC}		Quiescent current	V_{IN} = 0		380	500	µA
Bootstrapped supply voltage section							
V_{BOOT}	8	Bootstrap supply voltage				17	V
I_{QBS}		Quiescent current	IN = HIGH			100	µA
I_{LK}		High voltage leakage current	V_{hvg} = V_{OUT} = V_{BOOT} = 600 V			10	µA
R_{dson}		Bootstrap driver on-resistance(1)	$V_{CC} \geq$ 12.5 V; IN = LOW		125		Ω
High/low-side driver							
I_{so}	5, 7	Source short-circuit current	V_{IN} = V_{ih} (t_p < 10 µs)	300	400		mA
I_{si}		Sink short-circuit current	V_{IN} = V_{il} (t_p < 10 µs)	500	650		mA

Table 6. DC operation electrical characteristics (continued) (V_{CC} = 14.4 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs							
V_{il}	1, 3	Low level logic threshold voltage				1.5	V
V_{ih}		High level logic threshold voltage		3.6			V
I_{ih}		High level logic input current	V_{IN} = 15 V		50	70	µA
I_{il}		Low level logic input current	V_{IN} = 0 V			1	µA
I_{ref}	3	Deadtime setting current			28		µA
dt	3 vs. 5, 7	Deadtime setting range(2)	R_{dt} = 47 kΩ R_{dt} = 146 kΩ R_{dt} = 270 kΩ	0.4	0.5 1.5 2.7	 3.1	µs µs µs
V_{dt}	3	Shutdown threshold			0.5		V

1. $R_{DS(on)}$ is tested in the following way:

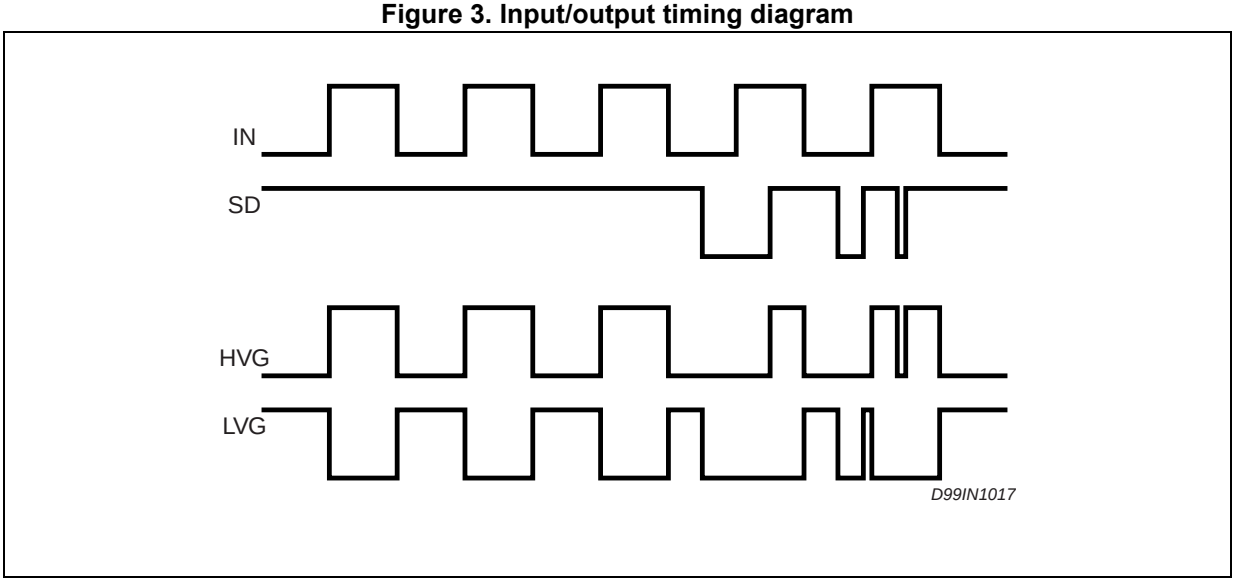
$$R_{DSON} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})}$$

Where I_1 is the pin 8 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

2. The pin 3 is a high impedance pin. Therefore dt can be set also forcing a certain voltage V_3 on this pin. The deadtime is the same obtained with an R_{dt} if it is: $R_{dt} \times I_{ref} = V_3$.

4.3 Timing diagram

Figure 3. Input/output timing diagram



5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4* a). In the L6384E device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 4* b. An internal charge pump (*Figure 4* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn-on.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOSFET can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOSFET total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

E.g.: HVG steady state consumption is lower than 100 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 0.5 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 0.5 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has a great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOSFET, R_{dson} is the on-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

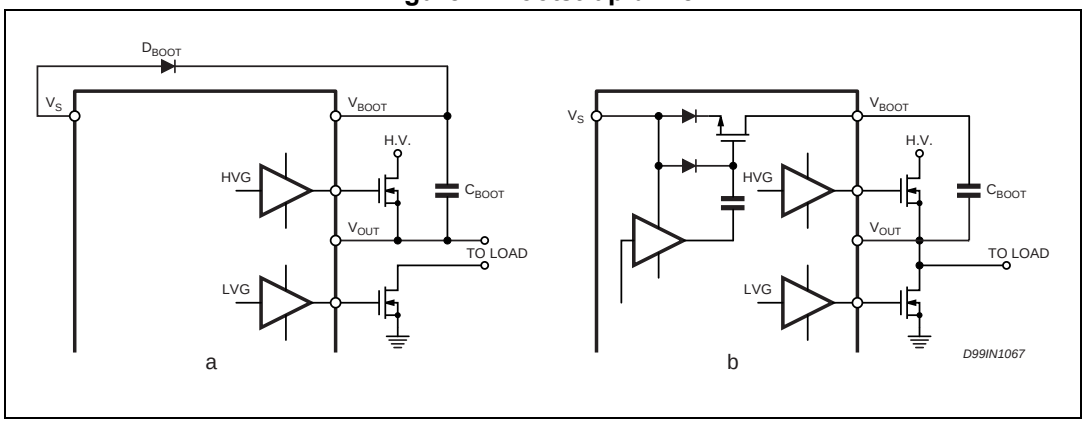
For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap driver



6 Typical characteristic

Figure 5. Typical rise and fall times vs. load capacitance

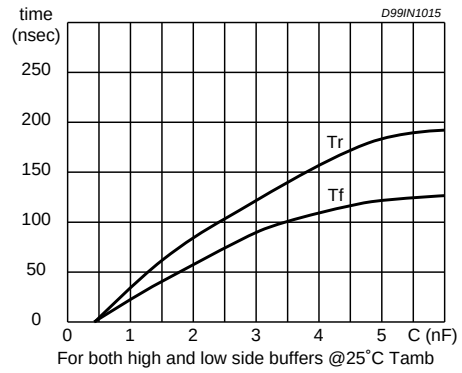


Figure 6. Quiescent current vs. supply voltage

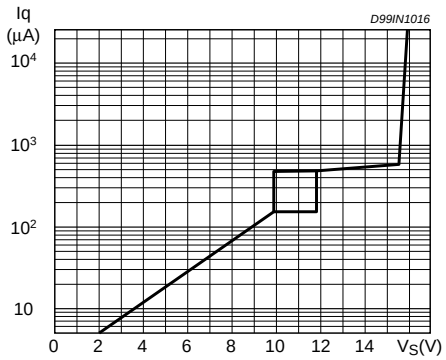


Figure 7. Deadtime vs. resistance

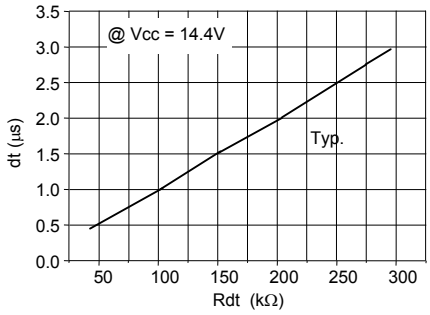


Figure 8. Driver propagation delay vs. temperature

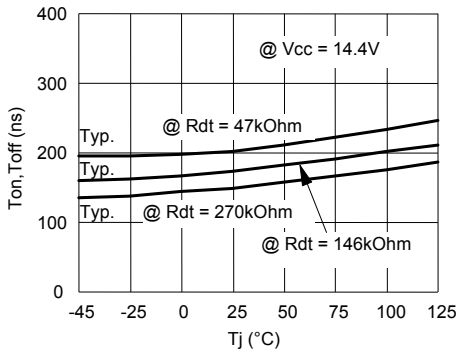


Figure 9. Deadtime vs. temperature

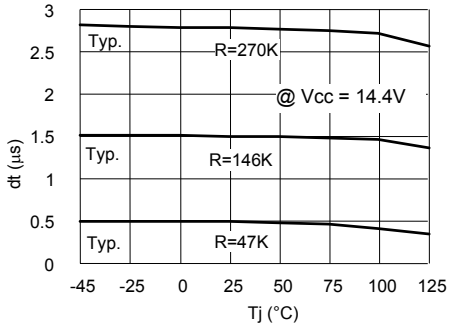


Figure 10. Shutdown threshold vs. temperature

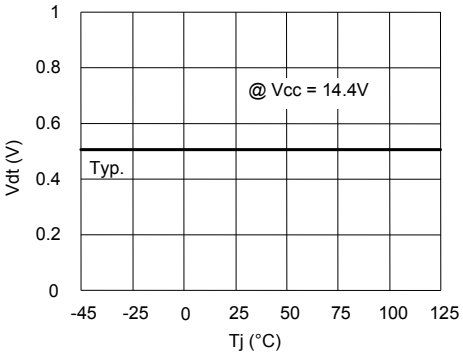


Figure 11. V_{CC} UV turn-on vs. temperature

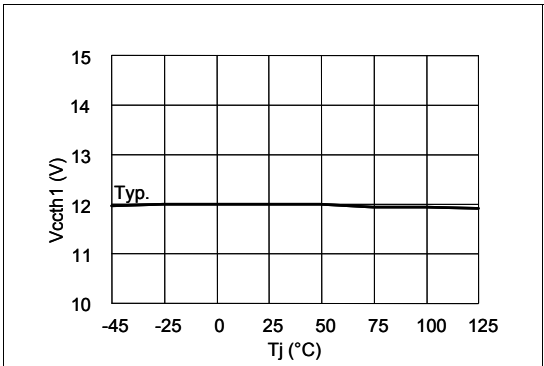


Figure 12. Output source current vs. temperature

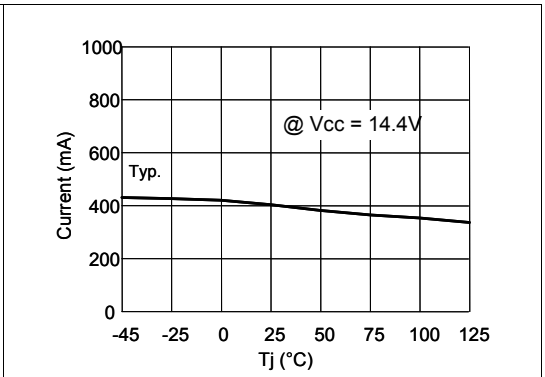


Figure 13. V_{CC} UV turn-off vs. temperature

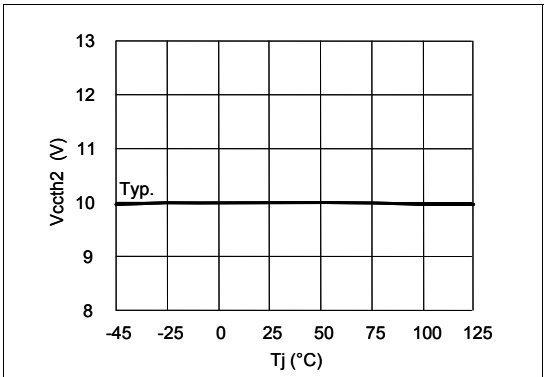
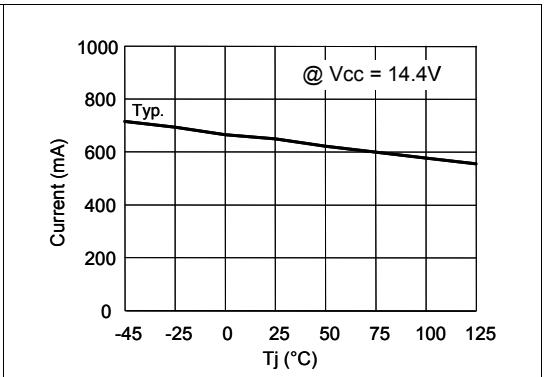


Figure 14. Output sink current vs. temperature



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 DIP-8 package information

Figure 15. DIP-8 package outline

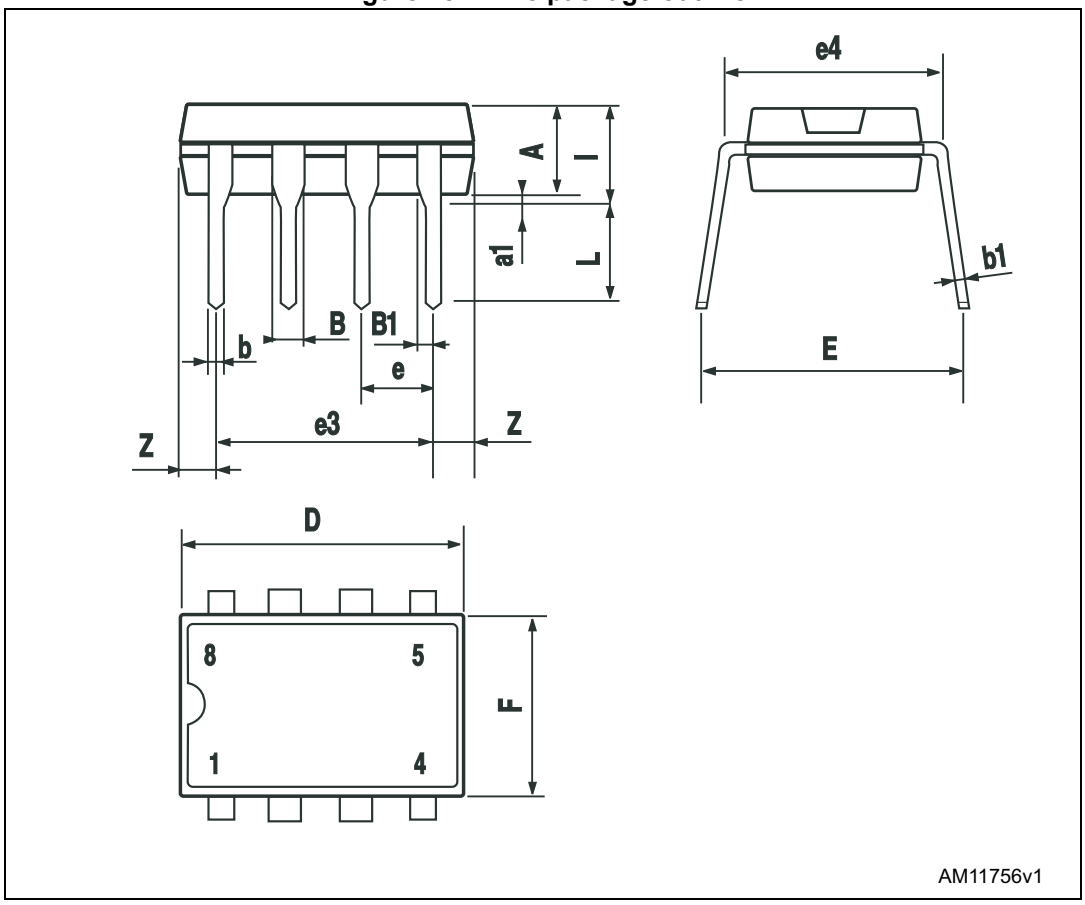


Table 7. DIP-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

7.2 SO-8 package information

Figure 16. SO-8 package outline

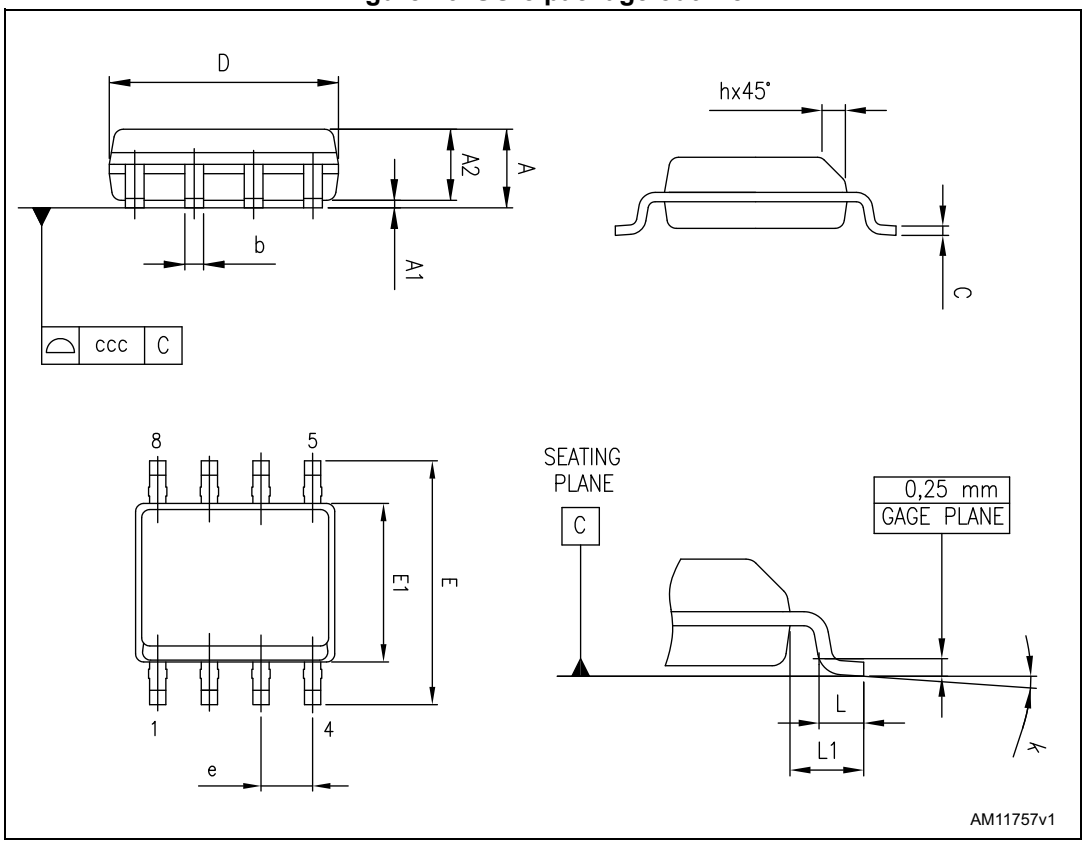


Table 8. SO-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D(1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

8 Order codes

Table 9. Order code

Order code	Package	Packaging
L6384E	DIP-8	Tube
L6384ED	SO-8	Tube
L6384ED013TR	SO-8	Tape and reel

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Oct-2007	1	First release
20-Jun-2014	2	Added *Section : Applications on page 1*. Updated *Section : Description on page 1* (replaced by new description). Updated *Table 1: Device summary on page 1* (moved from page 15 to page 1, updated title). Updated *Figure 1: Block diagram on page 3* (moved from page 1 to page 3, numbered and added title to *Section 1: Block diagram on page 3*). Updated *Section 2.1: Absolute maximum ratings on page 4* (removed note below *Table 2: Absolute maximum ratings*). Updated *Table 5: Pin description on page 5* (updated “Type” of several pins). Updated *Table 7 on page 6* (updated “Max.” value of I_{QBS} symbol). Updated *Section : C_{BOOT} selection and charging on page 8* (updated values of “E.g.: HVG”). Numbered *Equation 1 on page 8*, *Equation 2 on page 8* and *Equation 3 on page 9*. Updated *Section 7: Package information on page 12* [updated/added titles, updated ECOPACK text, reversed order of *Figure 15* and *Table 8*, *Figure 16* and *Table 9* (numbered tables), removed 3D package figures, minor modifications]. Minor modifications throughout document.
16-Sep-2015	3	Updated *Table 1 on page 4* (added ESD parameter and value, minor modifications). Updated note *1.* below *Table 6 on page 7* (replaced V_{CBOOTx} by V_{BOOTx}). Moved *Table 9 on page 17* (moved from page 1 to page 17, updated titles). Updated cross-references throughout document. Minor modifications throughout document.