Ordering Information

Part Number	Package Option	Packing
HV809K2-G	7-Lead TO-220	50/Tube
HV809LG-G	8-Lead SOIC	2500/Reel
HV809SG-G	8-Lead SOIC w/ heat slug	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
HV_{IN}, High voltage input	+210V
V_{DD}, Internal supply voltage	+15V
Operating temperature range	-25°C to +85°C
Storage temperature range	-55°C to +150°C
Power dissipation: 8-Lead SOIC 8-Lead SOIC w/ Heat Slug 7-Lead TO-220*	 500mW 1.5 Watts 15Watts

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

** With external heat sink mounted, refer to App Note AN-H36.*

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

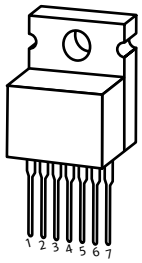
7-Lead TO-220

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

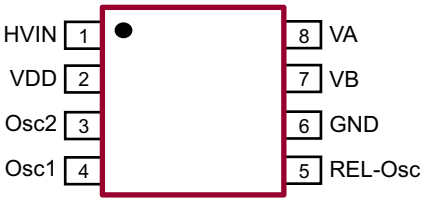
8-Lead SOIC

Pin Configuration

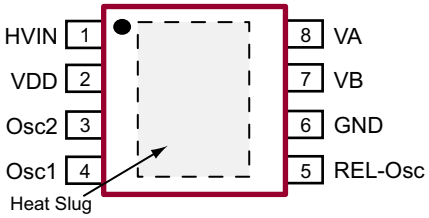


Pin 1: Osc1
Pin 2: VDD
Pin 3: REL-Osc
Pin 4: GND
Pin 5: VB
Pin 6: VA
Pin 7: HVIN
Tab: GND

7-Lead TO-220
(front view)



8-Lead SOIC
(top view)



8-Lead SOIC w/ Heat Slug
(top view)
(Heat slug is at ground potential)

Typical Thermal Resistance

Package	θ_{ja}
7-Lead TO-220	29°C/W
8-Lead SOIC	101°C/W
8-Lead SOIC w/ heat slug	84°C/W

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
HV_{IN}	High voltage input	50	-	200	V	---
C_L	Load capacitance	-	-	350	nF	R_{EL} = 1.0MΩ, HV_{IN} = 170V
		-	-	150	nF	R_{EL} = 390kΩ, HV_{IN} = 170V
T_A	Operating temperature	-25	-	85	°C	---

Electrical Characteristics

DC Characteristics *(Over recommended operating conditions unless otherwise specified - T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	High voltage supply current	-	-	70	mA	HV_{IN} = 170V, R_{EL} = 1.0MΩ, C_L = 350nF
		-	-	9.0	mA	HV_{IN} = 170V, R_{EL} = 1.0MΩ, C_L = 50nF
I_{INQ}	Quiescent supply current	-	-	400	µA	HV_{IN} = 170V, R_{EL} = 1.0MΩ, Osc1 = GND, No Load
		-	-	100	µA	HV_{IN} = 170V, R_{EL} = 1.0MΩ, Osc1 = V_{DD}, No Load
I_{SINK}	Osc2 sink current*	-	300	-	µA	V_{Osc2} = 1.0V
I_{SOURCE}	Osc2 source current*	-	100	-	µA	V_{Osc2} = V_{DD} -1.0V
I_{Osc1}	Osc1 logic input leakage current	-	±10	-	µA	V_{Osc1} = GND and V_{DD}
$V_{Osc1(hyst)}$	Osc1 hysteresis voltage	-	2.5	-	V	---
V_{A-B}	Min differential output voltage across lamp	-	-	400	V	HV_{IN} = 200V
V_{DD}	Internal supply voltage	8.0	10	12	V	No load on V_{DD}
$I_{DD\ (OUT)}$	Output V_{DD} current	4.0	-	-	mA	For HV809K2, ΔV_{DD} = 1.0V

** I_{SINK} and I_{SOURCE} are not valid for the TO-220 package.*

AC Characteristics *(Over recommended operating conditions unless otherwise specified - T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{EL}	V_{A-B} output drive frequency	320	400	480	Hz	R_{EL} = 1.0MΩ, Osc1 = GND, C_L = 350nF
		0.8	1.0	1.2	kHz	R_{EL} = 390kΩ, Osc1 = GND, C_L = 150nF
t_r	Output rise time	-	180	250	µs	C_L = 150nF, HV_{IN} = 170V
t_f	Output fall time	-	50	100	µs	C_L = 150nF, HV_{IN} = 170V

Function Table

Input	Outputs	
Osc1	VA	VB
GND	Enabled	Enabled
VDD	Disabled	Disabled

Figure 1. AC Off-Line EL Lamp

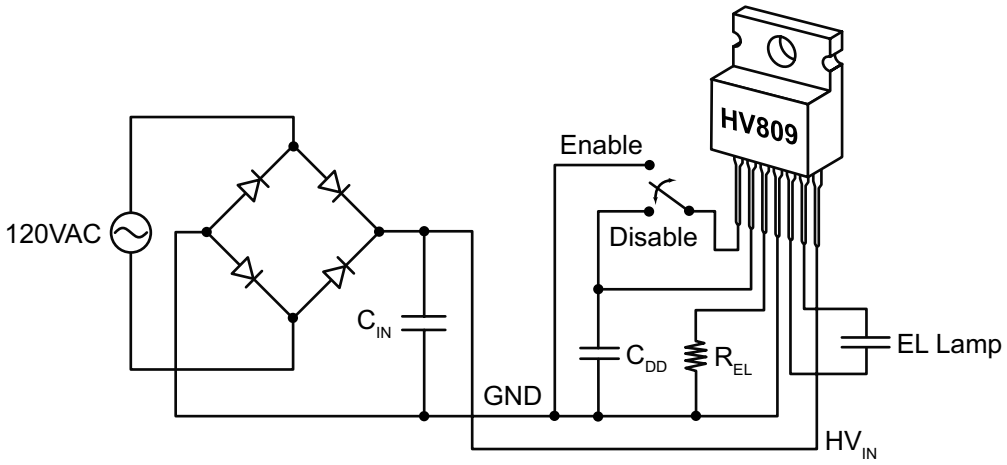


Figure 2. Pulsing EL Lamp

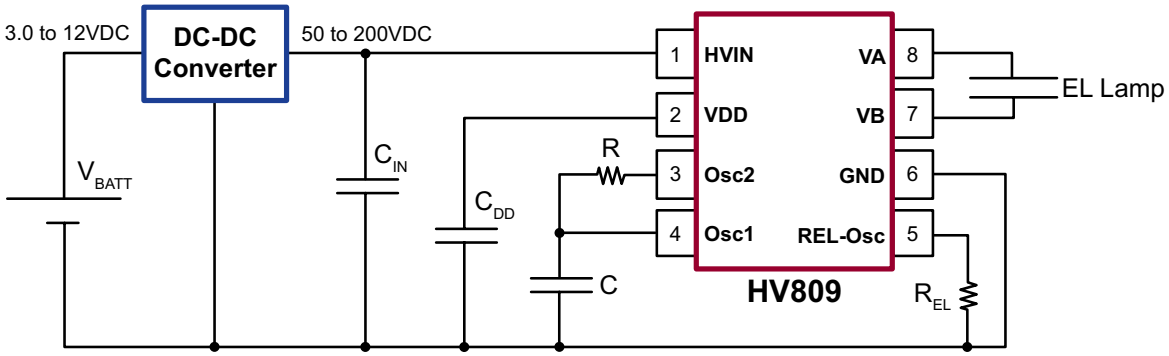
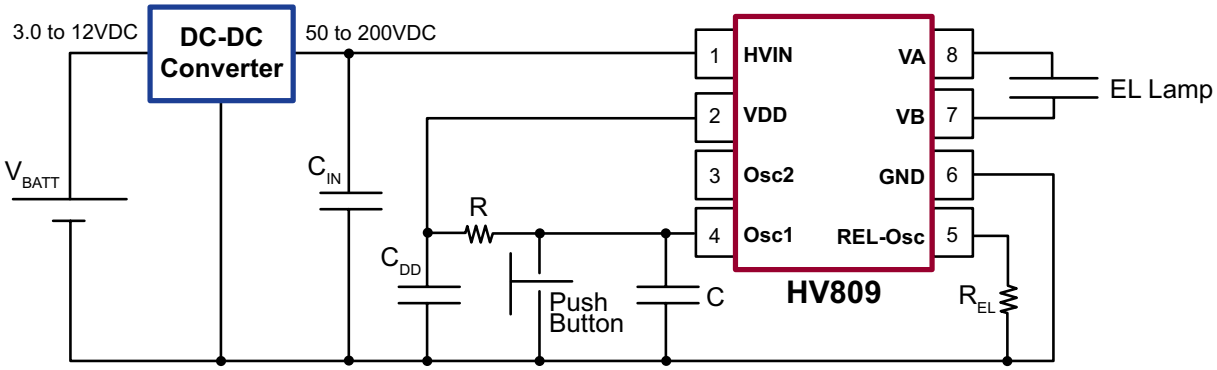
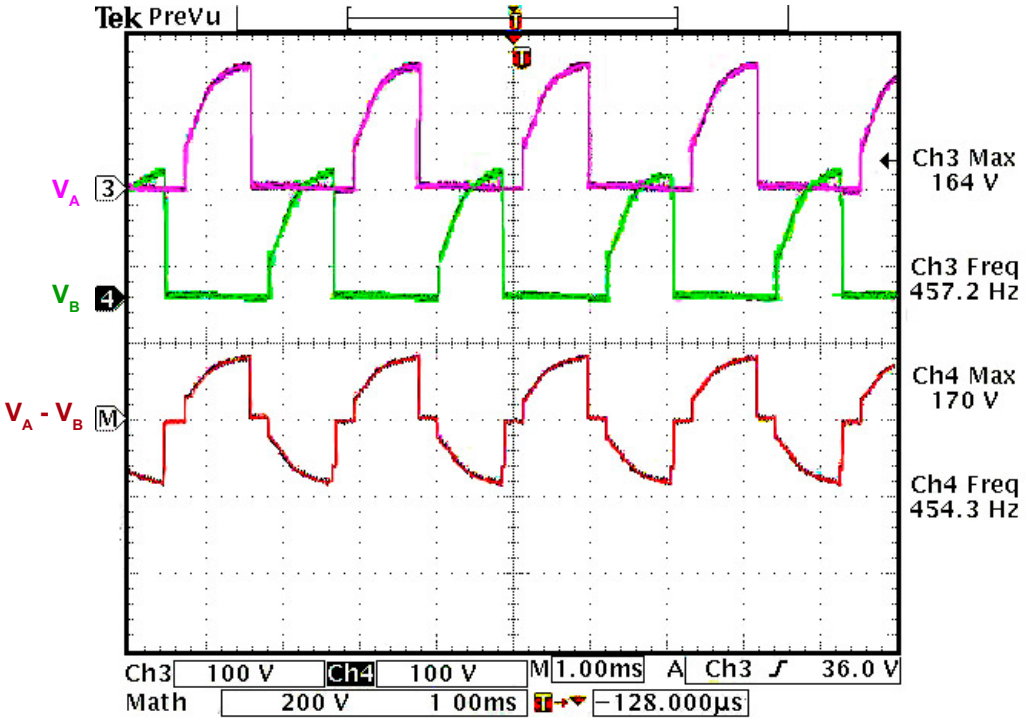


Figure 3. Push-Button, Delayed Turn Off



Typical Waveform on V_A, V_B, and Differential Waveform V_A - V_B

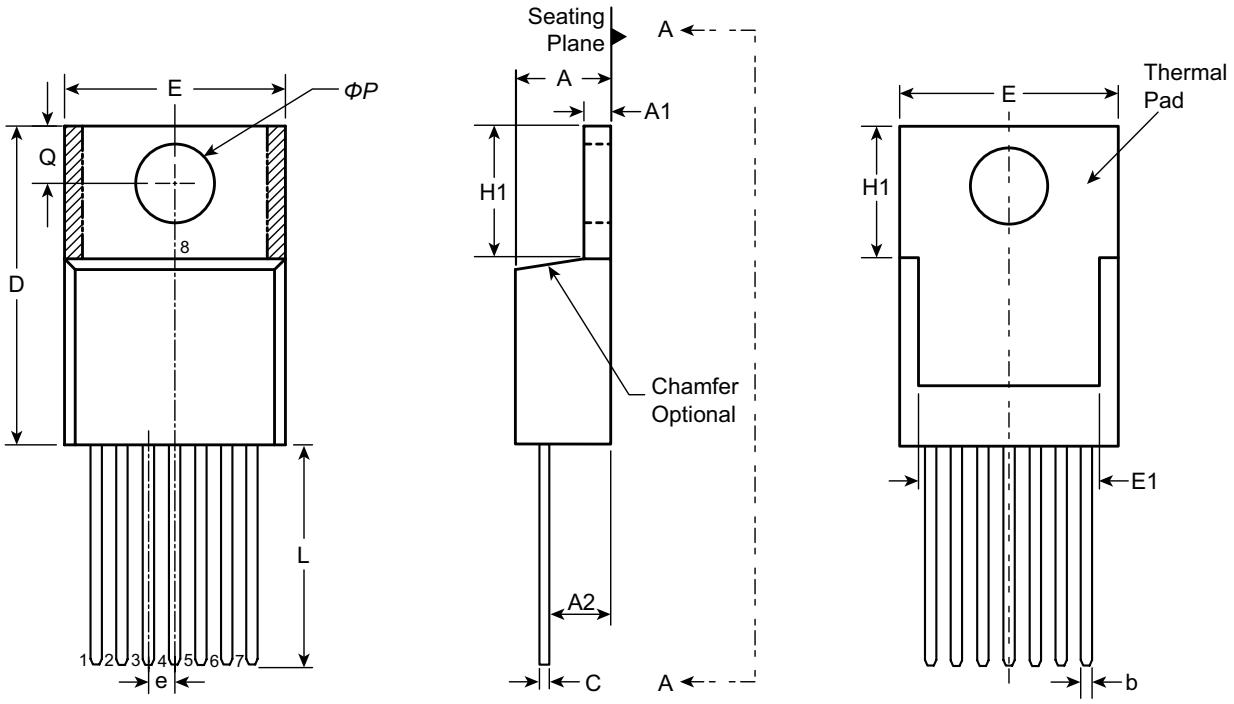
(HV_{IN} = 170V, R_{EL} = 1.0MΩ, and C_L = 350nF)



Function Table

Pin Name	Description
Osc1	The Output H-bridge can be enabled and disabled by connecting the Osc1 pin to the GND and VDD pins. The output can be left enabled by connecting the Osc1 pin to GND.
Osc2	The RC network can be connected between the oscillator's Osc1 and Osc2 pins to pulse the EL lamp on and off.
VDD	Internal supply voltage.
REL-Osc	EL lamp frequency is controlled via an external R_{EL} resistor connected between the REL-Osc and GND pins of the device.
VB	VB side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
VA	VA side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
HVIN	High voltage input supply pin.
GND	Ground pin.

7-Lead TO-220 Package Outline (K2)



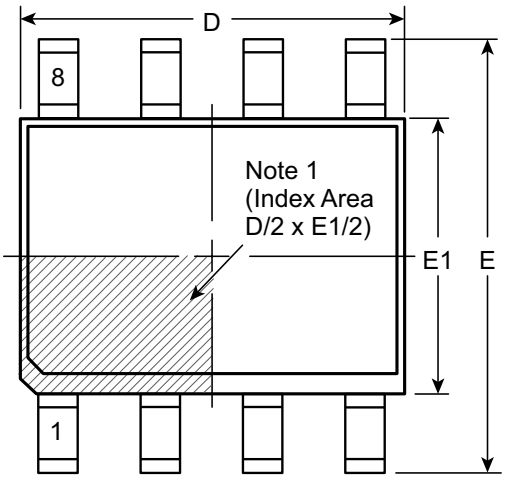
Front View **Side View** **View A - A**

Symbol		A	A1	A2	b	c	D	E	E1	e	H1	L	Q	ΦP
Dimension (inches)	MIN	.160	.045	.090	.023	.015	.560	.385	.300 REF	.045	.234	.540	.103	.146
	NOM	-	-	-	-	-	-	-		-	-	-	-	-
	MAX	.190	.055	.115	.037	.022	.590	.415		.055	.258	.560	.113	.156

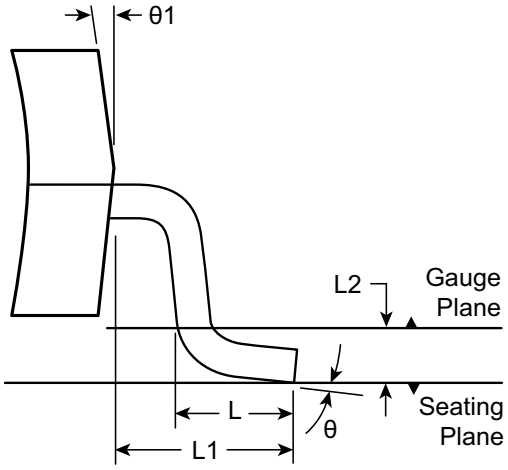
Drawings not to scale.
Supertex Doc. #: *DSPD-7TO220K2, Version NR090308.*

8-Lead SOIC (Narrow Body) Package Outline (LG)

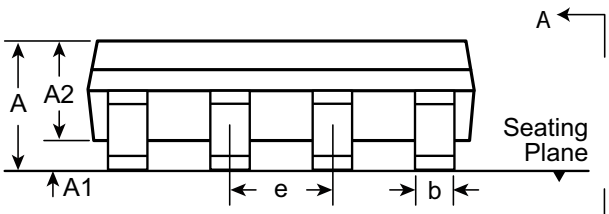
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



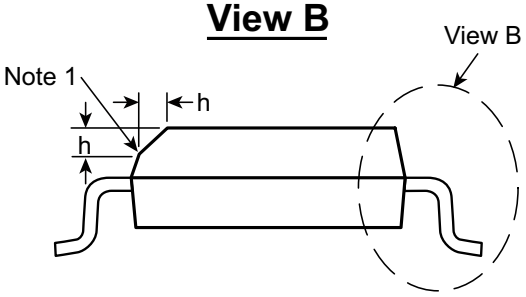
Top View



View B



Side View



View A-A

Note:

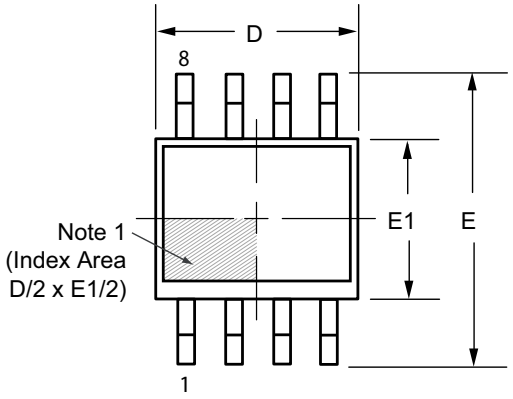
1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

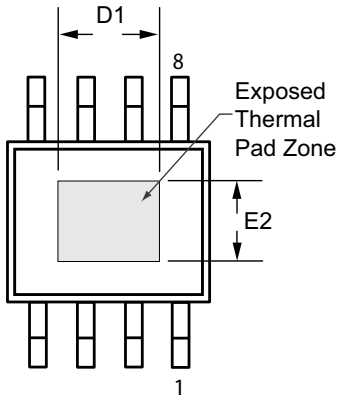
JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8SOLGTG, Version I041309.*

8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)

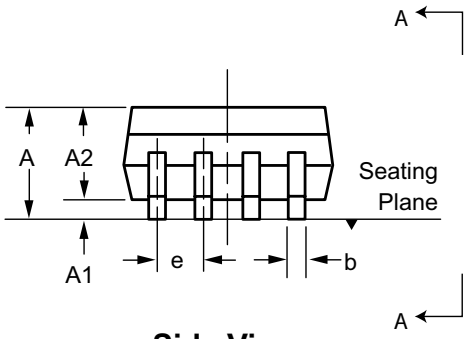
4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



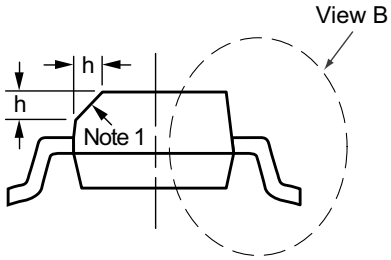
Top View



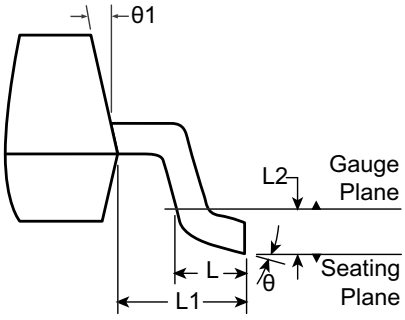
Bottom View



Side View



View A - A



View B

Note:

1. *If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/ identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30†	5.80*	3.80*	2.29†	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81†	6.20*	4.00*	2.79†		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc. #:** DSPD-8SOSG, Version D041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com