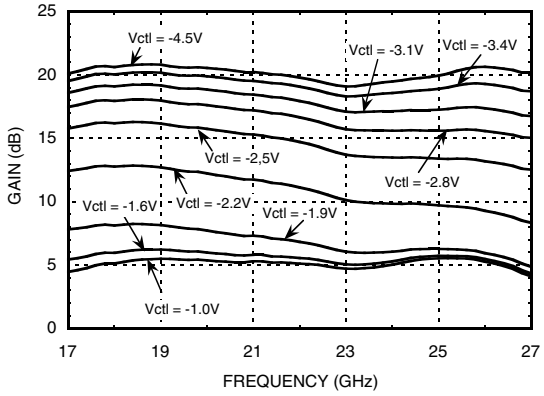
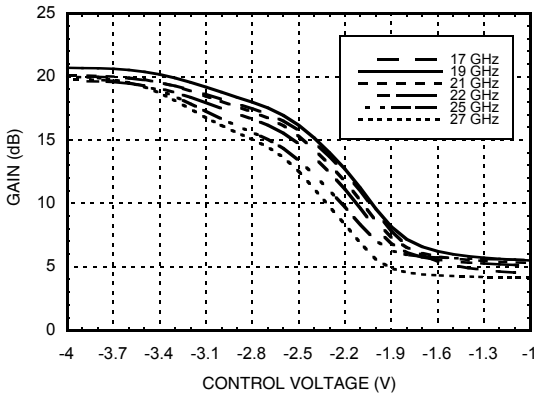
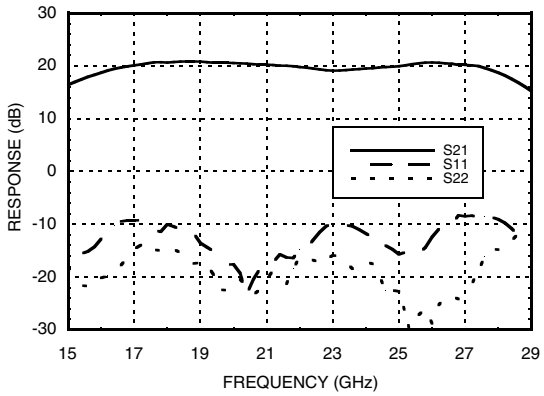
Gain vs. Control Voltage Range



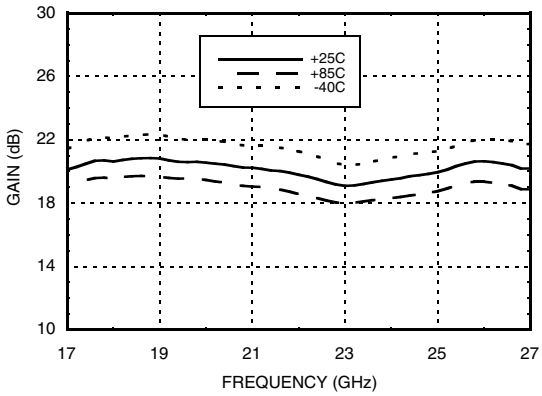
Gain vs. Control Voltage



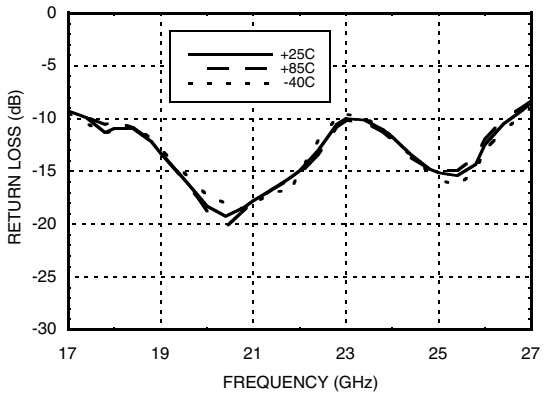
Broadband Gain & Return Loss



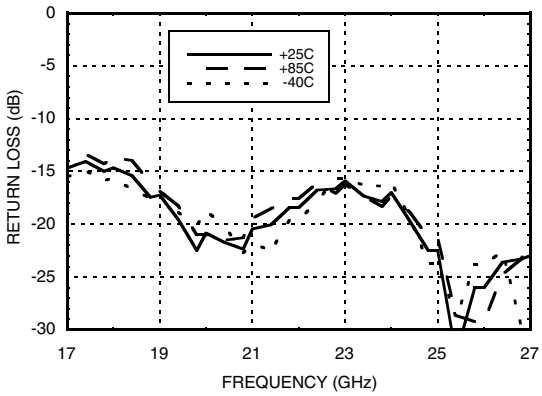
Gain vs. Temperature



Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



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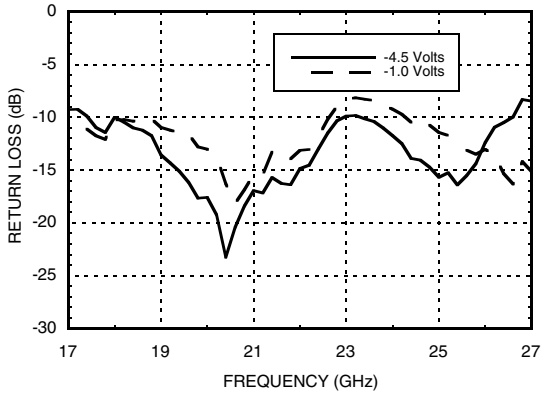
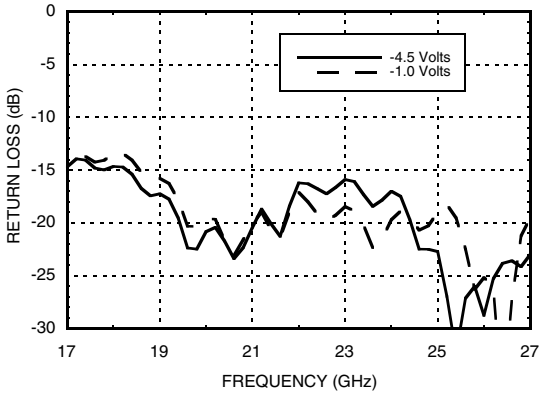
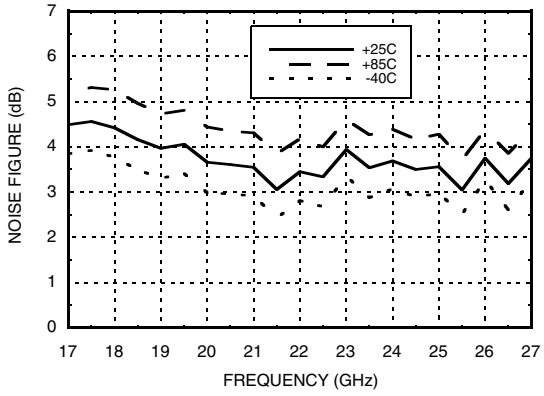
Input Return Loss @ Control Voltage Extreme



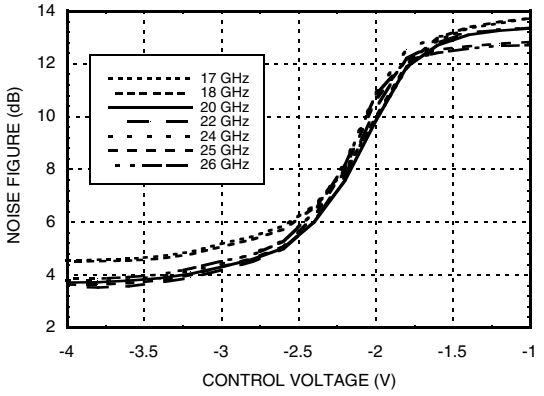
Output Return Loss @ Control Voltage Extreme



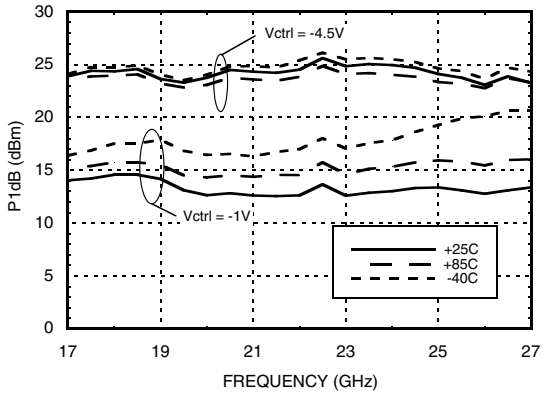
Noise Figure vs. Temperature



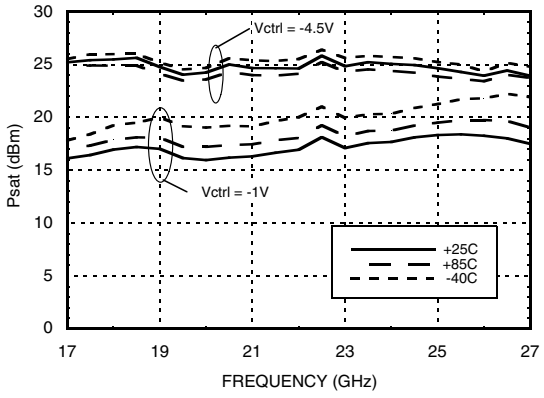
Noise Figure vs. Control Voltage



P1dB vs. Temperature



Psat vs. Temperature



[1] Tested with broadband bias tee on RF ports and C1 = 10,000 pF
[2] C1, C6 and C8 = 100 pF, L1 = 24 nF

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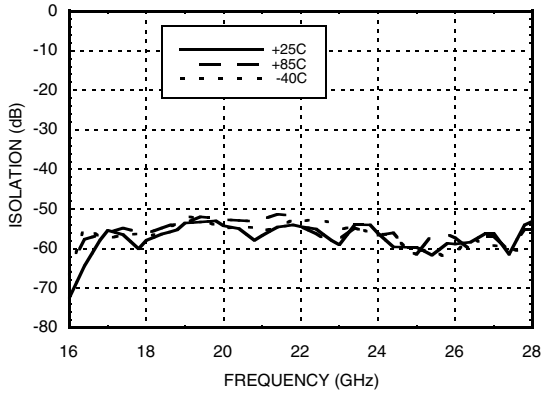
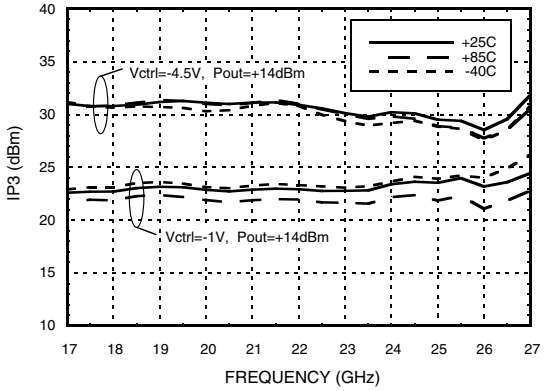
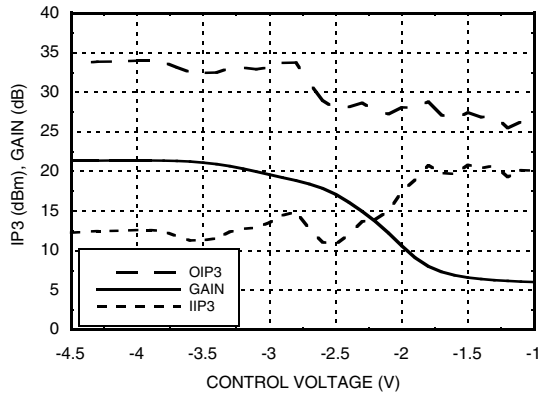
Reverse Isolation vs. Temperature



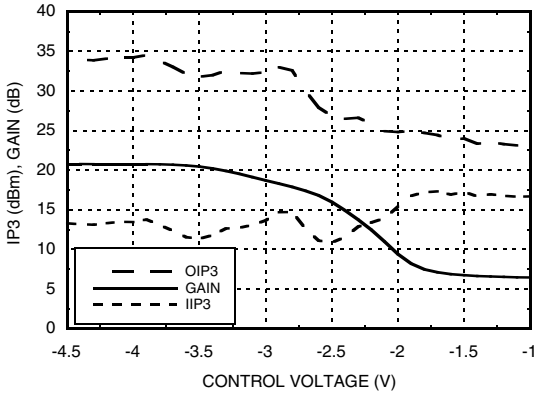
Output IP3 vs. Temperature



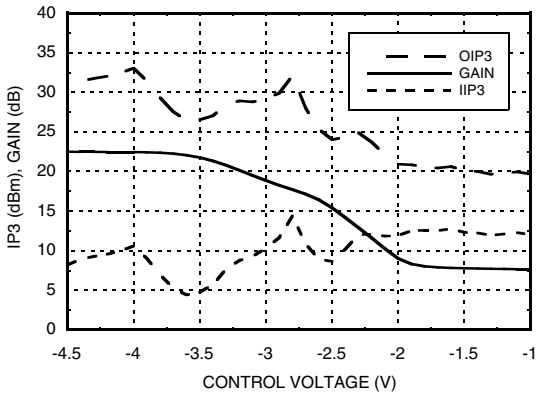
IP3 and Gain @ 18 GHz Pin = -20 dBm



IP3 and Gain @ 22 GHz Pin = -20 dBm



IP3 and Gain @ 26 GHz Pin = -20 dBm



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Absolute Maximum Ratings

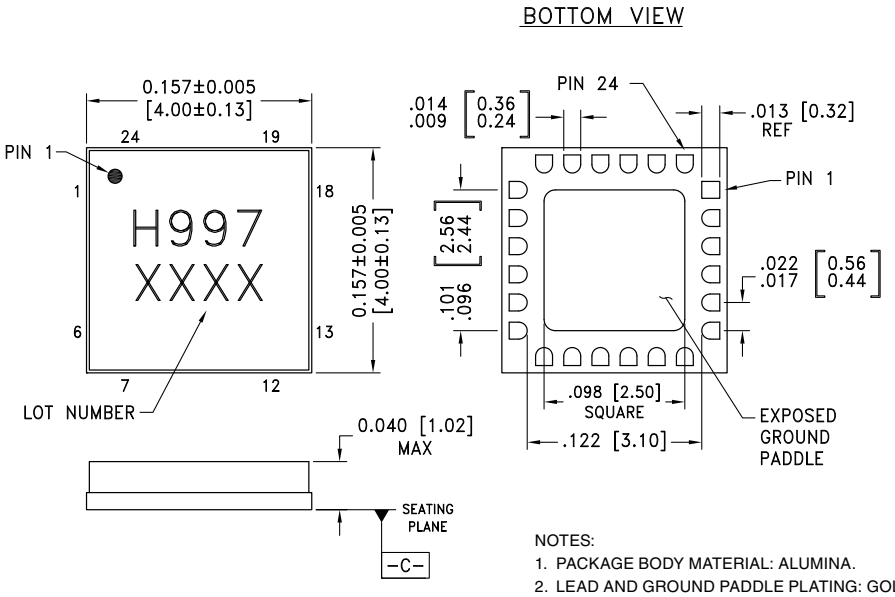
Drain Bias Voltage (Vdd1, 2, 3)	+5.5V
Gate Bias Voltage (Vgg1, 2)	-3 to 0V
Gain Control Voltage (Vctrl)	-5 to 0V
RF Power Input (RFIN)	+5 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 10.2 mW/°C above 85 °C) [1]	0.92 W
Thermal Resistance (Channel to ground paddle)	97.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0 Passed 100V

Bias Voltage

Vdd1,2,3 (V)	Idd Total (mA)
+5V	170
Vgg1,2 (V)	Igg Total (mA)
0V to -2V	<0.1 mA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA.
2. LEAD AND GROUND PADDLE PLATING: GOLD FLASH OVER NICKEL.
3. DIMENSIONS ARE IN INCHES (MILLIMETERS).
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 MM DATUM –C–
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC997LC4	Alumina, White	Gold over Nickel	MSL3 [1]	H997 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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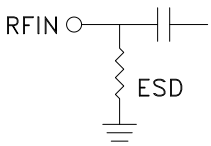
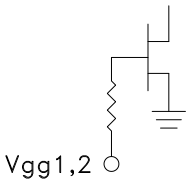
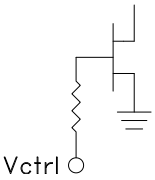
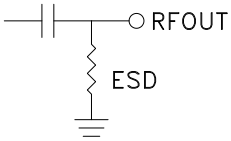
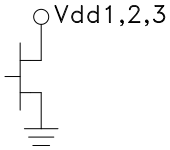
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 6, 8, 10, 11, 13, 17, 18, 20, 21, 23	N/C	The pins are not connected internally: however all data shown herein was measured with these pins connected to RF/DC ground externally	
3, 5, 14, 16	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	
4	RFIN	This pad is AC coupled and matched to 50 Ohm.	
7, 12	Vgg1, 2	Gate control for amplifier. Adjust voltage to achieve typical Idd. Please follow “MMIC Amplifier Biasing Procedure” application note.	
9	Vctrl	Gain control Voltage for the amplifier. See assembly diagram for required external components.	
15	RFOUT	This pad is AC coupled and matched to 50 Ohm.	
19, 22, 24	Vdd3, 2, 1	Drain Bias Voltage for the amplifier. See assembly diagram for required external components	

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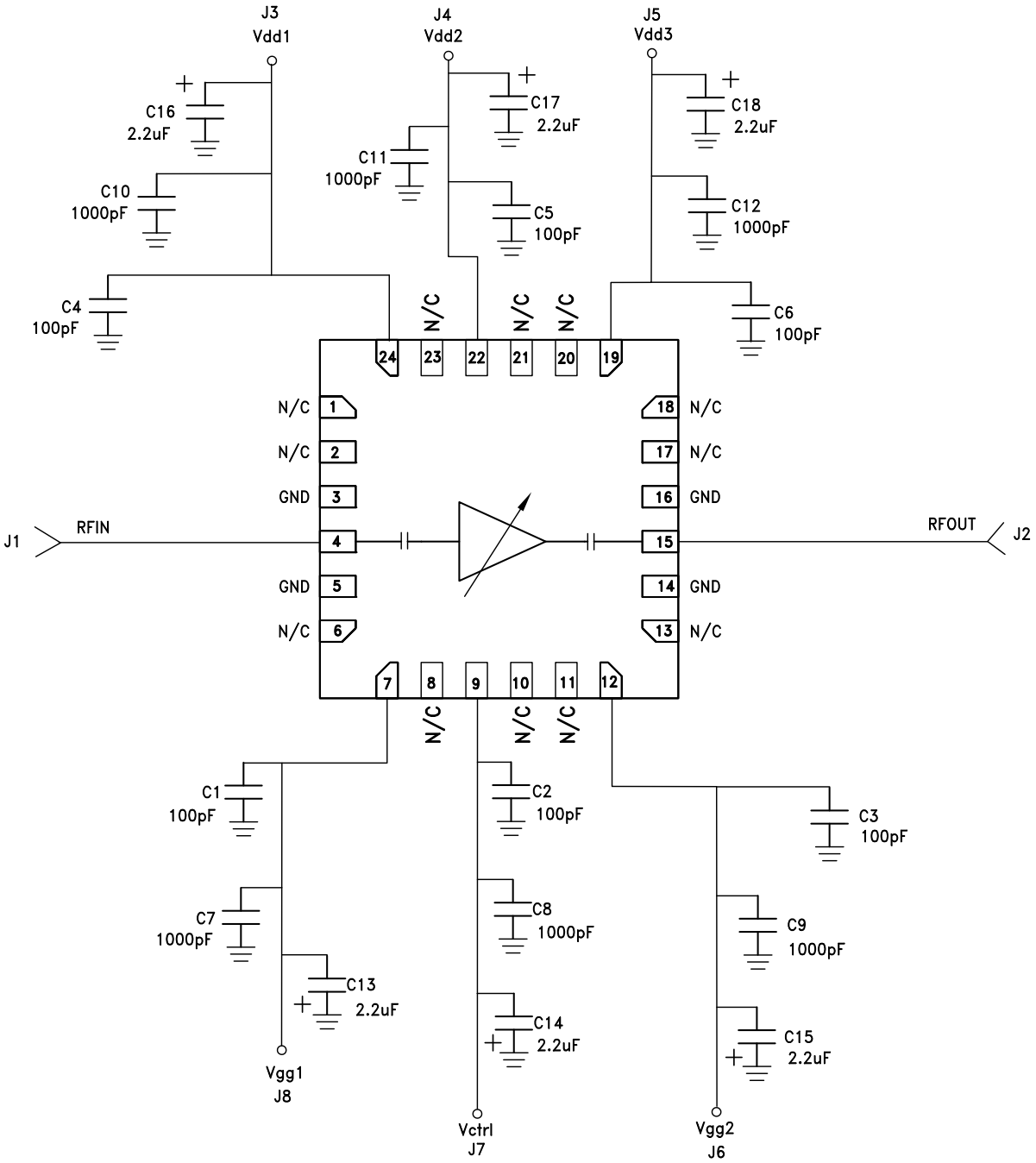
Application Circuit



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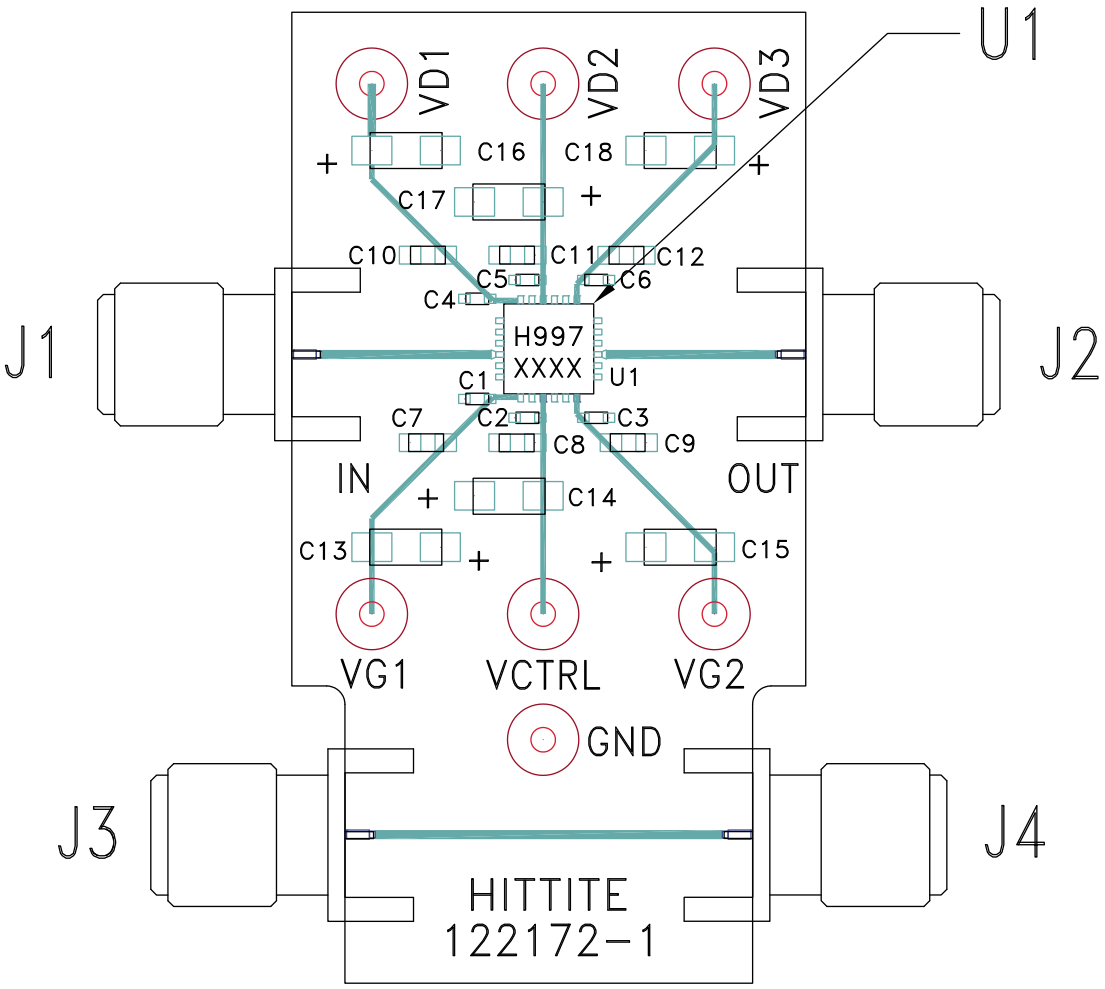
Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC997LC4 [1]

Item	Description
J1, J4	PCB Mount SMA RF Connectors
J5 - J10	DC Pin
C1 - C6	100 pF Capacitor, 0402 Pkg.
C7 - C12	1000 pF Capacitor, 0603 Pkg.
C13 - C18	2.2 µF Capacitor, CASE A
U1	HMC997LC4 Variable Gain Amplifier
PCB [2]	122172 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25 FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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