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2/2017—Rev. B to Rev. C

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11/2009—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

TEST SETUP

The EVAL-ADM2582E/EVAL-ADM2587E evaluation board is shown in Figure 2 with the default jumper settings on the LK1 through LK9 jumper blocks. In the default jumper connections, both the ADM2582E/ADM2587E driver and receiver are enabled. Figure 2 also shows the power connection on the J2 terminal block, input signal connection on the DI jack, and probes attached to the RXD, DI, Y, and Z test points for a loopback test (LK5 and LK7 are closed to connect the A pin to Y pin and B pin to Z pin, respectively).

JUMPER SETTINGS

The inputs to the ADM2582E/ADM2587E can be configured using the jumpers on the evaluation board (see Table 1). Do not place multiple jumpers on the LK1, LK6, and LK9 jumper blocks because doing so can short the import sources together. For each link, a single jumper block can move from one position to another, as specified in Table 1.

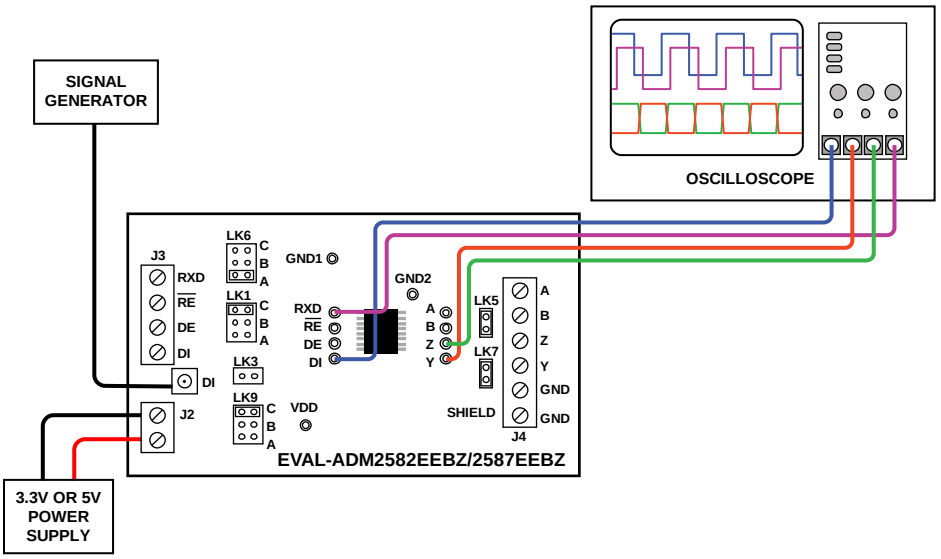

Figure 2. Basic Operation of the EN55022 Class B Compliant Evaluation Board for the ADM2582E/ADM2587E Isolated RS-485/RS-422 Transceivers

Table 1. Jumper Configurations

Link	Connection	Description
LK1	A	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to the V_{CC} pin. This setting enables the driver.
	B	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to the DE J3 terminal block connector.
	C	Connects the driver enable input (DE) of the ADM2582E/ADM2587E to the GND_1 pin. This setting disables the driver.
LK6	A	Connects the receiver enable input ($\overline{RE}$) of the ADM2582E/ADM2587E to the V_{CC} pin. This setting disables the receiver.
	B	Connects the receiver enable input ($\overline{RE}$) of the ADM2582E/ADM2587E to the $\overline{RE}$ J3 terminal block connector.
	C	Connects the receiver enable input ($\overline{RE}$) of the ADM2582E/ADM2587E to the GND_1 pin. This setting enables the receiver.
LK3	Closed	Connects the receiver enable input ($\overline{RE}$) of the ADM2582E/ADM2587E to the driver enable input (DE). This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK9	A	Connects the TxD pin of the ADM2582E/ADM2587E to the DI connector.
	B	Connects the TxD pin of the ADM2582E/ADM2587E to the DI J3 terminal block connector.
	C	Connects the TxD pin of the ADM2582E/ADM2587E to the on-board oscillator circuit.
LK5	Closed	Connects the ADM2582E/ADM2587E Receiver Input B to Driver Output Z. When LK5 and LK7 are both connected, the evaluation board is configured for half-duplex operation.
	Open	When LK5 and LK7 are both open, the evaluation board is configured for full-duplex operation.
LK7	Closed	Connects the ADM2582E/ADM2587E Receiver Input A to Driver Output Y. When LK5 and LK7 are both connected, the evaluation board is configured for half-duplex operation.
	Open	When LK5 and LK7 are both open, the evaluation board is configured for full-duplex operation.

TERMINATION AND PULL-UP/PULL-DOWN RESISTORS

The evaluation board includes the RT and RT1 footprints for fitting termination resistors between the A and B receiver inputs and the Y and Z driver outputs. By default, the board is not fitted with a 120 Ω resistor, RT, between A and B. This resistor must not be fitted if the board is connected to a bus that is already terminated at both ends. For more information about proper termination, see the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*.

Although the ADM2582E/ADM2587E have a built in receiver fail-safe for the bus idle condition, there are footprints on the evaluation board for fitting the R9 and R10 pull-up resistors to the V_{ISOOUT} supply of the ADM2582E/ADM2587E on Receiver Input A and Driver Output Y, as well as the R7 and R8 pull-down resistors to GND_2 on Receiver Input B and Driver Output Z. These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in the bus idle condition depends on the supply voltage (for example, 960 Ω for 3.3 V and 1440 Ω for 5 V).

For more information about the bus idle fail-safe, see the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*.

DECOUPLING AND RESERVOIR CAPACITORS

The evaluation board uses the following decoupling and reservoir capacitors:

- On the logic side of the board, the C3 and C4 capacitors must be 10 nF and 100 nF ceramic capacitors, respectively, and the C2 capacitor must be a 10 µF tantalum capacitor.
- On the logic side of the board, the C7 capacitor must be a 100 nF ceramic capacitor, and the C9 capacitor must be a 10 µF tantalum capacitor.
- On the logic side of the board, additional capacitors are added for the power regulation circuits. C12, C13, and C16 must be 10 µF tantalum capacitors, and C14 and C15 must be 100 nF ceramic capacitors.
- On the bus side of the board, the C5 and C6 capacitors must be 10 nF and 100 nF, respectively, and the C1 and C8 capacitors must be 100 nF and 10 µF, respectively.

BOARD INTERNAL LAYER THICKNESS

The EVAL-ADM2582EEBZ/EVAL-ADM2587EEBZ evaluation board consists of four layers. The spacing between the top and bottom layer is 1.6 mm.

The EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ PCB has a minimum distance of 0.4 mm of insulation along a bonded surface, meeting requirements for isolation standards IEC 61010, third edition, and IEC 60950 as described in the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with iCoupler® Devices*.

OVERLAPPING STITCHING CAPACITOR

The evaluation board implements an embedded stitching capacitor structure. An embedded PCB capacitor is created when two metal planes in a PCB overlap each other and are separated by dielectric material. This embedded stitching capacitor is formed by extending the internal reference planes from the primary and secondary layers across the area, which is used for creepage on the PCB surface. This capacitor provides a return path for high frequency common-mode noise currents across the isolation gap. The overlapping area is 53 mm × 7 mm and the distance between overlapping layers is 0.4064 mm, therefore, the plate capacitor is around 35 pF. The layout and implementation of embedded stitching capacitors is explained in detail in the AN-0971 Application Note.

PCB LAYOUT RECOMMENDATIONS

The EVAL-ADM2582EEBZ/EVAL-ADM2587EEBZ evaluation board is designed to reduce emissions generated by the high frequency switching elements used by the *iso*Power technology to transfer power through the ADM2582E/ADM2587E integrated transformer. The layout of the evaluation board is generated using the guidelines provided in the AN-1349 Application Note.

The AN-1349 Application Note provides examples of 4-layer PCBs. The EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ PCB layouts are 4-layer PCBs. To pass EN55022 Class B on a 4-layer PCB, the following layout guidelines are recommended:

- Ensure that there is good decoupling on the PCB (see the Decoupling and Reservoir Capacitors section).
- Place a ferrite bead between the PCB trace connections and the following IC pins: V_{ISOOUT} (Pin 12) and GND_2 (Pin 11 and Pin 14).
- Do not connect the V_{ISOOUT} pin to a power plane; connect between V_{ISOOUT} and V_{ISOIN} using a PCB trace. Ensure that V_{ISOIN} (Pin 19) is connected through the L3 ferrite to V_{ISOOUT} (Pin 12), as shown in Figure 3.
- Place an embedded stitching capacitor between GND_1 and GND_2 using internal layers of the PCB planes (see the Overlapping Stitching Capacitor section).

The following additional notes apply to the PCB layout; refer to the schematic and artwork in Figure 8 to Figure 13.

- Ensure that GND_2 (Pin 14) is connected to GND_2 (Pin 11) on the inside (device side) of the C1 100 nF capacitor.
- Ensure that the C1 capacitor is connected between V_{ISOOUT} (Pin 12) and GND_2 (Pin 11) on the device side of the L2 and L3 ferrites.
- Ensure that GND_2 (Pin 16) is connected to GND_2 (Pin 11) on the outside (bus side) of the L2 ferrite, as shown in Figure 3.
- Ensure that there is a keep out area for the GND_2 plane in the PCB layout around the L2 and L3 ferrites. The keep out area means there must not be a GND_2 fill on any layer below the L2 and L3 ferrites.

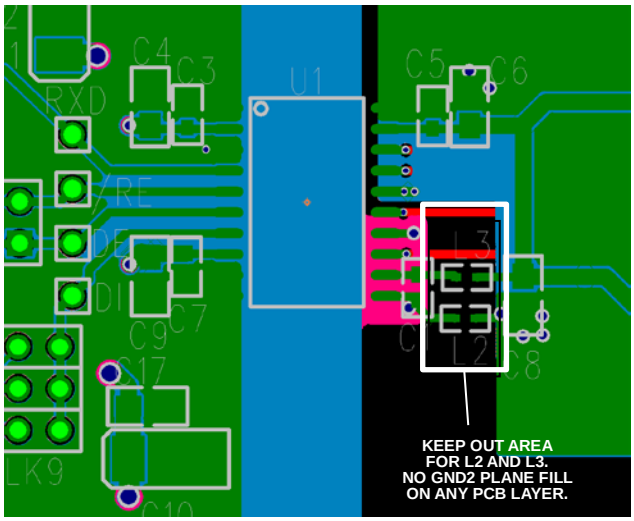

Figure 3. Layout Notes for EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ

- Locate the power delivery circuit in close proximity to the ADM2582E/ADM2587E device, so that the V_{CC} trace is as short as possible. The EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ PCB has a power delivery circuit located at the bottom of the PCB with a short trace from the ADP667ARZ regulator output to V_{CC} (Pin 8). This layout example minimizes the loop area in which high frequency current can flow. An increase in the loop area results in an increase in the emissions levels.

Table 2. PCB Stack Up

Primary V_{CC} Side	Secondary V_{ISO} Side
Layer 1: Ground 1 plane	Layer 1: Ground 2 plane
Layer 1: Ground 1 plane	Layer 2: Ground 2 plane
Layer 3: V_{CC} plane	Layer 3: Ground 2 plane (overlap stitching capacitor)
Layer 4: Ground 1 plane	Layer 4: Ground 2 plane

EN55022 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADM2587EEBZ evaluation board is tested and certified to pass EN55022 Class B with a >5 dB µV/m margin. The EVAL-ADM2582EEBZ evaluation board is tested and certified to pass EN55022 Class B. EN55022 certification documents for the EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ evaluation boards are available to users upon request from Analog Devices, Inc.

Table 3 provides a summary of the capability of the EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ evaluation boards. All EN55022 radiated emissions tests are performed with the PCB schematic and layout, as described in Figure 8 to Figure 13.

Table 3. EN55022 Test Results Summary

Device	Configuration	EN55022 Class B Result
ADM2582E	3.3 V V_{CC}, 16 Mbps, 60 Ω load	Pass (with 4.7 dB µV/m margin)
ADM2582E	5.0 V V_{CC}, 16 Mbps, 60 Ω load	Pass (with 6.5 dB µV/m margin)
ADM2587E	3.3 V V_{CC}, 500 kbps, 60 Ω load	Pass (with 5.5 dB µV/m margin)
ADM2587E	5.0 V V_{CC}, 500 kbps, 60 Ω load	Pass (with 8.5 dB µV/m margin)

The EVAL-ADM2582EEBZ and EVAL-ADM2587EEBZ evaluation boards are configured and tested with 3.3 V V_{CC} or 5.0 V V_{CC} power supplied to the ADM2582E and ADM2587E devices, with the power supplied from the ADP667ARZ regulator output to V_{CC} (Pin 8). The ADP667ARZ regulator input is supplied from a standard 9 V battery. All EN55022 radiated emissions testing is performed with 9 V batteries. Testing is performed at a 500 kbps clock (ADM2587E) or 16 Mbps clock (ADM2582E), with the clock supplied by the on-board oscillator. The ADM2582E/ADM2587E transceiver is connected in full-duplex mode and the bus pins are loaded with a 60 Ω termination resistor. Measurements are carried out in a semi anechoic chamber at 10 m from 30 MHz to 2 GHz . Figure 4 to Figure 7 show the results of the worst case horizontal scans, and Table 4 to Table 7 show the tabulated quasi-peak (QP) results.

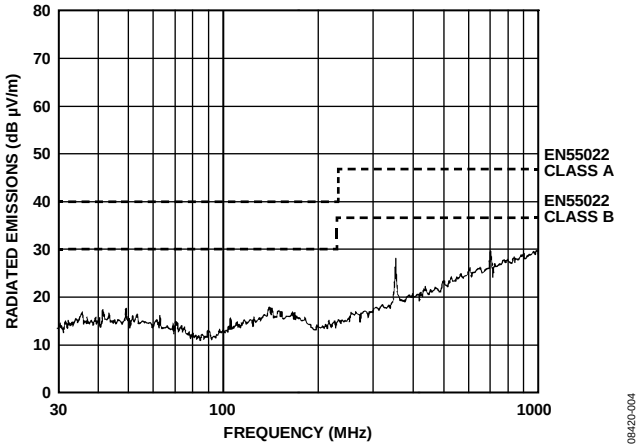

Figure 4. Horizontal Scan from 30 MHz to 1000 MHz (Corresponds to Worst Case for Table 4)

Table 4. ADM2587E 3.3 V V_{CC} Test Results

Frequency (MHz)	QP Level (dB µV/m)	EN55022 Class B (dB µV/m)	Antenna Position	Antenna Height (m)	Pass/Fail
353.0560	31.50	37	Horizontal	2.5	Pass
705.1640	27.1	37	Horizontal	1.2	Pass

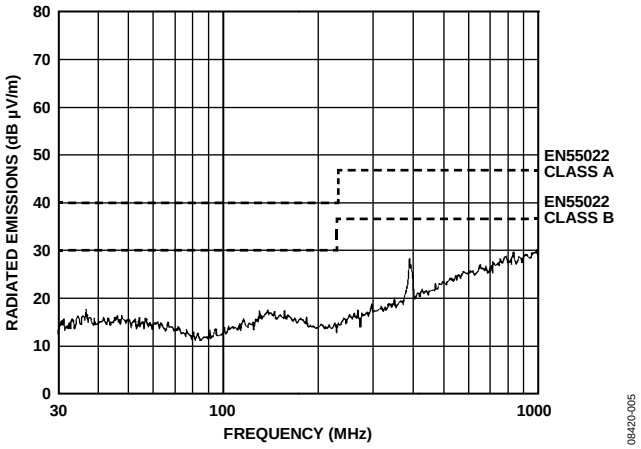

Figure 5. Horizontal Scan from 30 MHz to 1000 MHz (Corresponds to Worst Case for Table 5)

Table 5. ADM2587E 5.0 V V_{CC} Test Results

Frequency (MHz)	QP Level (dB µV/m)	EN55022 Class B (dB µV/m)	Antenna Position	Antenna Height (m)	Pass/Fail
391.7840	28.50	37	Horizontal	2.5	Pass

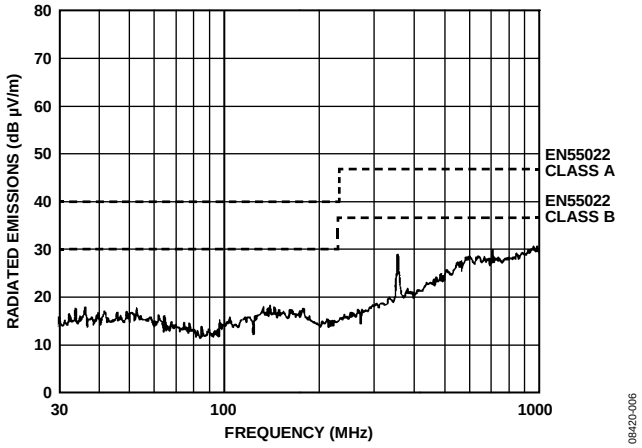

Figure 6. Horizontal Scan from 30 MHz to 1000 MHz (Corresponds to Worst Case for Table 6)

Table 6. ADM2582E 3.3 V V_{CC} Test Results[1]

Frequency (MHz)	QP Level (dB µV/m)	EN55022 Class B (dB µV/m)	Antenna Position	Antenna Height (m)	Pass/Fail
358.1160	17.10	37	Vertical	1	Pass
357.1520	32.30	37	Horizontal	2.5	Pass

[1] Not using a high voltage discrete capacitor between GND_1 and GND_2.

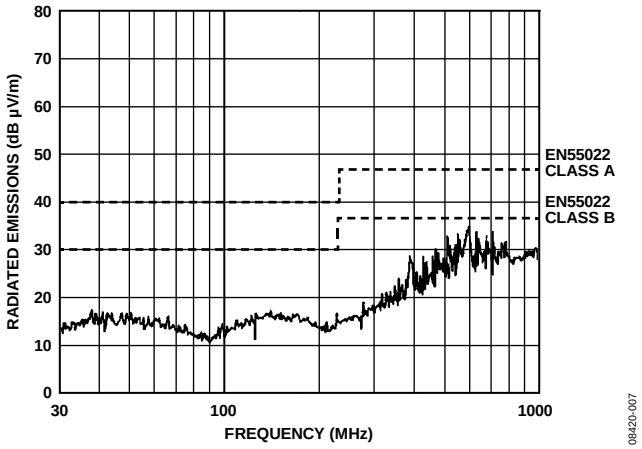

Figure 7. Horizontal Scan from 30 MHz to 1000 MHz (Corresponds to Worst Case for Table 7)

Table 7. ADM2582E 5.0 V V_{CC} Test Results

Frequency (MHz)	QP Level (dB µV/m)	EN55022 Class B (dB µV/m)	Antenna Position	Antenna Height (m)	Pass/Fail
360.0480	15.50	37	Horizontal	1	Pass
392.1560	30.50	37	Horizontal	2.5	Pass
432.8720	22.20	37	Horizontal	2	Pass
473.0560	24.70	37	Horizontal	2	Pass
513.2880	26.60	37	Horizontal	1.8	Pass
553.6760	26.30	37	Horizontal	1.5	Pass
604.1840	29.50	37	Horizontal	1.2	Pass
638.8040	25.10	37	Horizontal	1.5	Pass
719.7120	26.10	37	Horizontal	1.5	Pass
791.8040	30.00	37	Horizontal	1.2	Pass

EVALUATION BOARD SCHEMATICS AND ARTWORK

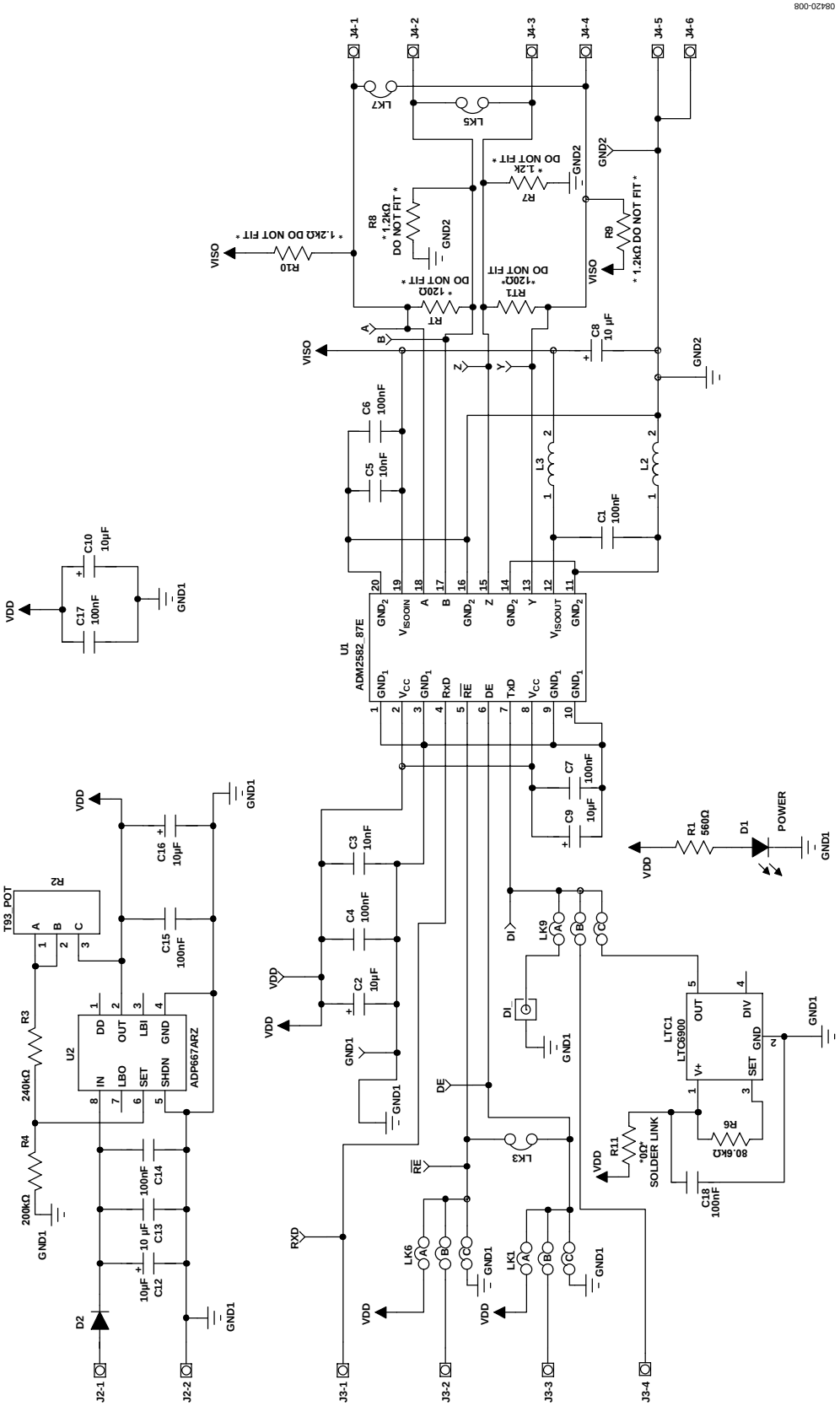

Figure 8. Schematic of the ADM2582E/ADM2587E Evaluation Board

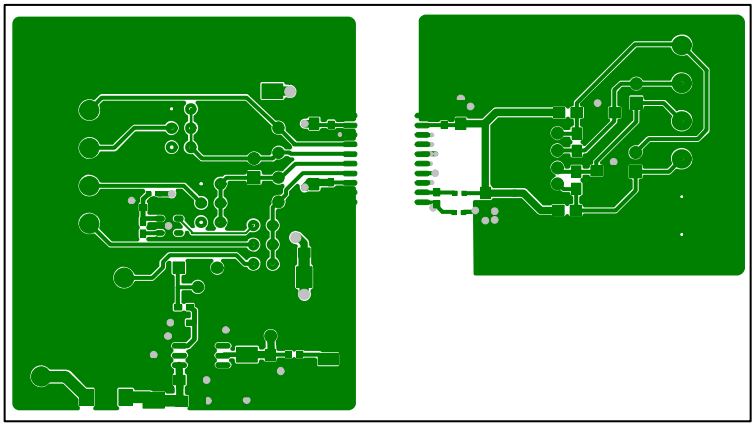

Figure 9. Top Layer

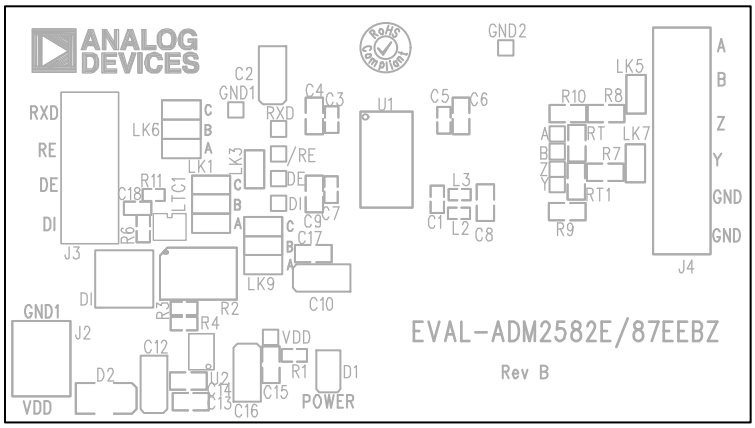

Figure 10. Silkscreen

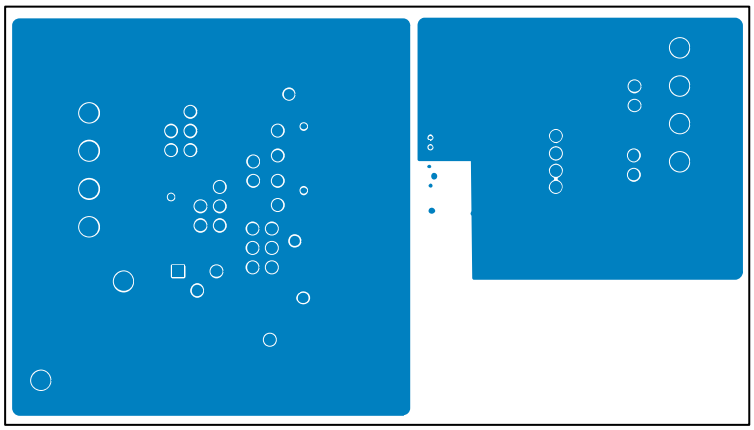

Figure 11. Second Layer

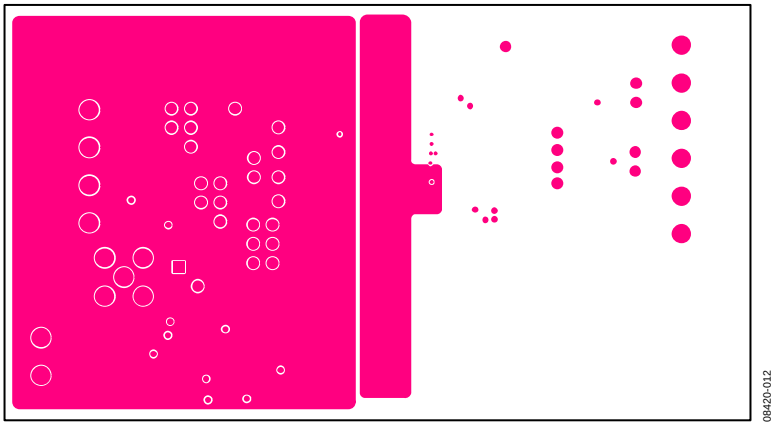

Figure 12. Third Layer

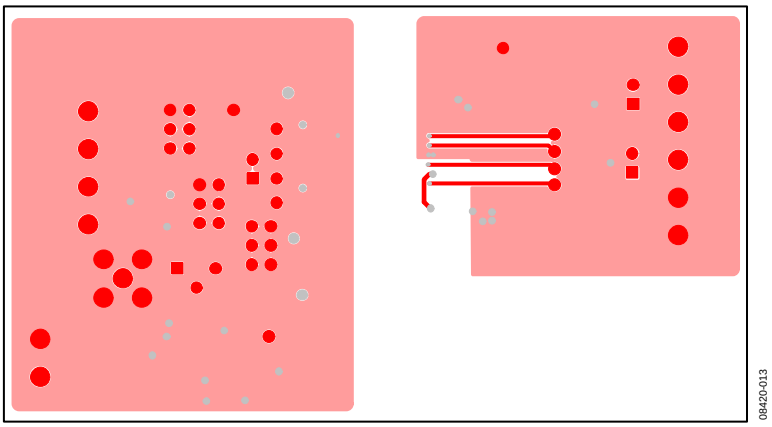

Figure 13. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 8. EVAL-ADM2582EEBZ

Qty	Reference Designator	Description	Manufacturer	Part Number
4	R7, R8, R9, R10	Resistors, size 0805 (not inserted)	Panasonic	ERA6AEB122V
1	R11	Resistor, 0 Ω, size 0402 (not inserted)	Multicomp	MCMR04X000 PTL
1	RT	Resistor, 120 Ω, size 0805 (not inserted)	Yageo	RC0805JR-07120RL
1	RT1	Resistor, 120 Ω, size 0805 (not inserted)	Yageo	RC0805JR-07120RL
3	C8, C9, C13	Capacitors, size 0805, 10 µF	AVX	08056C106KAT2A
5	C4, C6, C14, C15, C17	Capacitors, size 0805, 100 nF	Multicomp	MC0805F104Z160CT
4	C2, C10, C12, C16	Capacitors, tantalum, 10 µF	Kemet	B45196E3106K309
3	C1, C7, C18	Capacitors, size 0603, 100 nF	Yageo	CC0603KRX7R7BB104
2	C3, C5	Capacitors, size 0603, 10 nF	AVX	0603YC103KAT2A
1	J2	Power connector, 2-pin terminal block	Camdenboss	CTB5000/2
1	J3	Connector, 4-pin terminal block	Camdenboss	CTB5000/4
1	J4	Connector, 6-pin terminal block	Camdenboss	CTB5000/6
1	LTC1	Oscillator	LTC	LTC6900CS5#TRMPBF
1	R1	Resistor, 0603, 1%, 560 Ω	Multicomp	CRCW0603560RFKEAHP
1	R2	Trimmer, potentiometer, 500 kΩ, 23 turn	Vishay	T93YB504KT20
1	R3	Resistor, 0603, 240 kΩ, 5%	Vishay	CRCW0603240KFKEA
1	R4	Resistor, 0603, 200 kΩ, 5%	Bourns	CR0603-FX-2003ELF
1	R6	Resistor, 0603, 80.6 kΩ, 0.1%	Multicomp	MC0063W060312K49
3	LK1, LK6, LK9	6-pin (3 × 2), 2.54 mm header and shorting blocks	Harwin	M20-9983646 and M7566-05
3	LK3, LK5, LK7	2-pin (1 × 2), 2.54 mm header and shorting blocks	Harwin	M20-9990246
1	U1	20-lead, wide body SOIC	Analog Devices	ADM2582EBRWZ
1	U2	Adjustable voltage regulator	Analog Devices	ADP667ARZ
2	LK2, LK3	Ferrite beads, 0402	Taiyo Yuden	BKH1005LM182-T
1	DI	SMA, right hand jack	TE Connectivity	5-1814400-1
1	D1	LED, SMD	Avago	HSMS-C191
1	D2	Schottky diode, 1 A, SMB	ON Semiconductor	MBRS130T3G
11	RXD, $\overline{RE}$, DE, DI, A, B, Z, Y, VDD, GND1, GND2	Test points, yellow	Vero	20-313140

Table 9. EVAL-ADM2587EEBZ

Qty	Reference Designator	Description	Manufacturer	Part Number
4	R7, R8, R9, R10	Resistors, size 0805 (not inserted)	Panasonic	ERA6AEB122V
1	R11	Resistor, 0 Ω, size 0402 (not inserted)	Multicomp	MCMR04X000 PTL
1	RT	Resistor, 120 Ω, size 0805 (not inserted)	Yageo	RC0805JR-07120RL
1	RT1	Resistor, 120 Ω, size 0805 (not inserted)	Yageo	RC0805JR-07120RL
3	C8, C9, C13	Capacitors, size 0805, 10 µF	AVX	08056C106KAT2A
5	C4, C6, C14, C15, C17	Capacitors, size 0805, 100 nF	Multicomp	MC0805F104Z160CT
4	C2, C10, C12, C16	Capacitors, tantalum, 10 µF	Kemet	B45196E3106K309
3	C1, C7, C18	Capacitors, size 0603, 100 nF	Yageo	CC0603KRX7R7BB104
2	C3, C5	Capacitors, size 0603, 10 nF	AVX	0603YC103KAT2A
1	J2	Power connector, 2-pin terminal block	Camdenboss	CTB5000/2
1	J3	Connector, 4-pin terminal block	Camdenboss	CTB5000/4
1	J4	Connector, 6-pin terminal block	Camdenboss	CTB5000/6
1	LTC1	Oscillator	LTC	LTC6900CS5#TRMPBF
1	R1	Resistor, 0603, 1%, 560 Ω	Multicomp	CRCW0603560RFKEAHP
1	R2	Trimmer, potentiometer, 500 kΩ, 23 turn	Vishay	T93YB504KT20
1	R3	Resistor, 0603, 240 kΩ, 5%	Vishay	CRCW0603240KFKEA
1	R4	Resistor, 0603, 200 kΩ, 5%	Bourns	CR0603-FX-2003ELF
1	R6	Resistor, 0603, 2.49 kΩ, 0.1%	TE Connectivity	RP73D1J80K6BTDG

Qty	Reference Designator	Description	Manufacturer	Part Number
3	LK1, LK6, LK9	6-pin (3 × 2), 2.54 mm header and shorting blocks	Harwin	M20-9983646 and M7566-05
3	LK3, LK5, LK7	2-pin (1 × 2), 2.54 mm header and shorting blocks	Harwin	M20-9990246
1	U1	20-lead, wide body SOIC	Analog Devices	ADM2587EBRWZ
1	U2	Adjustable voltage regulator	Analog Devices	ADP667ARZ
2	LK2, LK3	Ferrite beads, 0402	Taiyo Yuden	BKH1005LM182-T
1	DI	SMA, right hand jack	TE Connectivity	5-1814400-1
1	D1	LED, SMD	Avago	HSMS-C191
1	D2	Schottky diode, 1 A, SMB	ON Semiconductor	MBRS130T3G
11	RXD, $\overline{RE}$, DE, DI, A, B, Z, Y, VDD, GND1,GND2	Test points, yellow	Vero	20-313140

RELATED LINKS

Resource	Description
ADM2587E	500 kbps, 2.5 kV rms signal and power isolated RS-485/RS-422 transceivers with ±15 kV ESD protection
ADM2582E	16 Mbps, 2.5 kV rms signal and power Isolated RS-485/RS-422 transceivers with ±15 kV ESD protection
AN-1349	Application Note, *PCB Implementation Guidelines to Minimize Radiated Emissions on the ADM2582E/ADM2587E RS-485/RS-422 Transceivers*
AN-960	Application Note, *RS-485/RS-422 Circuit Implementation Guide*
AN-1109	Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*
AN-0971	Application Note, *Control of Radiated Emissions with isoPower Devices*

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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