

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG290 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32GG290F512-BGA112	512	128	48	1.98 - 3.8	-40 - 85	BGA112
EFM32GG290F1024-BGA112	1024	128	48	1.98 - 3.8	-40 - 85	BGA112

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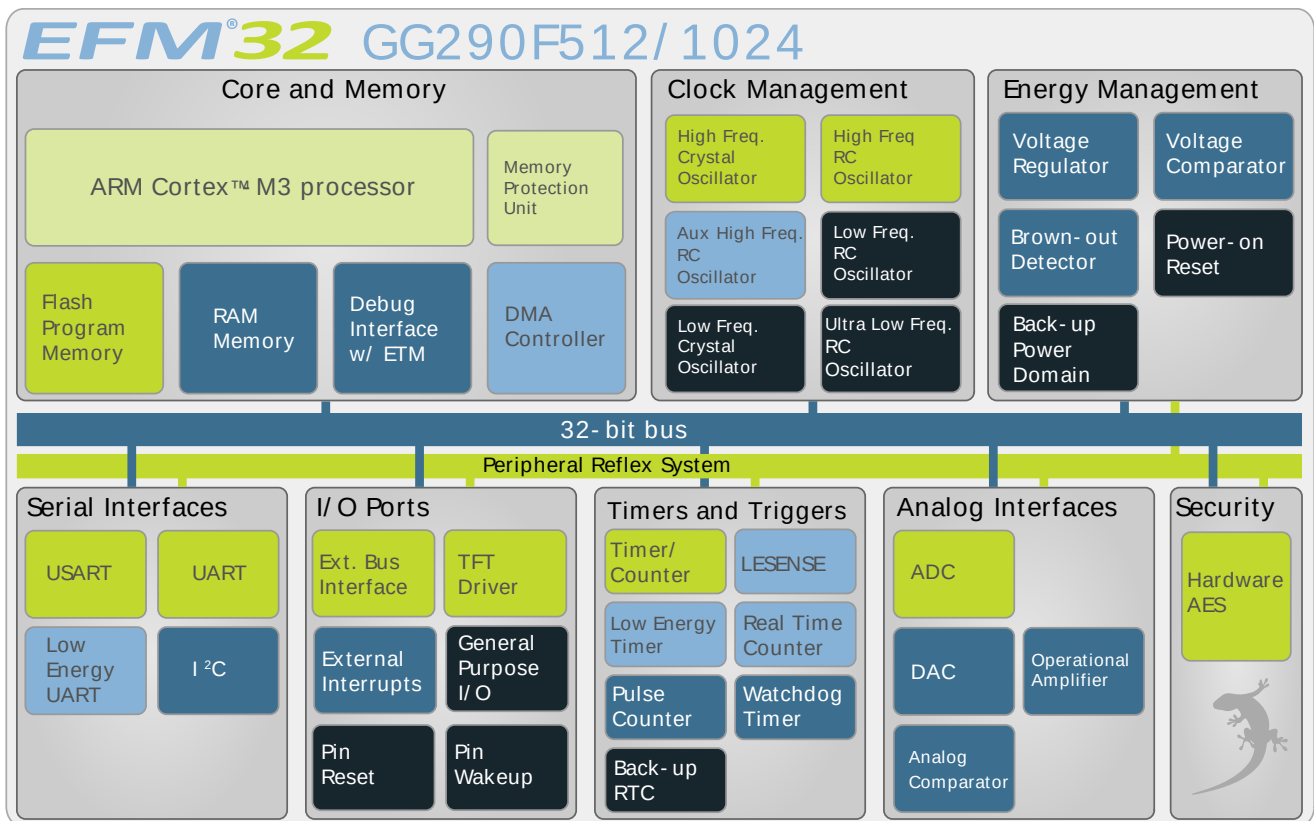
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG290 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG290 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32GG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32GG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32GG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32GG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In

that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

2.1.12 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.13 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.14 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.15 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.16 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.17 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.18 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.19 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.20 Low Energy Timer (LETIMER)

The unique LETIMER[™], the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.21 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.22 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.23 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.24 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.25 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.26 Operational Amplifier (OPAMP)

The EFM32GG290 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.27 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE[™]), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable

FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.28 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG290 to keep track of time and retain data, even if the main power source should drain out.

2.1.29 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.30 General Purpose Input/Output (GPIO)

In the EFM32GG290, there are 90 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.2 Configuration Summary

The features of the EFM32GG290 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

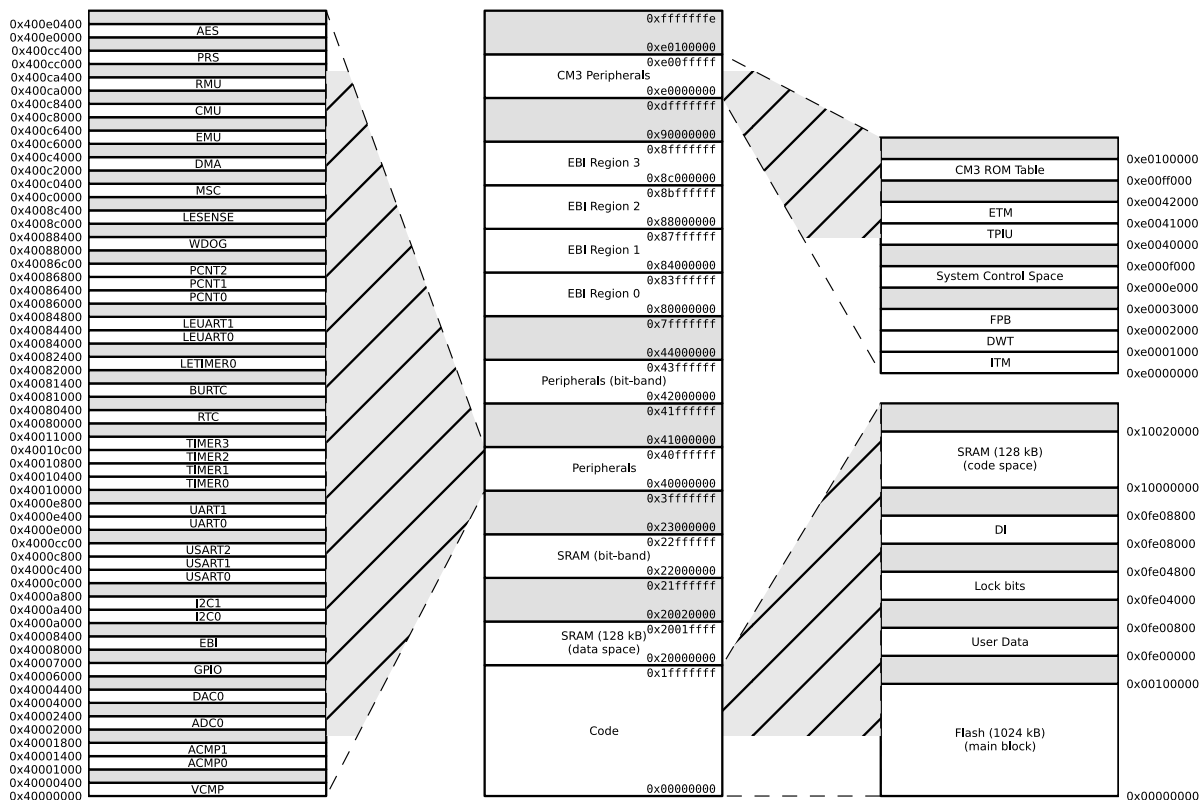
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0],

Module	Configuration	Pin Connections
		EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNc, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNc, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 62)

2.3 Memory Map

The *EFM32GG290* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32GG290 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150°C . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			48	MHz
f_{AHB}	Internal AHB clock frequency			48	MHz

3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ESDHBM}	ESD (Human Body Model HBM)	T _{AMB} =25°C			500	V
V _{ESDCDM}	ESD (Charged Device Model, CDM)	T _{AMB} =25°C			500	V

Latch-up sensitivity passed: $\pm 100 \text{ mA}/1.5 \times V_{\text{SUPPLY}}(\text{max})$ according to JEDEC JESD 78 method Class II, 85°C, except pin PD14: +100 mA/-65 mA.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from flash. (Production test condition = 14MHz)	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		219	240	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		214	261	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		220	263	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		223	270	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		225	273	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		230	282	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		283	338	$\mu\text{A}/\text{MHz}$
I_{EM1}	EM1 current (Production test condition = 14MHz)	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		80	90	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		80	90	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		81	91	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		83	99	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		85	100	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		90	102	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		122	152	$\mu\text{A}/\text{MHz}$
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		1.1 ¹	1.8 ¹	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		6.0 ¹	10.0 ¹	μA
I_{EM3}	EM3 current	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.8 ¹	1.3 ¹	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		5.8 ¹	9.8 ¹	μA
I_{EM4}	EM4 current	$V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		0.02	0.055	μA
		$V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$		0.5	0.9	μA

¹ Only one RAM block enabled.

3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.5. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μ s
t_{EM30}	Transition time from EM3 to EM0		2		μ s
t_{EM40}	Transition time from EM4 to EM0		163		μ s

3.6 Power Management

The EFM32GG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODintthr-}$	BOD threshold on falling internally regulated supply voltage		1.57		1.70	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μ s
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μ F

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			µs
t _{PERASE}	Page erase time	LPERASE == 0	20	20.4	20.8	ms
		LPERASE == 1	40	40.4	40.8	ms
t _{DERASE}	Device erase time				161.6	ms
I _{ERASE}	Erase current	LPERASE == 0			14 ¹	mA
		LPERASE == 1			7 ¹	mA
I _{WRITE}	Write current	LPWRITE == 0			14 ¹	mA
		LPWRITE == 1			7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹Measured at 25°C

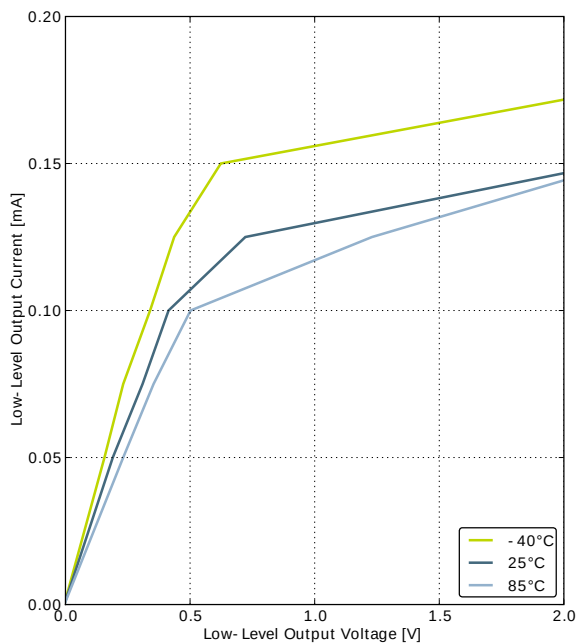
3.8 General Purpose Input Output

Table 3.8. GPIO

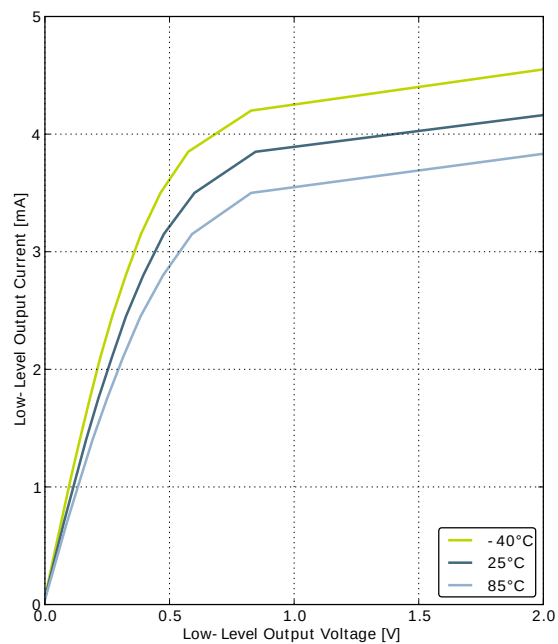
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60V_{DD}$			V
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80V_{DD}$			V
V_{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.20V_{DD}$		V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOWEST		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.10V_{DD}$		V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW		$0.05V_{DD}$		V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.30V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD			$0.20V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.35V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH			$0.20V_{DD}$	V
I_{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V_{DD}		± 0.1	± 100	nA
R_{PU}	I/O pin pull-up resistor			40		kOhm
R_{PD}	I/O pin pull-down resistor			40		kOhm
R_{IOESD}	Internal ESD series resistor			200		Ohm
$t_{IOGLITCH}$	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t_{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L=12.5-25$ pF.	$20+0.1C_L$		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600$ pF	$20+0.1C_L$		250	ns
V_{IOHYST}	I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$)	$V_{DD} = 1.98 - 3.8$ V	$0.10V_{DD}$			V

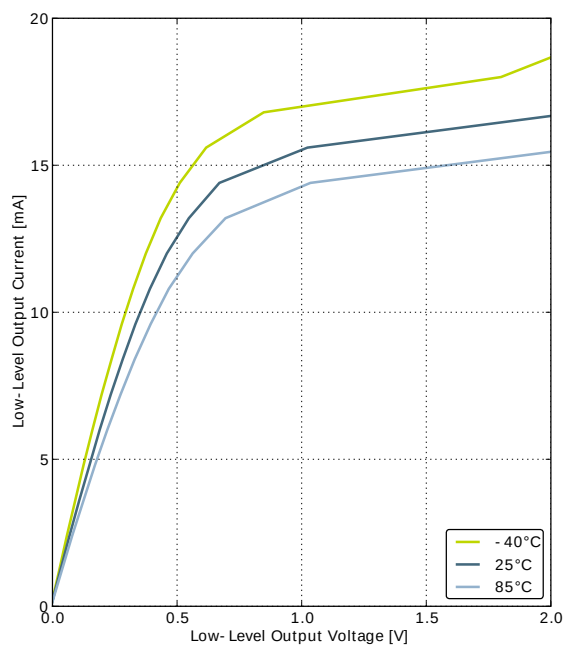
Figure 3.1. Typical Low-Level Output Current, 2V Supply Voltage



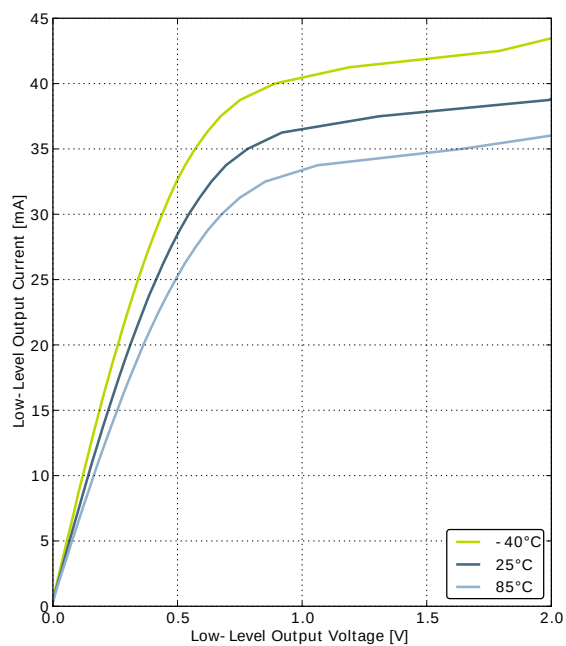
GPIO_Px_CTRL DRIVEMODE = LOWEST



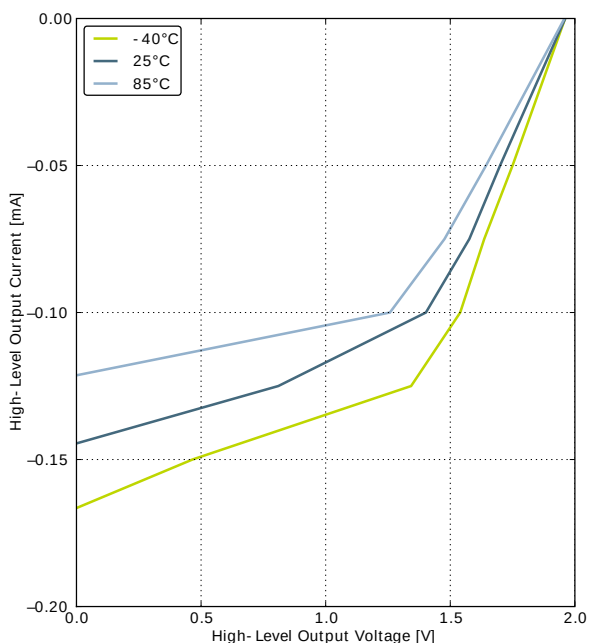
GPIO_Px_CTRL DRIVEMODE = LOW



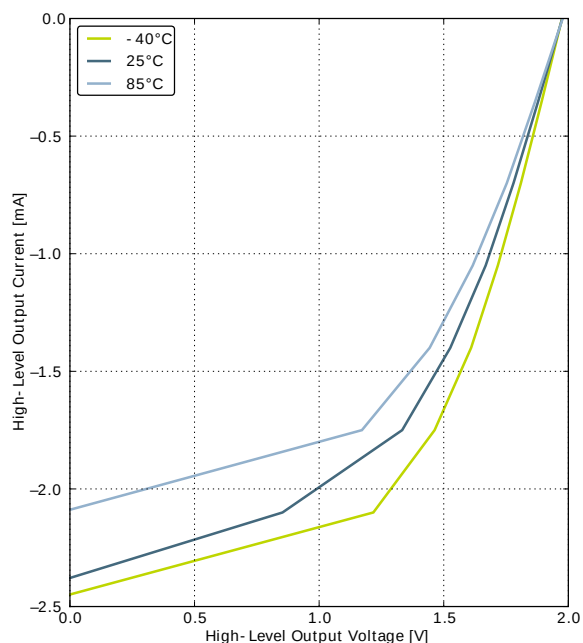
GPIO_Px_CTRL DRIVEMODE = STANDARD



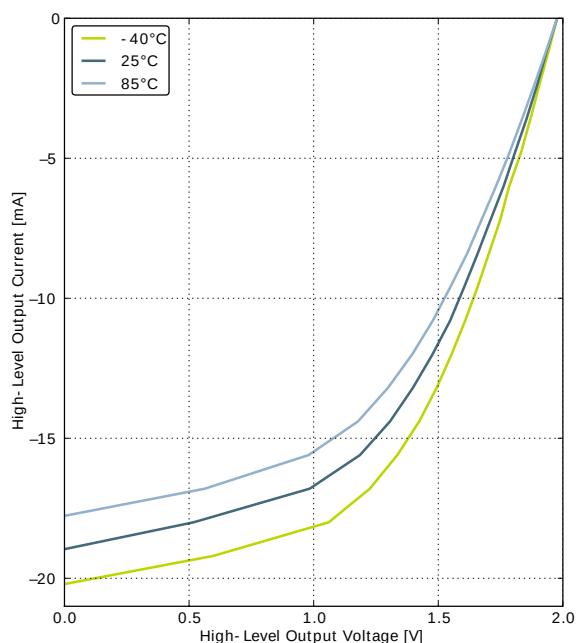
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.2. Typical High-Level Output Current, 2V Supply Voltage

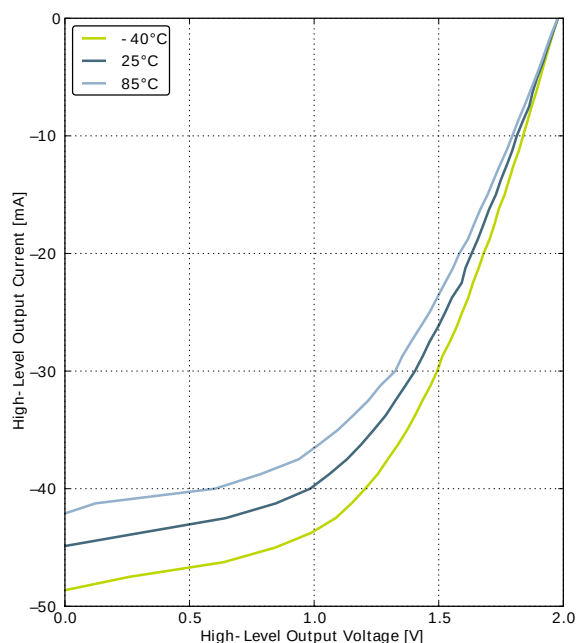
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

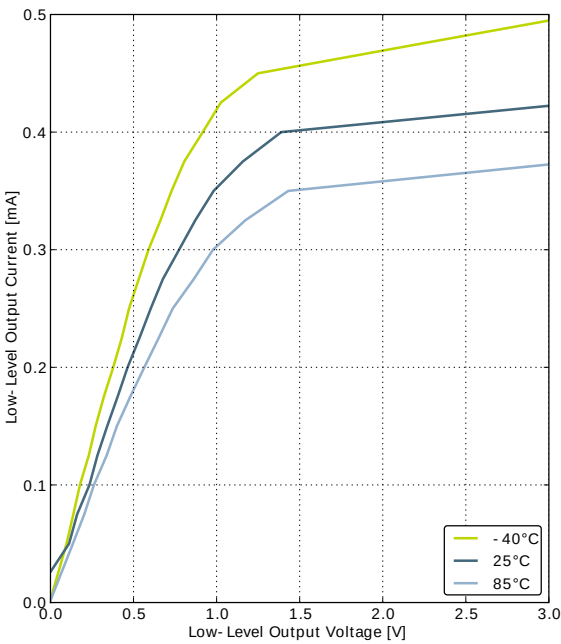


GPIO_Px_CTRL DRIVEMODE = STANDARD

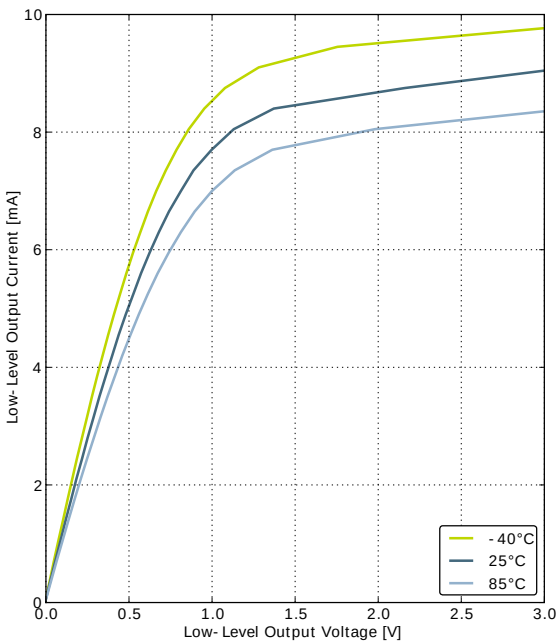


GPIO_Px_CTRL DRIVEMODE = HIGH

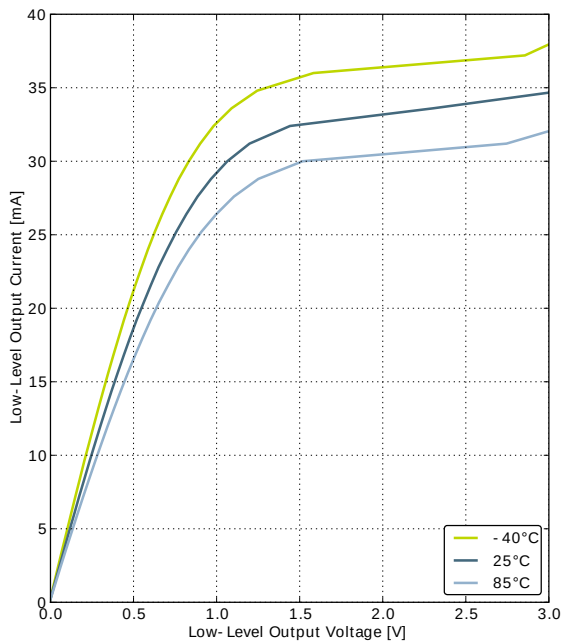
Figure 3.3. Typical Low-Level Output Current, 3V Supply Voltage



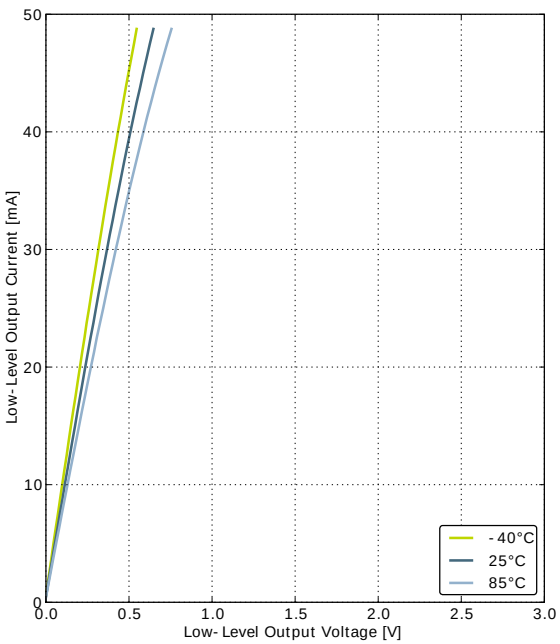
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

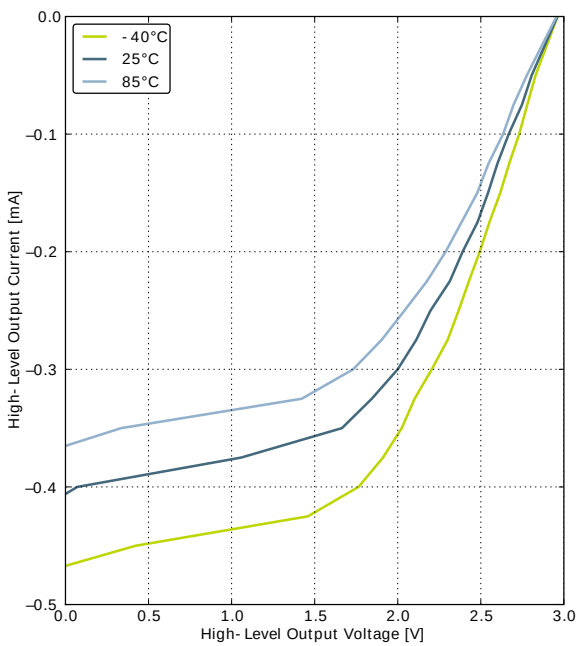


GPIO_Px_CTRL DRIVEMODE = STANDARD

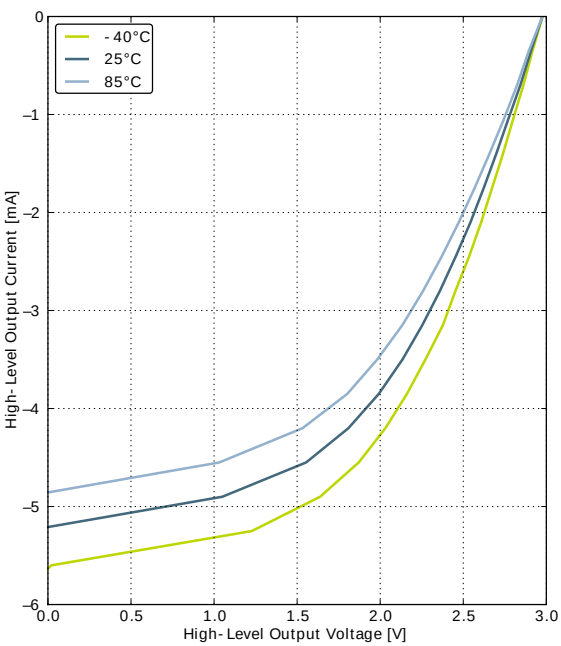


GPIO_Px_CTRL DRIVEMODE = HIGH

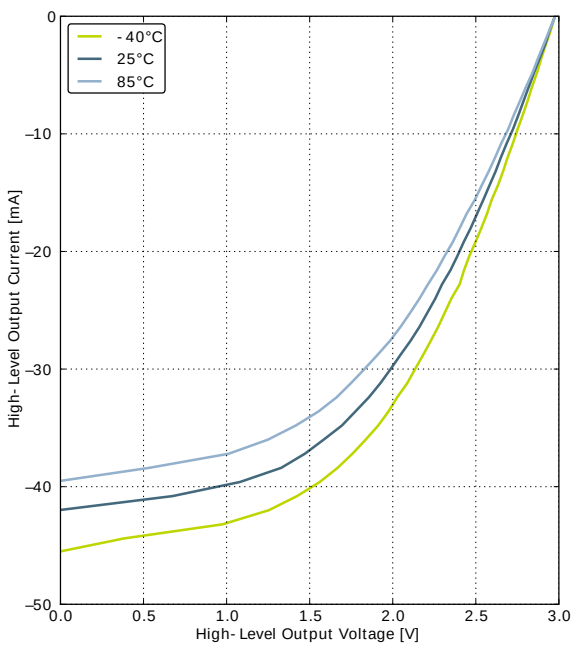
Figure 3.4. Typical High-Level Output Current, 3V Supply Voltage



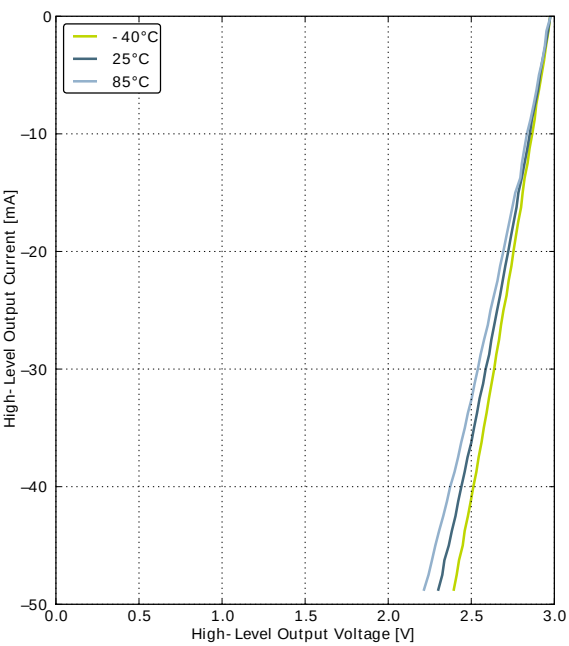
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

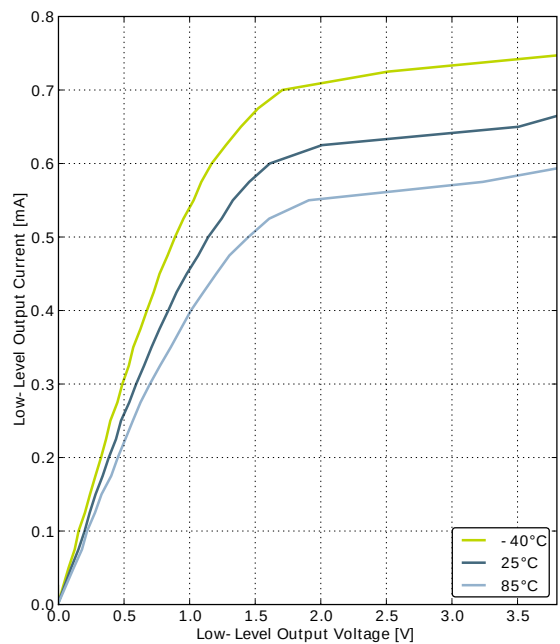


GPIO_Px_CTRL DRIVEMODE = STANDARD

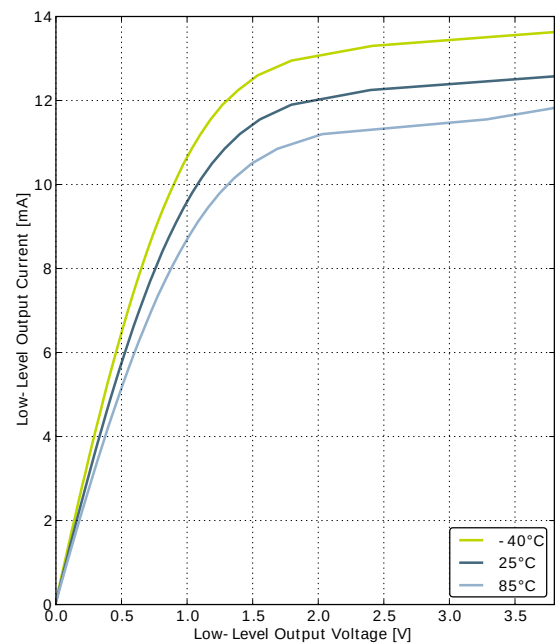


GPIO_Px_CTRL DRIVEMODE = HIGH

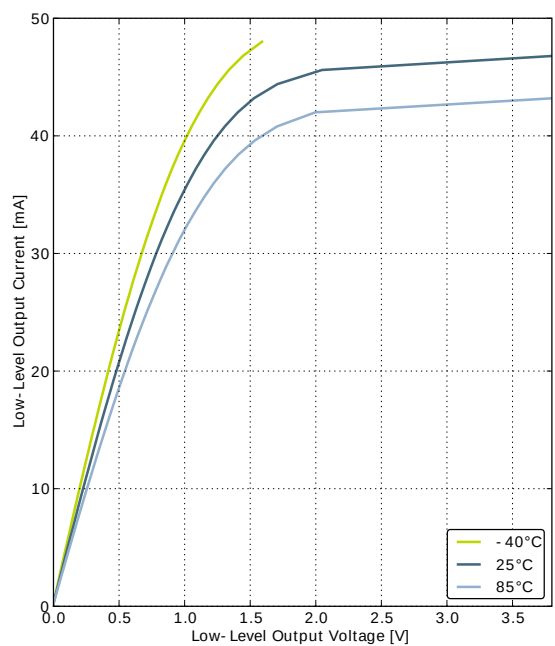
Figure 3.5. Typical Low-Level Output Current, 3.8V Supply Voltage



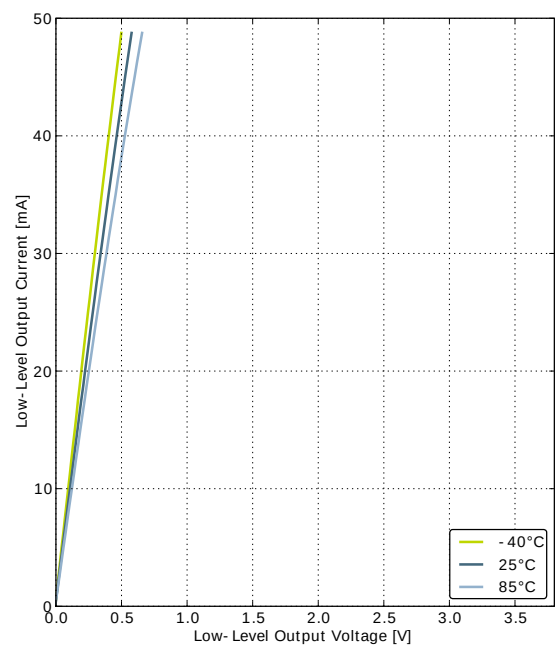
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

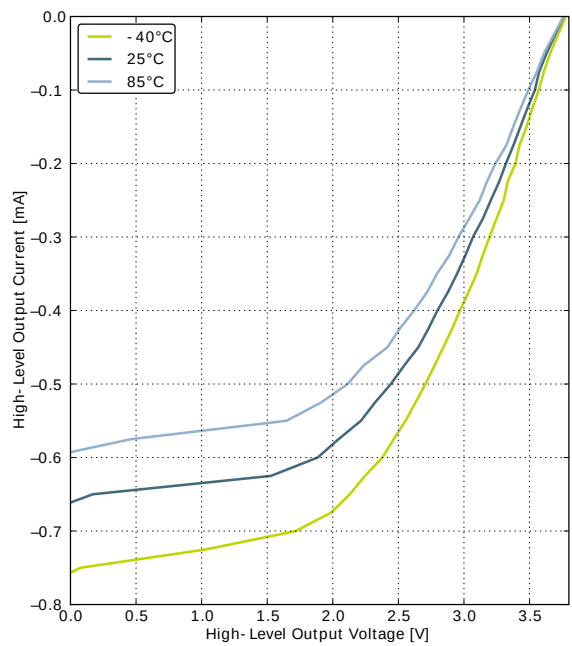


GPIO_Px_CTRL DRIVEMODE = STANDARD

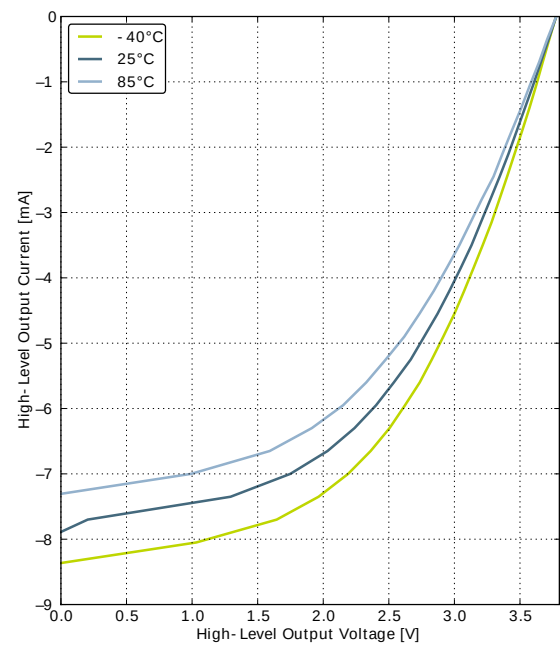


GPIO_Px_CTRL DRIVEMODE = HIGH

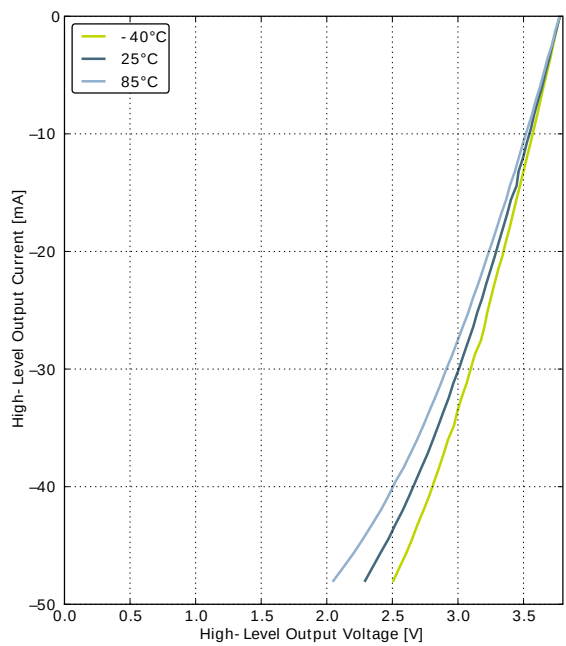
Figure 3.6. Typical High-Level Output Current, 3.8V Supply Voltage



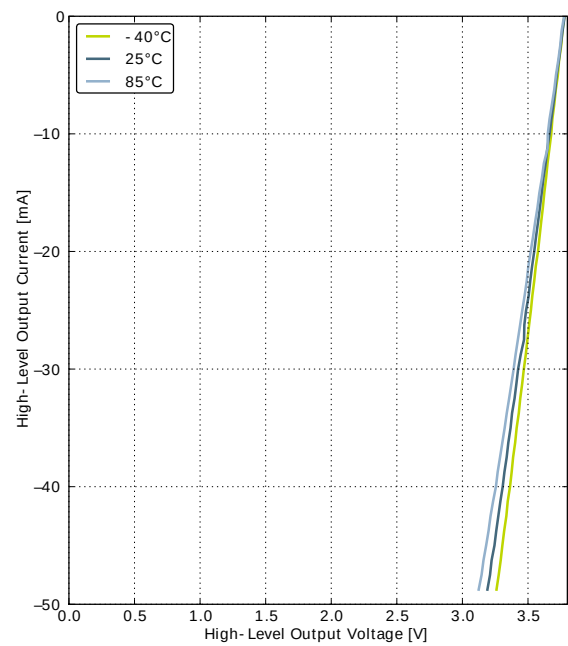
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		$\times^1$		25	pF
DC_{LFXO}	Duty cycle		48	50	53.5	%
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

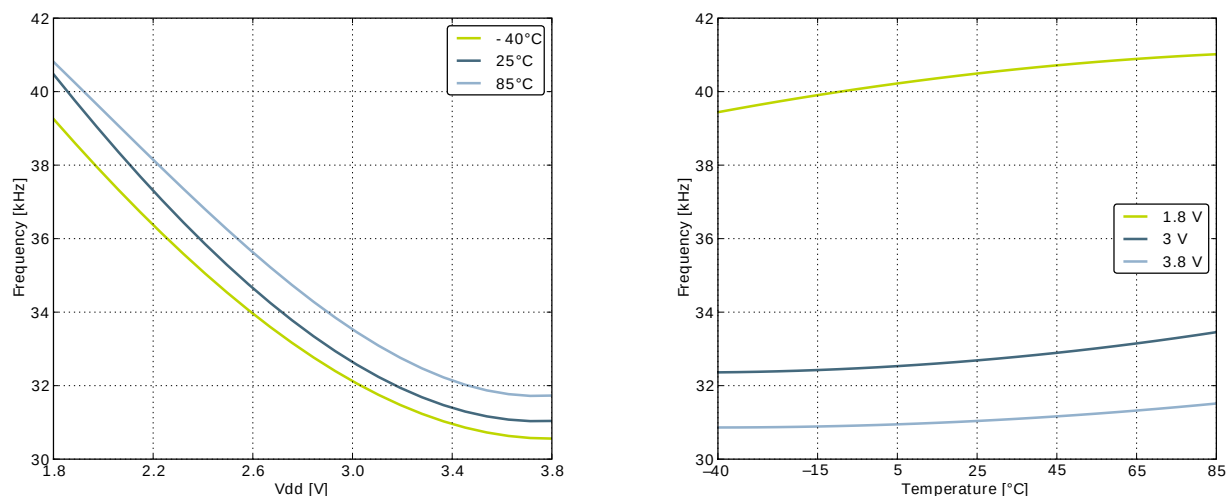
Table 3.10. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
DC_{HFXO}	Duty cycle		46	50	54	%
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, $C_L=20$ pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
		32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs

3.9.3 LFRCO

Table 3.11. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{\text{DD}}=3.0\text{ V}$, $T_{\text{AMB}}=25^\circ\text{C}$		31.29	32.768	34.28	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			300		nA
$\text{TUNESTEP}_{\text{LFRCO}}$	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.7. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

3.9.4 HFRCO

Table 3.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
$t_{\text{HFRCO_settling}}$	Settling time after start-up	$f_{\text{HFRCO}} = 14 \text{ MHz}$		0.6		Cycles
I_{HFRCO}	Current consumption (Production test condition = 14MHz)	$f_{\text{HFRCO}} = 28 \text{ MHz}$		165	190	μA
		$f_{\text{HFRCO}} = 21 \text{ MHz}$		134	155	μA
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		106	120	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		77	90	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		25	32	μA
DC_{HFRCO}	Duty cycle	$f_{\text{HFRCO}} = 14 \text{ MHz}$	48.5	50	51	%
$\text{TUNESTEP}_{\text{HFRCO}}$	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

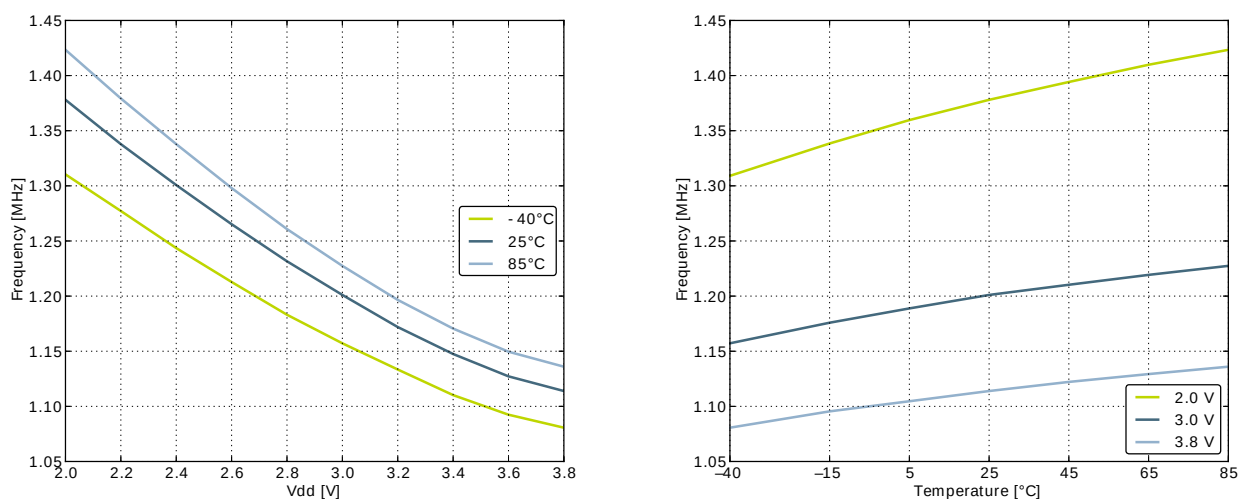
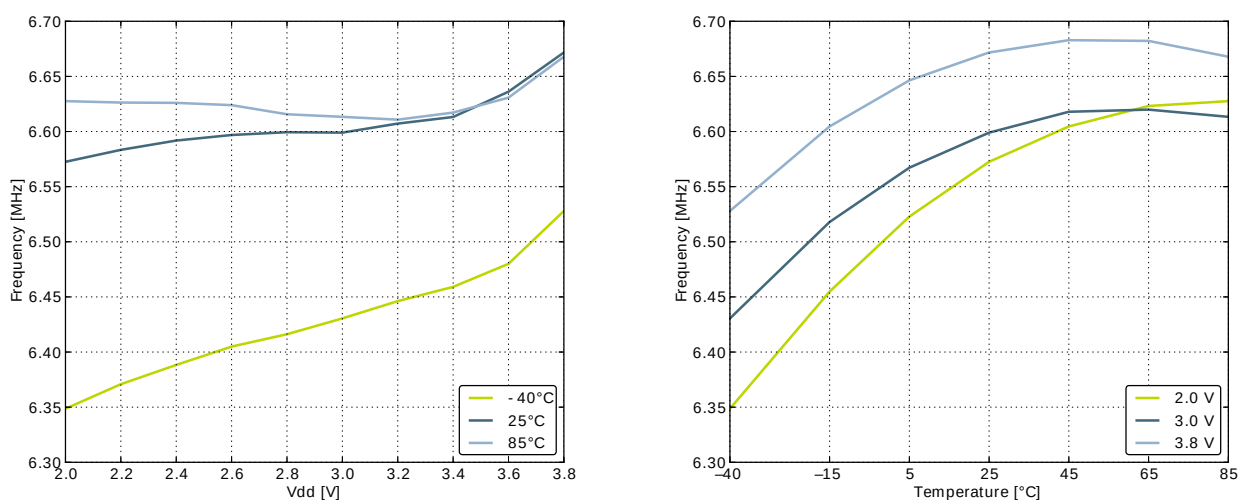
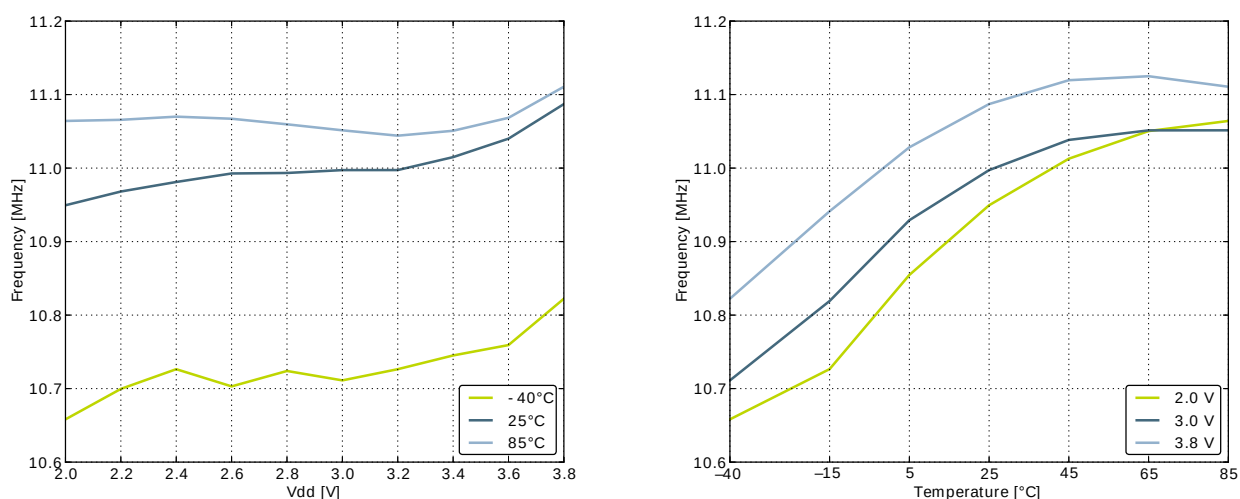
Figure 3.8. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.9. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.10. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**

Figure 3.11. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

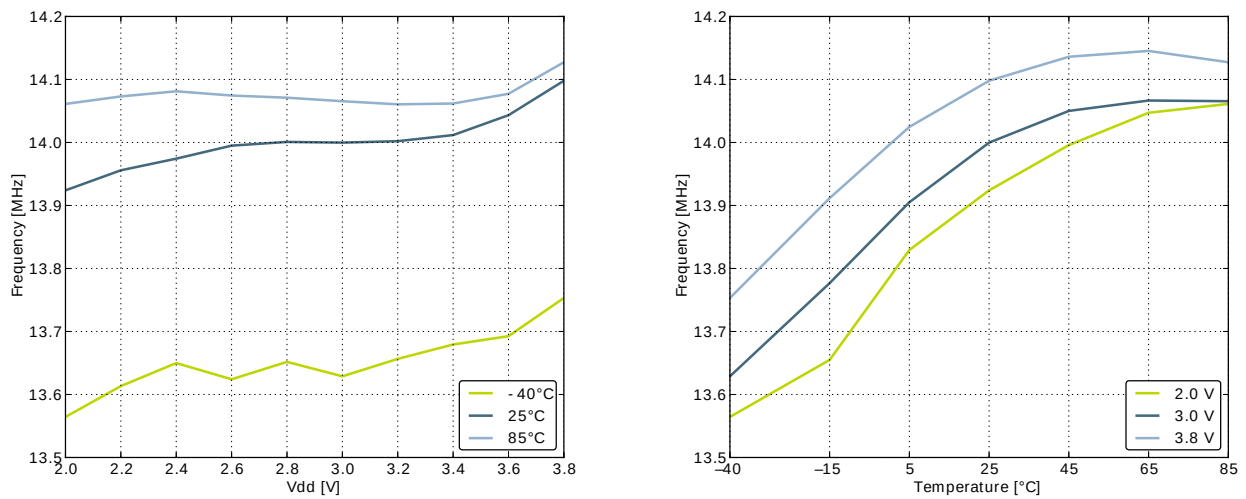


Figure 3.12. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

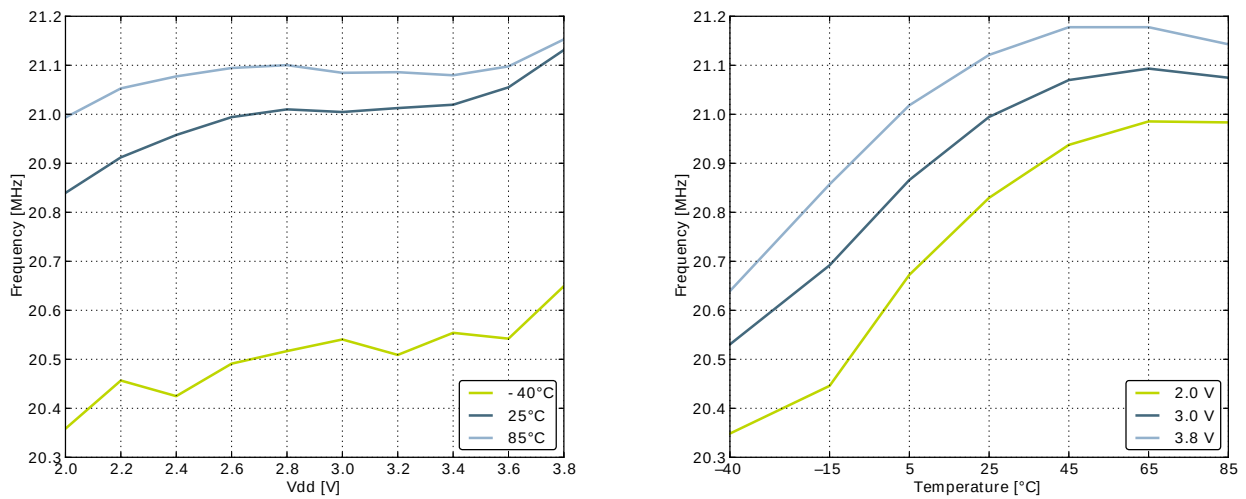
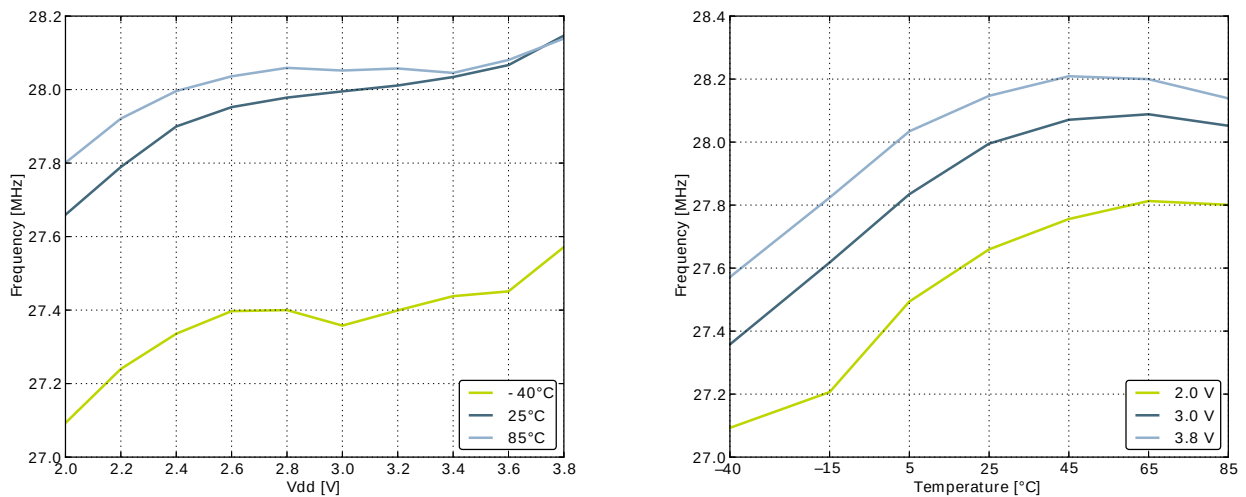


Figure 3.13. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.13. AUXHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{AUXHFRCO}	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$, $T_{\text{AMB}} = 25^\circ\text{C}$	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
$t_{\text{AUXHFRCO_settling}}$	Settling time after start-up	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$		0.6		Cycles
$\text{DC}_{\text{AUXHFRCO}}$	Duty cycle	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$	48.5	50	51	%
$\text{TUNESTEP}_{\text{AUXHFRCO}}$	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_AUXHFRCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

3.9.6 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
$\text{TC}_{\text{ULFRCO}}$	Temperature coefficient			0.05		%/°C
$\text{VC}_{\text{ULFRCO}}$	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{\text{REF}}/2$		$V_{\text{REF}}/2$	V
$V_{\text{ADCCREFIN}}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{\text{ADCCREFIN_CH7}}$	Input range of external negative reference voltage on channel 7	See $V_{\text{ADCCREFIN}}$	0		$V_{\text{DD}} - 1.1$	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ADCREFIN_CH6}	Input range of external positive reference voltage on channel 6	See V _{ADCREFIN}	0.625		V _{DD}	V
V _{ADCCMIN}	Common mode input range		0		V _{DD}	V
I _{ADCIN}	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input common mode rejection ratio			65		dB
I _{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
I _{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MΩ
R _{ADCFLT}	Input RC filter resistance			10		kΩ
C _{ADCFLT}	Input RC filter/de-coupling capacitance			250		fF
f _{ADCCLK}	ADC Clock Frequency				13	MHz
t _{ADCCONV}	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t _{ADCAcq}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
t _{ADCAcqVDD3}	Required acquisition time for VDD/3 reference		2			μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ADCSTART}	Startup time of reference generator and ADC core in NORMAL mode			5		μs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference		70		dB
$\text{SINAD}_{\text{ADC}}$	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	65		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc

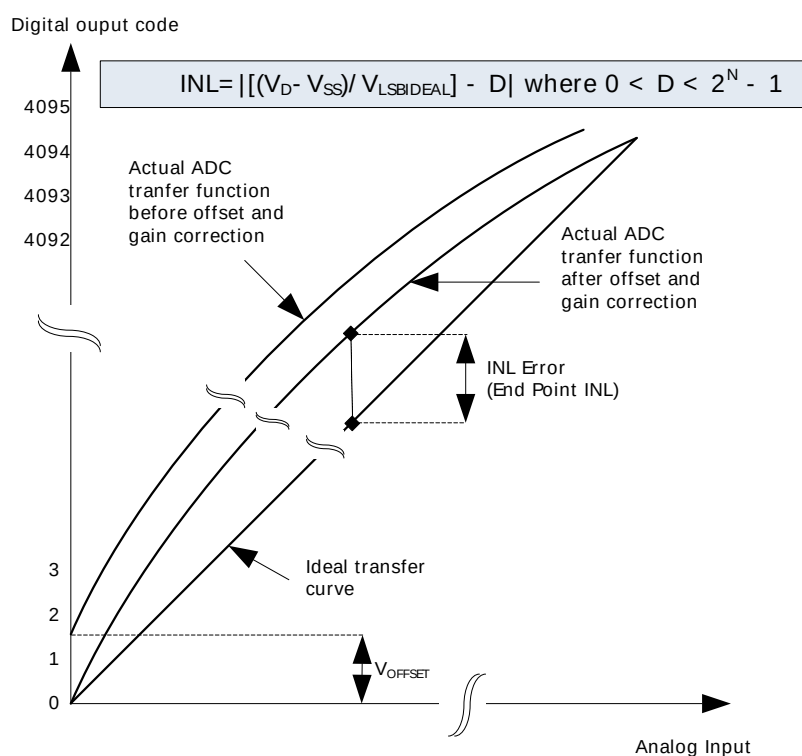
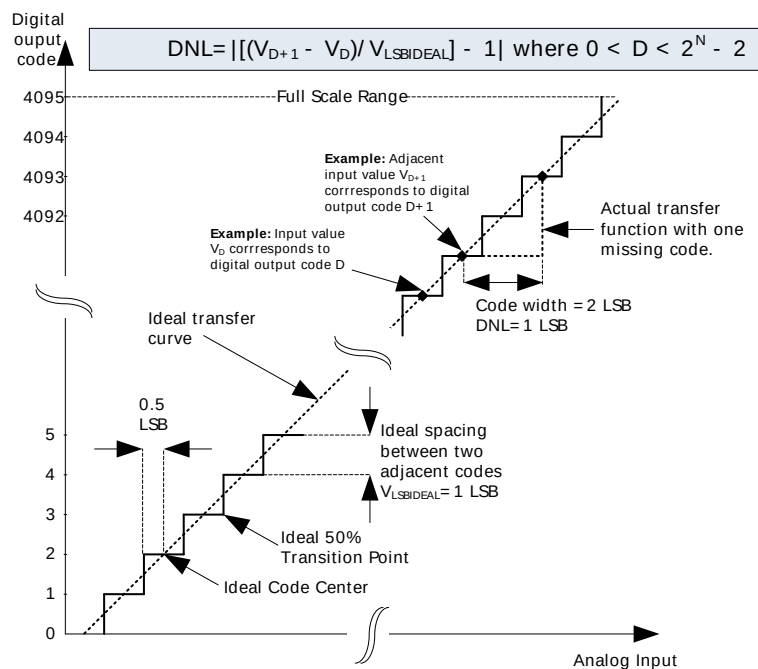
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended		0.3		mV
		After calibration, differential	-3	0.3	3	mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)		-1	± 0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method			± 1.2	± 3.0	LSB
MC_{ADC}	No missing codes		11.999 ¹	12		bits
$GAIN_{ED}$	Gain error drift	1.25V reference		0.01 ²	0.033 ³	%/°C
		2.5V reference		0.01 ²	0.03 ³	%/°C
$OFFSET_{ED}$	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
		2.5V reference		0.2 ²	0.62 ³	LSB/°C

¹On the average every ADC will have one missing code, most likely to appear around $2048 \pm n \times 512$ where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

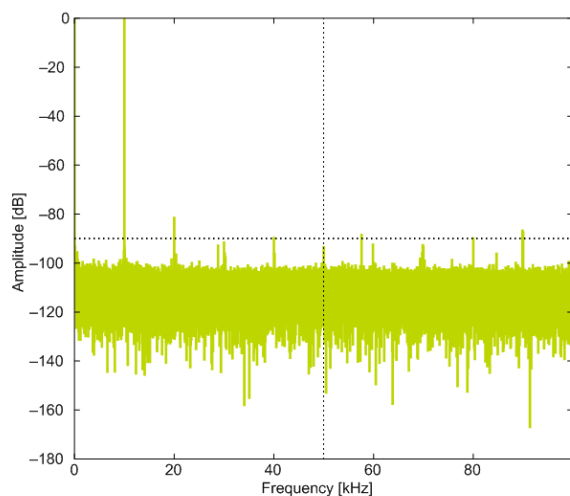
³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.14 (p. 32) and Figure 3.15 (p. 32), respectively.

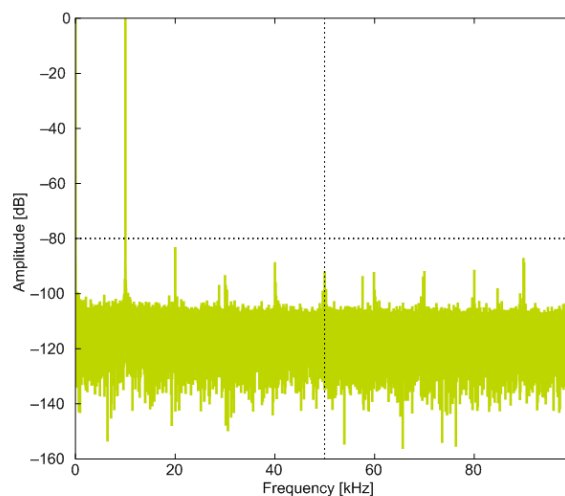
Figure 3.14. Integral Non-Linearity (INL)**Figure 3.15. Differential Non-Linearity (DNL)**

3.10.1 Typical performance

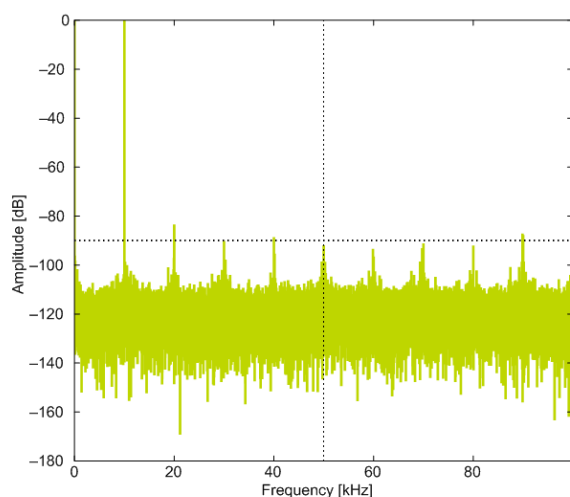
Figure 3.16. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



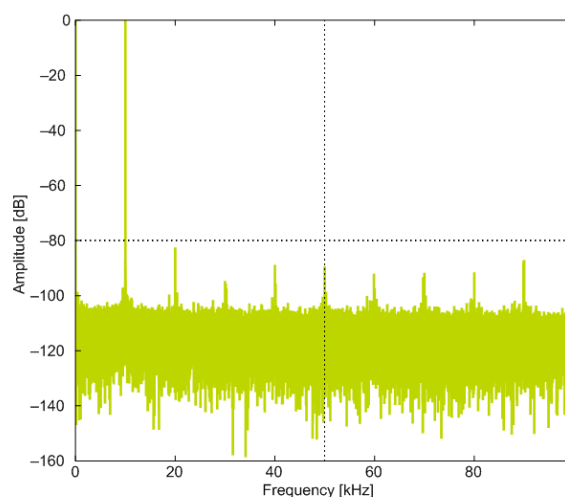
1.25V Reference



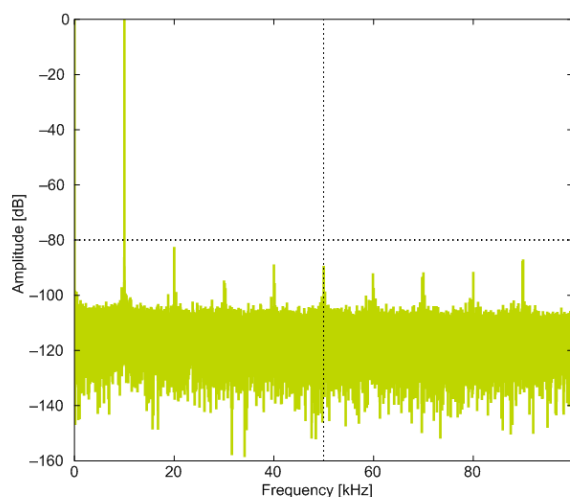
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

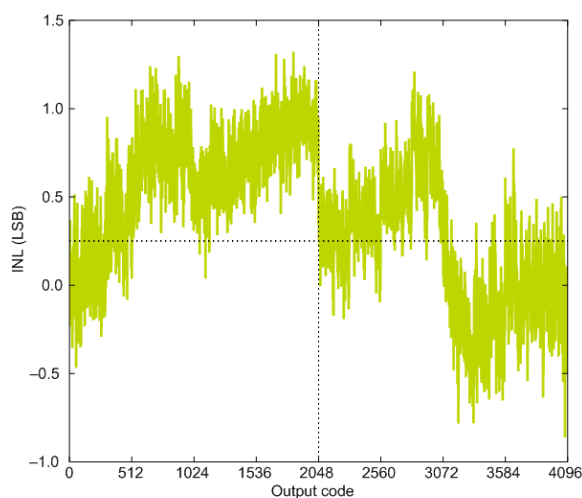
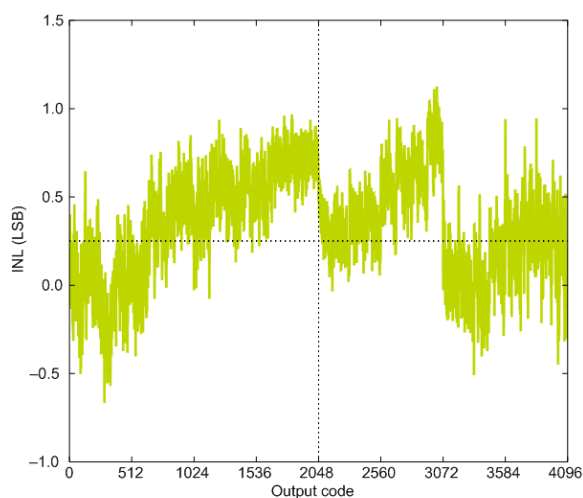
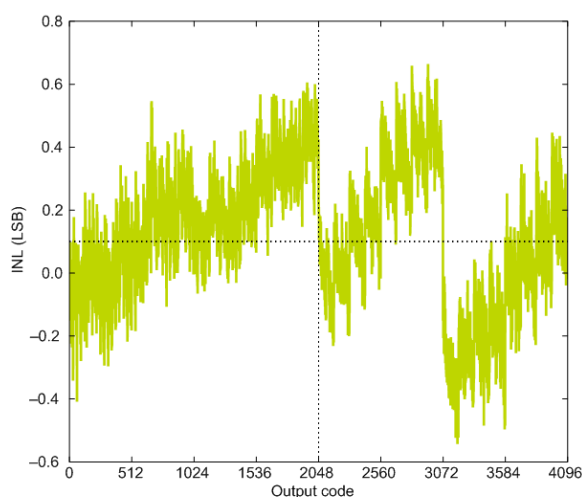
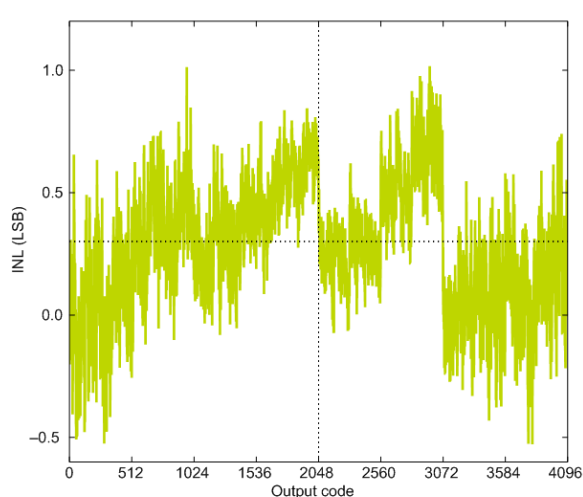
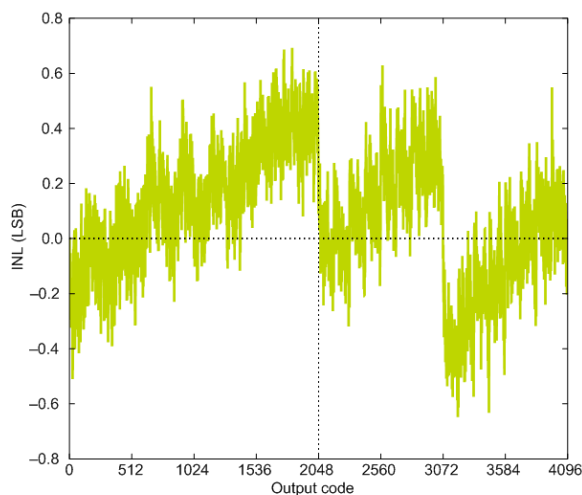
Figure 3.17. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

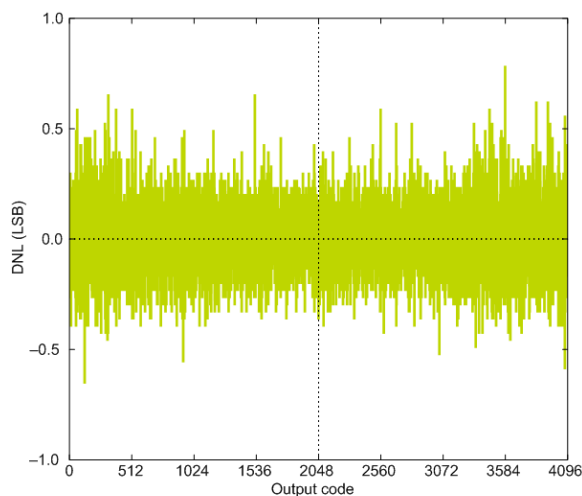
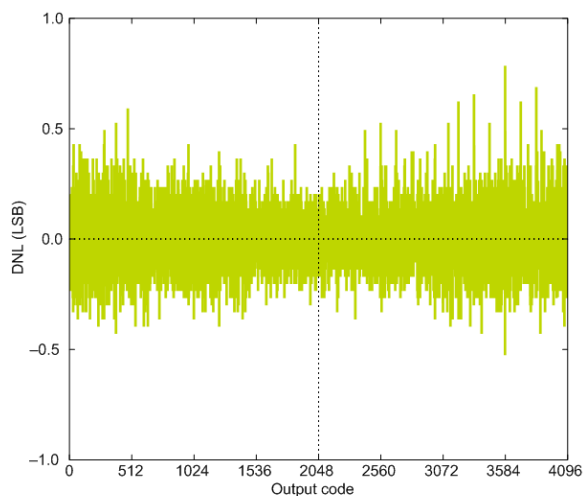
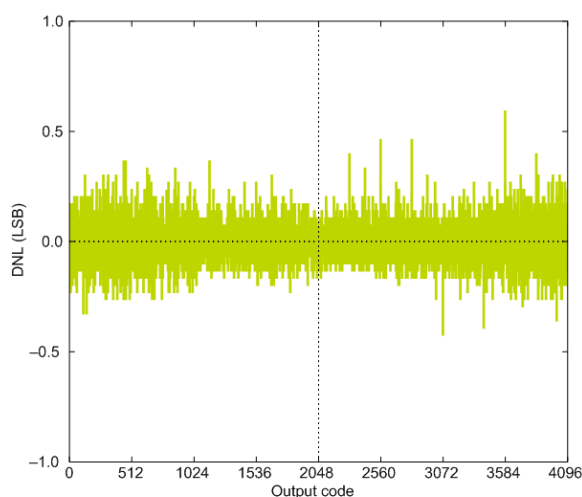
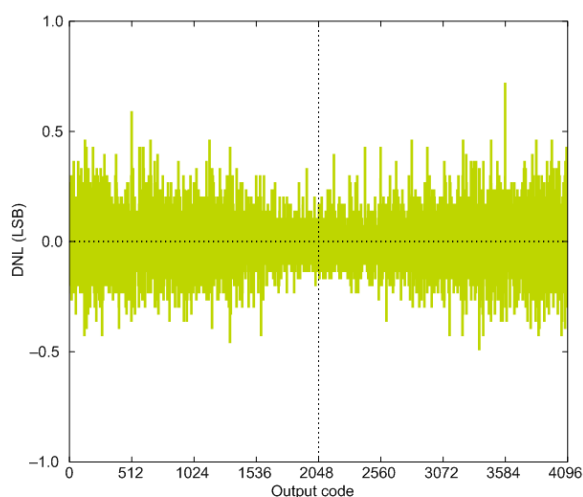
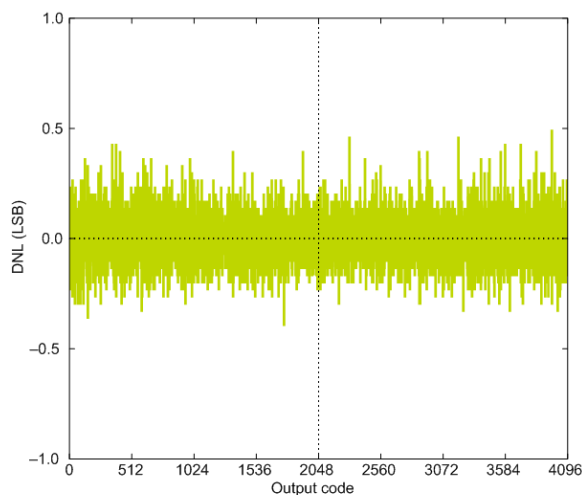
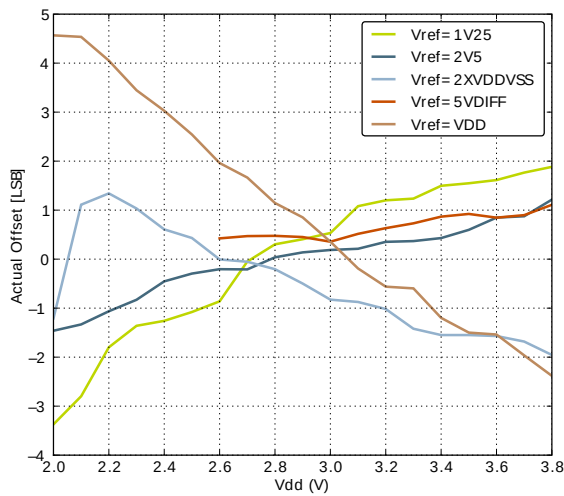
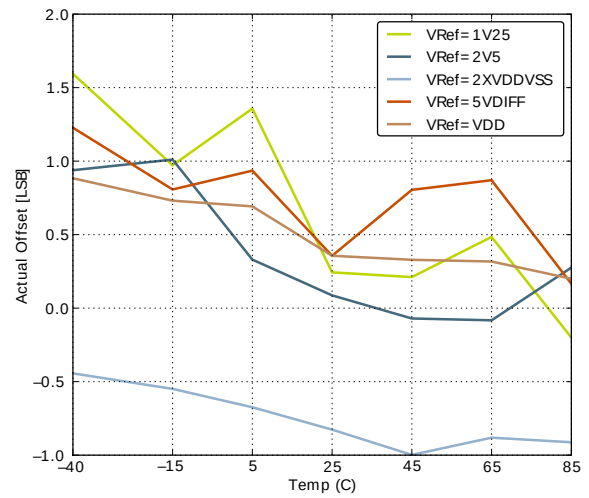
Figure 3.18. ADC Differential Linearity Error vs Code, V_{dd} = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Figure 3.19. ADC Absolute Offset, Common Mode = $V_{dd}/2$

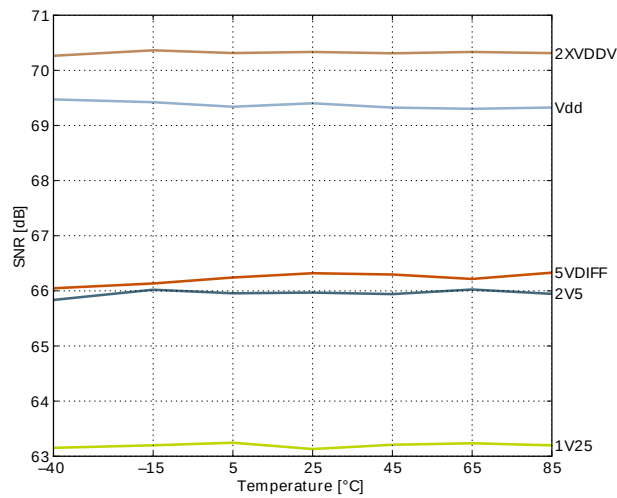


Offset vs Supply Voltage, Temp = 25°C

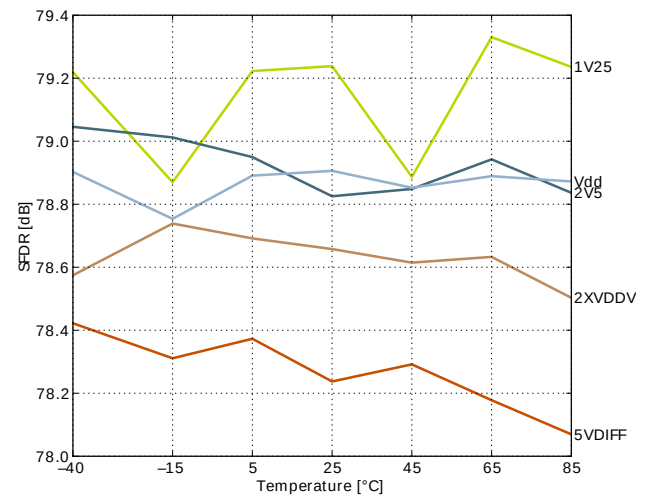


Offset vs Temperature, $V_{dd} = 3V$

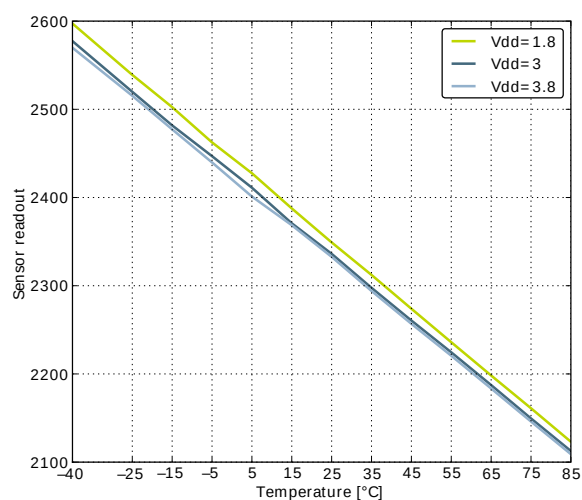
Figure 3.20. ADC Dynamic Performance vs Temperature for all ADC References, $V_{dd} = 3V$



Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

Figure 3.21. ADC Temperature sensor readout

3.11 Digital Analog Converter (DAC)

Table 3.16. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12 bit		400 ¹		μA
		100 kSamples/s, 12 bit		200 ¹		μA
		1 kSamples/s 12 bit NORMAL		17 ¹		μA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	Conversion time		2			μs
$t_{DACSETTLE}$	Settling time			5		μs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
SNDR _{DAC}	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
SFDR _{DAC}	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
V _{DACOFFSET}	Offset voltage	After calibration, single ended		2	9	mV
		After calibration, differential		2		mV
DNL _{DAC}	Differential non-linearity			±1		LSB
INL _{DAC}	Integral non-linearity			±5		LSB
MC _{DAC}	No missing codes			12		bits

¹ Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.17. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		350	405	μA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	115	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	17	μA
G _{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW _{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM _{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C _L =75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance		200			Ohm
I _{LOAD_DC}	DC Load Current				11	mA
V _{INPUT}	Input Voltage	OPAxHCMDIS=0	V _{SS}		V _{DD}	V
		OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
V _{OFFSET}	Input Offset Voltage	Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR _{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/μs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/μs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=1		141		μV _{RMS}

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		196		μV_{RMS}
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		229		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=0		1230		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=1		2130		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		1630		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		2590		μV_{RMS}

Figure 3.22. OPAMP Common Mode Rejection Ratio

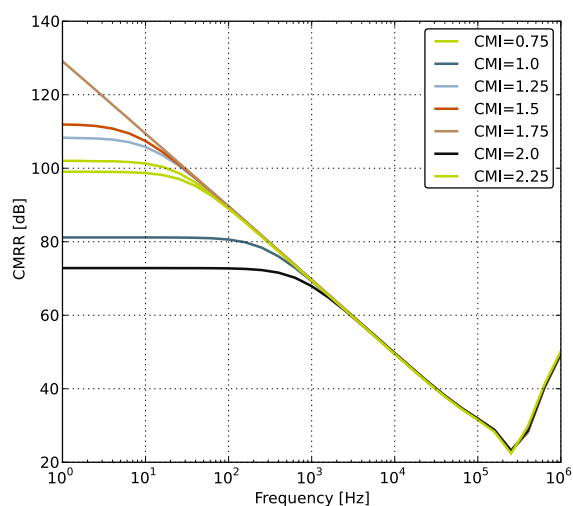


Figure 3.23. OPAMP Positive Power Supply Rejection Ratio

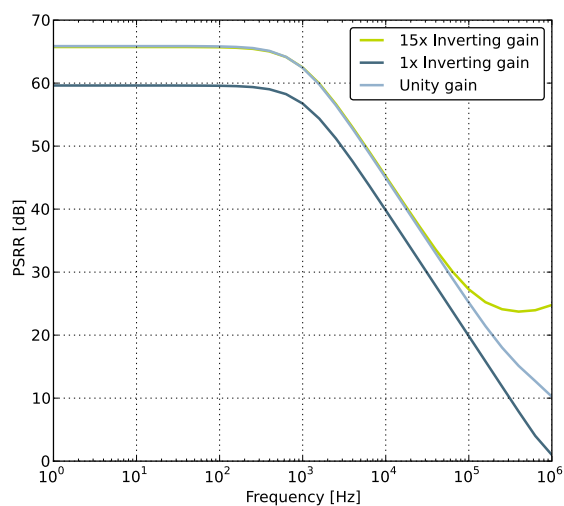
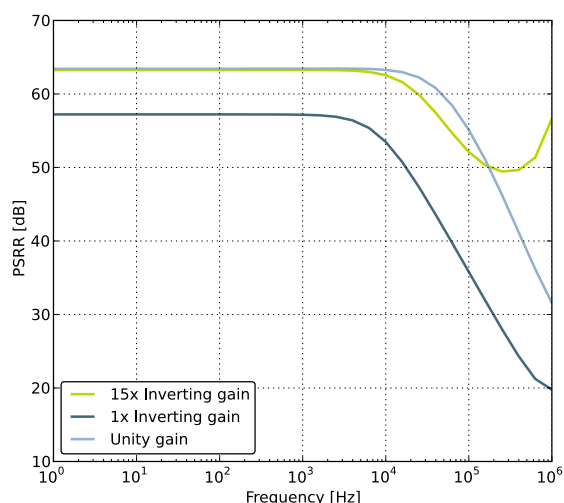
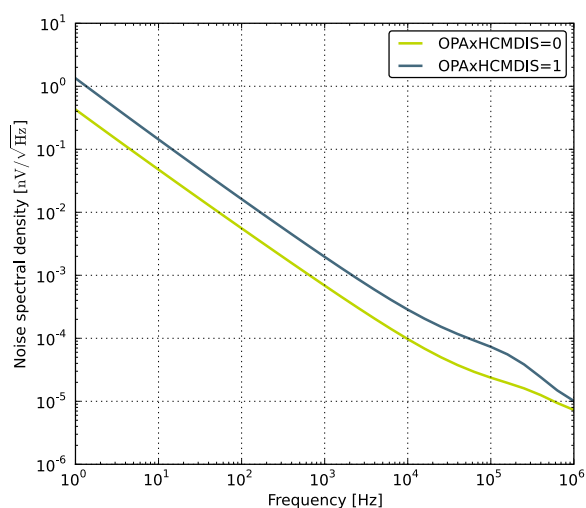
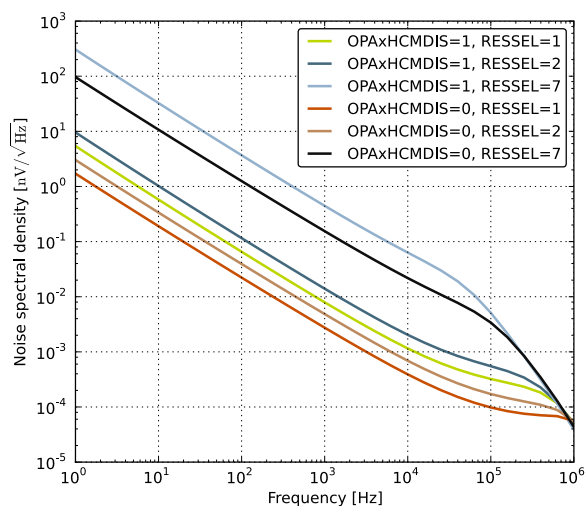


Figure 3.24. OPAMP Negative Power Supply Rejection Ratio**Figure 3.25. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}=1V$** **Figure 3.26. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)**

3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

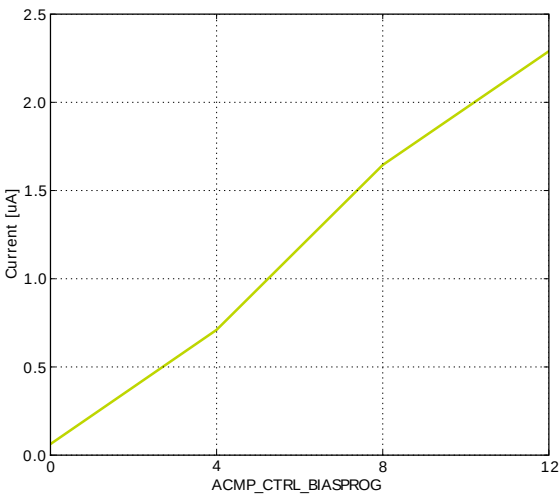
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 42) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

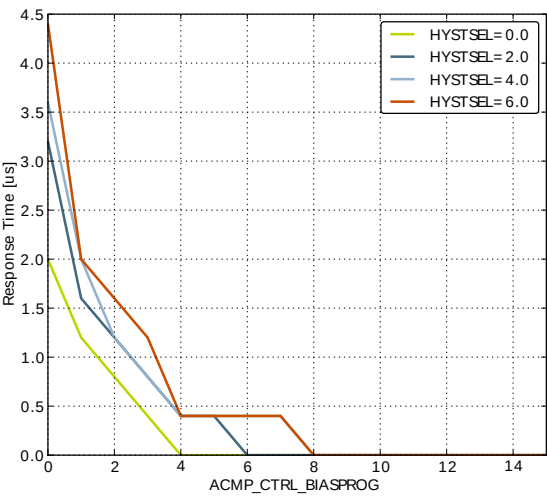
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

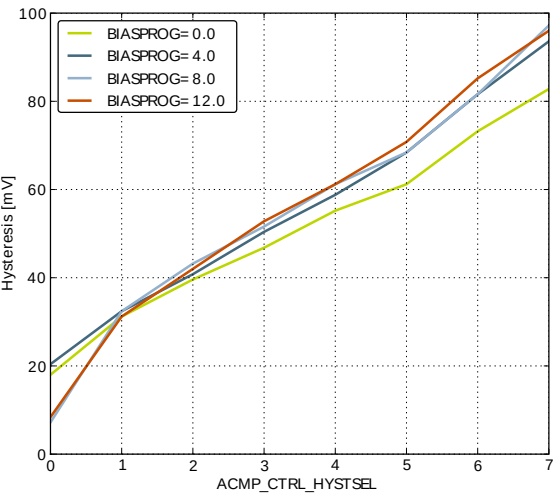
Figure 3.27. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

3.14 Voltage Comparator (VCMP)

Table 3.19. VCMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMPCM}	VCMP Common Mode voltage range			V _{DD}		V
I _{VCMP}	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	μA
t _{VCMPREF}	Startup time reference generator	NORMAL		10		μs
V _{VCMPOFFSET}	Offset voltage	Single ended		10		mV
		Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			61	210	mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

3.15 EBI

Figure 3.28. EBI Write Enable Timing

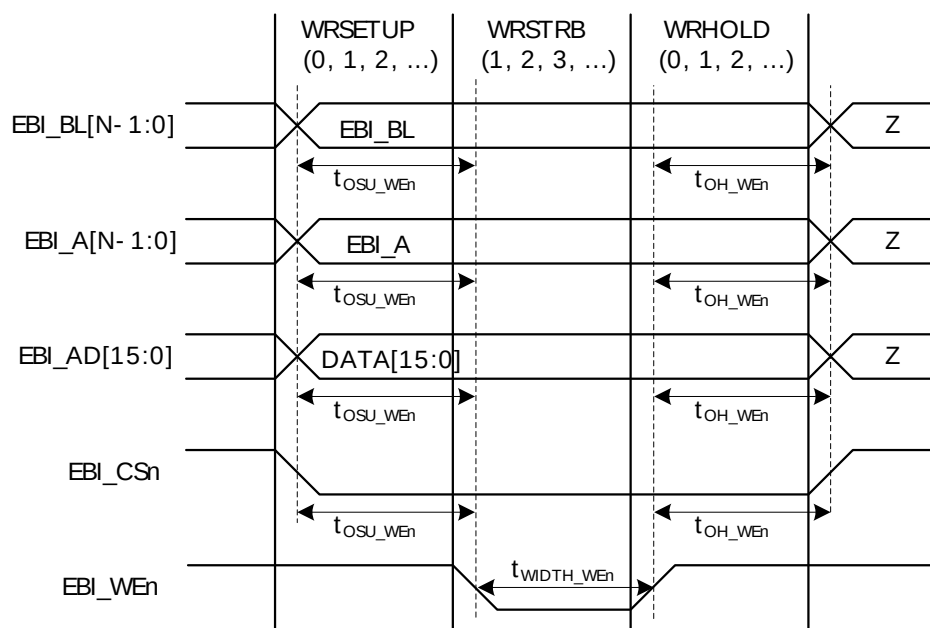


Table 3.20. EBI Write Enable Timing

Symbol	Parameter	Min	Typ	Max	Unit
$t_{OH_WEn}^{1\ 2\ 3\ 4}$	Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	$-6.00 + (WRHOLD * t_{HFCORECLK})$			ns
$t_{OSU_WEn}^{1\ 2\ 3\ 4\ 5}$	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge	$-14.00 + (WRSETUP * t_{HFCORECLK})$			ns
$t_{WIDTH_WEn}^{1\ 2\ 3\ 4\ 5}$	EBI_WEn/EBI_NANDWEn pulse width	$-7.00 + ((WRSTRB + 1) * t_{HFCORECLK})$			ns

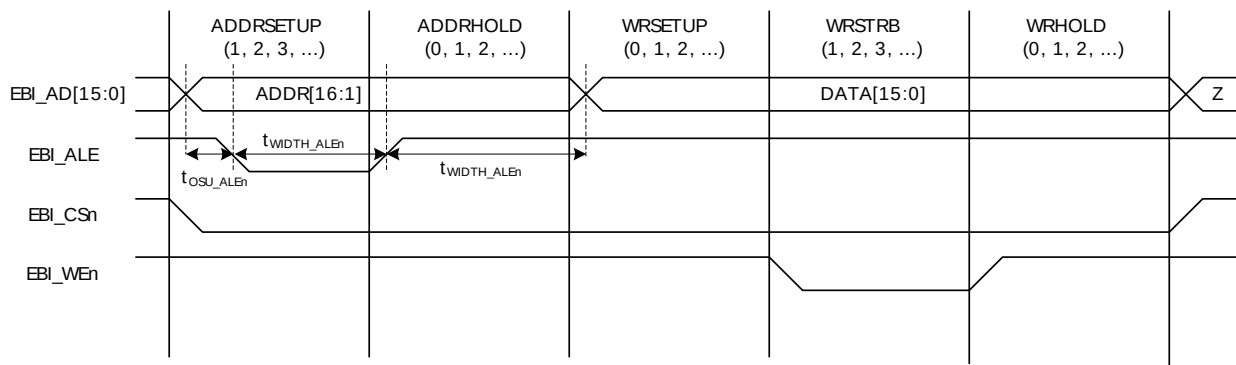
¹Applies for all addressing modes (figure only shows D16 addressing mode)

²Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

³Applies for all polarities (figure only shows active low signals)

⁴Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

⁵ The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by $1/2 * t_{HFCLKNODIV}$.

Figure 3.29. EBI Address Latch Enable Related Output Timing**Table 3.21. EBI Address Latch Enable Related Output Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{OH_ALEn}^{1\ 2\ 3\ 4}$	Output hold time, from trailing EBI_ALE edge to EBI_AD invalid	$-6.00 + (ADDRHOLD^5 * t_{HFCORECLK})$			ns
$t_{OSU_ALEn}^{1\ 2\ 4}$	Output setup time, from EBI_AD valid to leading EBI_ALE edge	$-13.00 + (0 * t_{HFCORECLK})$			ns
$t_{WIDTH_ALEn}^{1\ 2\ 3\ 4}$	EBI_ALEn pulse width	$-7.00 + (ADDRSETUP + 1) * t_{HFCORECLK}$			ns

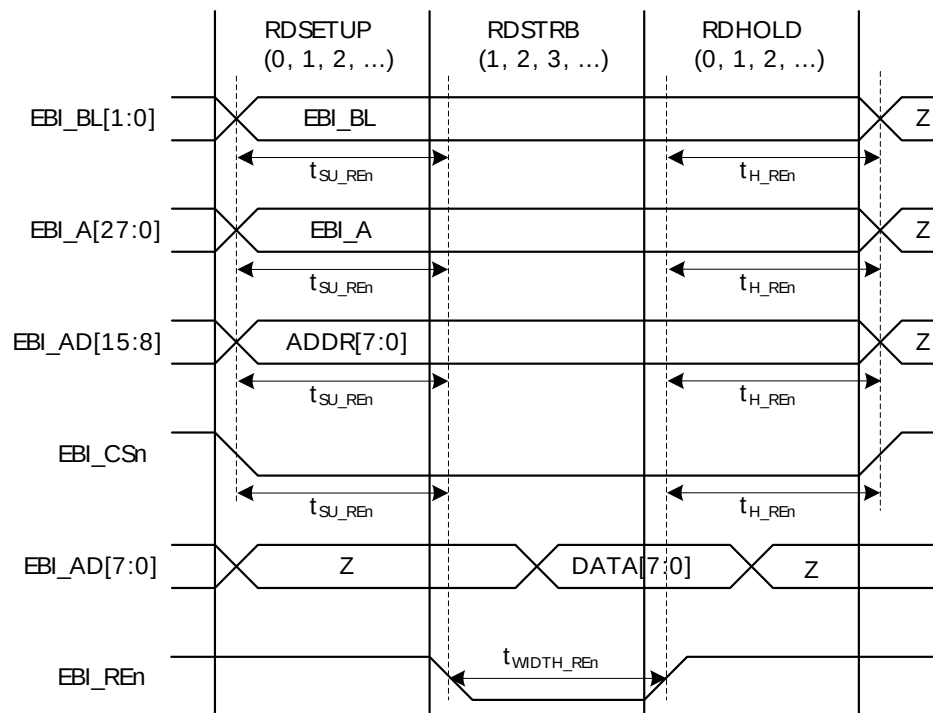
¹Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

²Applies for all polarities (figure only shows active low signals)

³ The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OH_ALEn} by $t_{HFCORECLK} - 1/2 * t_{HFCLKNODIV}$.

⁴Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

⁵Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

Figure 3.30. EBI Read Enable Related Output Timing**Table 3.22. EBI Read Enable Related Output Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{OH_REn}}^{1\ 2\ 3\ 4}$	Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CS, EBI_BLn invalid	$-10.00 + (\text{RDHOLD} * t_{\text{HFCORECLK}})$			ns
$t_{\text{OSU_REn}}^{1\ 2\ 3\ 4\ 5}$	Output setup time, from EBI_AD, EBI_A, EBI_CS, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge	$-10.00 + (\text{RDSETUP} * t_{\text{HFCORECLK}})$			ns
$t_{\text{WIDTH_REn}}^{1\ 2\ 3\ 4\ 5\ 6}$	EBI_REn pulse width	$-9.00 + ((\text{RDSTRB}+1) * t_{\text{HFCORECLK}})$			ns

¹Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

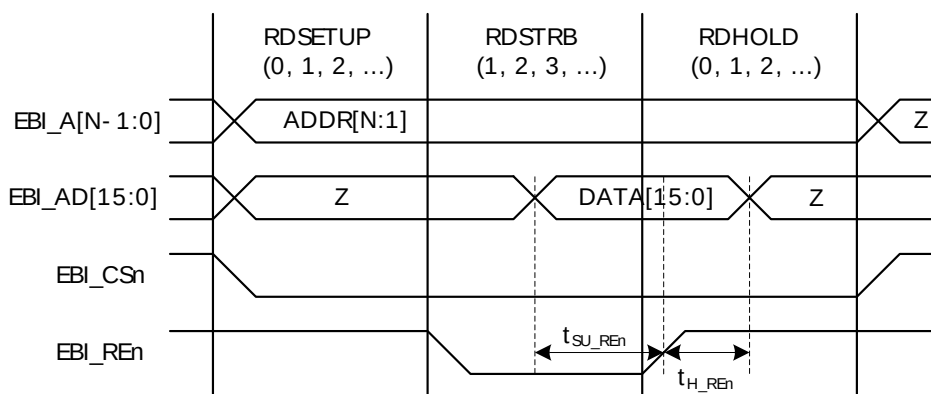
²Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

⁴Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

⁵The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{\text{WIDTH_REn}}$ and increases the length of $t_{\text{OSU_REn}}$ by $1/2 * t_{\text{HFCORECLK}}$.

⁶When page mode is used, RDSTRB is replaced by RDPA for page hits.

Figure 3.31. EBI Read Enable Related Timing Requirements**Table 3.23. EBI Read Enable Related Timing Requirements**

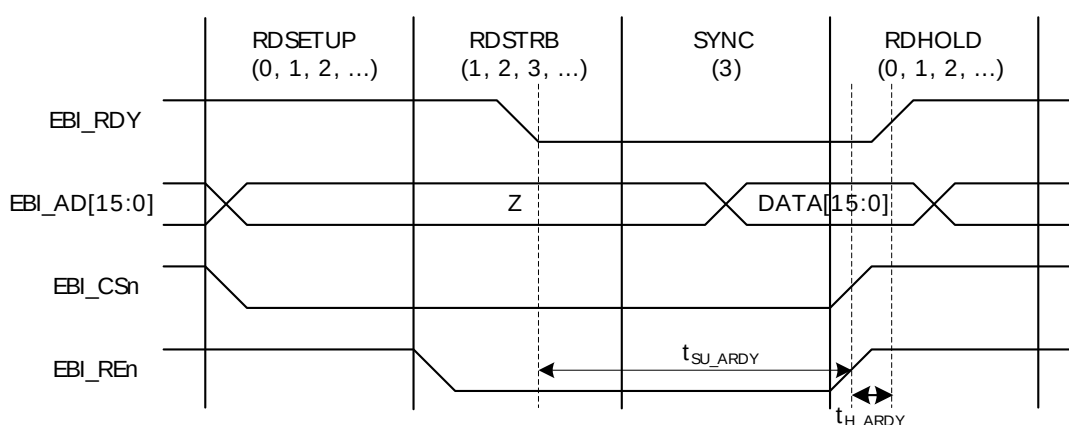
Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU_REn}^{1\ 2\ 3\ 4}$	Setup time, from EBI_AD valid to trailing EBI_REn edge		37		ns
$t_{H_Ren}^{1\ 2\ 3\ 4}$	Hold time, from trailing EBI_REn edge to EBI_AD invalid		-1		ns

¹Applies for all addressing modes (figure only shows D16A8).

²Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

⁴Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Figure 3.32. EBI Ready/Wait Related Timing Requirements**Table 3.24. EBI Ready/Wait Related Timing Requirements**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU_ARDY}^{1\ 2\ 3\ 4}$	Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	$37 + (3 * t_{HFCORECLK})$			ns

Symbol	Parameter	Min	Typ	Max	Unit
$t_{H_ARDY}^{1\ 2\ 3\ 4}$	Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	$-1 + (3 * t_{HFCORECLK})$			ns

¹Applies for all addressing modes (figure only shows D16A8.)

²Applies for EBI_REn, EBI_WEn (figure only shows EBI_REn)

³Applies for all polarities (figure only shows active low signals)

⁴Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.16 I2C

Table 3.25. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		100^1	kHz
t_{LOW}	SCL clock low time	4.7			μs
t_{HIGH}	SCL clock high time	4.0			μs
$t_{SU,DAT}$	SDA set-up time	250			ns
$t_{HD,DAT}$	SDA hold time	8		$3450^{2,3}$	ns
$t_{SU,STA}$	Repeated START condition set-up time	4.7			μs
$t_{HD,STA}$	(Repeated) START condition hold time	4.0			μs
$t_{SU,STO}$	STOP condition set-up time	4.0			μs
t_{BUF}	Bus free time between a STOP and START condition	4.7			μs

¹For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32GG Reference Manual.

²The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((3450 * 10^{-9} [s] * f_{HPPERCLK} [Hz]) - 4)$.

Table 3.26. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400^1	kHz
t_{LOW}	SCL clock low time	1.3			μs
t_{HIGH}	SCL clock high time	0.6			μs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		$900^{2,3}$	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			μs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			μs
$t_{SU,STO}$	STOP condition set-up time	0.6			μs
t_{BUF}	Bus free time between a STOP and START condition	1.3			μs

¹For the minimum HPPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32GG Reference Manual.

²The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

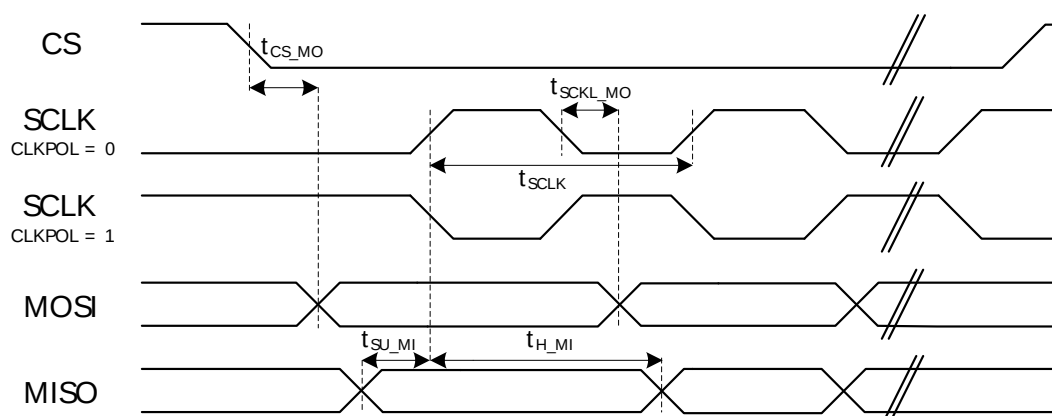
³When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 * 10^{-9} [s] * f_{HPPERCLK} [Hz]) - 4)$.

Table 3.27. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000 ¹	kHz
t_{LOW}	SCL clock low time	0.5			μ s
t_{HIGH}	SCL clock high time	0.26			μ s
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			μ s
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			μ s
$t_{SU,STO}$	STOP condition set-up time	0.26			μ s
t_{BUF}	Bus free time between a STOP and START condition	0.5			μ s

¹For the minimum HPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32GG Reference Manual.

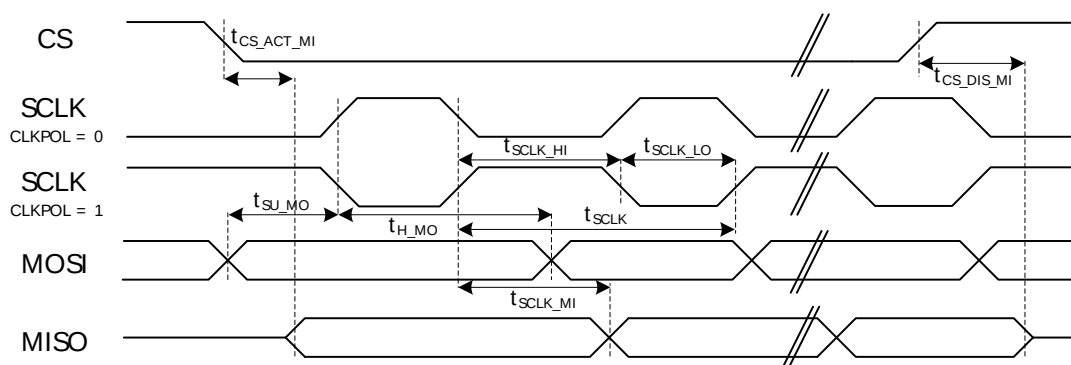
3.17 USART SPI

Figure 3.33. SPI Master Timing**Table 3.28. SPI Master Timing**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SCLK}^{1,2}$	SCLK period		$2 * t_{HFER-CLK}$			ns
$t_{CS_MO}^{1,2}$	CS to MOSI		-2.00		1.00	ns
$t_{SCLK_MO}^{1,2}$	SCLK to MOSI		-4.00		3.00	ns
$t_{SU_MI}^{1,2}$	MISO setup time	IOVDD = 1.98 V	36.00			ns
		IOVDD = 3.0 V	29.00			ns
$t_{H_MI}^{1,2}$	MISO hold time		-4.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Figure 3.34. SPI Slave Timing**Table 3.29. SPI Slave Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SCLK_sl}^{1,2}$	SCKL period	$2 * t_{HFER-CLK}$			ns
$t_{SCLK_hi}^{1,2}$	SCLK high period	$3 * t_{HFER-CLK}$			ns
$t_{SCLK_lo}^{1,2}$	SCLK low period	$3 * t_{HFER-CLK}$			ns
$t_{CS_ACT_MI}^{1,2}$	CS active to MISO	4.00		30.00	ns
$t_{CS_DIS_MI}^{1,2}$	CS disable to MISO	4.00		30.00	ns
$t_{SU_MO}^{1,2}$	MOSI setup time	4.00			ns
$t_{H_MO}^{1,2}$	MOSI hold time	$2 + 2 * t_{HF-PERCLK}$			ns
$t_{SCLK_MI}^{1,2}$	SCLK to MISO	$9 + t_{HFER-CLK}$		$36 + 2 * t_{HF-PERCLK}$	ns

¹ Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

² Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

3.18 Digital Peripherals

Table 3.30. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		4.9		$\mu A / MHz$
I_{UART}	UART current	UART idle current, clock enabled		3.4		$\mu A / MHz$
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		140		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.1		$\mu A / MHz$
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.9		$\mu A / MHz$
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		119		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{PCNT}	PCNT current	PCNT idle current, clock enabled		54		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		54		nA
I _{AES}	AES current	AES idle current, clock enabled		3.2		μA/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock enabled		3.7		μA/ MHz
I _{EBI}	EBI current	EBI idle current, clock enabled		11.8		μA/ MHz
I _{PRS}	PRS current	PRS idle current		3.5		μA/ MHz
I _{DMA}	DMA current	Clock enable		11.0		μA/ MHz

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG290.

4.1 Pinout

The EFM32GG290 pinout is shown in Figure 4.1 (p. 52) and Table 4.1 (p. 52). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32GG290 Pinout (top view, not to scale)

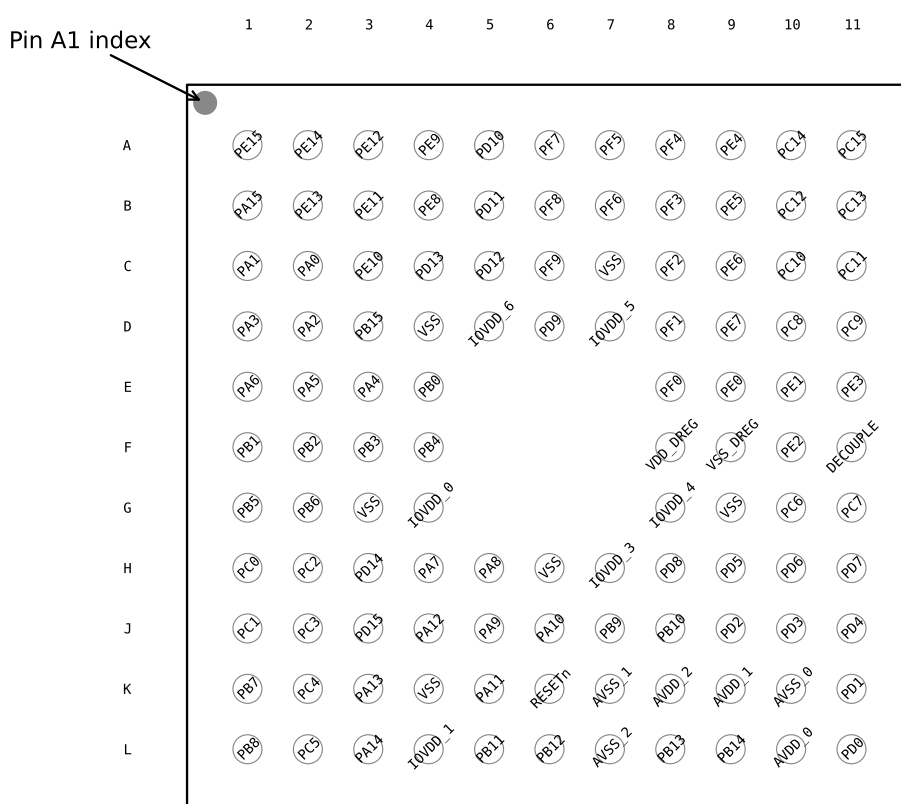


Table 4.1. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15		EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14		EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
A3	PE12		EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A4	PE9		EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD10		EBI_CS1 #0/1/2			
A6	PF7		EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A7	PF5		EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A8	PF4		EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A9	PE4		EBI_A11 #0/1/2		US0_CS #1	
A10	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
A11	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
B1	PA15		EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13		EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11		EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8		EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD11		EBI_CS2 #0/1/2			
B6	PF8		EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B7	PF6		EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B8	PF3		EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B9	PE5		EBI_A12 #0/1/2		US0_CLK #1	
B10	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
B11	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
C1	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	I2C0_SDA #0 LEU0_RX #4	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10		EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1
C5	PD12		EBI_CS3 #0/1/2			
C6	PF9		EBI_REn #1			ETM_TD0 #1
C7	VSS	Ground				
C8	PF2		EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
C9	PE6		EBI_A13 #0/1/2		US0_RX #1	
C10	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
C11	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
D1	PA3		EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
						ETM_TD1 #3
D2	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D4	VSS	Ground				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9		EBI_CS0 #0/1/2			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 I2C0_SCL #5 LEU0_RX #3	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
D9	PE7		EBI_A14 #0/1/2		US0_TX #1	
D10	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D11	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
E1	PA6		EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5		EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4		EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E4	PB0		EBI_A16 #0/1/2	TIM1_CC0 #2		
E8	PF0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 I2C0_SDA #5 LEU0_TX #3	DBG_SWCLK #0/1/2/3
E9	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
E10	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
E11	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
F1	PB1		EBI_A17 #0/1/2	TIM1_CC1 #2		
F2	PB2		EBI_A18 #0/1/2	TIM1_CC2 #2		
F3	PB3		EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
F4	PB4		EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
G1	PB5		EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6		EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		I2C0_SDA #2 LEU1_TX #0	LES_CH6 #0 ETM_TCLK #2

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
G11	PC7	ACMP0_CH7	EBI_A06 #0/1/2		I2C0_SCL #2 LEU1_RX #0	LES_CH7 #0 ETM_TD0 #2
H1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
H2	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
H3	PD14				I2C0_SDA #3	
H4	PA7		EBI_CSTFT #0/1/2			
H5	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
H6	VSS	Ground				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8	BU_VIN				CMU_CLK1 #1
H9	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
H10	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1		LETIM0_OUT0 #0 TIM1_CC1 #4 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H11	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1		LETIM0_OUT1 #0 TIM1_CC1 #4 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
J1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
J2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
J3	PD15				I2C0_SCL #3	
J4	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
J5	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
J6	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
J7	PB9		EBI_A03 #0/1/2		U1_TX #2	
J8	PB10		EBI_A04 #0/1/2		U1_RX #2	
J9	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	US1_CLK #1	DBG_SWO #3
J10	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
J11	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
K1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
K2	PC4	ACMP0_CH4 DAC0_P0 / OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
K3	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
K4	VSS	Ground				
K5	PA11		EBI_HSNC #0/1/2			
K6	RESETn	Reset input, active low.				

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
		To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
L2	PC5	ACMP0_CH5 DAC0_N0 / OPAMP_N0	EBI_NANDWE _n #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
L3	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		LETIM0_OUT0 #1 TIM1_CC2 #3	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 56). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13		PB10	PE3				UART1 Receive input.
U1_TX	PC12		PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
								USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG290* is shown in Table 4.3 (p. 62). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

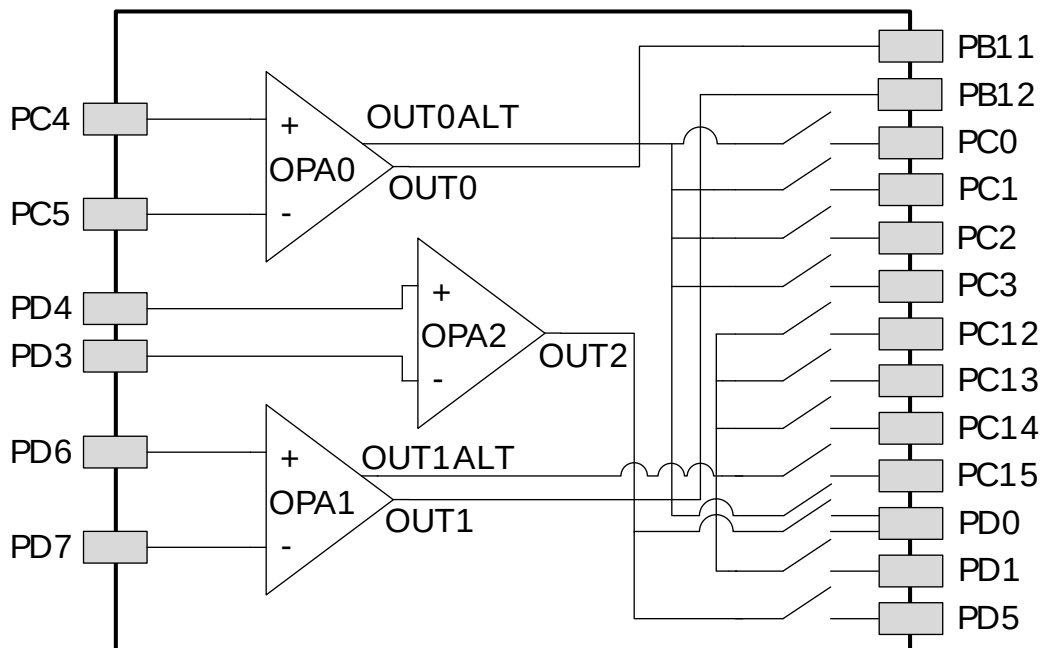
Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 Opamp Pinout Overview

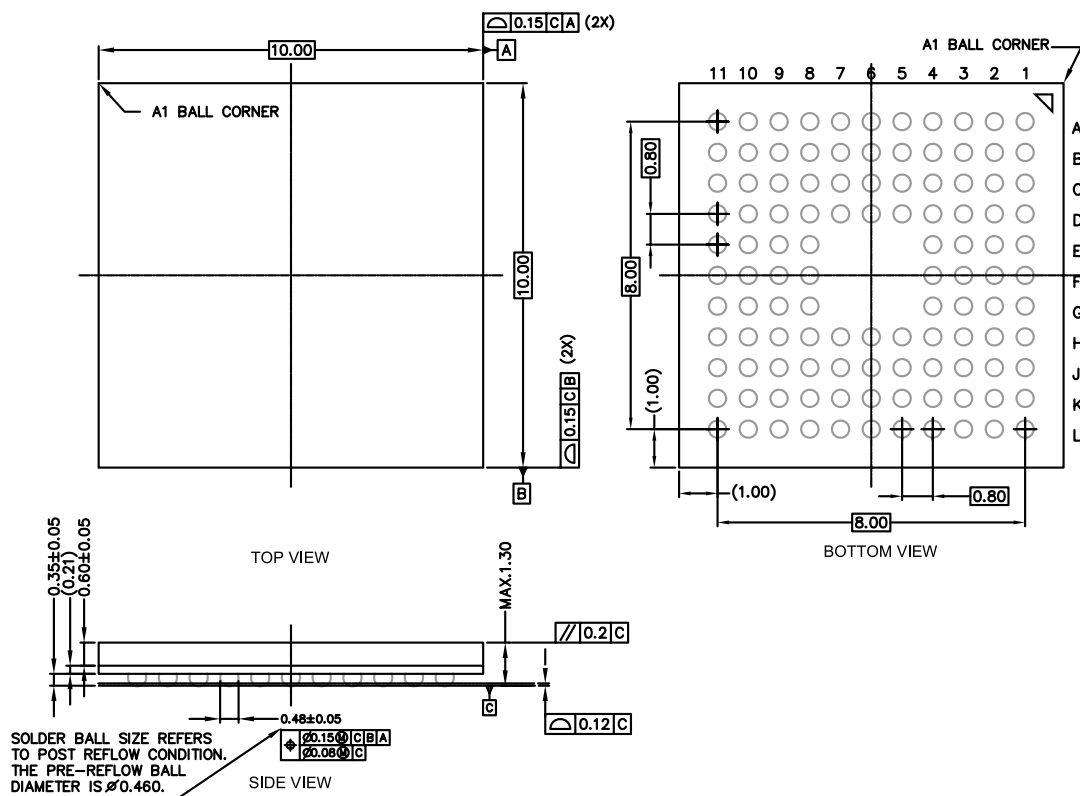
The specific opamp terminals available in *EFM32GG290* is shown in Figure 4.2 (p. 63) .

Figure 4.2. Opamp Pinout



4.5 BGA112 Package

Figure 4.3. BGA112



Rev: 97SP01315A_X03_06Jun11

Note:

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

The BGA112 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:

<http://www.silabs.com/support/quality/pages/default.aspx>

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. BGA112 PCB Land Pattern

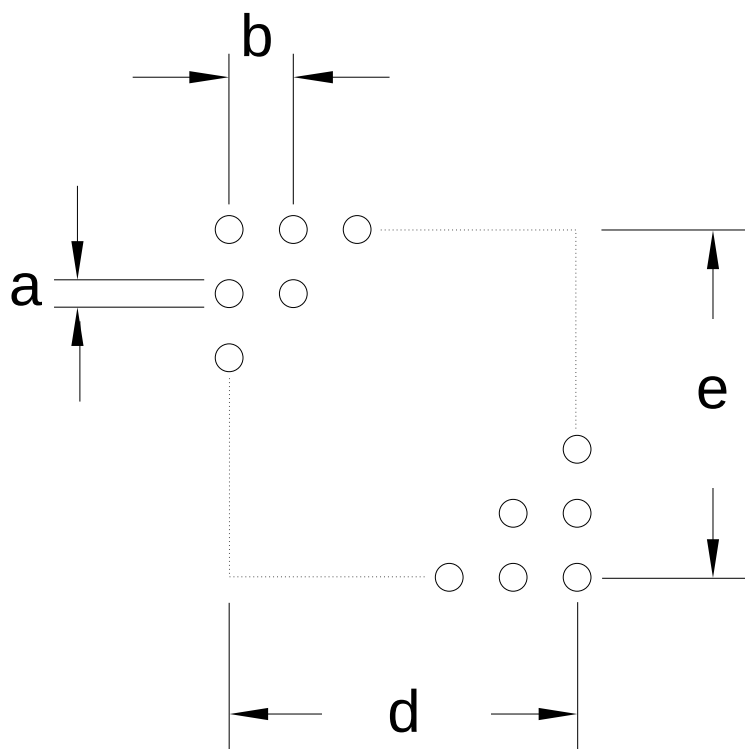


Table 5.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.35
b	0.80
d	8.00
e	8.00

Figure 5.2. BGA112 PCB Solder Mask

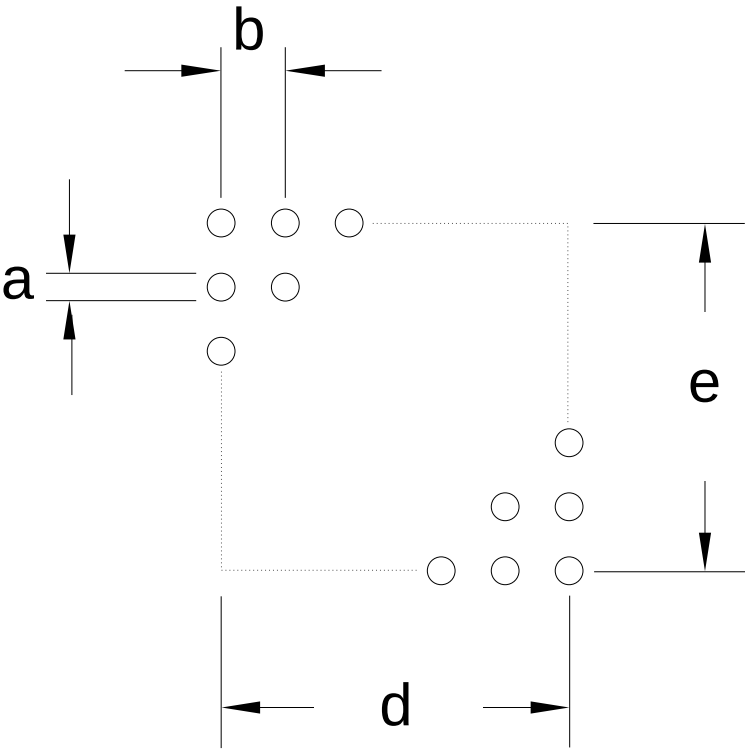
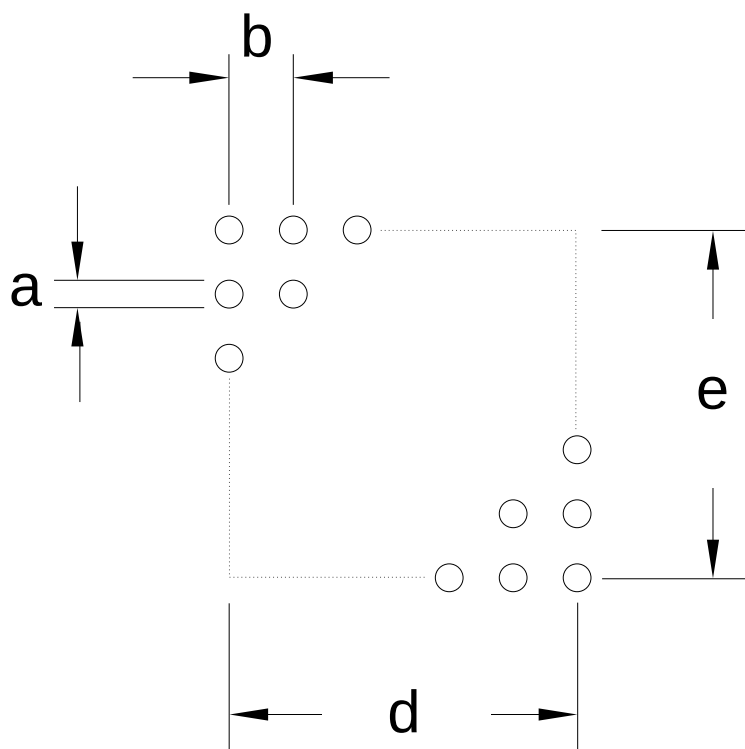


Table 5.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

Figure 5.3. BGA112 PCB Stencil Design**Table 5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	0.33
b	0.80
d	8.00
e	8.00

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 63) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

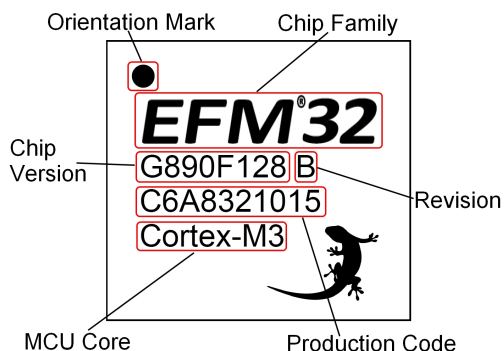
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions.

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 68) .

6.3 Errata

Please see the errata document for EFM32GG290 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

7 Revision History

7.1 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

7.2 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.3 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Added EBI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.10

June 28th, 2013

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.6 Revision 0.98

May 25th, 2012

Corrected BGA solder balls material description.

Corrected EM3 current consumption in the Electrical Characteristics section.

7.7 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected BGA112 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.8 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected BGA112 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.91

March 21th, 2011

Added new alternative locations for EBI and SWO.

Corrected slew rate data for Opamps.

7.10 Revision 0.90

February 4th, 2011

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

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Table of Contents

1. Ordering Information	2
2. System Summary	3
2.1. System Introduction	3
2.2. Configuration Summary	7
2.3. Memory Map	8
3. Electrical Characteristics	10
3.1. Test Conditions	10
3.2. Absolute Maximum Ratings	10
3.3. General Operating Conditions	10
3.4. Current Consumption	12
3.5. Transition between Energy Modes	12
3.6. Power Management	13
3.7. Flash	14
3.8. General Purpose Input Output	14
3.9. Oscillators	22
3.10. Analog Digital Converter (ADC)	27
3.11. Digital Analog Converter (DAC)	37
3.12. Operational Amplifier (OPAMP)	38
3.13. Analog Comparator (ACMP)	42
3.14. Voltage Comparator (VCMP)	44
3.15. EBI	44
3.16. I2C	48
3.17. USART SPI	49
3.18. Digital Peripherals	50
4. Pinout and Package	52
4.1. Pinout	52
4.2. Alternate Functionality Pinout	56
4.3. GPIO Pinout Overview	62
4.4. Opamp Pinout Overview	62
4.5. BGA112 Package	63
5. PCB Layout and Soldering	65
5.1. Recommended PCB Layout	65
5.2. Soldering Information	67
6. Chip Marking, Revision and Errata	68
6.1. Chip Marking	68
6.2. Revision	68
6.3. Errata	68
7. Revision History	69
7.1. Revision 1.30	69
7.2. Revision 1.21	69
7.3. Revision 1.20	69
7.4. Revision 1.10	70
7.5. Revision 1.00	70
7.6. Revision 0.98	70
7.7. Revision 0.96	70
7.8. Revision 0.95	70
7.9. Revision 0.91	71
7.10. Revision 0.90	71
A. Disclaimer and Trademarks	72
A.1. Disclaimer	72
A.2. Trademark Information	72
B. Contact Information	73
B.1.	73

List of Figures

2.1. Block Diagram	3
2.2. EFM32GG290 Memory Map with largest RAM and Flash sizes	9
3.1. Typical Low-Level Output Current, 2V Supply Voltage	16
3.2. Typical High-Level Output Current, 2V Supply Voltage	17
3.3. Typical Low-Level Output Current, 3V Supply Voltage	18
3.4. Typical High-Level Output Current, 3V Supply Voltage	19
3.5. Typical Low-Level Output Current, 3.8V Supply Voltage	20
3.6. Typical High-Level Output Current, 3.8V Supply Voltage	21
3.7. Calibrated LFRCO Frequency vs Temperature and Supply Voltage	24
3.8. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature	25
3.9. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature	25
3.10. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature	25
3.11. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature	26
3.12. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature	26
3.13. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature	26
3.14. Integral Non-Linearity (INL)	32
3.15. Differential Non-Linearity (DNL)	32
3.16. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C	33
3.17. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C	34
3.18. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C	35
3.19. ADC Absolute Offset, Common Mode = Vdd / 2	36
3.20. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V	36
3.21. ADC Temperature sensor readout	37
3.22. OPAMP Common Mode Rejection Ratio	40
3.23. OPAMP Positive Power Supply Rejection Ratio	40
3.24. OPAMP Negative Power Supply Rejection Ratio	41
3.25. OPAMP Voltage Noise Spectral Density (Unity Gain) V _{out} =1V	41
3.26. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)	41
3.27. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1	43
3.28. EBI Write Enable Timing	44
3.29. EBI Address Latch Enable Related Output Timing	45
3.30. EBI Read Enable Related Output Timing	46
3.31. EBI Read Enable Related Timing Requirements	47
3.32. EBI Ready/Wait Related Timing Requirements	47
3.33. SPI Master Timing	49
3.34. SPI Slave Timing	50
4.1. EFM32GG290 Pinout (top view, not to scale)	52
4.2. Opamp Pinout	63
4.3. BGA112	63
5.1. BGA112 PCB Land Pattern	65
5.2. BGA112 PCB Solder Mask	66
5.3. BGA112 PCB Stencil Design	67
6.1. Example Chip Marking (top view)	68

List of Tables

1.1. Ordering Information	2
2.1. Configuration Summary	7
3.1. Absolute Maximum Ratings	10
3.2. General Operating Conditions	10
3.3. Environmental	11
3.4. Current Consumption	12
3.5. Energy Modes Transitions	13
3.6. Power Management	13
3.7. Flash	14
3.8. GPIO	14
3.9. LFXO	22
3.10. HFXO	23
3.11. LFRCO	23
3.12. HFRCO	24
3.13. AUXHFRCO	27
3.14. ULFRCO	27
3.15. ADC	27
3.16. DAC	37
3.17. OPAMP	38
3.18. ACMP	42
3.19. VCMP	44
3.20. EBI Write Enable Timing	45
3.21. EBI Address Latch Enable Related Output Timing	45
3.22. EBI Read Enable Related Output Timing	46
3.23. EBI Read Enable Related Timing Requirements	47
3.24. EBI Ready/Wait Related Timing Requirements	47
3.25. I2C Standard-mode (Sm)	48
3.26. I2C Fast-mode (Fm)	48
3.27. I2C Fast-mode Plus (Fm+)	49
3.28. SPI Master Timing	49
3.29. SPI Slave Timing	50
3.30. Digital Peripherals	50
4.1. Device Pinout	52
4.2. Alternate functionality overview	56
4.3. GPIO Pinout	62
5.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)	65
5.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)	66
5.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)	67

List of Equations

3.1. Total ACMP Active Current 42

3.2. VCMP Trigger Level as a Function of Level Setting 44

