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## REVISION HISTORY

**4/13—Rev. F to Rev. G**

Changed Reference Low Input Current from 0 mA (min), 2 mA (typ), 2.75 mA (max) to −2.75 mA (min), −2 mA (typ), 0 mA (max); Table 1 ... 3
Changes to Reference Configurations Section ... 17

**9/09—Rev. E to Rev. F**

Updated Figure Numbering ... Universal
Removed Figure 7 ... 6
Changes to Ordering Guide ... 20

**6/07—Rev. D to Rev. E**

Updated Format ... Universal
Added CERDIP Package ... Universal
Changes to Specifications Section ... 3
Changes to Absolute Maximum Ratings Section ... 7
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 20

**3/00—Rev. C to Rev. D**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = +15.0 V, $V_{SS}$ = −15.0 V, $V_{LOGIC}$ = +5.0 V, $V_{REFH}$ = +10.0 V, $V_{REFL}$ = −10.0 V,−40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.[1]

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Integral Nonlinearity Error | INL | E grade | | ±0.25 | ±0.5 | LSB |
| | | F grade | | | ±1 | LSB |
| Differential Nonlinearity Error | DNL | Monotonic over temperature | −1 | | | LSB |
| Min-Scale Error | $V_{ZSE}$ | $R_L$ = 2 kΩ | | | ±2 | LSB |
| Full-Scale Error | $V_{FSE}$ | $R_L$ = 2 kΩ | | | ±2 | LSB |
| Min-Scale Temperature Coefficient | $TCV_{ZSE}$ | $R_L$ = 2 kΩ | | 15 | | ppm/°C |
| Full-Scale Temperature Coefficient | $TCV_{FSE}$ | $R_L$ = 2 kΩ | | 20 | | ppm/°C |
| Linearity Matching | | Adjacent DAC Matching | | ±1 | | LSB |
| REFERENCE | | | | | | |
| Positive Reference Input Voltage Range[2] | | | $V_{REFL}$ + 2.5 | | $V_{DD}$ − 2.5 | V |
| Negative Reference Input Voltage Range[2] | | | −10 | | $V_{REFH}$ − 2.5 | V |
| Reference High Input Current | $I_{REFH}$ | | −2.75 | +1.5 | +2.75 | mA |
| Reference Low Input Current | $I_{REFL}$ | | −2.75 | −2 | 0 | mA |
| Large Signal Bandwidth | BW | −3 dB, $V_{REFH}$ = 0 V to 10 V p-p | | 160 | | kHz |
| AMPLIFIER CHARACTERISTICS | | | | | | |
| Output Current | $I_{OUT}$ | $R_L$ = 2 kΩ, $C_L$ = 100 pF | −5 | | +5 | mA |
| Settling Time | $t_S$ | To 0.01%, 10 V step, $R_L$ = 1 kΩ | | 10 | | µs |
| Slew Rate | SR | 10% to 90% | | 2.2 | | V/µs |
| Analog Crosstalk | | | | 72 | | dB |
| LOGIC CHARACTERISTICS | | | | | | |
| Logic Input High Voltage | $V_{INH}$ | $T_A$ = 25°C | 2.4 | | | V |
| Logic Input Low Voltage | $V_{INL}$ | $T_A$ = 25°C | | | 0.8 | V |
| Logic Output High Voltage | $V_{OH}$ | $I_{OH}$ = 0.4 mA | 2.4 | | | V |
| Logic Output Low Voltage | $V_{OL}$ | $I_{OL}$ = −1.6 mA | | | 0.4 | V |
| Logic Input Current | $I_{IN}$ | | | | 1 | µA |
| Input Capacitance | $C_{IN}$ | | | 8 | | pF |
| Digital Feedthrough[3] | | $V_{REFH}$ = 2.5 V, $V_{REFL}$ = 0 V | | 5 | | nV-sec |
| LOGIC TIMING CHARACTERISTICS[3, 4] | | | | | | |
| Chip Select Write Pulse Width | $t_{WCS}$ | | 80 | | | ns |
| Write Setup | $t_{WS}$ | $t_{WCS}$ = 80 ns | 0 | | | ns |
| Write Hold | $t_{WH}$ | $t_{WCS}$ = 80 ns | 0 | | | ns |
| Address Setup | $t_{AS}$ | | 0 | | | ns |
| Address Hold | $t_{AH}$ | | 0 | | | ns |
| Load Setup | $t_{LS}$ | | 70 | | | ns |
| Load Hold | $t_{LH}$ | | 30 | | | ns |
| Write Data Setup | $t_{WDS}$ | $t_{WCS}$ = 80 ns | 20 | | | ns |
| Write Data Hold | $t_{WDH}$ | $t_{WCS}$ = 80 ns | 0 | | | ns |
| Load Data Pulse Width | $t_{LDW}$ | | 170 | | | ns |
| Reset Pulse Width | $t_{RESET}$ | | 140 | | | ns |
| Chip Select Read Pulse Width | $t_{RCS}$ | | 130 | | | ns |
| Read Data Hold | $t_{RDH}$ | $t_{RCS}$ = 130 ns | 0 | | | ns |
| Read Data Setup | $t_{RDS}$ | $t_{RCS}$ = 130 ns | 0 | | | ns |
| Data to High-Z | $t_{DZ}$ | $C_L$ = 10 pF | | | 200 | ns |
| Chip Select to Data | $t_{CSD}$ | $C_L$ = 100 pF | | | 160 | ns |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Sensitivity | PSS | 14.25 V ≤ $V_{DD}$ ≤ 15.75 V | | | 150 | ppm/V |
| Positive Supply Current | $I_{DD}$ | $V_{REFH}$ = 2.5 V | | 8.5 | 12 | mA |
| Negative Supply Current | $I_{SS}$ | | −10 | −6.5 | | mA |
| Power Dissipation | $P_{DISS}$ | | | | 330 | mW |

[1] All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.
[2] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[3] All parameters are guaranteed by design.
[4] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

$V_{DD}$ = $V_{LOGIC}$ = +5.0 V ± 5%, $V_{SS}$ = 0.0 V, $V_{REFH}$ = +2.5 V, $V_{REFL}$ = 0.0 V, $V_{SS}$ = −5.0 V ± 5%, $V_{REFL}$ = −2.5 V, −40°C ≤ $T_A$ ≤ +85°C, unless otherwise noted.[1]

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Integral Nonlinearity Error | INL | E grade | | ±0.5 | ±1 | LSB |
| | | F grade | | | ±2 | LSB |
| | | $V_{SS}$ = 0.0 V, E grade[2] | | | ±2 | LSB |
| | | $V_{SS}$ = 0.0 V, F grade[2] | | | ±4 | LSB |
| Differential Nonlinearity Error | DNL | Monotonic over temperature | −1 | | | LSB |
| Min-Scale Error | $V_{ZSE}$ | $V_{SS}$ = −5.0 V | | | ±4 | LSB |
| Full-Scale Error | $V_{FSE}$ | $V_{SS}$ = −5.0 V | | | ±4 | LSB |
| Min-Scale Error | $V_{ZSE}$ | $V_{SS}$ = 0.0 V | | | ±8 | LSB |
| Full-Scale Error | $V_{FSE}$ | $V_{SS}$ = 0.0 V | | | ±8 | LSB |
| Min-Scale Temperature Coefficient | $TCV_{ZSE}$ | | | 100 | | ppm/°C |
| Full-Scale Temperature Coefficient | $TCV_{FSE}$ | | | 100 | | ppm/°C |
| Linearity Matching | | Adjacent DAC matching | | ±1 | | LSB |
| REFERENCE | | | | | | |
| Positive Reference Input Voltage Range[3] | | | $V_{REFL}$ + 2.5 | | $V_{DD}$ − 2.5 | V |
| Negative Reference Input Voltage Range | | $V_{SS}$ = 0.0 V | 0 | | $V_{REFH}$ − 2.5 | V |
| | | $V_{SS}$ = −5.0 V | −2.5 | | $V_{REFH}$ − 2.5 | V |
| Reference High Input Current | $I_{REFH}$ | Code 0x000 | −1.0 | | +1.0 | mA |
| Large Signal Bandwidth | BW | −3 dB, $V_{REFH}$ = 0 V to 2.5 V p-p | | 450 | | kHz |
| AMPLIFIER CHARACTERISTICS | | | | | | |
| Output Current | $I_{OUT}$ | $R_L$ = 2 kΩ, $C_L$ = 100 pF | −1.25 | | +1.25 | mA |
| Settling Time | $t_S$ | To 0.01%, 2.5 V step, $R_L$ = 1 kΩ | | 7 | | µs |
| Slew Rate | SR | 10% to 90% | | 2.2 | | V/µs |
| LOGIC CHARACTERISTICS | | | | | | |
| Logic Input High Voltage | $V_{INH}$ | $T_A$ = 25°C | 2.4 | | | V |
| Logic Input Low Voltage | $V_{INL}$ | $T_A$ = 25°C | | | 0.8 | V |
| Logic Output High Voltage | $V_{OH}$ | $I_{OH}$ = 0.4 mA | 2.4 | | | V |
| Logic Output Low Voltage | $V_{OL}$ | $I_{OL}$ = −1.6 mA | | | 0.45 | V |
| Logic Input Current | $I_{IN}$ | | | | 1 | µA |
| Input Capacitance | $C_{IN}$ | | | 8 | | pF |
| LOGIC TIMING CHARACTERISTICS[4, 5] | | | | | | |
| Chip Select Write Pulse Width | $t_{WCS}$ | | 150 | | | ns |
| Write Setup | $t_{WS}$ | $t_{WCS}$ = 150 ns | 0 | | | ns |
| Write Hold | $t_{WH}$ | $t_{WCS}$ = 150 ns | 0 | | | ns |
| Address Setup | $t_{AS}$ | | 0 | | | ns |
| Address Hold | $t_{AH}$ | | 0 | | | ns |
| Load Setup | $t_{LS}$ | | 70 | | | ns |
| Load Hold | $t_{LH}$ | | 50 | | | ns |

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Write Data Setup | $t_{WDS}$ | $t_{WCS}$ = 150 ns | 20 | | | ns |
| Write Data Hold | $t_{WDH}$ | $t_{WCS}$ = 150 ns | 0 | | | ns |
| Load Data Pulse Width | $t_{LDW}$ | | 180 | | | ns |
| Reset Pulse Width | $t_{RESET}$ | | 150 | | | ns |
| Chip Select Read Pulse Width | $t_{RCS}$ | | 170 | | | ns |
| Read Data Hold | $t_{RDH}$ | $t_{RCS}$ = 170 ns | 20 | | | ns |
| Read Data Setup | $t_{RDS}$ | $t_{RCS}$ = 170 ns | 0 | | | ns |
| Data to High-Z | $t_{DZ}$ | $C_L$ = 10 pF | | | 200 | ns |
| Chip Select to Data | $t_{CSD}$ | $C_L$ = 100 pF | | | 320 | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Sensitivity | PSS | | | 100 | | ppm/V |
| Positive Supply Current | $I_{DD}$ | | | 7 | 12 | mA |
| Negative Supply Current | $I_{SS}$ | $V_{SS}$ = −5.0 V | −10 | | | mA |
| Power Dissipation | $P_{DISS}$ | $V_{SS}$ = 0 V | | 60 | | mW |
| | | $V_{SS}$ = −5.0 V | | 110 | | mW |

[1] All supplies can be varied ±5%, and operation is guaranteed. Device is tested with $V_{DD}$ = 4.75 V.
[2] For single-supply operation only ($V_{REFL}$ = 0.0 V, $V_{SS}$ = 0.0 V). Due to internal offset errors, INL and DNL are measured beginning at 0x005.
[3] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[4] All parameters are guaranteed by design.
[5] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

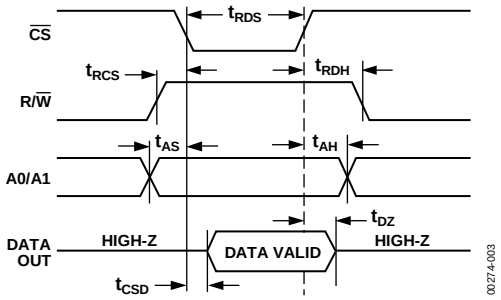



*Figure 3. Data Output (Read Timing)*

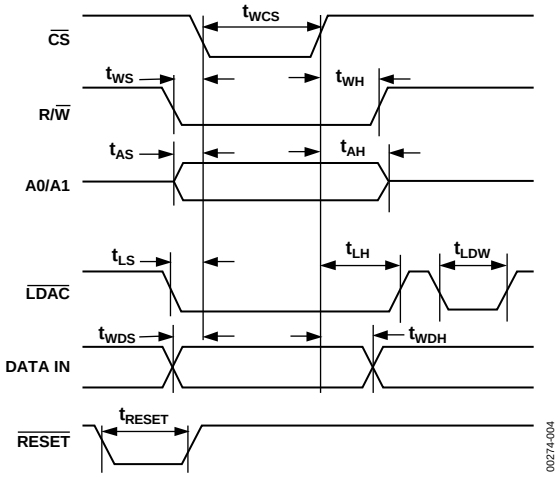



*Figure 4. Data Write (Input and Output Registers) Timing*

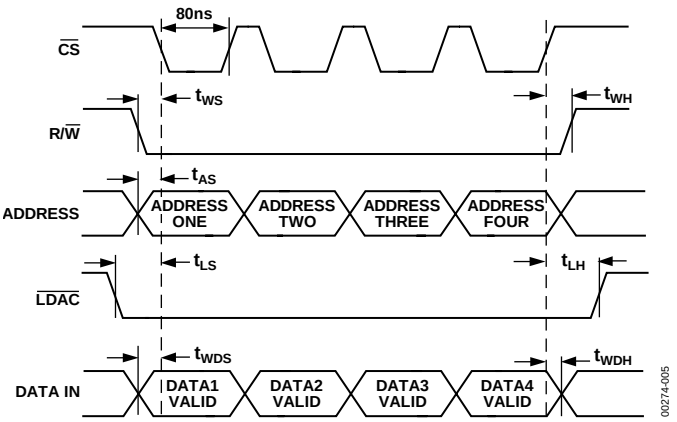



Figure 5. Single-Buffer Mode

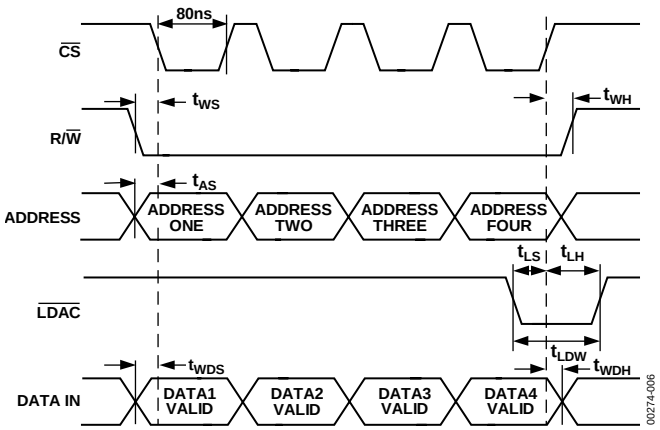



Figure 6. Double-Buffer Mode

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = +25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{SS}$ to $V_{DD}$ | −0.3 V, +33.0 V |
| $V_{SS}$ to $V_{LOGIC}$ | −0.3 V, +33.0 V |
| $V_{LOGIC}$ to DGND | −0.3 V, +7.0 V |
| $V_{SS}$ to $V_{REFL}$ | −0.3 V, +$V_{SS}$ − 2.0 V |
| $V_{REFH}$ to $V_{DD}$ | +2.0 V, +33.0 V |
| $V_{REFH}$ to $V_{REFL}$ | +2.0 V, $V_{SS}$ − $V_{DD}$ |
| Current into Any $V_{SS}$ pin | ±15 mA |
| Digital Input Voltage to DGND | −0.3 V, $V_{LOGIC}$ + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V, +7.0 V |
| Operating Temperature Range | |
| EP, FP, FPC | −40°C to +85°C |
| AT, BT, BTC | −55°C to +125°C |
| Junction Temperature | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Power Dissipation Package | 1000 mW |
| Lead Temperature | JEDEC Industry Standard |
| Soldering | J-STD-020 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case mounting conditions, that is, a device in socket.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 28-Lead Plastic DIP (PDIP) | 48 | 22 | °C/W |
| 28-Terminal Ceramic Leadless Chip Carrier (LLC) | 70 | 28 | °C/W |
| 28-Lead Plastic Leaded Chip Carrier (PLLC) | 63 | 25 | °C/W |
| 28-Lead Ceramic Dual In-Line Package (CERDIP) | 51 | 9 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

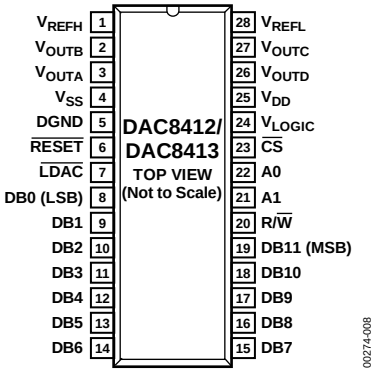



Figure 7. PDIP/CERDIP

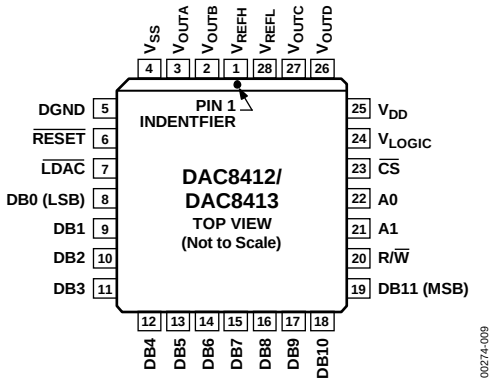



Figure 8. PLCC

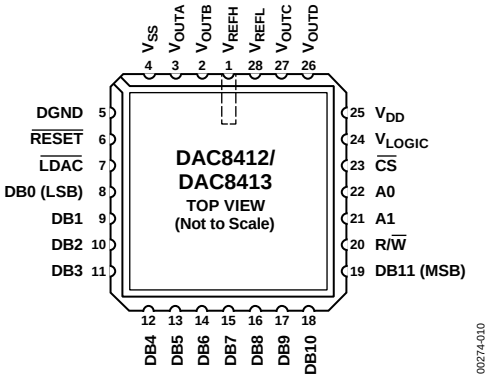



Figure 9. LCC

**Table 5. Pin Function Descriptions**

| Pin Number | Mnemonic | Description |
|---|---|---|
| 1 | $V_{REFH}$ | High-Side DAC Reference Input. |
| 2 | $V_{OUTB}$ | DAC B Output. |
| 3 | $V_{OUTA}$ | DAC A Output. |
| 4 | $V_{SS}$ | Lower Rail Power Supply. |
| 5 | DGND | Digital Ground. |
| 6 | $\overline{RESET}$ | Reset Input and Output Registers to all 0s, Enabled at Active Low. |
| 7 | $\overline{LDAC}$ | Load Data to DAC, Enabled at Active Low. |
| 8 | DB0 | Data Bit 0, LSB. |
| 9 | DB1 | Data Bit 1. |
| 10 | DB2 | Data Bit 2. |
| 11 | DB3 | Data Bit 3. |
| 12 | DB4 | Data Bit 4. |
| 13 | DB5 | Data Bit 5. |
| 14 | DB6 | Data Bit 6. |
| 15 | DB7 | Data Bit 7. |
| 16 | DB8 | Data Bit 8. |
| 17 | DB9 | Data Bit 9. |
| 18 | DB10 | Data Bit 10. |
| 19 | DB11 | Data Bit 11, MSB. |
| 20 | R/$\overline{W}$ | Active Low to Write Data to DAC. Active high to readback previous data at data bit pins with $V_{LOGIC}$ connected to 5 V. |
| 21 | A1 | Address Bit 1. |
| 22 | A0 | Address Bit 0. |
| 23 | $\overline{CS}$ | Chip Select, Enabled at Active Low. |
| 24 | $V_{LOGIC}$ | Voltage Supply for Readback Function. Can be open circuit if not used. |
| 25 | $V_{DD}$ | Upper Rail Power Supply. |
| 26 | $V_{OUTD}$ | DAC D Output. |
| 27 | $V_{OUTC}$ | DAC C Output. |
| 28 | $V_{REFL}$ | Low-Side DAC Reference Input. |

# TYPICAL PERFORMANCE CHARACTERISTICS

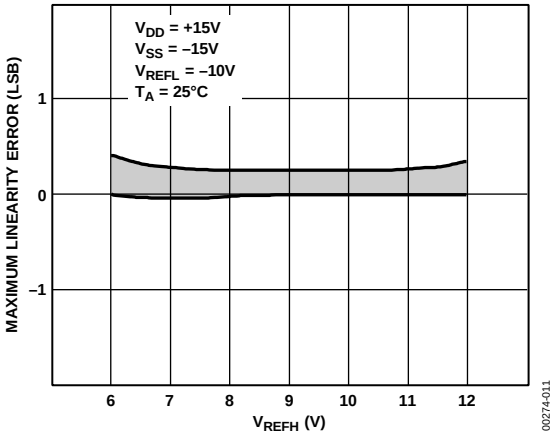



Figure 10. DNL vs. $V_{REFH}$

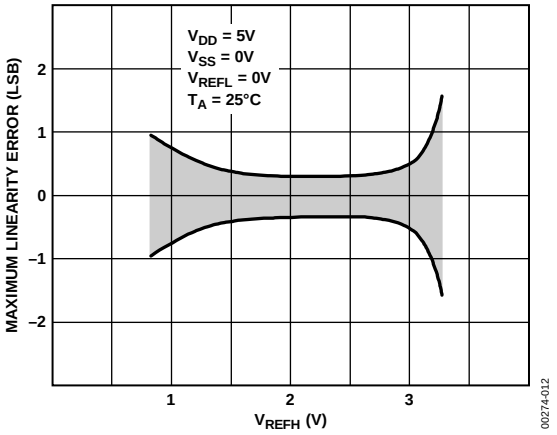



Figure 13. DNL vs. $V_{REFH}$

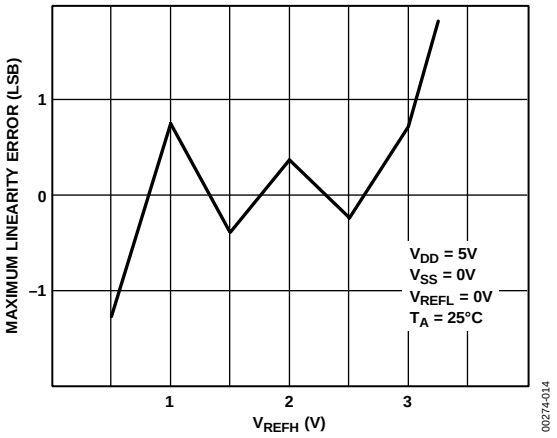



Figure 11. INL vs. $V_{REFH}$

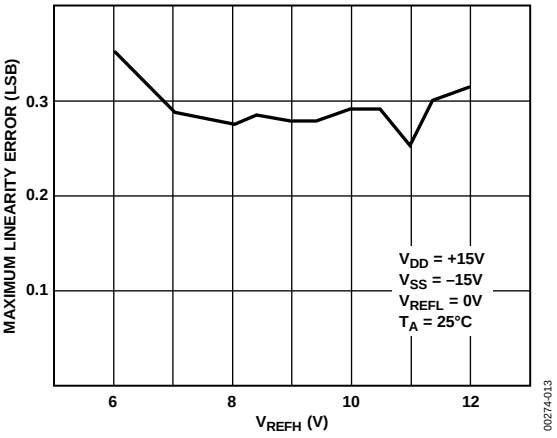



Figure 14. INL vs.$V_{REFH}$

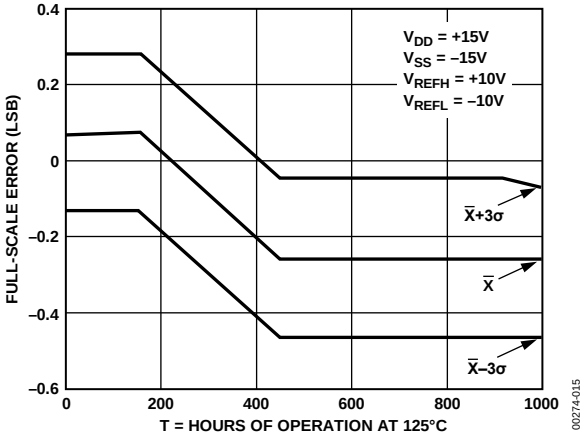



Figure 12. Full-Scale Error vs. Time Accelerated by Burn-in

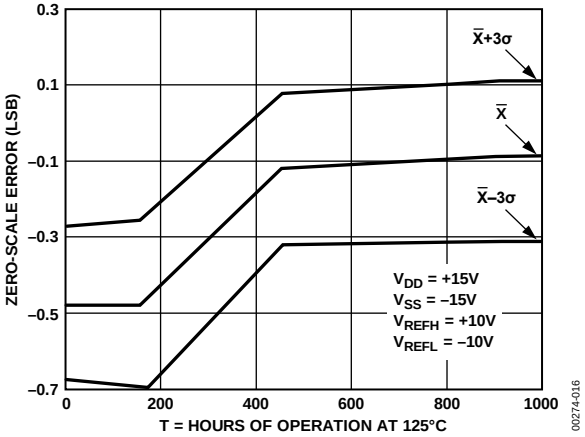



Figure 15. Zero-Scale Error vs. Time Accelerated by Burn-In

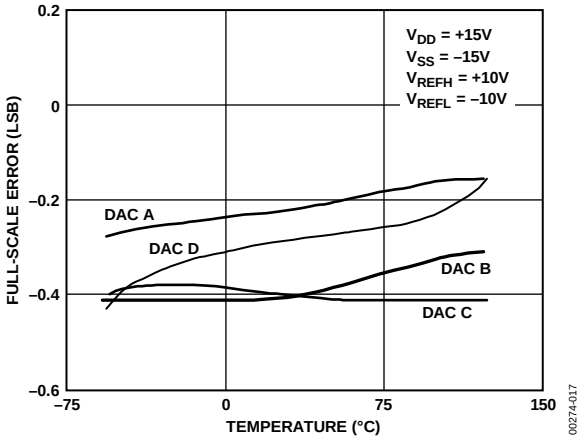



Figure 16. Full-Scale Error vs. Temperature

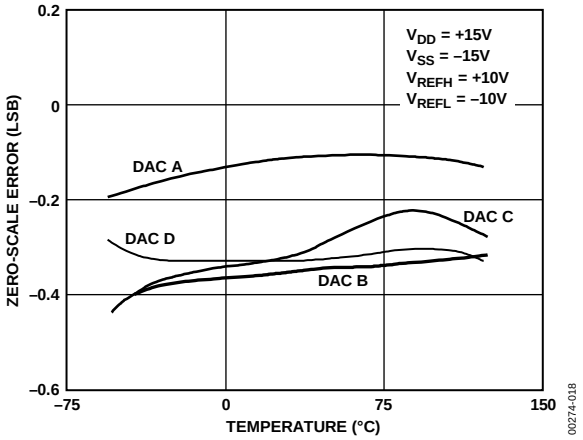



Figure 17. Zero-Scale Error vs. Temperature

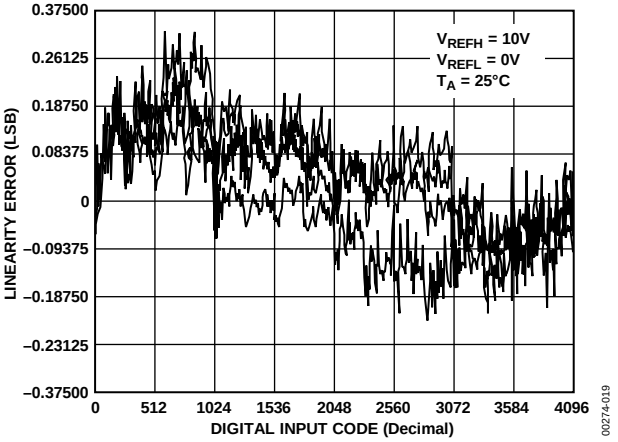



Figure 18. Channel-to-Channel Matching ($V_{SUPPLY}$ = ±15 V)

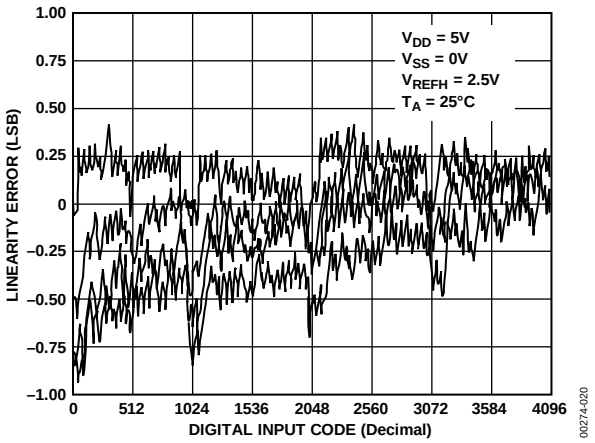



Figure 19. Channel-to-Channel Matching ($V_{SUPPLY}$ = +5 V/GND)

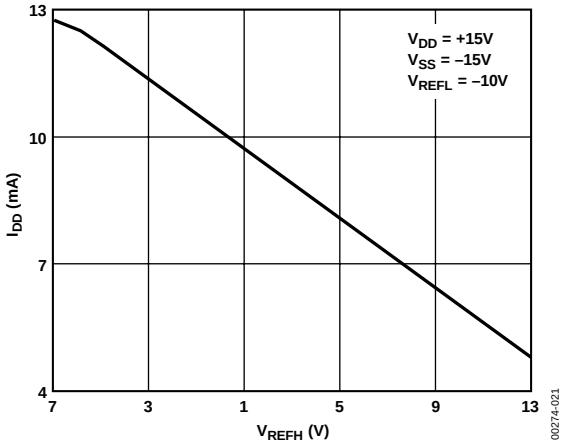



Figure 20. $I_{DD}$ vs. $V_{REFH}$ (All DACs High)

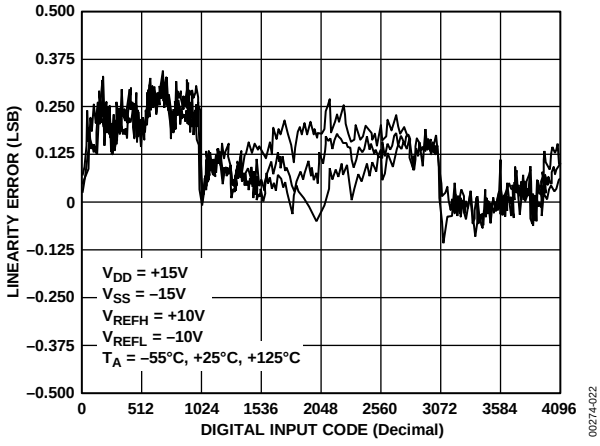



Figure 21. INL vs. Code

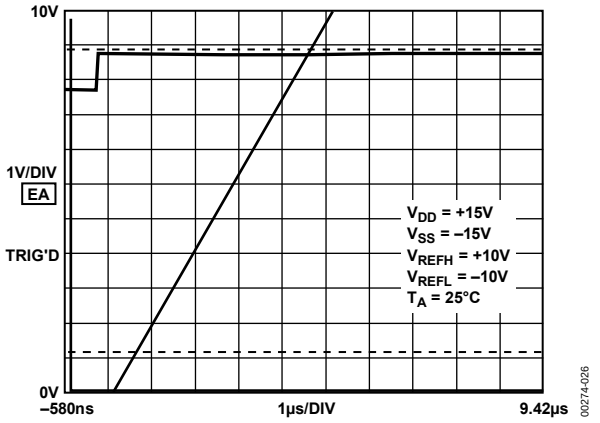



Figure 22. Positive Slew Rate

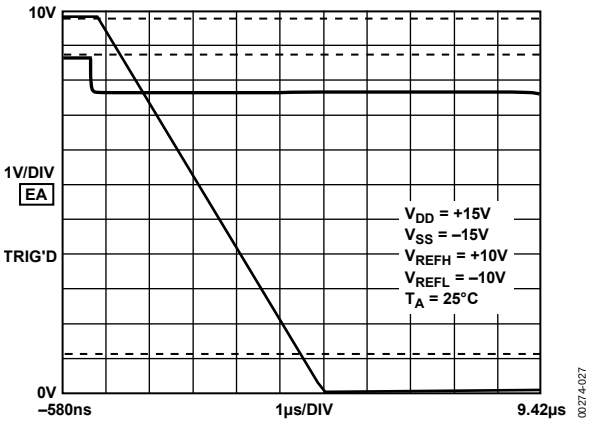



Figure 25. Negative Slew Rate

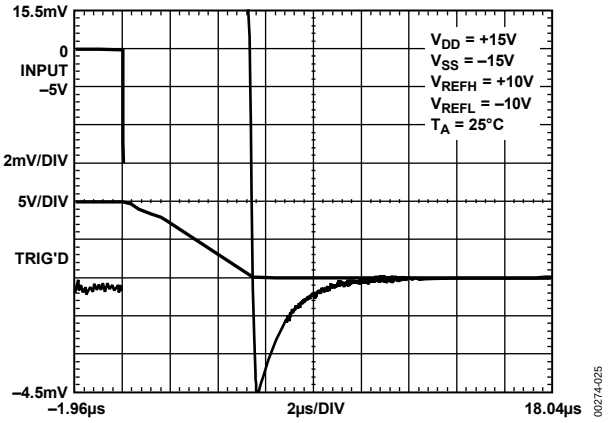



Figure 23. Settling Time (Negative)

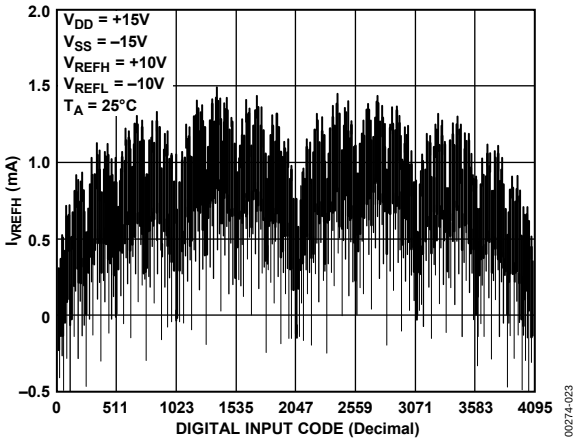



Figure 26. $I_{VREFH}$ vs. Code

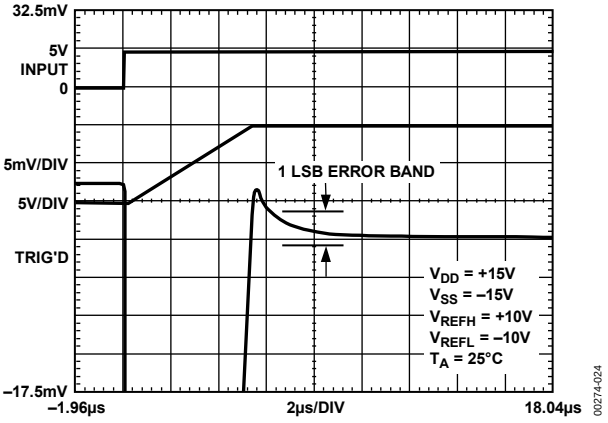



Figure 24. Settling Time (Positive)

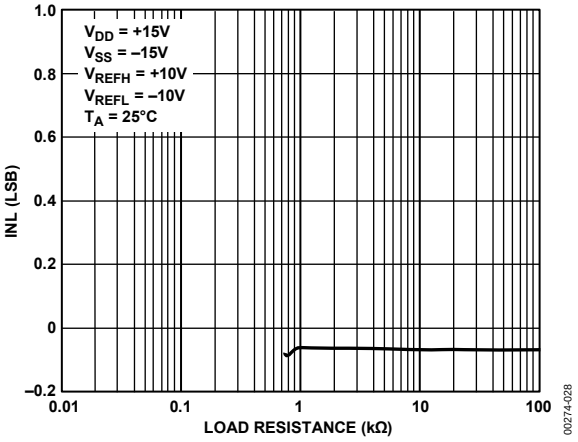



Figure 27. INL vs. Load Resistance

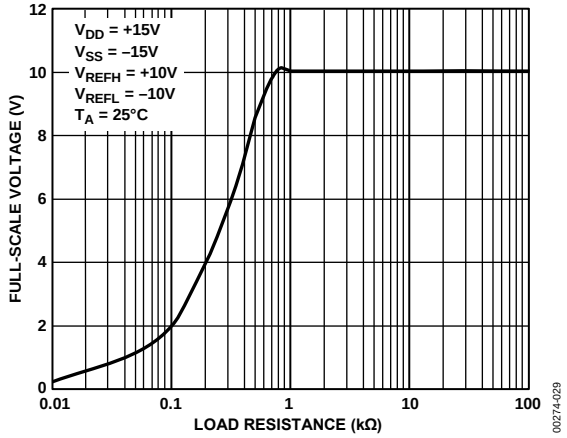



Figure 28. Output Swing vs. Load Resistance

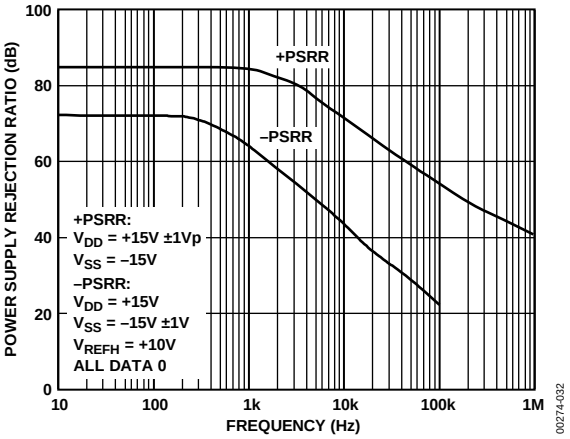



Figure 31. PSRR vs. Frequency

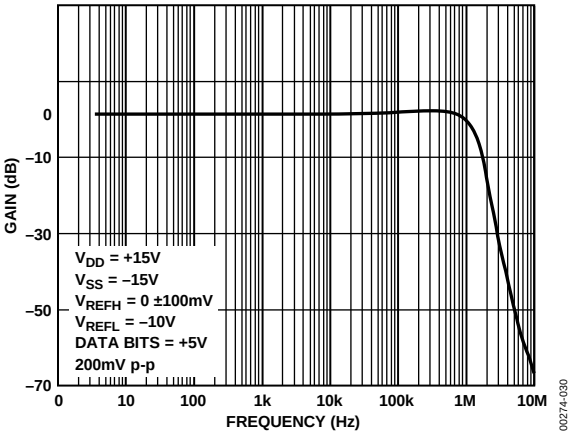



Figure 29. Small Signal Response

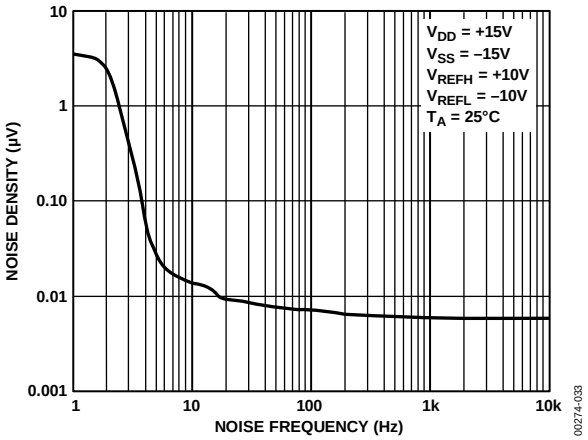



Figure 32. Noise Density vs. Noise Frequency

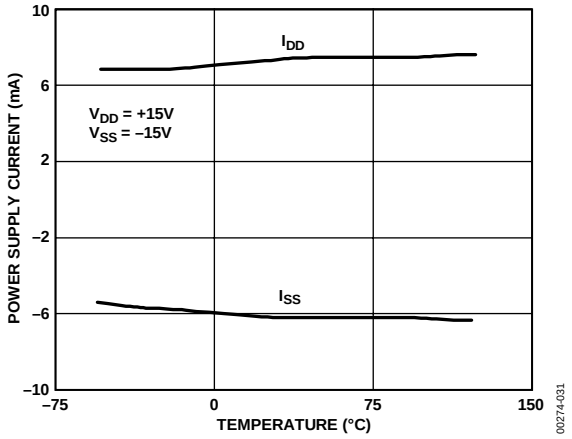



Figure 30. Power Supply Current vs. Temperature

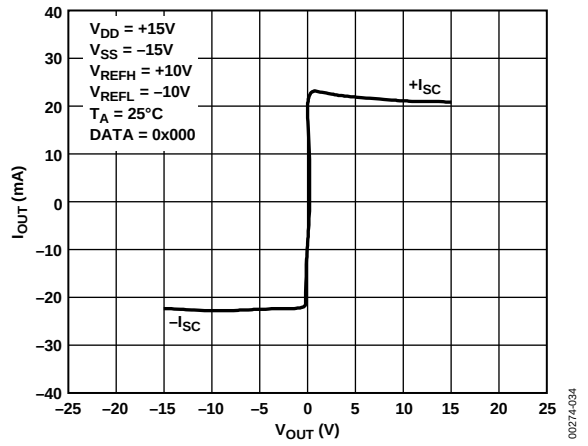



Figure 33. $I_{OUT}$ vs. $V_{OUT}$

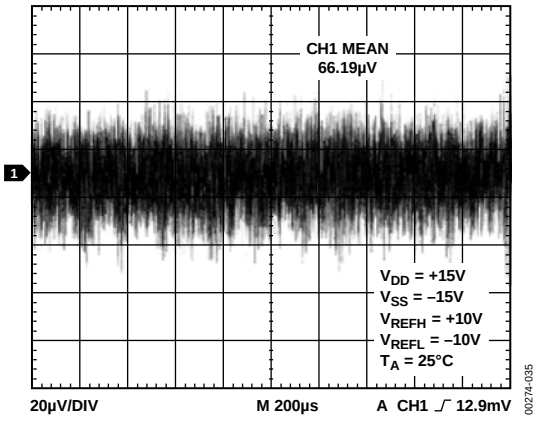



Figure 34. Broadband Noise

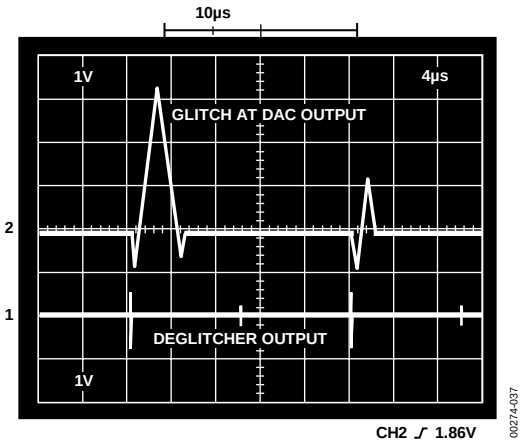



Figure 36. Glitch and Deglitched Results

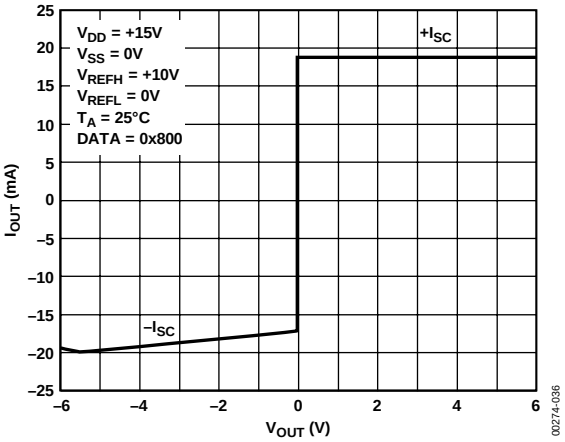



Figure 35. $I_{OUT}$ vs. $V_{OUT}$

# THEORY OF OPERATION

## INTRODUCTION

The DAC8412/DAC8413 are quad, voltage output, 12-bit parallel input DACs featuring a 12-bit data bus with readback capability. The only differences between the DAC8412/DAC8413 are the reset functions. The DAC8412 resets to midscale (Code 0x800), and the DAC8413 resets to minimum scale (Code 0x000).

The ability to operate from a single 5 V supply is a unique feature of these DACs.

Operation of the DAC8412/DAC8413 can be viewed by dividing the system into three separate functional groups: the digital I/O and logic, the digital-to-analog converters, and the output amplifiers.

## DACS

Each DAC is a voltage switched, high impedance (R = 50 kΩ), R-2R ladder configuration. Each 2R resistor is driven by a pair of switches that connect the resistor to either $V_{REFH}$ or $V_{REFL}$.

## GLITCH

Worst-case glitch occurs at the transition between Half-Scale Digital Code 1000 0000 0000 to half-scale minus 1 LSB, 0111 1111 1111. It can be measured at about 2 V µs (see Figure 36). For demanding applications such as waveform generation or precision instrumentation control, a deglitcher circuit can be implemented with a standard sample-and-hold circuit (see Figure 37). When $\overline{CS}$ is enabled by synchronizing the hold period to be longer than the glitch tradition, the output voltage can be smoothed with minimum disturbance. A quad sample-and-hold amplifier, SMP04, has been used to illustrate the deglitching result (see Figure 36).

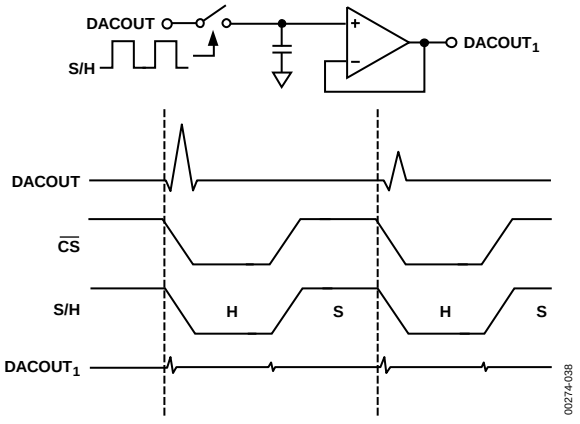



*Figure 37. Data Output (Read Timing)*

## REFERENCE INPUTS

All four DACs share common reference high ($V_{REFH}$) and reference low ($V_{REFL}$) inputs. The voltages applied to these reference inputs set the output high and low voltage limits of all four of the DACs. Each reference input has voltage restrictions with respect to the other reference and to the power supplies. The $V_{REFL}$ can be set at any voltage between $V_{SS}$ and $V_{REFH}$ − 2.5 V, and $V_{REFH}$ can be set to any value between $+V_{DD}$ − 2.5 V and $V_{REFL}$ + 2.5 V. Note that because of these restrictions, the DAC8412 references cannot be inverted (that is, $V_{REFL}$ cannot be greater than $V_{REFH}$).

It is important to note that the DAC8412 $V_{REFH}$ input both sinks and sources current. In addition, the input current of both $V_{REFH}$ and $V_{REFL}$ are code-dependent. Many references have limited current-sinking capability and must be buffered with an amplifier to drive $V_{REFH}$. The $V_{REFL}$ has no such special requirements.

It is recommended that the reference inputs be bypassed with 0.2 µF capacitors when operating with ±10 V references. This limits the reference bandwidth.

## DIGITAL I/O

See Table 6 for the digital control logic truth table. Digital I/O consists of a 12-bit bidirectional data bus, two registers select inputs, A0 and A1, a R/$\overline{W}$ input, a $\overline{RESET}$ input, a chip select ($\overline{CS}$), and a load DAC ($\overline{LDAC}$) input. Control of the DACs and bus direction is determined by these inputs as shown in Table 6. Digital data bits are labeled with the MSB defined as Data Bit 11 and the LSB as Data Bit 0. All digital pins are TTL/CMOS compatible.

See Figure 38 for a simplified I/O logic diagram. The register select inputs A0 and A1 select individual DAC registers A (Binary Code 00) through D (Binary Code 11). Decoding of the registers is enabled by the $\overline{CS}$ input. When $\overline{CS}$ is high, no decoding takes place, and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the asynchronous $\overline{LDAC}$ input. By taking $\overline{LDAC}$ low while $\overline{CS}$ is enabled, all output registers can be updated simultaneously. Note that the $t_{LDW}$ required pulse width for updating all DACs is a minimum of 170 ns.

The R/$\overline{W}$ input, when enabled by $\overline{CS}$, controls the writing to and reading from the input register.

## CODING

Both DAC8412/DAC8413 use binary coding. The output voltage can be calculated by

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \times N}{4096}$$

where *N* is the digital code in decimal.

## $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ function can be used either at power-up or at any time during DAC operation. The $\overline{\text{RESET}}$ function is independent of $\overline{\text{CS}}$. This pin is active low and sets the DAC output registers to either center code for the DAC8412, or zero code for the DAC8413. The reset-to-center code is most useful when the DAC is configured for bipolar references and an output of 0 V after reset is desired.

## SUPPLIES

Supplies required are $V_{SS}$, $V_{DD}$, and $V_{LOGIC}$. The $V_{SS}$ supply can be set between −15 V and 0 V. $V_{DD}$ is the positive supply; its operating range is between 5 V and 15 V.

$V_{LOGIC}$ is the digital output supply voltage for the readback function. It is normally connected to +5 V. This pin is a logic reference input only. It does not supply current to the device. If the readback function is not being used, $V_{LOGIC}$ can be left open-circuit. While $V_{LOGIC}$ does not supply current to the DAC8412, it does supply currents to the digital outputs when readback is used.

## AMPLIFIERS

Unlike many voltage output DACs, the DAC8412 features buffered voltage outputs. Each output is capable of both sourcing and sinking 5 mA at ±10 V, eliminating the need for external amplifiers when driving 500 pF or smaller capacitive load in most applications. These amplifiers are short-circuit protected.

**Table 6. DAC8412/DAC8413 Logic Table**

| A1 | A0 | R/$\overline{\text{W}}$ | $\overline{\text{CS}}$ | $\overline{\text{RS}}$ | $\overline{\text{LDAC}}$ | Input Register | Output Register | Mode | DAC |
|---|---|---|---|---|---|---|---|---|---|
| L | L | L | L | H | L | Write | Write | Transparent | A |
| L | H | L | L | H | L | Write | Write | Transparent | B |
| H | L | L | L | H | L | Write | Write | Transparent | C |
| H | H | L | L | H | L | Write | Write | Transparent | D |
| L | L | L | L | H | H | Write | Hold | Write input | A |
| L | H | L | L | H | H | Write | Hold | Write input | B |
| H | L | L | L | H | H | Write | Hold | Write input | C |
| H | H | L | L | H | H | Write | Hold | Write input | D |
| L | L | H | L | H | H | Read | Hold | Read input | A |
| L | H | H | L | H | H | Read | Hold | Read input | B |
| H | L | H | L | H | H | Read | Hold | Read input | C |
| H | H | H | L | H | H | Read | Hold | Read input | D |
| X | X | X | H | H | L | Hold | Update all output registers | | All |
| X | X | X | H | H | H | Hold | Hold | Hold | All |
| X | X | X | X | L | X | All registers reset to midscale/zero-scale[1] | | | All |
| X | X | X | H | ↓ | X | All registers latched to midscale/zero-scale[1] | | | All |

[1] DAC8412 resets to midscale, and DAC8413 resets to zero scale. L = logic low; H = logic high; X = don't care. Input and output registers are transparent when asserted.

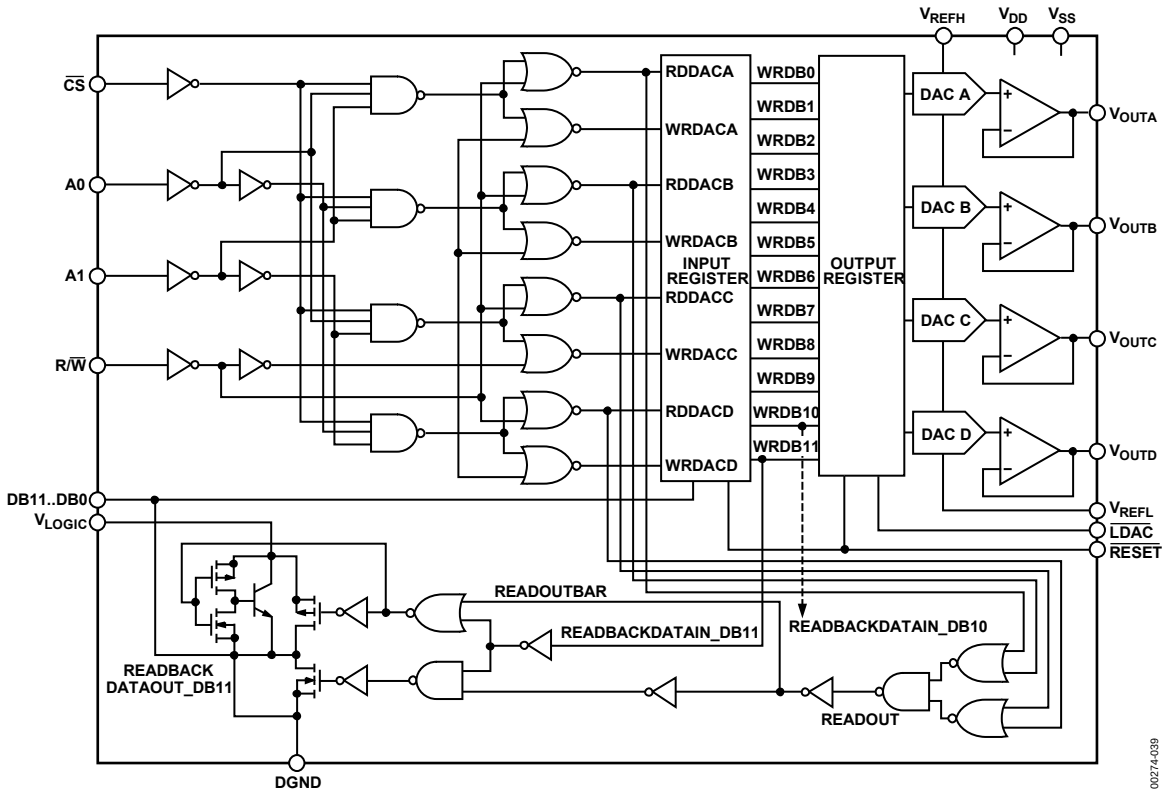



*Figure 38. Simplified I/O Logic Diagram*

Careful attention to grounding is important for accurate operation of the DAC8412. This is not because the DAC8412 is more sensitive than other 12-bit DACs, but because with four outputs and two references, there is greater potential for ground loops. Because the DAC8412 has no analog ground, the ground must be specified with respect to the reference.

## REFERENCE CONFIGURATIONS

Output voltage ranges can be configured as either unipolar or bipolar, and within these choices, a wide variety of options exists. The unipolar configuration can be either positive or negative voltage output, and the bipolar configuration can be either symmetrical or nonsymmetrical.

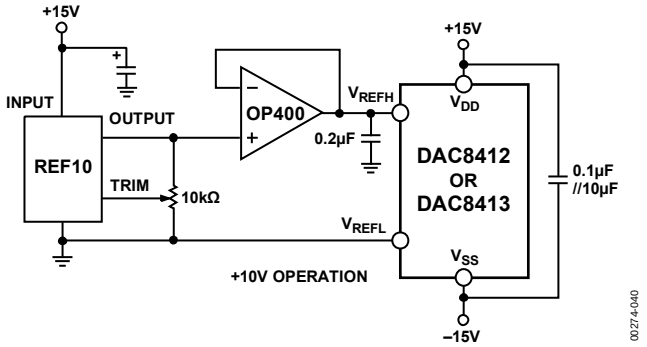



*Figure 39. Unipolar +10 V Operation*

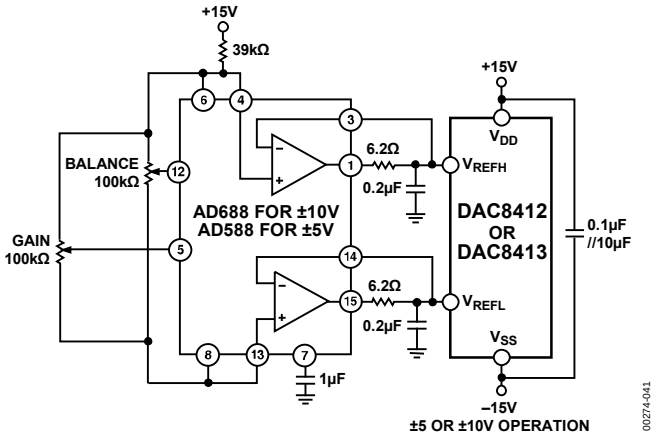



*Figure 40. Symmetrical Bipolar Operation*

Figure 40 (symmetrical bipolar operation) shows the DAC8412 configured for ±10 V operation. See the AD688 data sheet for a full explanation of reference operation. Adjustments may not be required for many applications since the AD688 is a very high accuracy reference. However, if additional adjustments are required, adjust the DAC8412 full scale first. Begin by loading the digital full-scale code (0xFFF), and then adjust the gain adjust potentiometer to attain a DAC output voltage of 9.9976 V. Then, adjust the balance adjust to set the center-scale output voltage to 0.000 V.

The 0.2 µF bypass capacitors shown at the reference inputs in Figure 40 should be used whenever ±10 V references are used. Applications with single references or references to ±5 V may not require the 0.2 µF bypassing. The 6.2 Ω resistor in series with the output of the reference amplifier keeps the amplifier from oscillating with the capacitive load. This 6.2 Ω resistor has been found to be large enough to stabilize this circuit. Larger resistor values are acceptable, provided that the drop across the resistor does not exceed $V_{BE}$. Assuming a minimum $V_{BE}$ of 0.6 V and a maximum current of 2.75 mA, then the resistor should be under 200 Ω for the loading of a single DAC8412.

Using two separate references is not recommended. Having two references can cause different drifts with time and temperature; whereas with a single reference, most drifts track.

Unipolar positive full-scale operation can usually be set with a reference with the correct output voltage. This is preferable to using a reference and dividing down to the required value. For a 10 V full-scale output, the circuit can be configured as shown in Figure 41. In this configuration, the full-scale value is set first by adjusting the 10 kΩ resistor for a full-scale output of 9.9976 V.

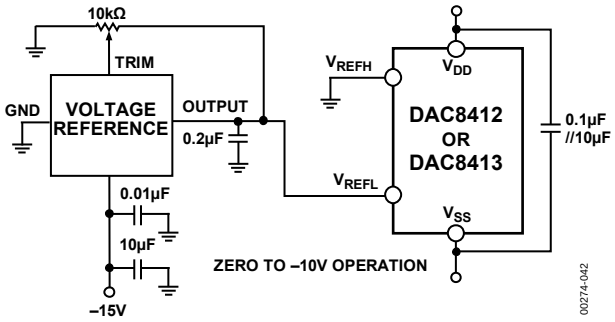



*Figure 41. Unipolar –10 V Operation*

Figure 41 shows the DAC8412 configured for –10 V to 0 V operation. A –10 V full-scale output voltage reference is connected directly to $V_{REFL}$ for the reference voltage.

## SINGLE +5 V SUPPLY OPERATION

For operation with a 5 V supply, the reference voltage should be set between 1.0 V and 2.5 V for optimum linearity. Figure 42 shows a REF43 used to supply a 2.5 V reference voltage. The headroom of the reference and DAC are both sufficient to support a 5 V supply with ±5% tolerance. $V_{DD}$ and $V_{LOGIC}$ should be connected to the same supply. Separate bypassing to each pin should also be used.

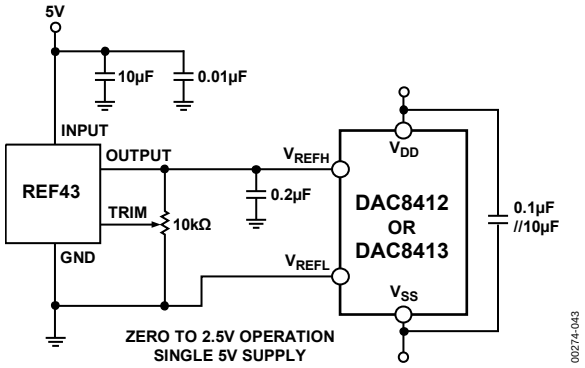
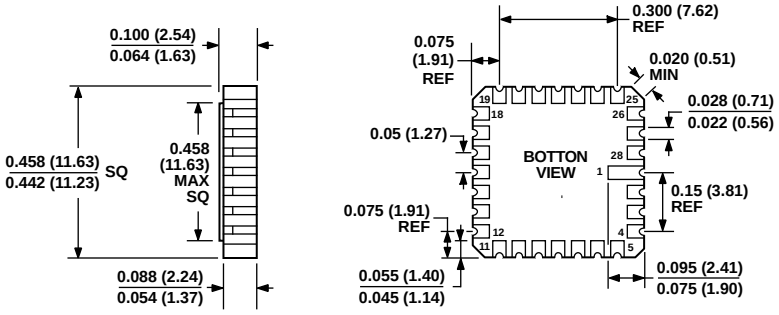



*Figure 42. +5 V Single-Supply Operation*

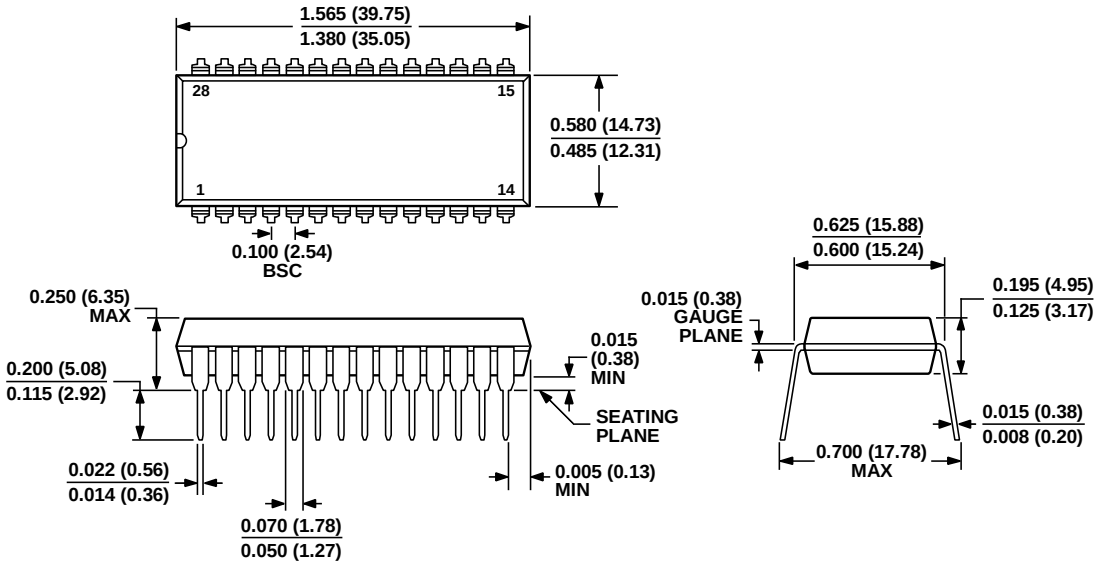
# OUTLINE DIMENSIONS




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

022106-A

*Figure 43. 28-Terminal Ceramic Leadless Chip Carrier [LCC]*
*(E-28-1)*
*Dimensions shown in inches and (millimeters)*

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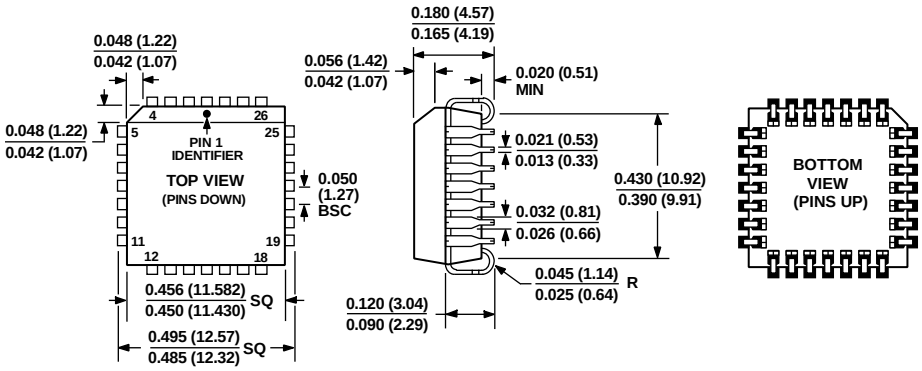
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

*Figure 44. 28-Lead Plastic Dual In-Line Package [PDIP]*
*Wide Body*
*(N-28-2)*
*Dimensions shown in inches and (millimeters)*




COMPLIANT TO JEDEC STANDARDS MO-047-AB
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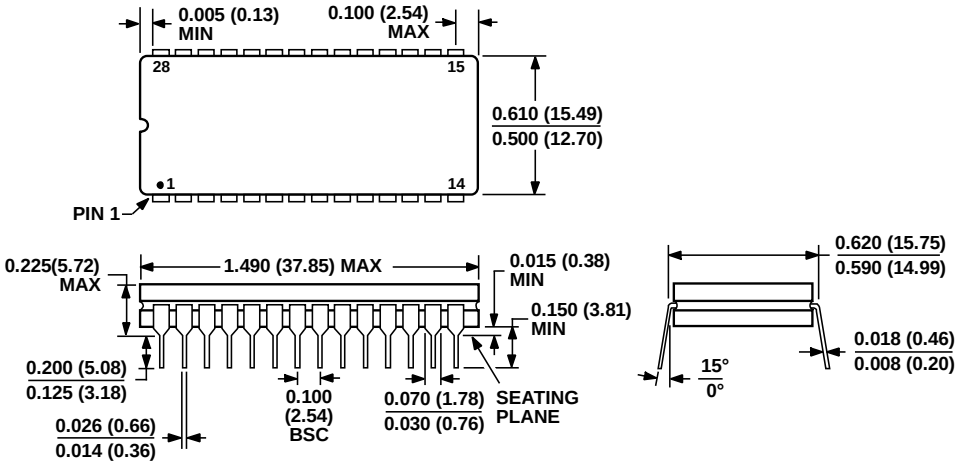
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

042508-A

*Figure 45. 28-Lead Plastic Leaded Chip Carrier [PLCC]*
*(P-28)*
*Dimensions shown in inches and (millimeters)*




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

030106-A

*Figure 46. 28-Lead Ceramic Dual In-Line Package [CERDIP]*
*(Q-28-2)*
*Dimensions shown in inches and (millimeters)*

## ORDERING GUIDE

| Model[1] | Notes | Temperature Range | INL | Package Description | Package Option |
|---|---|---|---|---|---|
| DAC8412AT/883C | | −55°C to +125°C | ±0.75 | 28-Lead Ceramic Dual In-Line Package [CERDIP] | Q-28-2 |
| DAC8412BT/883C | | −55°C to +125°C | ±1.5 | 28-Lead Ceramic Dual In-Line Package [CERDIP] | Q-28-2 |
| DAC8412BTC/883C | | −55°C to +125°C | ±1.5 | 28-Terminal Ceramic Leadless Chip Carrier [LCC] | E-28-1 |
| DAC8412EP | [2] | −40°C to +85°C | ±0.5 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8412EPZ | [2] | −40°C to +85°C | ±0.5 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8412FP | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8412FPC | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8412FPC-REEL | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8412FPCZ | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8412FPCZ-REEL | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8412FPZ | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8413AT/883C | | −55°C to +125°C | ±0.75 | 28-Lead Ceramic Dual In-Line Package [CERDIP] | Q-28-2 |
| DAC8413BT/883C | | −55°C to +125°C | ±1.5 | 28-Lead Ceramic Dual In-Line Package [CERDIP] | Q-28-2 |
| DAC8413BTC/883C | | −55°C to +125°C | ±1.5 | 28-Terminal Ceramic Leadless Chip Carrier [LCC] | E-28-1 |
| DAC8413EP | [2] | −40°C to +85°C | ±0.5 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8413EPZ | [2] | −40°C to +85°C | ±0.5 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8413FP | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8413FPC | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8413FPC-REEL | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8413FPCZ | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Leaded Chip Carrier [PLCC] | P-28 |
| DAC8413FPC-REEL | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |
| DAC8413FPZ | [2] | −40°C to +85°C | ±1 | 28-Lead Plastic Dual In-Line Package [PDIP] | N-28-2 |

[1] Z = RoHS Compliant Part.
[2] If burn-in is required, these models are available in CERDIP. Contact sales.