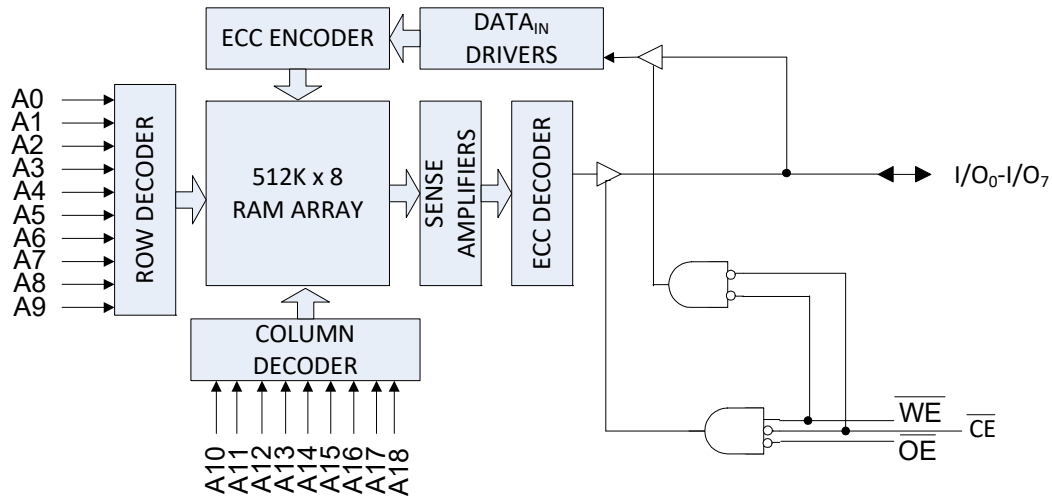
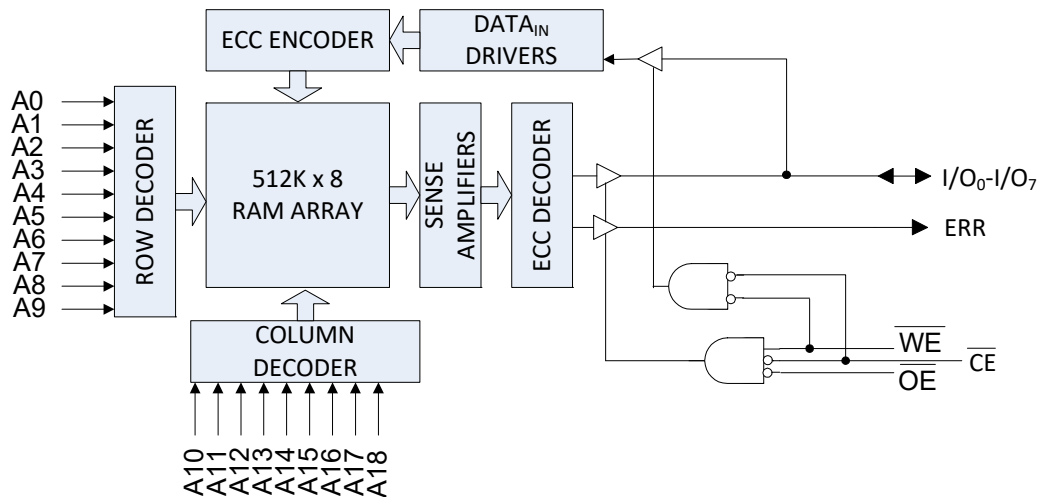


## Logic Block Diagram – CY7C1049G



## Logic Block Diagram – CY7C1049GE

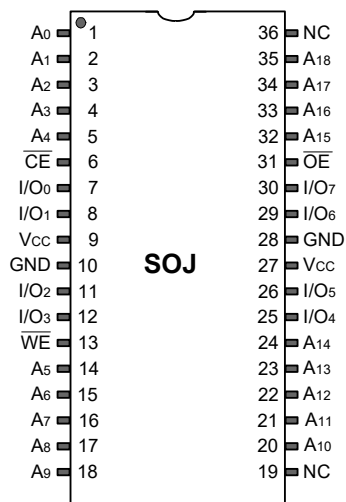


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## Pin Configurations

Figure 1. 36-pin SOJ pinout, Single Chip Enable without ERR - CY7C1049G <sup>[5]</sup>

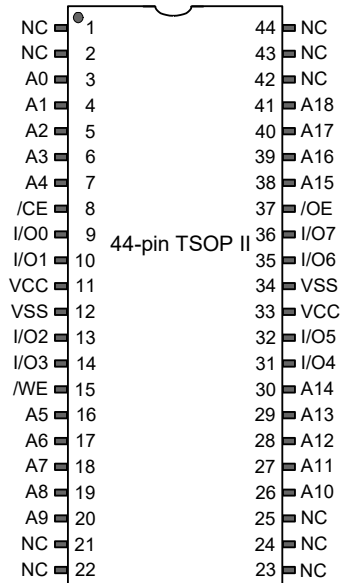


### Note

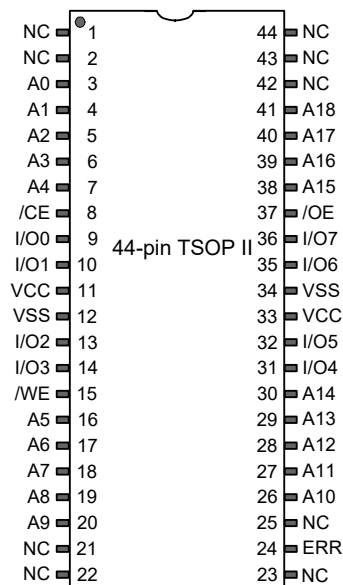
5. NC pins are not connected internally to the die.

## Pin Configurations (continued)

**Figure 2. 44-pin TSOP II pinout, Single Chip Enable without ERR - CY7C1049G** [6]



**Figure 3. 44-pin TSOP II pinout, Single Chip Enable with ERR - CY7C1049GE** [6, 7]



### Notes

6. NC pins are not connected internally to the die.
7. ERR is an output pin.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on  $V_{CC}$  relative to GND <sup>[8]</sup> ..... -0.5 to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in HI-Z State <sup>[8]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[8]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (in LOW state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description		Test Conditions	10 ns / 15 ns			Unit
				Min	Typ <sup>[9]</sup>	Max	
$V_{OH}$	Output HIGH voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	1.4	—	—	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2	—	—	
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.2	—	—	
		3.0 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5$ <sup>[10]</sup>	—	—	
$V_{OL}$	Output LOW voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	—	—	0.2	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 2 \text{ mA}$	—	—	0.4	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$	—	—	0.4	
$V_{IH}$	Input HIGH voltage	1.65 V to 2.2 V	—	1.4	—	$V_{CC} + 0.2$ <sup>[8]</sup>	V
		2.2 V to 2.7 V	—	2	—	$V_{CC} + 0.3$ <sup>[8]</sup>	
		2.7 V to 3.6 V	—	2	—	$V_{CC} + 0.3$ <sup>[8]</sup>	
		4.5 V to 5.5 V	—	2	—	$V_{CC} + 0.5$ <sup>[8]</sup>	
$V_{IL}$	Input LOW voltage	1.65 V to 2.2 V	—	-0.2 <sup>[8]</sup>	—	0.4	V
		2.2 V to 2.7 V	—	-0.3 <sup>[8]</sup>	—	0.6	
		2.7 V to 3.6 V	—	-0.3 <sup>[8]</sup>	—	0.8	
		4.5 V to 5.5 V	—	-0.5 <sup>[8]</sup>	—	0.8	
$I_{IX}$	Input leakage current		$\text{GND} \leq V_{IN} \leq V_{CC}$	-1	—	+1	μA
$I_{OZ}$	Output leakage current		$\text{GND} \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1	—	+1	μA
$I_{CC}$	Operating supply current		Max $V_{CC}$ , $I_{OUT} = 0 \text{ mA}$ , CMOS levels	f = 100 MHz	—	38	mA
				f = 66.7 MHz	—	40	
$I_{SB1}$	Automatic CE power-down current – TTL inputs		Max $V_{CC}$ , $\overline{\text{CE}} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , f = $f_{MAX}$	—	—	15	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs		Max $V_{CC}$ , $\overline{\text{CE}} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , f = 0	—	6	8	mA

### Notes

8.  $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8 \text{ V}$  (for  $V_{CC}$  range of 1.65 V – 2.2 V),  $V_{CC} = 3 \text{ V}$  (for  $V_{CC}$  range of 2.2 V – 3.6 V), and  $V_{CC} = 5 \text{ V}$  (for  $V_{CC}$  range of 4.5 V – 5.5 V),  $T_A = 25 \text{ °C}$ .

10. This parameter is guaranteed by design and not tested.

## Capacitance

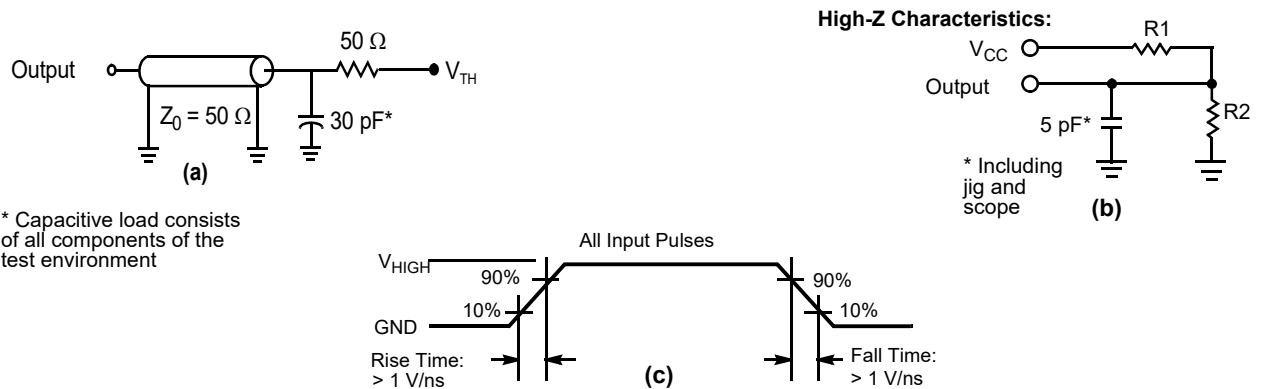
Parameter <sup>[11]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC}(\text{typ})$	10	10	pF
$C_{OUT}$	I/O capacitance		10	10	pF

## Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	68.85	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		31.48	15.97	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms<sup>[12]</sup>



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	$\Omega$
R2	1538	351	351	$\Omega$
$V_{TH}$	0.9	1.5	1.5	V
$V_{HIGH}$	1.8	3	3	V

### Notes

11. Tested initially and after any design or process changes that may affect these parameters.
12. Full-device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC}(\text{min})$  and a 100- $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.

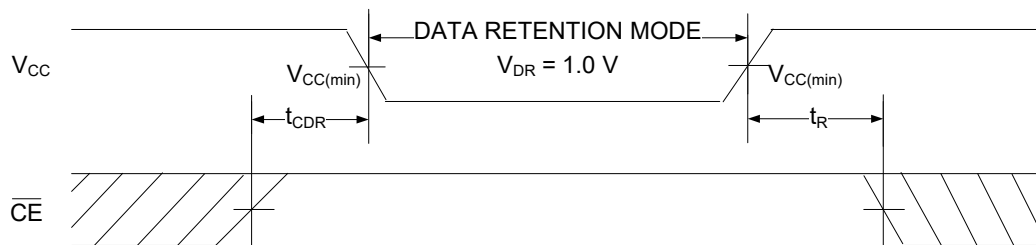
## Data Retention Characteristics

Over the operating range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ <sup>[14]</sup> , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ , or $V_{IN} \leq 0.2\text{ V}$	–	8	mA
$t_{CDR}$ <sup>[13]</sup>	Chip deselect to data retention time		0	–	ns
$t_R$ <sup>[13, 14]</sup>	Operation recovery time	$V_{CC} \geq 2.2\text{ V}$	10	–	ns
		$V_{CC} < 2.2\text{ V}$	15	–	ns

## Data Retention Waveform

Figure 5. Data Retention Waveform<sup>[14]</sup>



### Notes

13. These parameters are guaranteed by design.

14. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the operating range of -40 °C to 85 °C

Parameter <sup>[15]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>RC</sub>	Read cycle time	10	–	15	–	ns
t <sub>AA</sub>	Address to data / ERR valid	–	10	–	15	ns
t <sub>OHA</sub>	Data / ERR hold from address change	3	–	3	–	ns
t <sub>ACE</sub>	CE LOW to data / ERR valid	–	10	–	15	ns
t <sub>DOE</sub>	OE LOW to data / ERR valid	–	4.5	–	8	ns
t <sub>LZOE</sub>	OE LOW to low impedance <sup>[16]</sup>	0	–	0	–	ns
t <sub>HZOE</sub>	OE HIGH to HI-Z <sup>[16]</sup>	–	5	–	8	ns
t <sub>LZCE</sub>	CE LOW to low impedance <sup>[16]</sup>	3	–	3	–	ns
t <sub>HZCE</sub>	CE HIGH to HI-Z <sup>[16]</sup>	–	5	–	8	ns
t <sub>PU</sub>	CE LOW to power-up <sup>[17, 18]</sup>	0	–	0	–	ns
t <sub>PD</sub>	CE HIGH to power-down <sup>[17, 18]</sup>	–	10	–	15	ns
Write Cycle <sup>[18, 19]</sup>						
t <sub>WC</sub>	Write cycle time	10	–	15	–	ns
t <sub>SCE</sub>	CE LOW to write end	7	–	12	–	ns
t <sub>AW</sub>	Address setup to write end	7	–	12	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	0	–	ns
t <sub>PWE</sub>	WE pulse width	7	–	12	–	ns
t <sub>SD</sub>	Data setup to write end	5	–	8	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	0	–	ns
t <sub>LZWE</sub>	WE HIGH to low impedance <sup>[16]</sup>	3	–	3	–	ns
t <sub>HZWE</sub>	WE LOW to HI-Z <sup>[16]</sup>	–	5	–	8	ns

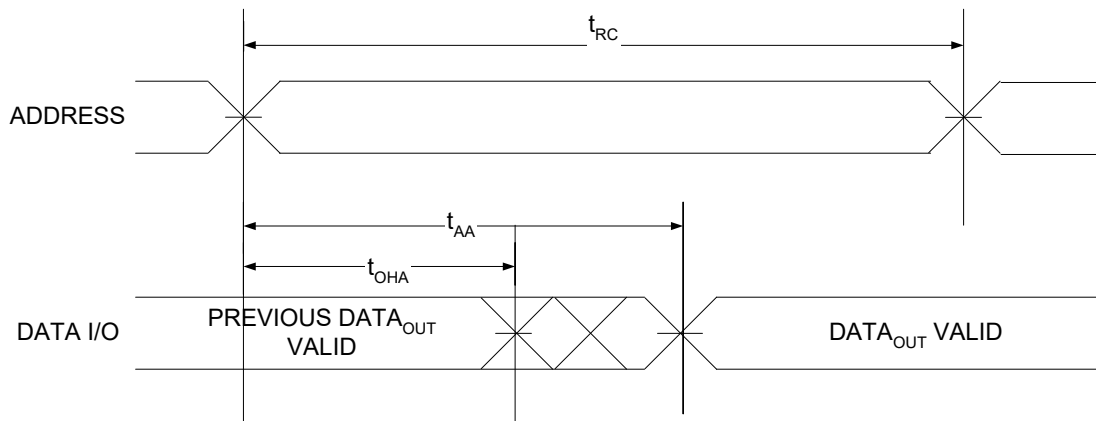
### Notes

15. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 4 on page 7, unless specified otherwise.
16.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{LZWE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ , and  $t_{LZWE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 4 on page 7. Transition is measured  $\pm 200$  mV from steady state voltage.
17. These parameters are guaranteed by design and are not tested.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width in Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{DS}$  and  $t_{HZWE}$ .

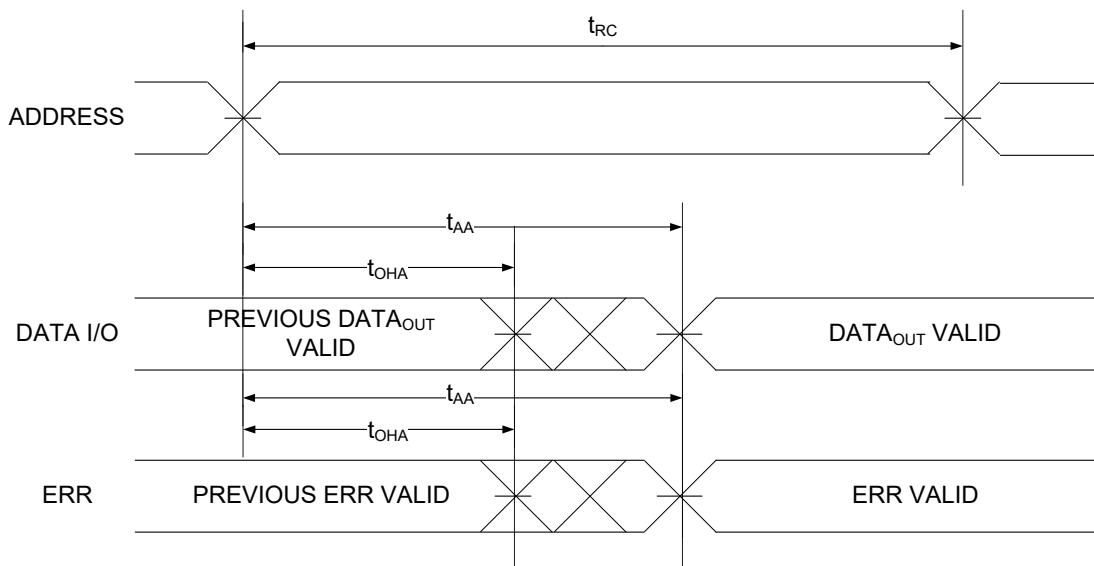


## Switching Waveforms

**Figure 6. Read Cycle No. 1 of CY7C1049G (Address Transition Controlled)** [20, 21]



**Figure 7. Read Cycle No. 1 of CY7C1049GE (Address Transition Controlled)** [20, 21]



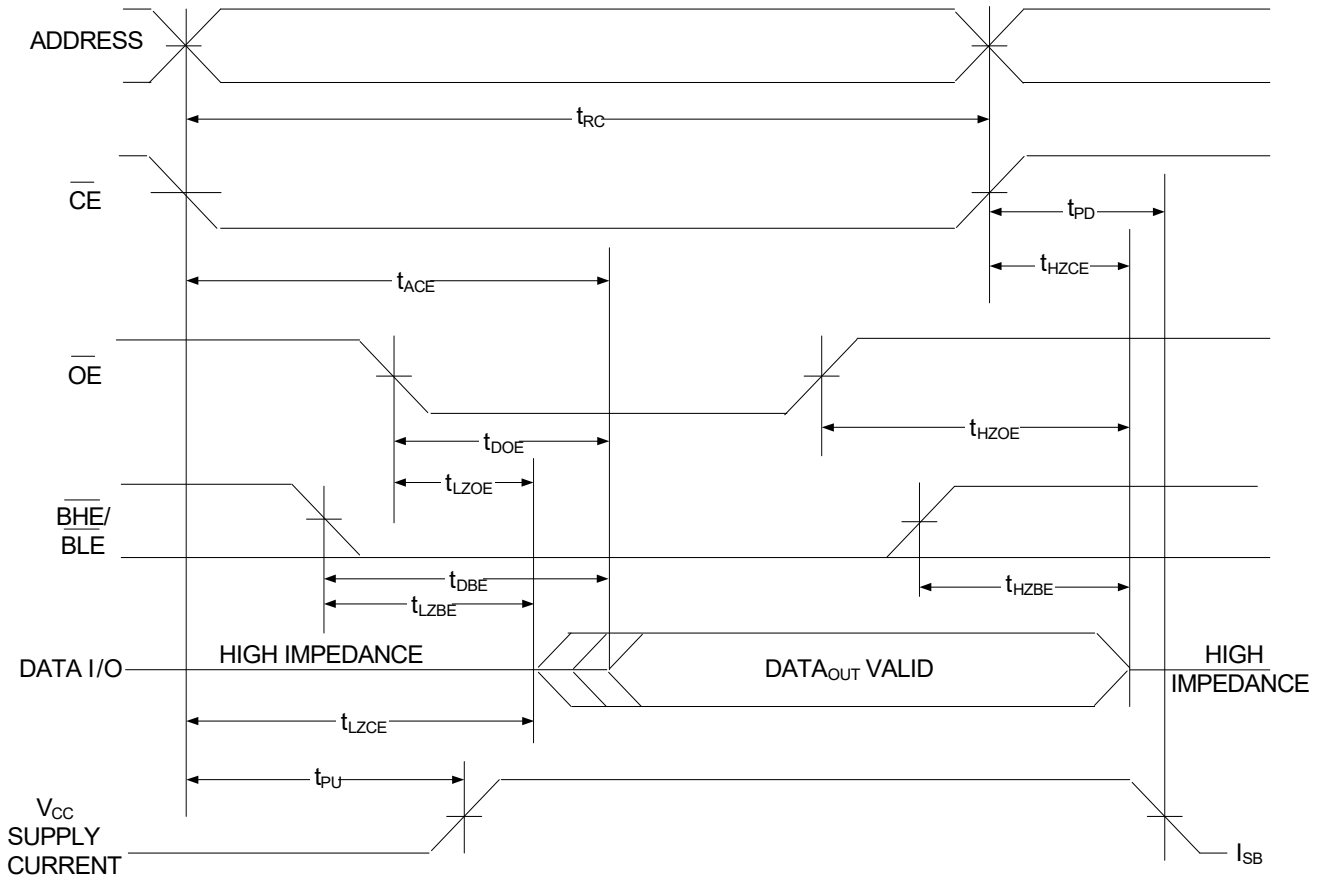
### Notes

20. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ .

21.  $\overline{WE}$  is HIGH for the read cycle.

## Switching Waveforms (continued)

**Figure 8. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [22, 23]



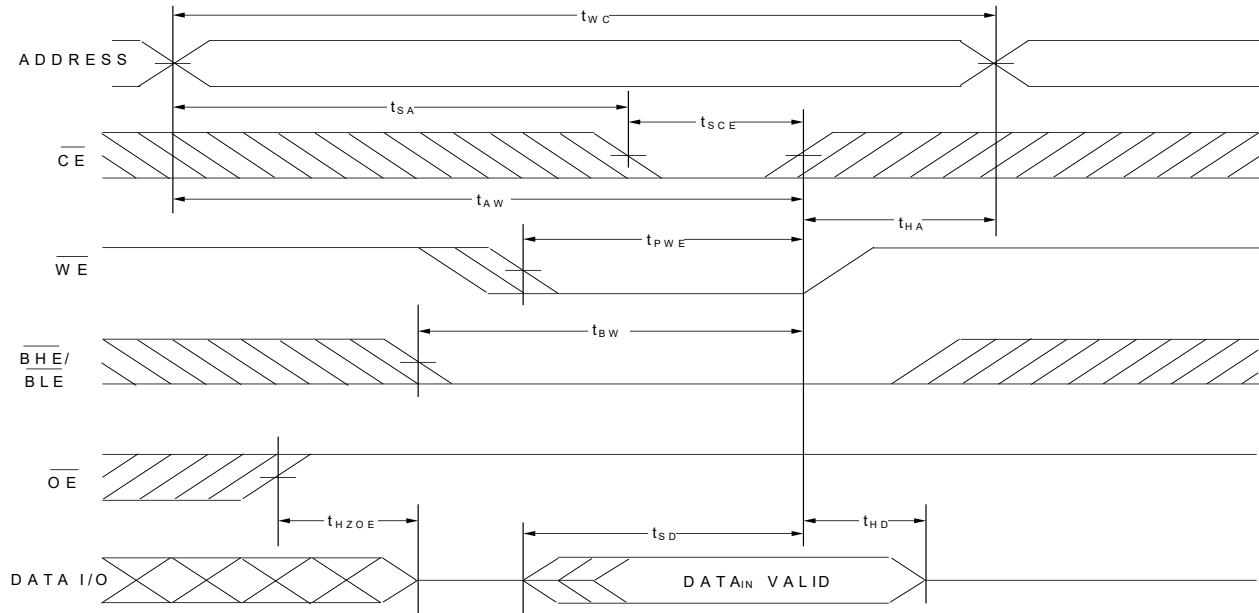
### Notes

22.  $\overline{\text{WE}}$  is HIGH for the read cycle.

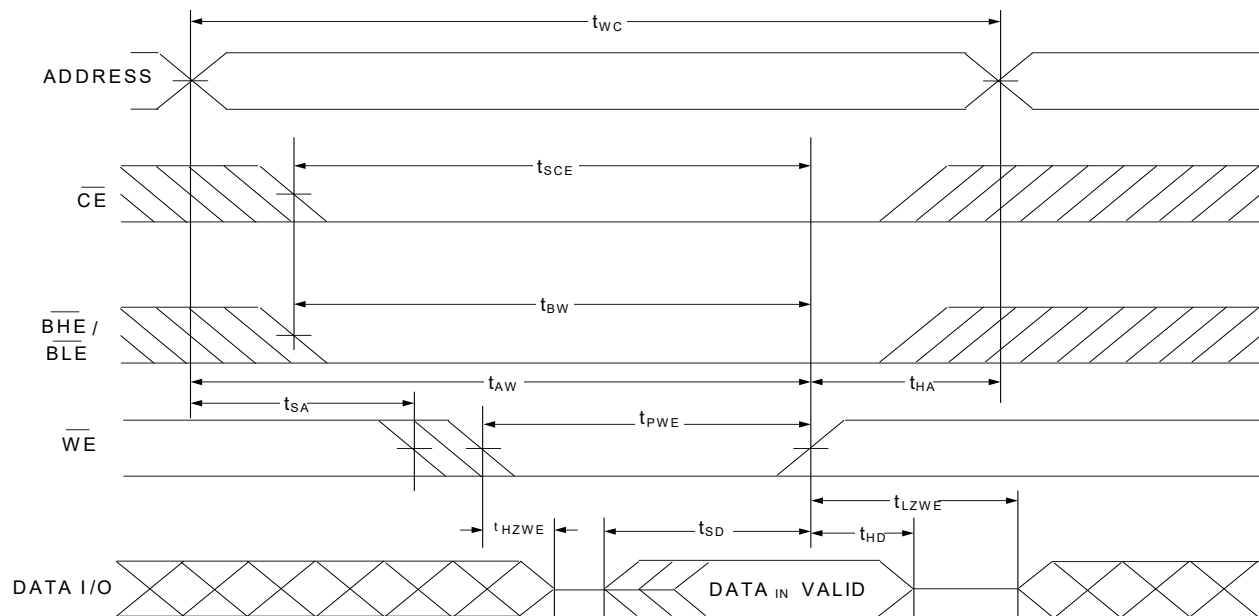
23. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)** [24, 25]



**Figure 10. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)** [24, 25, 26]



### Notes

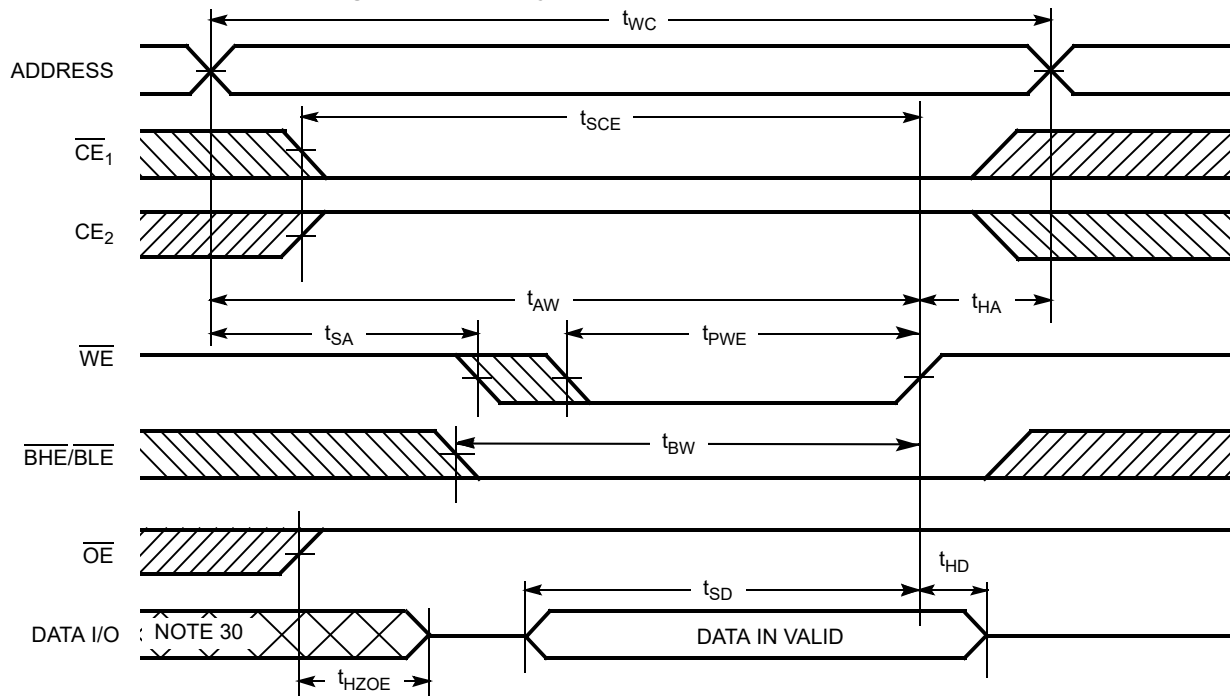
24. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$ .

26. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms (continued)

**Figure 11. Write Cycle No. 3 ( $\overline{WE}$  Controlled)** [27, 28, 29]



### Notes

27. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
28. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ .
29. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
30. During this period the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X <sup>[31]</sup>	X <sup>[31]</sup>	HI-Z	Power down	Standby (I <sub>SB</sub> )
L	L	H	Data out	Read all bits	Active (I <sub>CC</sub> )
L	X	L	Data in	Write all bits	Active (I <sub>CC</sub> )
L	H	H	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

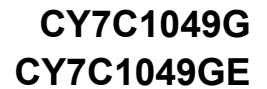
## ERR Output – CY7C1049GE

Output <sup>[32]</sup>	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
HI-Z	Device deselected or outputs disabled or Write operation.

### Notes

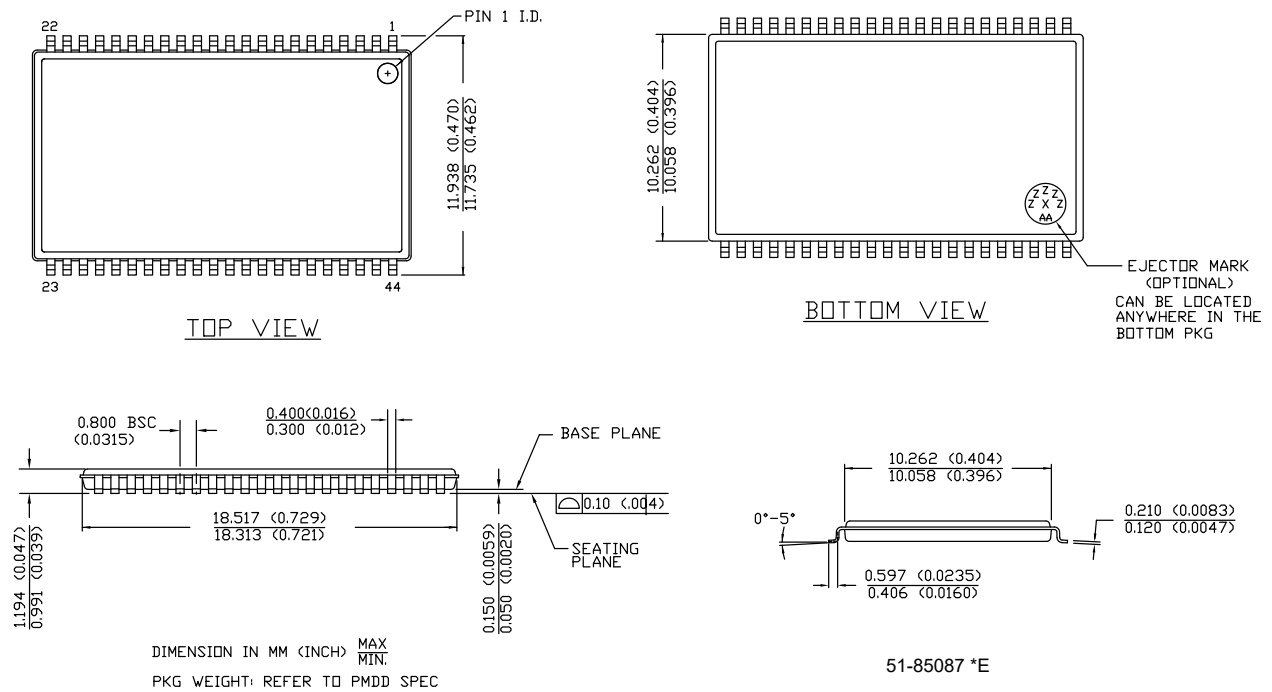
31. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

32. ERR pin is an output pin. It should be left floating when not used.

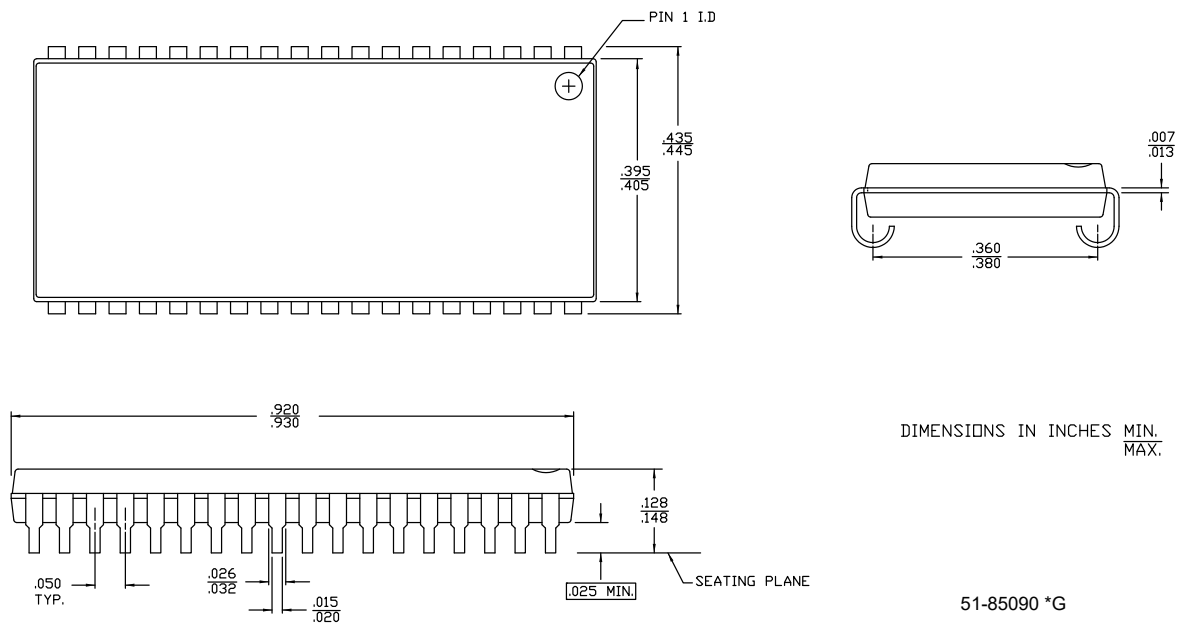


## Package Diagrams

**Figure 12. 44-pin TSOP II Package Outline, 51-85087**



**Figure 13. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090**



## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degrees Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Document History Page

Document Title: CY7C1049G/CY7C1049GE, 4-Mbit (512K words × 8-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95412				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	4685774	VINI	03/13/2015	New data sheet.
*A	4831087	NILE	07/10/2015	Updated <a href="#">Package Diagrams</a> : Added spec 51-85090 *G ( <a href="#">Figure 13</a> ). Removed spec 51-85082 *E. Removed spec 51-85150 *H.
*B	4968879	NILE	10/16/2015	Fixed typo in bookmarks.
*C	5020573	VINI	11/25/2015	Changed status from Preliminary to Final. Updated <a href="#">Pin Configurations</a> : Removed figure "36-pin SOJ Single Chip Enable with ERR CY7C1049GE". Updated <a href="#">Ordering Information</a> : Updated part numbers.
*D	5429076	NILE	09/07/2016	Updated <a href="#">Maximum Ratings</a> : Updated Note 8 (Replaced "2 ns" with "20 ns"). Updated <a href="#">DC Electrical Characteristics</a> : Removed Operating Range "2.7 V to 3.6 V" and all values corresponding to V <sub>OH</sub> parameter. Included Operating Ranges "2.7 V to 3.0 V" and "3.0 V to 3.6 V" and all values corresponding to V <sub>OH</sub> parameter. Changed minimum value of V <sub>IH</sub> parameter from 2.2 V to 2 V corresponding to Operating Range "4.5 V to 5.5 V". Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template.
*E	5725349	AESATMP7	05/03/2017	Updated Cypress Logo and Copyright.
*F	6118848	NILE	04/03/2018	Updated <a href="#">Features</a> : Added Note 2 and referred the same note in "Embedded ECC for single-bit error correction". Updated to new template. Completing Sunset Review.

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