CY29946

2.5 V or 3.3 V, 200 MHz, 1:10 Clock Distribution Buffer

Features

- 2.5 V or 3.3 V operation
- 200 MHz clock support
- Two LVCMOS-/LVTTL-compatible inputs
- Ten clock outputs: drive up to 20 clock lines
- 1× or 1/2× configurable outputs
- Output three-state control
- 250-ps max output-to-output skew
- Pin-compatible with MPC946, MPC9446
- Available in commercial and industrial temperature range
- 32-pin TQFP package

Functional Description

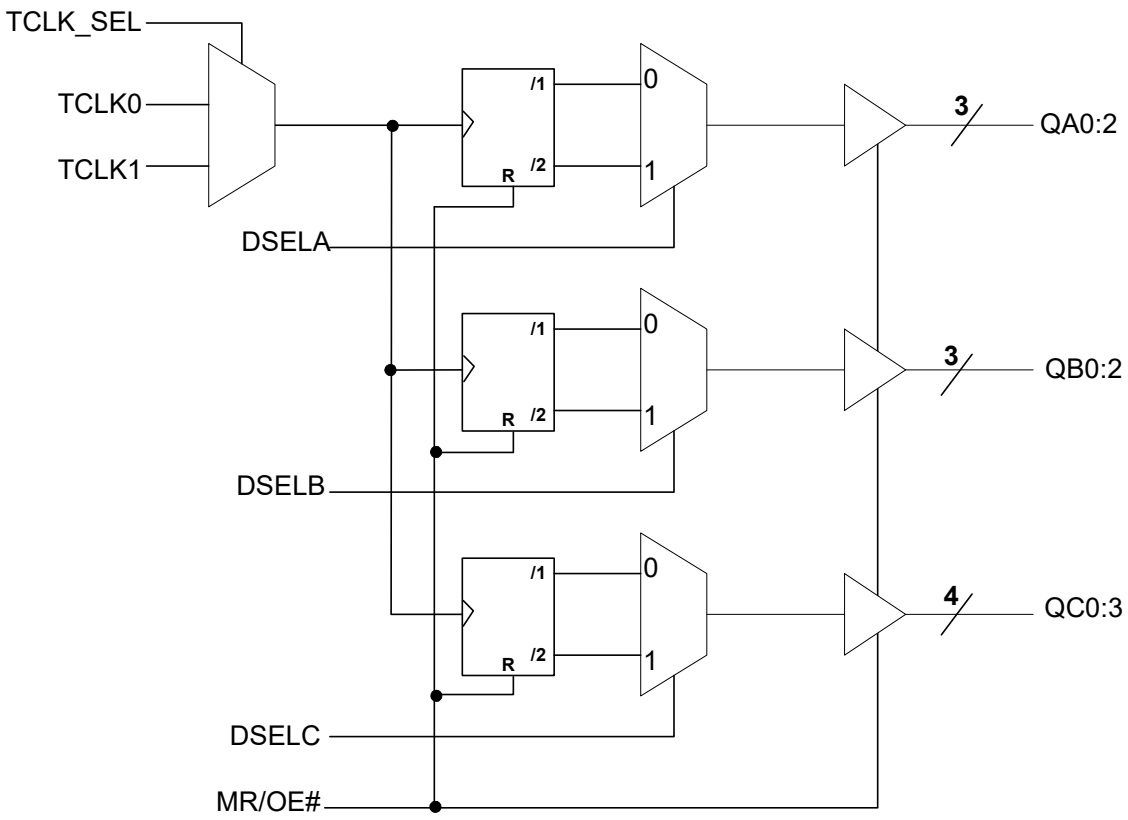
The CY29946 is a low-voltage 200-MHz clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 10 outputs are LVCMOS or LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:20.

The CY29946 is capable of generating 1× and 1/2× signals from a 1× source. These signals are generated and retimed internally to ensure minimal skew between the 1× and 1/2× signals. SEL(A:C) inputs allow flexibility in selecting the ratio of 1× to1/2× outputs.

The CY29946 outputs can also be three-stated via MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

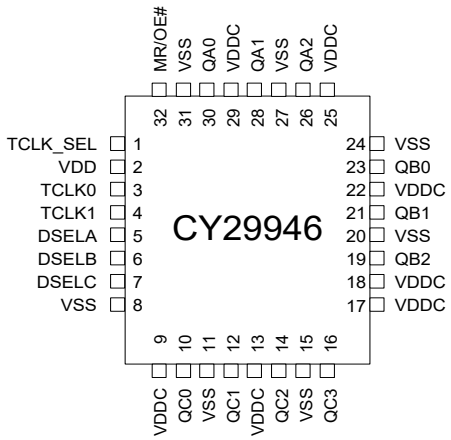
For a complete list of related documentation, click here.

Block Diagram



Not Recommended for New Designs

Pin Configuration



Pin Description

Pin	Name	PWR	I/O [1]	Description
3, 4	TCLK(0,1)		I, PU	External Reference/Test Clock Input
26, 28, 30	QA(2:0)	VDDC	O	Clock Outputs
19, 21, 23	QB(2:0)	VDDC	O	Clock Outputs
10, 12, 14, 16	QC(0:3)	VDDC	O	Clock Outputs
5, 6, 7	DSEL(A:C)		I, PD	**Divider Select Inputs**. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
1	TCLK_SEL		I, PD	**TCLK Select Input**. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
32	MR/OE#		I, PD	**Output Enable Input**. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 Bank is being used in /2 Mode, a reset must be performed (MR/OE# Asserted High) after power-up to ensure all internal flip-flops are set to the same state.
9, 13, 17, 18, 22, 25, 29	VDDC			2.5 V or 3.3 V Power Supply for Output Clock Buffers
2	VDD			2.5 V or 3.3 V Power Supply
8, 11, 15, 20, 24, 27, 31	VSS			Common Ground

Note
1. PD = Internal pull-down. PU = Internal pull-up.

Absolute Maximum Conditions[2]

Maximum Input Voltage Relative to V_{SS} ..... V_{SS} – 0.3 V
Maximum Input Voltage Relative to V_{DD} ..... V_{DD} + 0.3 V
Storage Temperature ..... –65 °C to +150 °C
Operating Temperature ..... –40 °C to +85 °C
Maximum ESD protection ..... 2 kV
Maximum Power Supply ..... 5.5 V
Maximum Input Current ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications

$V_{DD} = V_{DDC}$ = 3.3 V ± 10% or 2.5 V ± 5%, over the specified temperature range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		V_{SS}	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low Current[3]		–	–	–100	µA
I_{IH}	Input High Current[3]		–	–	100	µA
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA	–	–	0.4	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3 V	2.5	–	–	V
		I_{OH} = –20 mA, V_{DD} = 2.5 V	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3 V, Outputs @ 100 MHz, C_L = 30 pF	–	130	–	mA
		V_{DD} = 3.3 V, Outputs @ 160 MHz, C_L = 30 pF	–	225	–	
		V_{DD} = 2.5 V, Outputs @ 100 MHz, C_L = 30 pF	–	95	–	
		V_{DD} = 2.5 V, Outputs @ 160 MHz, C_L = 30 pF	–	160	–	
Z_{Out}	Output Impedance	V_{DD} = 3.3 V	12	15	18	W
		V_{DD} = 2.5 V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

Notes
2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
5. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

V_{DD} = V_{DDC} = 3.3 V ± 10% or 2.5 V ± 5%, over the specified temperature range[6]

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{max}	Input Frequency[7]	V_{DD} = 3.3 V	–	–	200	MHz
		V_{DD} = 2.5 V	–	–	170	
T_{pd}	TTL_CLK To Q Delay[7]		5.0	–	11.5	ns
F_{outDC}	Output Duty Cycle[7, 8]	Measured at V_{DD}/2	45	–	55	%
t_{pZL}, t_{pZH}	Output enable time (all outputs)		2	–	10	ns
t_{pLZ}, t_{pHZ}	Output disable time (all outputs)		2	–	10	ns
T_{skew}	Output-to-Output Skew[7, 9]		–	150	250	ps
$T_{skew(pp)}$	Part-to-Part Skew[10]		–	2.0	4.5	ns
T_r/T_f	Output Clocks Rise/Fall Time[9]	0.8 V to 2.0 V, V_{DD} = 3.3 V	0.10	–	1.0	ns
		0.6 V to 1.8 V, V_{DD} = 2.5 V	0.10	–	1.3	

Notes
6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. See Figure 1 on page 5.
10. Part-to-Part skew at a given temperature and voltage.

Figure 1. LVCMOS_CLK CY29946 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

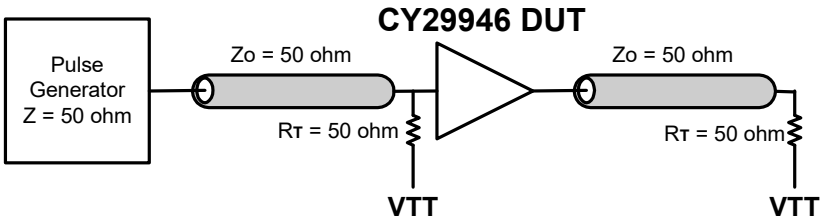


Figure 2. LVCMOS Propagation Delay (T_{PD}) Test Reference

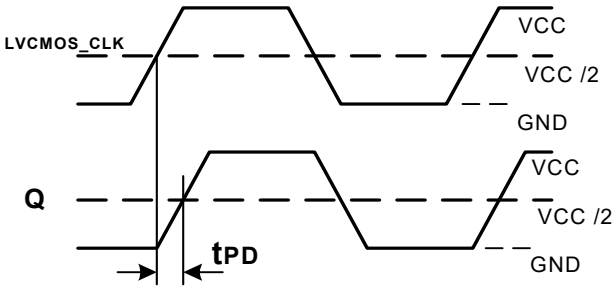


Figure 3. Output Duty Cycle (F_{outDC})

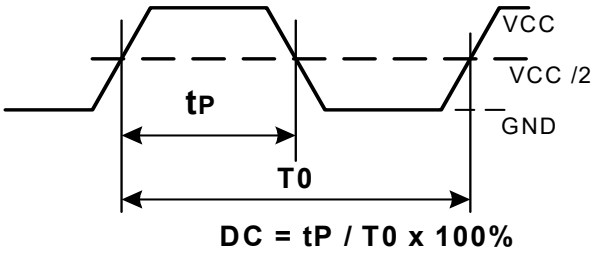
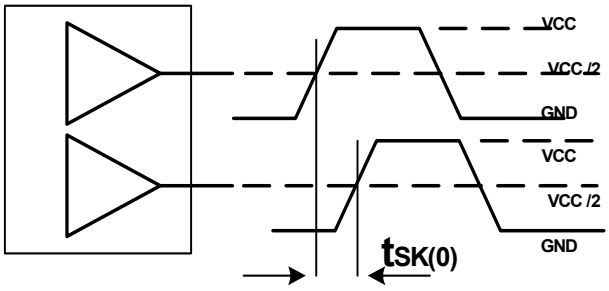


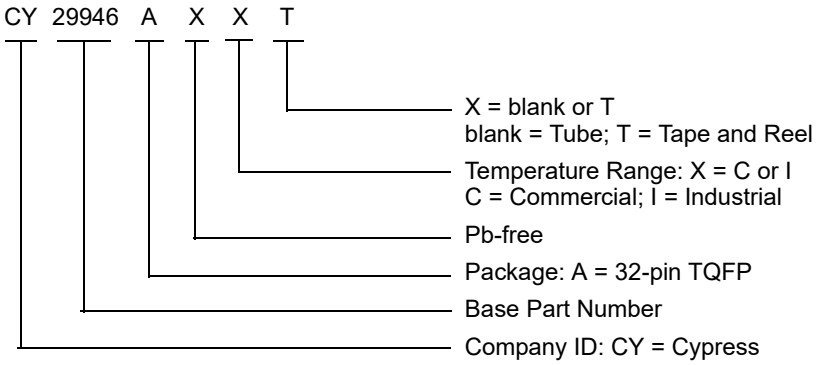
Figure 4. Output-to-Output Skew $t_{sk(0)}$



Ordering Information

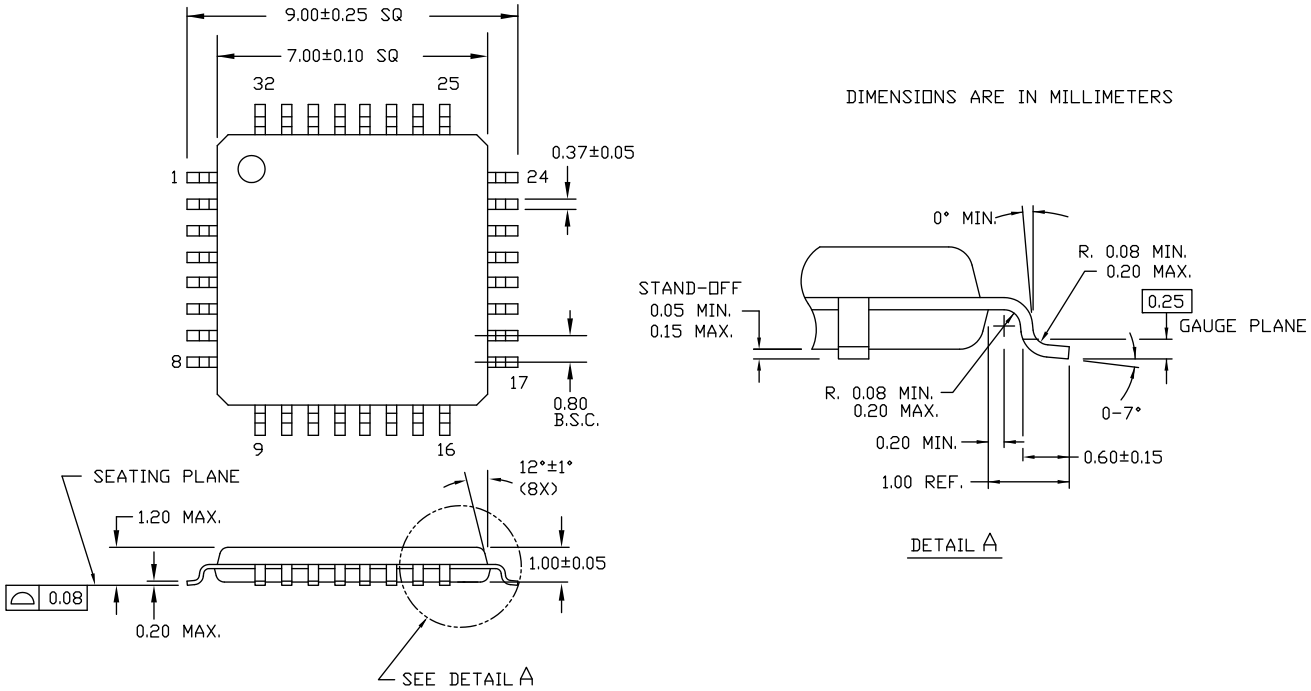
Part Number	Package Type	Production Flow
CY29946AXC	32-pin TQFP	Commercial, 0 °C to +70 °C
CY29946AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29946AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 5. 32-pin TQFP 7 × 7 × 1.0 mm A3210



51-85063 *E

Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
LVCMOS	low voltage complementary metal oxide semiconductor
LVTTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY29946, 2.5 V or 3.3 V, 200 MHz, 1:10 Clock Distribution Buffer Document Number: 38-07286			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	111097	02/07/2002	New data sheet.
*A	116780	08/15/2002	Added Commercial Temperature Range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Drawing and Dimensions: Removed existing spec. Added spec 51-85063 *B.
*B	122878	12/22/2002	Updated Absolute Maximum Conditions[2]: Added Note 2 and referred the same note in heading.
*C	130007	10/15/2003	Updated Block Diagram. Updated Pin Description: Updated details in “Description” column corresponding to MK/$\overline{OE}$ pin.
*D	131375	11/21/2003	Updated Document History Page (Revision *C): To reflect changes that were not listed.
*E	221587	04/28/2004	Minor Change: Moved up the word Block Diagram in the first page.
*F	2899714	03/26/2010	Updated Ordering Information: Updated part numbers. Updated Package Drawing and Dimensions: spec 51-85063 – Changed revision from *B to *C.
*G	3254185	05/11/2011	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	4389717	05/30/2014	Updated Package Drawing and Dimensions: spec 51-85063 – Changed revision from *C to *D. Completing Sunset Review.
*I	4586288	12/03/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*J	5270507	05/13/2016	Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85063 – Changed revision from *D to *E. Updated to new template.
*K	5754145	05/29/2017	Updated to new template. Completing Sunset Review.
*L	6903402	06/22/2020	Added watermark “Not Recommended for New Designs” across the document. Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support