TABLE OF CONTENTS

REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changes to SNR in Features Section ... 1
Added Mode IV to Table 1 and Table 1 Conditions ... 3
Added Mode IV Clock Rate Parameters and Changed t_{EH} and t_{EL} from 6.25 ns to 4.8 ns; Table 3 ... 7
Changes to Active Impedance Matching Section ... 23
Added Table 9 ... 24
Changes to Figure 56 and Figure 57 ... 28
Changes to Digital Outputs and Timing Section ... 30
Changes to 0x01 Bits[7:0] Description, Changes to 0x02 Bits[5:4] Description and Default Value; Table 19 ... 40
Updated Outline Dimensions ... 43

10/10—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature range (−40°C to +85°C), f_{IN} = 5 MHz, R_S = 50 Ω, R_{FB} = ∞ (unterminated), LNA gain = 21.3 dB, LNA bias = default, PGA gain = 24 dB, GAIN− = 0.8 V, GAIN+ = 0 V, AAF LPF cutoff = f_{SAMPLE}/3 (MODE I/II/III), AAF LPF cutoff = f_{SAMPLE}/4.5 (MODE IV), HPF cutoff = LPF cutoff/12, MODE I = f_{SAMPLE} = 40 MSPS, MODE II = f_{SAMPLE} = 25 MSPS, MODE III = f_{SAMPLE} = 50 MSPS, MODE IV = f_{SAMPLE} = 65 MSPS, low power LVDS mode, unless otherwise noted.

Table 1.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-ended input to differential output		15.6/17.9/21.3		dB
	Single-ended input to single-ended output		9.6/11.9/15.3		dB
0.1 dB Input Compression Point					
	LNA gain = 15.6 dB		1.00		V p-p
	LNA gain = 17.9 dB		0.75		V p-p
	LNA gain = 21.3 dB		0.45		V p-p
1 dB Input Compression Point					
	LNA gain = 15.6 dB		1.20		V p-p
	LNA gain = 17.9 dB		0.90		V p-p
	LNA gain = 21.3 dB		0.60		V p-p
Input Common Mode (LI-x, LG-x)			2.2		V
Output Common Mode (LO-x)					V
Output Common Mode (LOSW-x)	Switch off		High-Z		Ω
	Switch on		1.5		V
Input Resistance (LI-x)	R_{FB} = 350 Ω, LNA gain = 21.3 dB		50		Ω
	R_{FB} = 1400 Ω, LNA gain = 21.3 dB		200		Ω
	R_{FB} = ∞, LNA gain = 21.3 dB		15		kΩ
Input Capacitance (LI-x)			22		pF
−3 dB Bandwidth	LNA gain = 15.6 dB		100		MHz
	LNA gain = 17.9 dB		80		MHz
	LNA gain = 21.3 dB		50		MHz
Input Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.60		nV/√Hz
	LNA gain = 17.9 dB		1.42		nV/√Hz
	LNA gain = 21.3 dB		1.27		nV/√Hz
Input Noise Current	R_{FB} = ∞		1.5		pA/√Hz
Noise Figure	R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 200 Ω		7.8		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		6.7		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		5.6		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		6.1		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		5.3		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		4.7		dB
FULL-CHANNEL (TGC) CHARACTERISTICS					
AAF Low-Pass Cutoff	−3 dB, programmable	8		18	MHz
In Range AAF Bandwidth Tolerance			±10		%
Group Delay Variation	f = 1 MHz to 18 MHz, GAIN+ = 0 V to 1.6 V		±0.3		ns

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Input-Referred Noise Voltage	GAIN+ = 1.6 V, R_{FB} = ∞				
	LNA gain = 15.6 dB		1.7		nV/√Hz
	LNA gain = 17.9 dB		1.5		nV/√Hz
	LNA gain = 21.3 dB		1.3		nV/√Hz
Noise Figure	GAIN+ = 1.6 V, R_S = 50 Ω				
Active Termination Matched	LNA gain = 15.6 dB, R_{FB} = 200 Ω		9.2		dB
	LNA gain = 17.9 dB, R_{FB} = 250 Ω		7.7		dB
	LNA gain = 21.3 dB, R_{FB} = 350 Ω		6.3		dB
Unterminated	LNA gain = 15.6 dB, R_{FB} = ∞		6.7		dB
	LNA gain = 17.9 dB, R_{FB} = ∞		5.7		dB
	LNA gain = 21.3 dB, R_{FB} = ∞		4.9		dB
Correlated Noise Ratio	No signal, correlated/uncorrelated		−30		dB
Output Offset		−35		+35	LSB
Signal-to-Noise Ratio (SNR)	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V,		65		dBFS
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		57		dBFS
Harmonic Distortion					
Second Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−70		dBc
Third Harmonic	f_{IN} = 5 MHz at −10 dBFS, GAIN+ = 0 V		−70		dBc
	f_{IN} = 5 MHz at −1 dBFS, GAIN+ = 1.6 V		−70		dBc
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, A_{RF1} = 0 dB, A_{RF2} = −20 dB, GAIN+ = 1.6 VIMD3 relative to A_{RF2}		−70		dBc
Channel-to-Channel Crosstalk	f_{IN1} = 5.0 MHz at −1 dBFS		−60		dB
	Overrange condition[2]		−55		dB
Channel-to-Channel Delay Variation	Full TGC path, f_{IN} = 5 MHz, GAIN+ = 0 V to 1.6 V		0.3		Degrees
PGA Gain	Differential input to differential output		21/24/27/30		dB
GAIN ACCURACY	25°C				
Gain Law Conformance Error	0 < GAIN+ < 0.16 V		0.5		dB
	0.16 V < GAIN+ < 1.44 V	−1.6		+1.6	dB
	1.44 V < GAIN+ < 1.6 V		0.5		dB
Linear Gain Error	GAIN+ = 0.8 V, normalized for ideal AAF loss	−1.6		+1.6	dB
Channel-to-Channel Matching	0.16 V < GAIN+ < 1.44 V		0.1		dB
GAIN CONTROL INTERFACE					
Control Range	Differential	−0.8		+0.8	V
	Single-ended	0		1.6	V
Gain Range	GAIN+ = 0 V to 1.6 V		45		dB
Scale Factor			28		dB/V
Response Time	45 dB change		750		ns
Gain+ Impedance	Single-ended		10		MΩ
Gain− Impedance	Single-ended		70		kΩ
CW DOPPLER MODE					
LO Frequency	$f_{LO} = f_{4LO}/4$	1		10	MHz
Phase Resolution	Per channel		22.5		Degrees
Output DC Bias (Single-Ended)	CWI+, CWI−, CWQ+, CWQ−		1.5		V
Output AC Current Range	Per CWI+, CWI−, CWQ+, CWQ−, each channel enabled			±1.25	mA
Transconductance (Differential)	Demodulated I_{OUT}/V_{IN}, per CWI+, CWI−, CWQ+, CWQ−				
	LNA gain = 15.6 dB		1.8		mA/V
	LNA gain = 17.9 dB		2.4		mA/V
	LNA gain = 21.3 dB		3.5		mA/V

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Input-Referred Noise Voltage	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		2.0		nV/√Hz
	LNA gain = 17.9 dB		1.9		nV/√Hz
	LNA gain = 21.3 dB		1.8		nV/√Hz
Noise Figure	R_S = 50 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		7.8		dB
	LNA gain = 17.9 dB		7.3		dB
	LNA gain = 21.3 dB		6.9		dB
Input-Referred Dynamic Range	R_S = 0 Ω, R_{FB} = ∞				
	LNA gain = 15.6 dB		162		dBFS/√Hz
	LNA gain = 17.9 dB		160		dBFS/√Hz
	LNA gain = 21.3 dB		157		dBFS/√Hz
Output-Referred SNR	−3 dBFS input, f_{RF} = 2.5 MHz, f_{4LO} = 10 MHz, 1 kHz offset		153		dBc/√Hz
Two-Tone Intermodulation (IMD3)	f_{RF1} = 5.015 MHz, f_{RF2} = 5.020 MHz, f_{4LO} = 20 MHz, A_{RF1} = −1 dBFS, A_{RF2} = −21 dBFS, IMD3 relative to A_{RF2}		−58		dB
Quadrature Phase Error	I to Q, all phases, 1 σ		0.15		Degrees
I/Q Amplitude Imbalance	I to Q, all phases, 1 σ		0.015		dB
Channel-to-Channel Matching	Phase I to I, Q to Q, 1 σ		0.5		Degrees
	Amplitude I to I, Q to Q, 1 σ		0.25		dB
POWER SUPPLY, MODE I/II/III/IV					
AVDD1		1.7	1.8	1.9	V
AVDD2[3]		2.7	3.0	3.6	V
DRVDD		1.7	1.8	1.9	V
I_{AVDD1}	TGC mode		178/145/ 215/260		mA
	CW Doppler mode		32		mA
I_{AVDD2}	TGC mode, no signal		108		mA
	CW Doppler mode		63		mA
I_{DRVDD}	ANSI-644 mode		47/44/48/53		mA
	Low power (IEEE 1596.3 similar) mode		33/31/34/38		
Total Power Dissipation (Including Output Drivers)	TGC mode, no signal		704/640/ 772/860	815/755/ 908/996	mW
	CW Doppler mode		252		mW
Power-Down Dissipation				5	mW
Standby Power Dissipation			420		mW
Power Supply Rejection Ratio (PSRR)			1.6		mV/V
ADC RESOLUTION			12		Bits
ADC REFERENCE					
Output Voltage Error	VREF = 1 V			±50	mV
Load Regulation at 1.0 mA	VREF = 1 V		2		mV
Input Resistance			6		kΩ

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] The overrange condition is specified as 6 dB more than the full-scale input range.
[3] When the LNA gain is set to 15.6 dB, AVDD2 ≥3.0 V.

DIGITAL SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, 1.0 V internal ADC reference, full temperature, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
CW 4LO INPUTS (4LO+, 4LO−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, STBY, SCLK, RESET)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC OUTPUT (SDIO)[3]					
Logic 1 Voltage (I_{OH} = 800 µA)	Full	1.2		DRVDD + 0.3	V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.3	V
Input Resistance	25°C		30		
Input Capacitance	25°C		2		
DIGITAL OUTPUTS (DOUTx+, DOUTx−), (ANSI-644)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	247		454	mV
Output Offset Voltage (V_{OS})	Full	1.125		1.375	V
Output Coding (Default)			Offset binary		
DIGITAL OUTPUTS (DOUTx+, DOUTx−), (LOW POWER, REDUCED SIGNAL OPTION)					
Logic Compliance			LVDS		
Differential Output Voltage (V_{OD})	Full	150		250	mV
Output Offset Voltage (V_{OS})	Full	1.10		1.30	V
Output Coding (Default)			Offset binary		
LOGIC OUTPUT (GPO0/GPO1/GPO2/GPO3)					
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.05	V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.0 V, DRVDD = 1.8 V, full temperature, unless otherwise noted.

Table 3.

Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate					
25 MSPS (Mode II)	Full	18.5		25	MHz
40 MSPS (Mode I)	Full	18.5		40	MHz
50 MSPS (Mode III)	Full	18.5		50	MHz
65 MSPS (Mode IV)	Full	18.5		65	MHz
Clock Pulse Width High (t_{EH})	Full		4.8		ns
Clock Pulse Width Low (t_{EL})	Full		4.8		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	(t_{SAMPLE}/2) + 1.5	(t_{SAMPLE}/2) + 2.3	(t_{SAMPLE}/2) + 3.1	ns
DCO Propagation Delay (t_{CPD})[4]	Full		t_{FCO} + (t_{SAMPLE}/24)		ns
DCO to Data Delay (t_{DATA})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
DCO to FCO Delay (t_{FRAME})[4]	Full	(t_{SAMPLE}/24) − 300	(t_{SAMPLE}/24)	(t_{SAMPLE}/24) + 300	ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±100	±350	ps
Wake-Up Time (Standby), GAIN+ = 0.5 V	25°C		2		µs
Wake-Up Time (Power-Down)	25°C		1		ms
Pipeline Latency	Full		8		Clock cycles
APERTURE					
Aperture Uncertainty (Jitter)	25°C		<1		ps rms
LO GENERATION					
4LO Frequency	Full	4		40	MHz
LO Divider RESET Setup Time[5]	Full	5			ns
LO Divider RESET Hold Time[5]	Full	5			ns
LO Divider RESET High Pulse Width	Full	20			ns

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and information about how these tests were completed.
[2] Can be adjusted via the SPI.
[3] Measurements were made using a part soldered to FR-4 material.
[4] t_{SAMPLE}/24 is based on the number of bits divided by 2 because the delays are based on half duty cycles.
[5] RESET edge to rising 4LO edge.

ADC TIMING DIAGRAMS

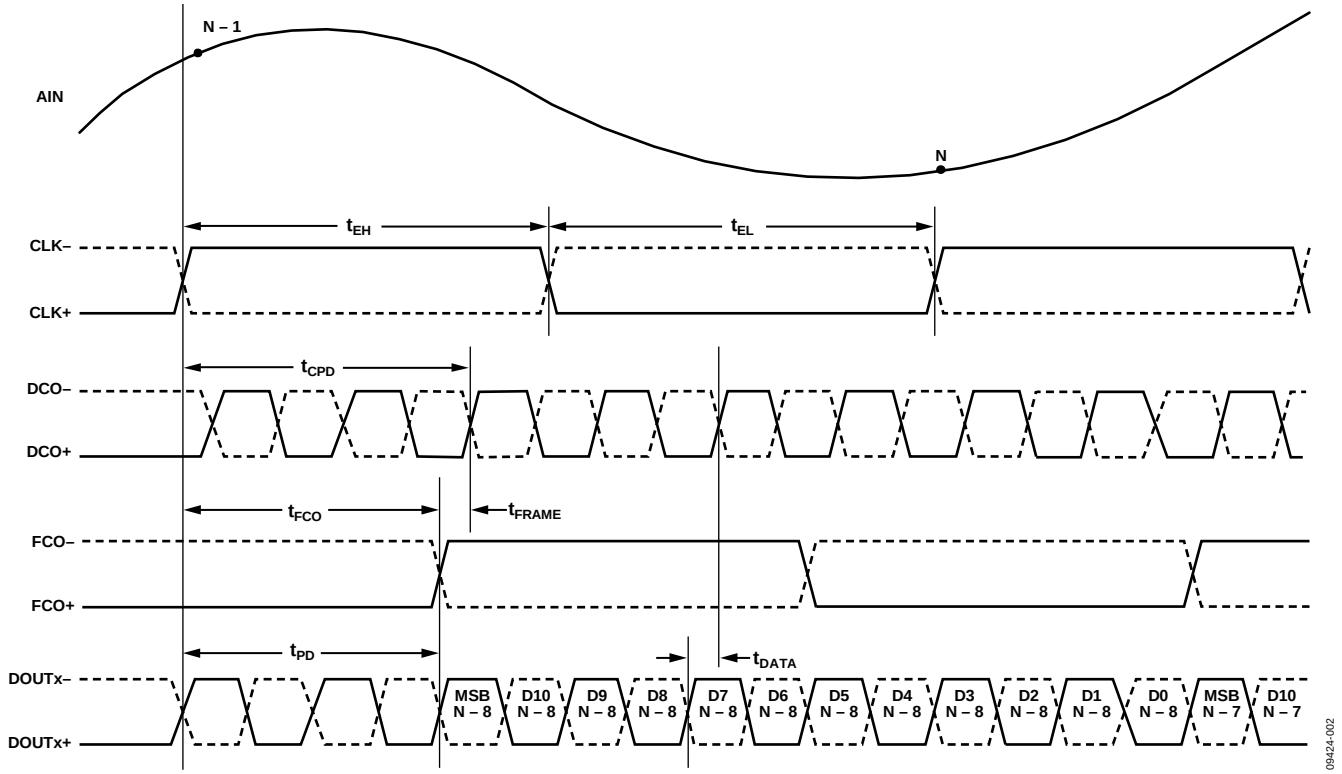

Figure 2. 12-Bit Data Serial Stream (Default)

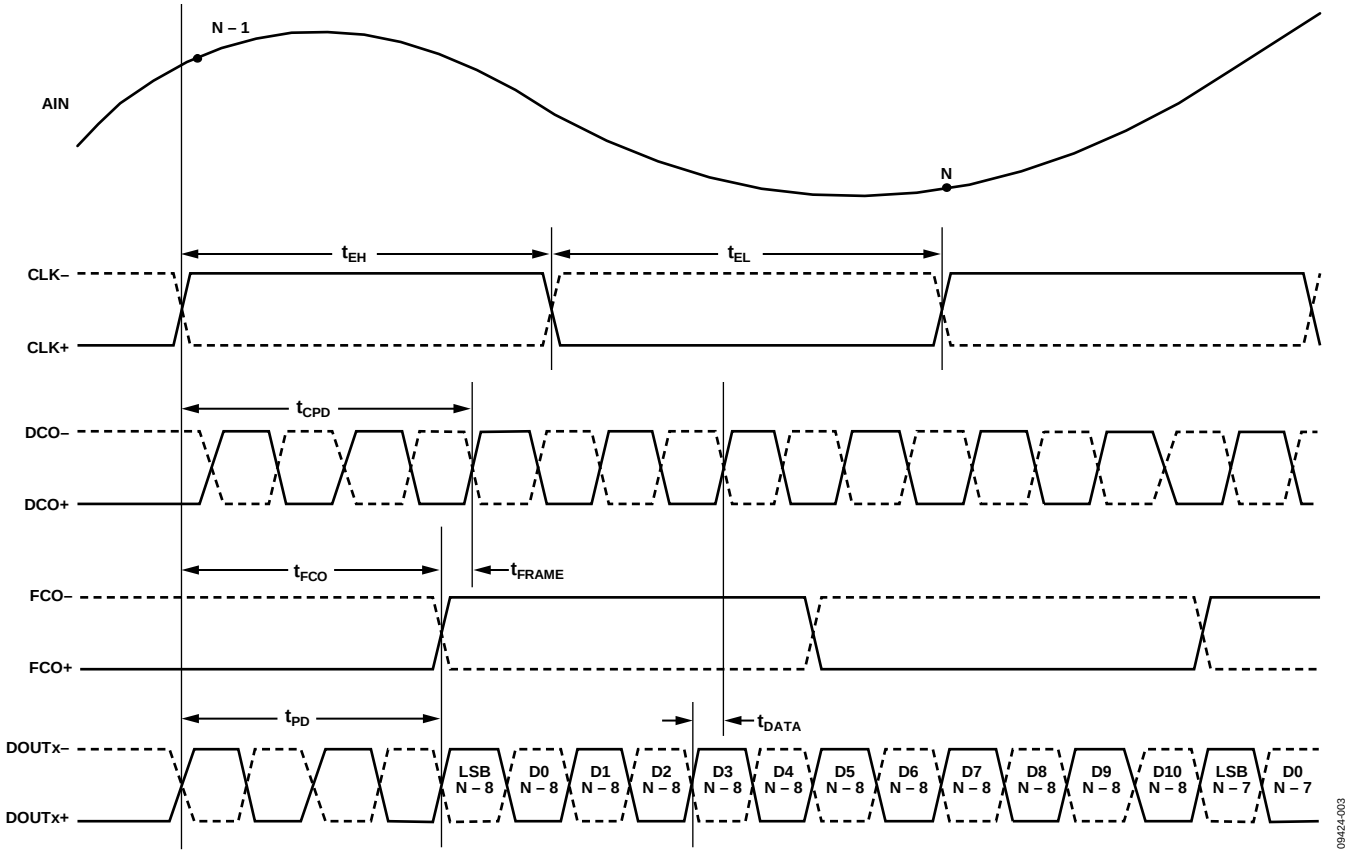

Figure 3. 12-Bit Data Serial Stream, LSB First

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD1 to GND	−0.3 V to +2.0 V
AVDD2 to GND	−0.3 V to +3.9 V
DRVDD to GND	−0.3 V to +2.0 V
GND to GND	−0.3 V to +0.3 V
AVDD2 to AVDD1	−2.0 V to +3.9 V
AVDD1 to DRVDD	−2.0 V to +2.0 V
AVDD2 to DRVDD	−2.0 V to +3.9 V
Digital Outputs (DOUTx+, DOUTx−, DCO+, DCO−, FCO+, FCO−) to GND	−0.3 V to DRVDD + 0.3 V
CLK+, CLK−, SDIO to GND	−0.3 V to AVDD1 + 0.3 V
LI-x, LO-x, LOSW-x to GND	−0.3 V to AVDD2 + 0.3 V
CWI−, CWI+, CWQ−, CWQ+ to GND	−0.3 V to AVDD2 + 0.3 V
PDWN, STBY, SCLK, CSB to GND	−0.3 V to AVDD1 + 0.3 V
GAIN+, GAIN−, RESET, 4LO+, 4LO−, GPO0, GPO1, GPO2, GPO3 to GND	−0.3 V to AVDD2 + 0.3 V
VREF to GND	−0.3 V to AVDD1 + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE

Table 5.

Symbol	Description	Value[1]	Units
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/s air flow per JEDEC JESD51-2 (still air)	22.0	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter, 0 m/s air flow per JEDEC JESD51-8 (still air)	9.2	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/s air flow per JEDEC JESD51-2 (still air)	0.12	°C/W

[1] Results are from simulations. PCB is JEDEC multilayer. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	LI-E	LI-F	LI-G	LI-H	VREF	RBIAS	GAIN+	GAIN–	LI-A	LI-B	LI-C	LI-D
B	LG-E	LG-F	LG-G	LG-H	GND	GND	AVDD2	GND	LG-A	LG-B	LG-C	LG-D
C	LO-E	LO-F	LO-G	LO-H	GND	GND	GND	GND	LO-A	LO-B	LO-C	LO-D
D	LOSW-E	LOSW-F	LOSW-G	LOSW-H	GND	GND	GND	GND	LOSW-A	LOSW-B	LOSW-C	LOSW-D
E	GND	AVDD2	AVDD2	AVDD2	GND	GND	GND	GND	AVDD2	AVDD2	AVDD2	GND
F	AVDD1	GND	AVDD1	GND	AVDD1	GND	GND	AVDD1	GND	AVDD1	GND	AVDD1
G	GND	AVDD1	GND	AVDD1	GND	GND	GND	GND	AVDD1	GND	AVDD1	GND
H	CLK–	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CSB
J	CLK+	GND	CWQ+	GND	CWI+	AVDD2	4LO+	GND	GPO3	GPO1	PDWN	SDIO
K	GND	GND	CWQ–	GND	CWI–	AVDD2	4LO–	RESET	GPO2	GPO0	STBY	SCLK
L	DRVDD	DOUTH+	DOUTG+	DOUTF+	DOUTE+	DCO+	FCO+	DOUTD+	DOUTC+	DOUTB+	DOUTA+	DRVDD
M	GND	DOUTH–	DOUTG–	DOUTF–	DOUTE–	DCO–	FCO–	DOUTD–	DOUTC–	DOUTB–	DOUTA–	GND

09424-004

Figure 4. Pin Configuration

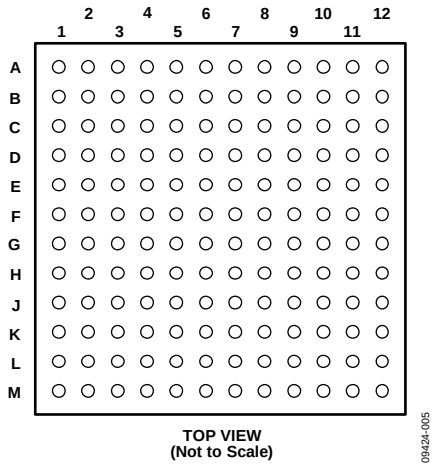

Figure 5.

Table 6. Pin Function Descriptions

Pin No.	Name	Description
B5, B6, B8, C5, C6, C7, C8, D5, D6, D7, D8, E1, E5, E6, E7, E8, E12, F2, F4, F6, F7, F9, F11, G1, G3, G5, G6, G7, G8, G10, G12, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, J2, J4, J8, K1, K2, K4, M1, M12	GND	Ground (should be tied to a quiet analog ground)
F1, F3, F5, F8, F10, F12, G2, G4, G9, G11	AVDD1	1.8 V Analog Supply
B7, E2, E3, E4, E9, E10, E11, J6, K6	AVDD2	3.0 V Analog Supply
L1, L12	DRVDD	1.8 V Digital Output Driver Supply
A1	LI-E	LNA Analog Input for Channel E
B1	LG-E	LNA Ground for Channel E
C2	LO-F	LNA Analog Inverted Output for Channel F
D2	LOSW-F	LNA Analog Switched Output for Channel F
A2	LI-F	LNA Analog Input for Channel F
B2	LG-F	LNA Ground for Channel F
C3	LO-G	LNA Analog Inverted Output for Channel G
D3	LOSW-G	LNA Analog Switched Output for Channel G
A3	LI-G	LNA Analog Input for Channel G
B3	LG-G	LNA Ground for Channel G
C4	LO-H	LNA Analog Inverted Output for Channel H
D4	LOSW-H	LNA Analog Switched Output for Channel H
A4	LI-H	LNA Analog Input for Channel H
B4	LG-H	LNA Ground for Channel H
H1	CLK–	Clock Input Complement
J1	CLK+	Clock Input True
M2	DOUTH–	ADC H Digital Output Complement
L2	DOUTH+	ADC H Digital Output True
M3	DOUTG–	ADC G Digital Output Complement
L3	DOUTG+	ADC G Digital Output True
M4	DOUTF–	ADC F Digital Output Complement
L4	DOUTF+	ADC F Digital Output True
M5	DOUTE–	ADC E Digital Output Complement
L5	DOUTE+	ADC E Digital Output True
M6	DCO–	Digital Clock Output Complement
L6	DCO+	Digital Clock Output True
M7	FCO–	Frame Clock Digital Output Complement
L7	FCO+	Frame Clock Digital Output True
M8	DOUTD–	ADC D Digital Output Complement
L8	DOUTD+	ADC D Digital Output True
M9	DOUTC–	ADC C Digital Output Complement
L9	DOUTC+	ADC C Digital Output True
M10	DOUTB–	ADC B Digital Output Complement
L10	DOUTB+	ADC B Digital Output True
M11	DOUTA–	ADC A Digital Output Complement
L11	DOUTA+	ADC A Digital Output True
K11	STBY	Standby Power-Down
J11	PDWN	Full Power-Down
K12	SCLK	Serial Clock
J12	SDIO	Serial Data Input/Output
H12	CSB	Chip Select Bar
B9	LG-A	LNA Ground for Channel A
A9	LI-A	LNA Analog Input for Channel A
D9	LOSW-A	LNA Analog Switched Output for Channel A
C9	LO-A	LNA Analog Inverted Output for Channel A

Pin No.	Name	Description
B10	LG-B	LNA Ground for Channel B
A10	LI-B	LNA Analog Input for Channel B
D10	LOSW-B	LNA Analog Switched Output for Channel B
C10	LO-B	LNA Analog Inverted Output for Channel B
B11	LG-C	LNA Ground for Channel C
A11	LI-C	LNA Analog Input for Channel C
D11	LOSW-C	LNA Analog Switched Output for Channel C
C11	LO-C	LNA Analog Inverted Output for Channel C
B12	LG-D	LNA Ground for Channel D
A12	LI-D	LNA Analog Input for Channel D
D12	LOSW-D	LNA Analog Switched Output for Channel D
C12	LO-D	LNA Analog Inverted Output for Channel D
K10	GPO0	General Purpose Open Drain Output 0
J10	GPO1	General Purpose Open Drain Output 1
K9	GPO2	General Purpose Open Drain Output 2
J9	GPO3	General Purpose Open Drain Output 3
K8	RESET	Reset for Synchronizing 4LO Divide-by-4 Counter
K7	4LO−	CW Doppler 4LO Input Complement
J7	4LO+	CW Doppler 4LO Input True
A8	GAIN−	Gain Control Voltage Input Complement
A7	GAIN+	Gain Control Voltage Input True
A6	RBIAS	External Resistor to Set the Internal ADC Core Bias Current
A5	VREF	Voltage Reference Input/Output
K5	CWI−	CW Doppler I Output Complement
J5	CWI+	CW Doppler I Output True
K3	CWQ−	CW Doppler Q Output Complement
J3	CWQ+	CW Doppler Q Output True
C1	LO-E	LNA Analog Inverted Output for Channel E
D1	LOSW-E	LNA Analog Switched Output for Channel E

TYPICAL PERFORMANCE CHARACTERISTICS

TGC MODE

f_{SAMPLE} = 40 MSPS, f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = mid-high, PGA gain = 24 dB, GAIN− = 0.8 V, AAF LPF cutoff = f_{SAMPLE}/3.0, HPF cutoff = LPF cutoff/12.00 (default).

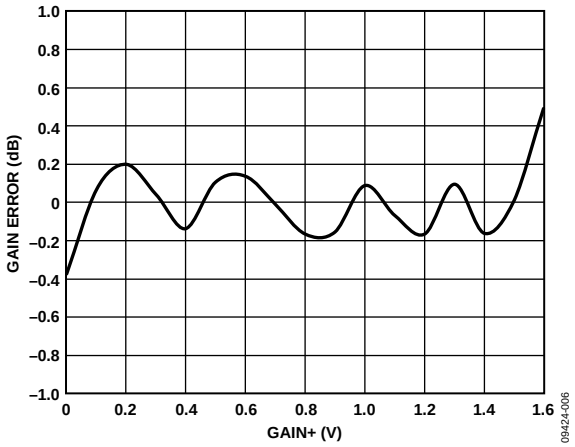

Figure 6. Gain Error vs. GAIN+

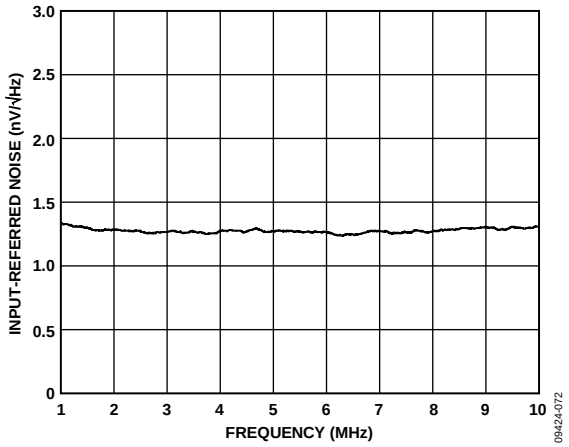

Figure 9. Short-Circuit, Input-Referred Noise vs. Frequency, LNA Gain = 21.3 dB, PGA Gain = 30 dB, GAIN+ = 1.6 V

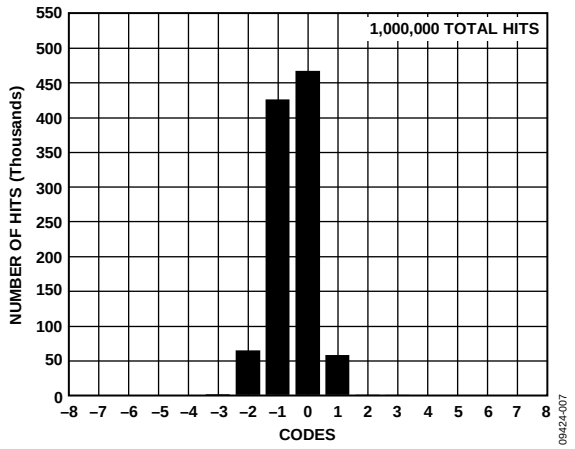

Figure 7. Output-Referred Noise Histogram, GAIN+ = 0.0 V

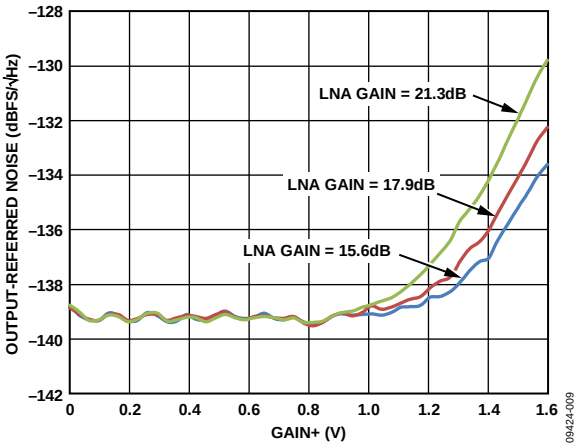

Figure 10. Short-Circuit, Output-Referred Noise vs. GAIN+

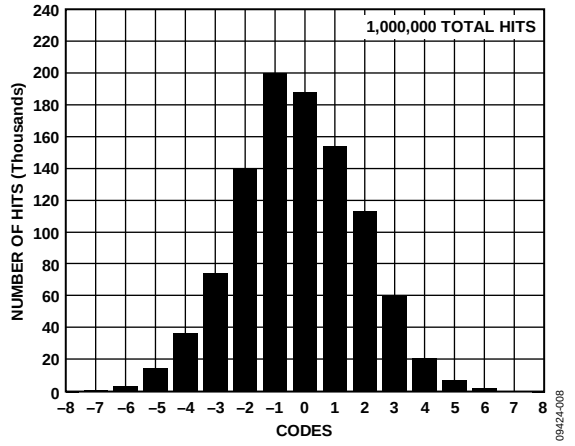

Figure 8. Output-Referred Noise Histogram, GAIN+ = 1.6 V

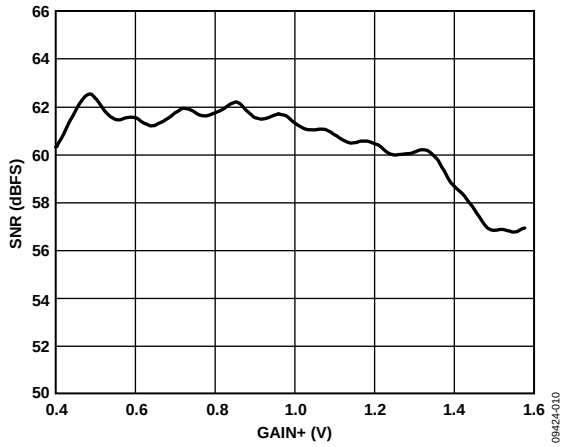

Figure 11. SNR vs. GAIN+, AOUT = −1.0 dBFS

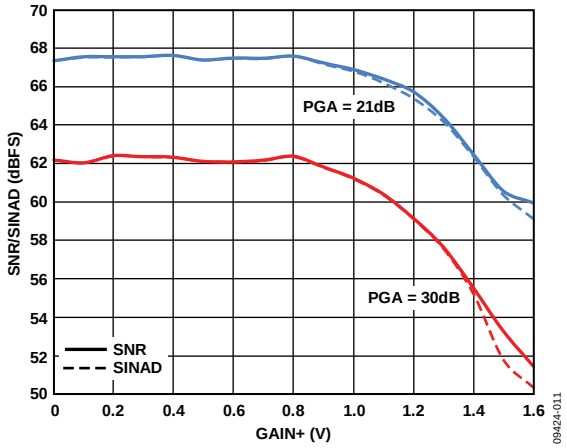

Figure 12. SNR/SINAD vs. GAIN+, AIN = −45 dBm

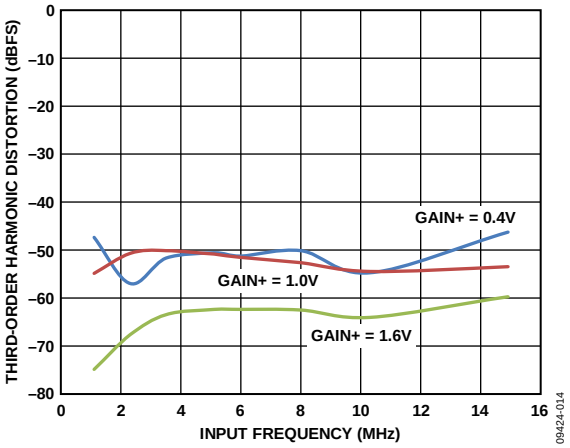

Figure 15. Third-Order Harmonic Distortion vs. Frequency, AOUT = −1.0 dBFS

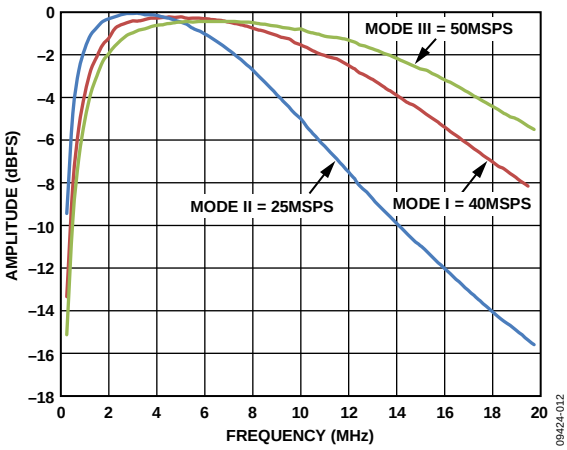

Figure 13. Antialiasing Filter (AAF) Pass-Band Response, LPF Cutoff = 1 × (1/3) × f_{SAMPLE}

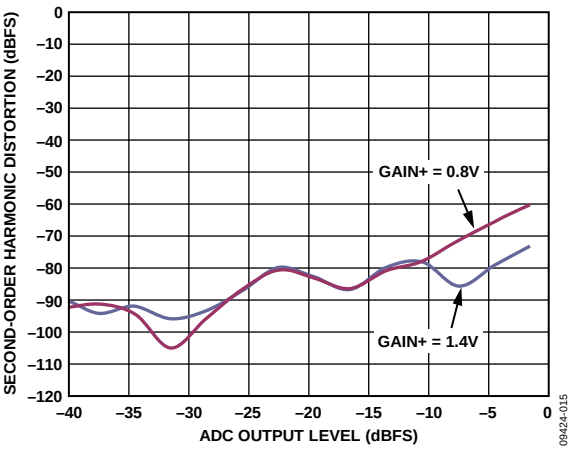

Figure 16. Second-Order Harmonic Distortion vs. ADC Output Level, AOUT

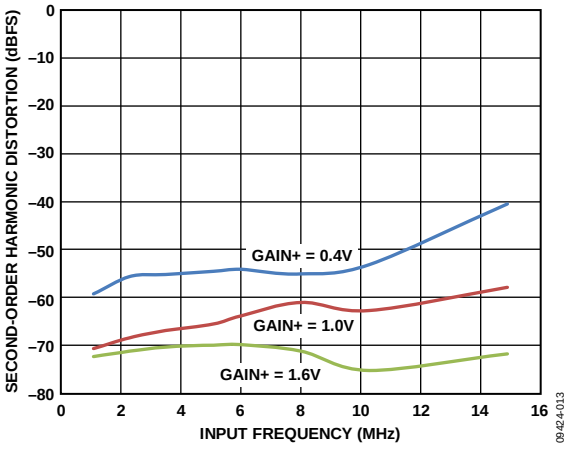

Figure 14. Second-Order Harmonic Distortion vs. Frequency, AOUT = −1.0 dBFS

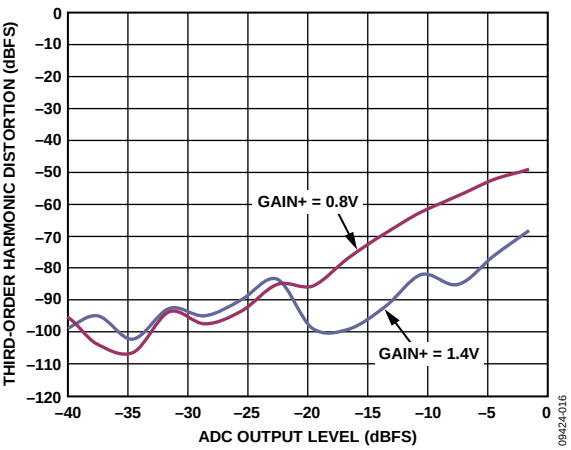

Figure 17. Third-Order Harmonic Distortion vs. ADC Output Level

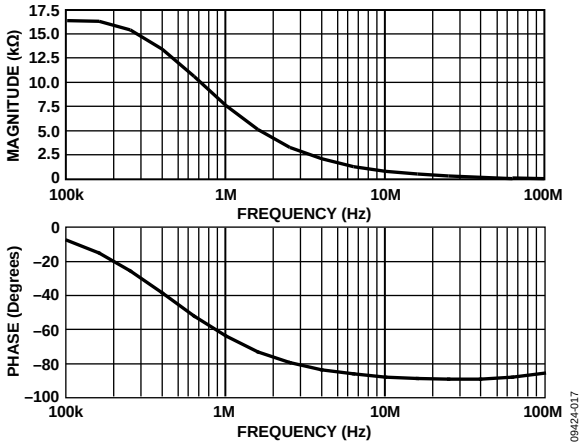

Figure 18. LNA Input Impedance Magnitude and Phase, Unterminated

CW DOPPLER MODE

f_{IN} = 5 MHz, R_S = 50 Ω, LNA gain = 21.3 dB, LNA bias = mid-high, all CW channels enabled, phase rotation 0 degrees.

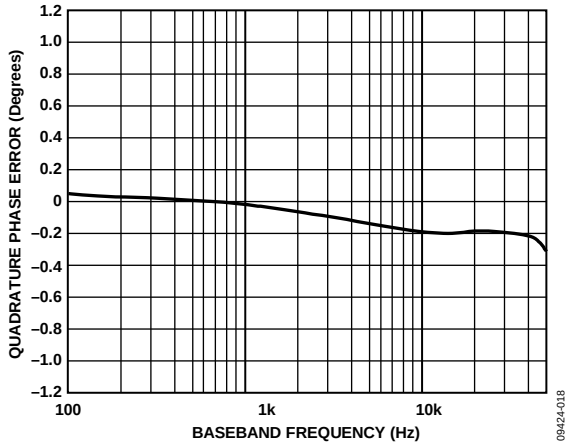

Figure 19. Quadrature (I/Q) Phase Error vs. Baseband Frequency

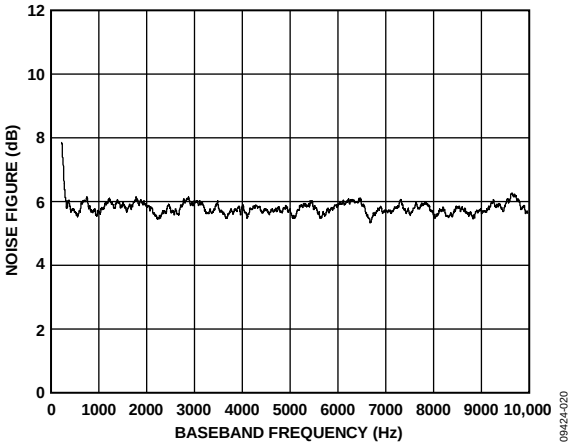

Figure 21. Noise Figure vs. Baseband Frequency

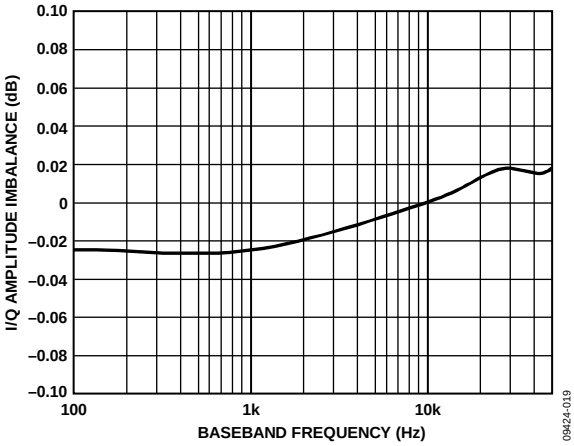

Figure 20. Quadrature (I/Q) Amplitude Error vs. Baseband Frequency

EQUIVALENT CIRCUITS

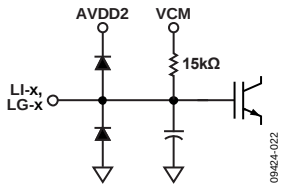

Figure 22. Equivalent LNA Input Circuit (VCM = Common-Mode Voltage)

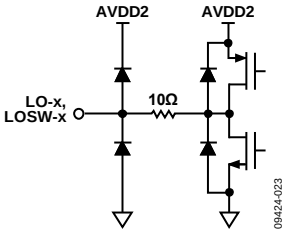

Figure 23. Equivalent LNA Output Circuit

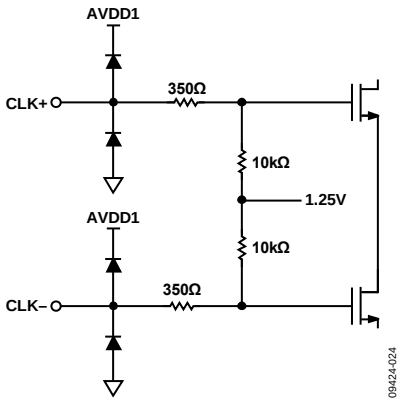

Figure 24. Equivalent Clock Input Circuit

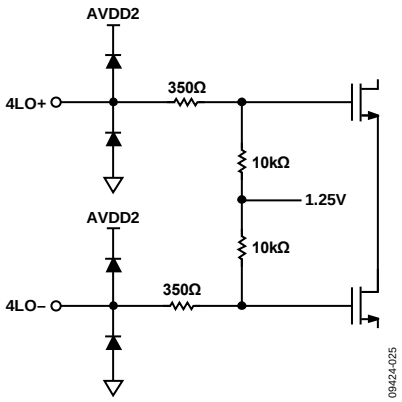

Figure 25. Equivalent 4LO Input Circuit

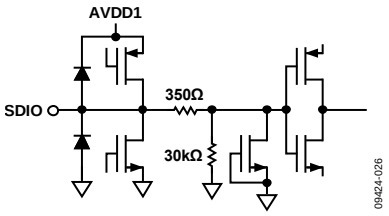

Figure 26. Equivalent SDIO Input Circuit

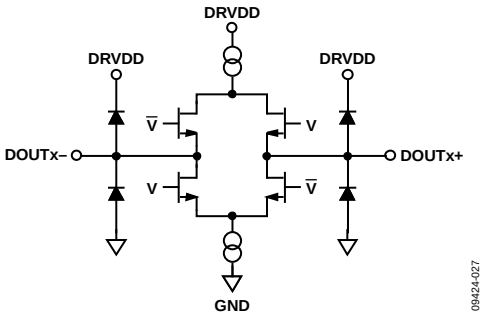

Figure 27. Equivalent Digital Output Circuit

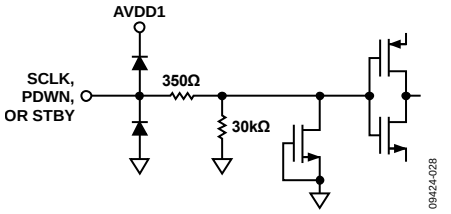

Figure 28. Equivalent SCLK, PDWN, or STBY Input Circuit

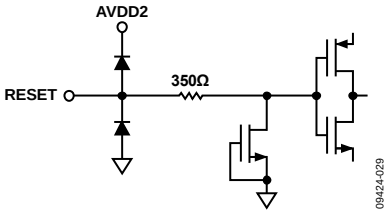

Figure 29. Equivalent RESET Input Circuit

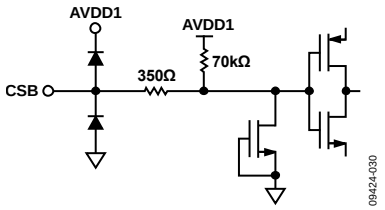

Figure 30. Equivalent CSB Input Circuit

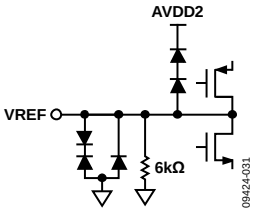

Figure 31. Equivalent VREF Circuit

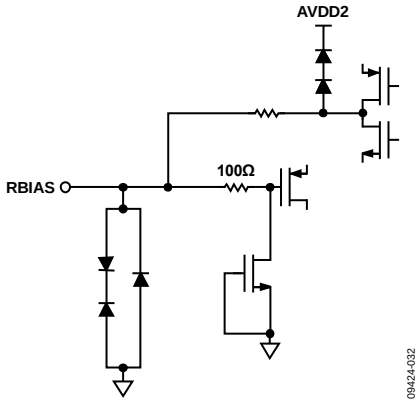

Figure 32. Equivalent RBIAS Circuit

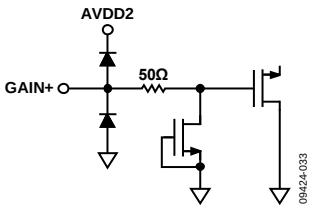

Figure 33. Equivalent GAIN+ Input Circuit

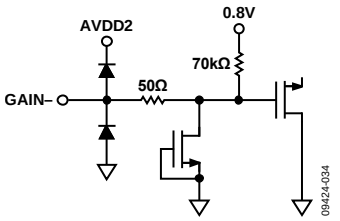

Figure 34. Equivalent GAIN– Input Circuit

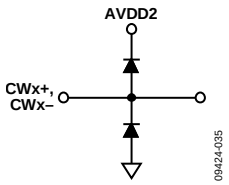

Figure 35. Equivalent CWI±, CWQ± Output Circuit

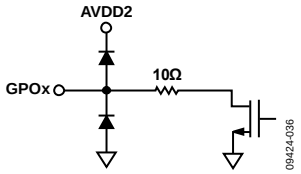

Figure 36. Equivalent GPOx Output Circuit

ULTRASOUND THEORY OF OPERATION

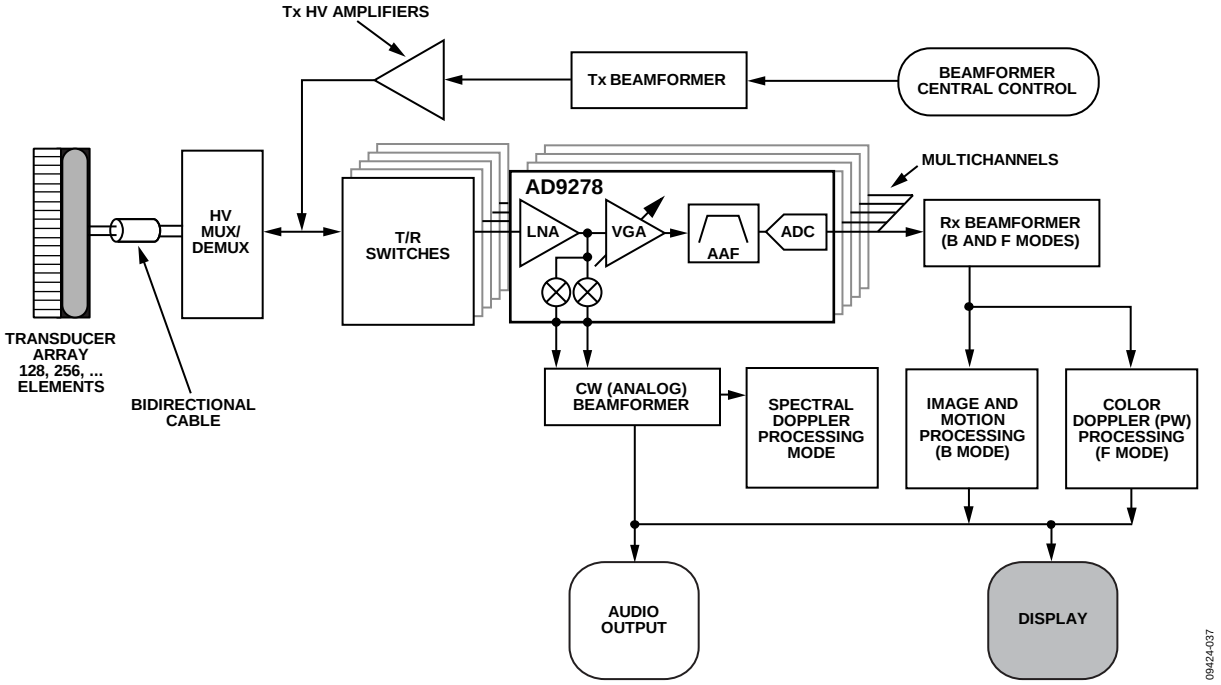

Figure 37. Simplified Ultrasound System Block Diagram

The primary application for the AD9278 is medical ultrasound. Figure 37 shows a simplified block diagram of an ultrasound system. A critical function of an ultrasound system is the time gain control (TGC) compensation for physiological signal attenuation. Because the attenuation of ultrasound signals is exponential with respect to distance (time), a linear-in-dB VGA is the optimal solution.

Key requirements in an ultrasound signal chain are very low noise, active input termination, fast overload recovery, low power, and differential drive to an ADC. Because ultrasound machines use beamforming techniques requiring large binary-weighted numbers of channels (for example, 32 to 512), using the lowest power at the lowest possible noise is of chief importance.

Most modern ultrasound machines use digital beamforming. In this technique, the signal is converted to digital format immediately following the TGC amplifier, and then beamforming is accomplished digitally.

The ADC resolution of 12 bits with up to 50 MSPS sampling satisfies the requirements of both general-purpose and high end systems. The power dissipation of the ADC scales with programmable speed modes for optimum power performance depending on system architecture.

Power conservation, high performance, and low cost are three of the most important factors in low end and portable ultrasound machines, and the AD9278 is designed to meet these criteria.

For additional information regarding ultrasound systems, see "How Ultrasound System Considerations Influence Front-End Component Choice," *Analog Dialogue*, Volume 36, Number 3, May–July 2002, and "The AD9271—A Revolutionary Solution for Portable Ultrasound," *Analog Dialogue*, Volume 41, Number 7, July 2007.

CHANNEL OVERVIEW

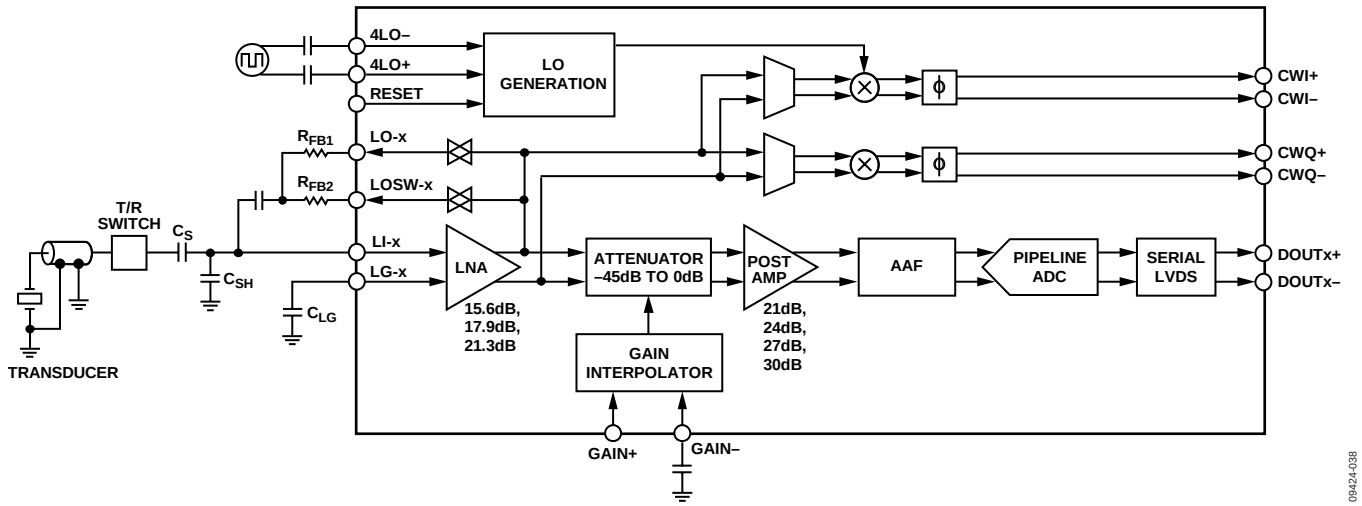

Figure 38. Simplified Block Diagram of a Single Channel

Each channel contains both a TGC signal path and a CW Doppler signal path. Common to both signal paths, the LNA provides four user-adjustable input impedance termination options for matching different probe impedances. The CW Doppler path includes an I/Q demodulator with programmable phase rotation needed for analog beamforming. The TGC path includes a differential X-AMP® VGA, an antialiasing filter, and an ADC. Figure 38 shows a simplified block diagram with external components.

TGC OPERATION

The TGC signal path is fully differential throughout to maximize signal swing and reduce even-order distortion; however, the LNAs are designed to be driven from a single-ended signal source. Gain values are referenced from the single-ended LNA input to the differential ADC input. A simple exercise in understanding the maximum and minimum gain requirements is shown in Figure 39.

The maximum gain required is determined by

(*ADC Noise Floor*/*LNA Input Noise Floor*) + *Margin* =
20 log(224/5.8) + 11 dB = 42 dB

The minimum gain required is determined by

(*ADC Input FS*/*LNA Input FS*) + *Margin* =
20 log(2/0.45) − 10 dB = 3 dB

Therefore, 42 dB of gain range for a 12-bit, 40 MSPS ADC with 15 MHz of bandwidth should suffice in achieving the dynamic range required for most of today's ultrasound systems.

The system gain is distributed as listed in Table 7.

Table 7. Channel Gain Distribution

Section	Nominal Gain (dB)
LNA	15.6/17.9/21.3
Attenuator	0 to −45
VGA Amplifier	21/24/27/30
Filter	0
ADC	0

The linear-in-dB gain (law conformance) range of the TGC path is 45 dB. The slope of the gain control interface is 28 dB/V, and the gain control range is −0.8 V to +0.8 V. Equation 3 is the expression for the differential voltage, V_{GAIN}, at the gain control interface. Equation 4 is the expression for the VGA attenuation, VGA_{ATT}, as a function of V_{GAIN}.

$$V_{GAIN}\,(\mathrm{V}) = (GAIN+) - (GAIN-) \quad (3)$$

$$VGA_{ATT}\,(\mathrm{dB}) = -28\frac{\mathrm{dB}}{\mathrm{V}}(0.8 - V_{GAIN}) \quad (4)$$

The total channel gain can then be calculated as in Equation 5.

$$ChannelGain\,(\mathrm{dB}) = LNA_{GAIN} + VGA_{ATT} + PGA_{GAIN} \quad (5)$$

In its default condition, the LNA has a gain of 21.3 dB (12×), and the VGA postamp gain is 24 dB if the voltage on the GAIN+ pin is 0 V and the voltage on the GAIN− pin is 0.8 V (42 dB attenuation). This results in a total gain (or ICPT) of 3.6 dB through the TGC path if the LNA input is unmatched or a total gain of −2.4 dB if the LNA is matched to 50 Ω (R_{FB} = 350 Ω). However, if the voltage on the GAIN+ pin is 1.6 V and the voltage on the GAIN− pin is 0.8 V (0 dB attenuation), the VGA gain is 24 dB. This results in a total gain of 45 dB through the TGC path if the LNA input is unmatched or in a total gain of 39 dB if the LNA input is matched.

Each LNA output is dc-coupled to a VGA input. The VGA consists of an attenuator with a range of −42 dB, followed by an amplifier with 21 dB/24 dB/27 dB/30 dB of gain. The X-AMP gain interpolation technique results in low gain error and uniform bandwidth, and differential signal paths minimize distortion.

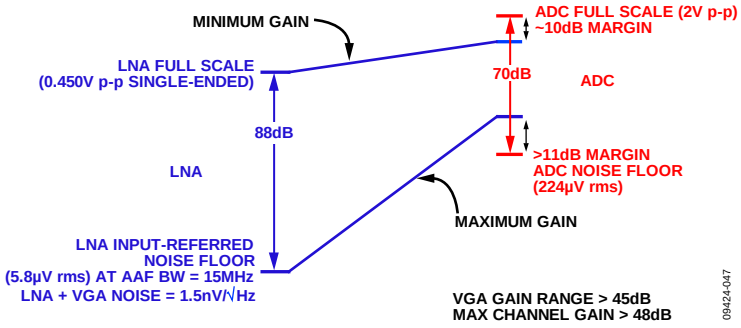

Figure 39. Gain Requirements of TGC Operation for a 12-Bit, 40 MSPS ADC

Table 8. Sensitivity and Dynamic Range of Trade-Offs[1, 2, 3]

LNA				VGA	Channel		
Gain					Typical Output Dynamic Range (dB)		
(V/V)	(dB)	Full-Scale Input (V p-p)	Input Noise (nV/√Hz)	Postamp Gain (dB)	GAIN+ = 0 V[4]	GAIN+ = 1.6 V[5]	Input-Referred Noise[6] at GAIN+ = 1.6 V (nV/√Hz)
6	15.6	0.733	1.60	21	68.6	63.6	1.863
				24	67.8	61.2	1.773
				27	66.5	58.5	1.725
				30	64.7	55.7	1.701
7.8	17.9	0.550	1.42	21	68.6	62.6	1.590
				24	67.8	60.0	1.531
				27	66.5	57.3	1.500
				30	64.7	54.4	1.485
11.6	21.3	0.367	1.27	21	68.6	60.6	1.347
				24	67.8	57.9	1.316
				27	66.5	55.0	1.301
				30	64.7	52.1	1.293

[1] LNA: output full scale = 4.4 V p-p differential.
[2] Filter: loss ~ 1 dB, NBW = 13.3 MHz, GAIN− = 0.8 V.
[3] ADC: 40 MSPS, 70 dB SNR, 2 V p-p full-scale input.
[4] Output dynamic range at minimum VGA gain (VGA dominated).
[5] Output dynamic range at maximum VGA gain (LNA dominated).
[6] Channel noise at maximum VGA gain.

Table 8 demonstrates the sensitivity and dynamic range of trade-offs that can be achieved relative to various LNA and VGA gain settings.

For example, when the VGA is set for the minimum gain voltage, the TGC path is dominated by VGA noise and achieves the maximum output SNR. However, as the postamp gain options are increased, the input-referred noise is reduced and the SNR is degraded.

If the VGA is set for the maximum gain voltage, the TGC path is dominated by LNA noise and achieves the lowest input-referred noise but with degraded output SNR. The higher the TGC (LNA + VGC) gain, the lower the output SNR. As the postamp gain is increased, the input-referred noise is reduced.

At low gains, the VGA should limit the system noise performance (SNR); at high gains, the noise is defined by the source and the LNA. The maximum voltage swing is bound by the full-scale peak-to-peak ADC input voltage (2 V p-p).

Both the LNA and VGA have full-scale limitations within each section of the TGC path. These limitations are dependent on the gain setting of each function block and on the voltage applied to the GAIN+ and GAIN− pins. The LNA has three limitations, or full-scale settings, that can be applied through the SPI. Similarly, the VGA has four postamp gain settings that can be applied through the SPI. The voltage applied to the GAIN± pins determines which amplifier (the LNA or VGA) saturates first. The maximum signal input level prior to 0.1 dB compression on the output of the LNA that can be applied as a function of voltage on the GAIN± pins for the selectable gain options of the SPI is shown in Figure 40 to Figure 42.

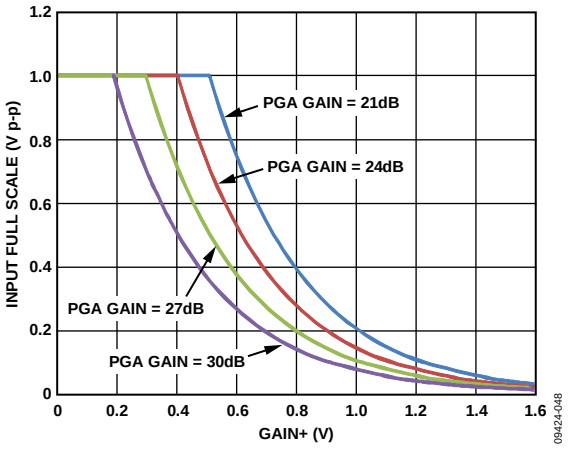

Figure 40. LNA with 15.6 dB Gain Setting/VGA Full-Scale Limitations

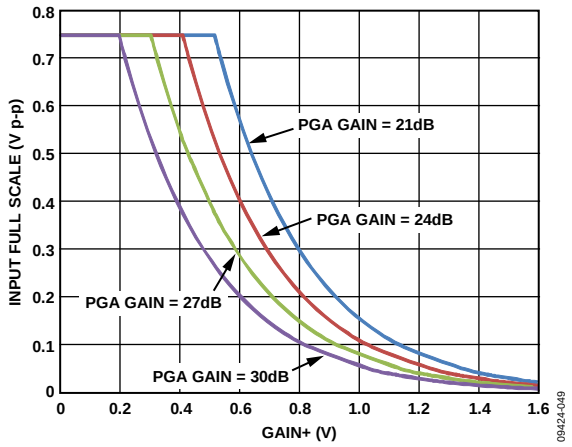

Figure 41. LNA with 17.9 dB Gain Setting/VGA Full-Scale Limitations

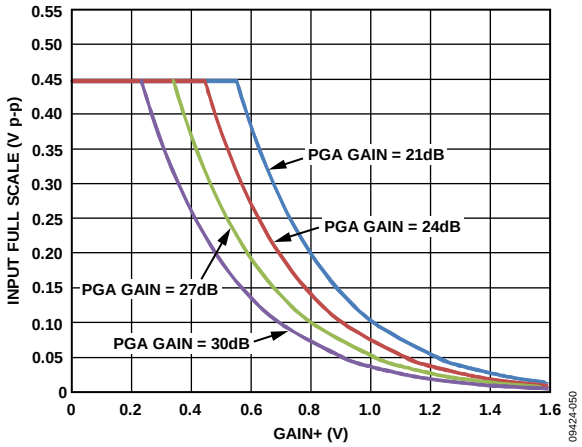

Figure 42. LNA with 21.3 dB Gain Setting/VGA Full-Scale Limitations

Low Noise Amplifier (LNA)

Good system sensitivity relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contribution in the following VGA. Active impedance control optimizes noise performance for applications that benefit from input impedance matching.

The LNA input, LI-x, is capacitively coupled to the source. An on-chip bias generator establishes dc input bias voltages of approximately 2.2 V and centers the output common-mode levels at 1.5 V (AVDD2 divided by 2). A capacitor, C_{LG}, of the same value as the input coupling capacitor, C_S, is connected from the LG-x pin to ground.

It is highly recommended that the LG-x pins form a Kelvin type connection to the input or probe connection ground. Simply connecting the LG-x pin to ground near the device can allow differences in potential to be amplified through the LNA. This generally shows up as a dc offset voltage that can vary from channel to channel and part to part depending on the application and the layout of the PCB.

The LNA supports a nominal differential output voltage of 4.4 V p-p with positive and negative excursions of ±1.1 V from a common-mode voltage of 1.5 V. The LNA differential gain sets the maximum input signal before saturation. One of three gains is set through the SPI. Overload protection ensures quick recovery time from large input voltages. Because the inputs are capacitively coupled to a bias voltage near midsupply, very large inputs can be handled without interacting with the ESD protection.

Low value feedback resistors and the current-driving capability of the output stage allow the LNA to achieve a low input-referred noise voltage of 1.3 nV/√Hz (at a gain of 21.3 dB). On-chip resistor matching results in precise single-ended gains, which are critical for accurate impedance control. The use of a fully differential topology and negative feedback minimizes distortion. Low second-order harmonic distortion is particularly important in second harmonic ultrasound imaging applications. Differential signaling enables smaller swings at each output, further reducing third-order harmonic distortion.

Active Impedance Matching

The LNA consists of a single-ended voltage gain amplifier with differential outputs and the negative output externally available. For example, with a fixed gain of 8× (17.9 dB), an active input termination is synthesized by connecting a feedback resistor between the negative output pin, LO-x, and the positive input pin, LI-x. This well-known technique is used for interfacing multiple probe impedances to a single system. The input resistance is shown in Equation 1.

$$R_{IN} = \frac{R_{FB}}{(1 + A/2)} \quad (1)$$

where:
$A/2$ is the single-ended gain or the gain from the LI-x inputs to the LO-x outputs.

Because the amplifier has a gain of 8× from its input to its differential output, it is important to note that the gain, A/2, is the gain from Pin LI-x to Pin LO-x and that it is 6 dB less than the gain of the amplifier, or 12.1 dB (4×). The input resistance is reduced by an internal bias resistor of 15 kΩ in parallel with the source resistance connected to Pin LI-x, with Pin LG-x ac grounded. Equation 2 can be used to calculate the required R_{FB} for a desired R_{IN}, even for higher values of R_{IN}.

$$R_{IN} = \frac{R_{FB}}{(1+4)} || 15\,k\Omega \quad (2)$$

For example, to set R_{IN} to 200 Ω, the value of R_{FB} must be 1000 Ω. If the simplified equation (Equation 2) is used to calculate R_{IN}, the value is 197 Ω, resulting in a gain error of less than 0.11 dB. Some factors, such as the presence of a dynamic source resistance, may influence the absolute gain accuracy more significantly. At higher frequencies, the input capacitance of the LNA must be considered. The user must determine the level of matching accuracy and adjust R_{FB} accordingly.

R_{FB} is the resulting impedance of the R_{FB1} and R_{FB2} combination (see Figure 38). Using Register 0x2C in the SPI memory, the AD9278 can be programmed for four impedance matching options: three active terminations and unterminated. Table 9 shows an example of how to select R_{FB1} and R_{FB2} for 66 Ω, 100 Ω, and 200 Ω input impedance for LNA gain = 21.3 dB (12×).

Table 9. Active Termination Example for LNA Gain = 21.3 dB, R_{FB1} = 700 Ω, R_{FB2} = 1400 Ω

Register 0x2C Value	R_S (Ω)	LO-x Switch	LOSW-x Switch	R_{FB} (Ω)	R_{IN} (Ω) (Eq. 1)
00 (default)	100	On	Off	R_{FB1}	100
01	50	On	On	$R_{FB1}\|\|R_{FB2}$	66
10	200	Off	On	R_{FB2}	200
11	N/A	Off	Off	∞	∞

The bandwidth (BW) of the LNA is greater than 100 MHz. Ultimately, the BW of the LNA limits the accuracy of the synthesized R_{IN}. For R_{IN} = R_S up to about 200 Ω, the best match is between 100 kHz and 10 MHz, where the lower frequency limit is determined by the size of the ac coupling capacitors, and the upper limit is determined by the LNA BW. Furthermore, the input capacitance and R_S limit the BW at higher frequencies. Figure 43 shows R_{IN} vs. frequency for various values of R_{FB}.

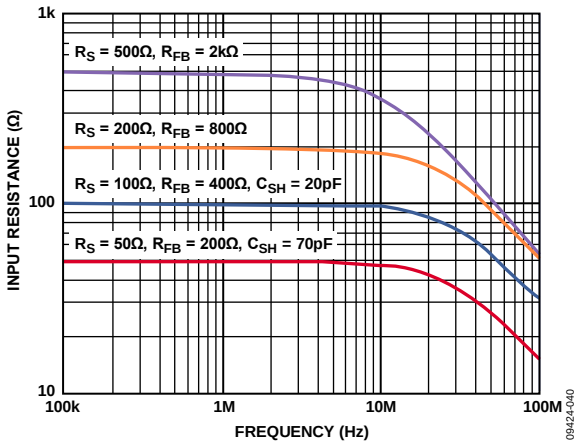

Figure 43. R_{IN} vs. Frequency for Various Values of R_{FB} (Effects of R_{SH} and C_{SH} Are Also Shown)

Note that, at the lowest value of R_{IN} (50 Ω), R_{IN} peaks at frequencies greater than 10 MHz. This is due to the BW roll-off of the LNA.

However, as can be seen for larger R_{IN} values, parasitic capacitance starts rolling off the signal BW before the LNA can produce peaking. C_{SH} further degrades the match; therefore, C_{SH} should not be used for values of R_{IN} that are greater than 100 Ω.

Table 10 lists the recommended values for R_{FB} and C_{SH} in terms of R_{IN}.

C_{FB} is needed in series with R_{FB} because the dc levels at Pin LO-x and Pin LI-x are unequal.

Table 10. Active Termination External Component Values

LNA Gain (dB)	R_{IN} (Ω)	R_{FB} (Ω)	Minimum C_{SH} (pF)	BW (MHz)
15.6	50	200	90	57
17.9	50	250	70	69
21.3	50	350	50	88
15.6	100	400	30	57
17.9	100	500	20	69
21.3	100	700	10	88
15.6	200	800	N/A	72
17.9	200	1000	N/A	72
21.3	200	1400	N/A	72

LNA Noise

The short-circuit noise voltage (input-referred noise) is an important limit on system performance. The short-circuit noise voltage for the LNA is 1.3 nV/√Hz at a gain of 21.3 dB, including the VGA noise at a VGA postamp gain of 27 dB. These measurements, which were taken without a feedback resistor, provide the basis for calculating the input noise and noise figure (NF) performance of the configurations shown in Figure 44.

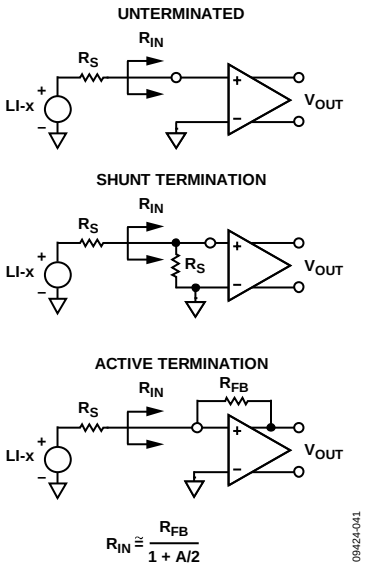

Figure 44. Input Configurations

Figure 45 and Figure 46 are simulations of noise figure vs. R_S results using these configurations and an input-referred noise voltage of 3.5 nV/√Hz for the VGA. Unterminated (R_{FB} = ∞) operation exhibits the lowest equivalent input noise and noise figure. Figure 46 shows the noise figure vs. source resistance rising at low R_S—where the LNA voltage noise is large compared with the source noise—and at high R_S due to the noise contribution from R_{FB}. The lowest NF is achieved when R_S matches R_{IN}.

The main purpose of input impedance matching is to improve the transient response of the system. With shunt termination, the input noise increases due to the thermal noise of the matching resistor and the increased contribution of the LNA input voltage noise generator. With active termination, however, the contributions of both are smaller (by a factor of 1/(1 + LNA Gain)) than they would be for shunt termination.

Figure 45 shows the relative noise figure performance. With an LNA gain of 21.3 dB, the input impedance was swept with R_S to preserve the match at each point. The noise figures for a source impedance of 50 Ω are 7.3 dB, 4.2 dB, and 2.8 dB for the shunt termination, active termination, and unterminated configurations, respectively. The noise figures for 200 Ω are 4.5 dB, 1.7 dB, and 1.0 dB, respectively.

Figure 46 shows the noise figure as it relates to R_S for various values of R_{IN}, which is helpful for design purposes.

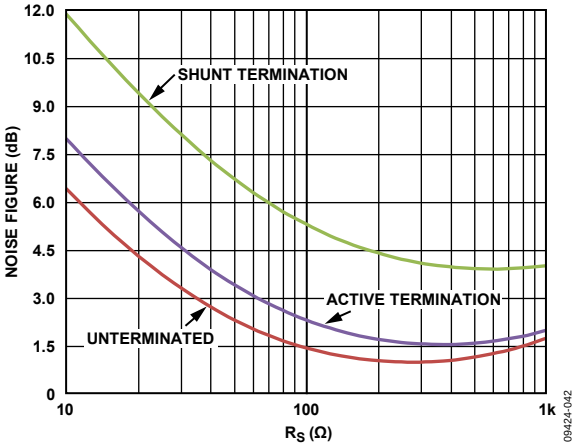

Figure 45. Noise Figure vs. R_S for Shunt Termination, Active Termination Matched and Unterminated Inputs, V_{GAIN} = 1.6 V

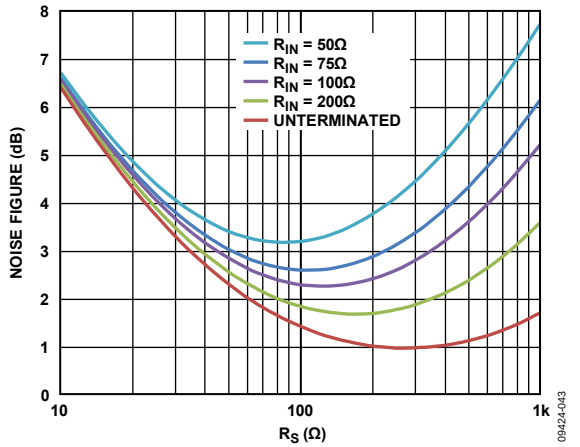

Figure 46. Noise Figure vs. R_S for Various Fixed Values of R_{IN}, Active Termination Matched Inputs, V_{GAIN} = 1.6 V

Input Overdrive

Excellent overload behavior is of primary importance in ultrasound. Both the LNA and VGA have built-in overdrive protection and quickly recover after an overload event.

As with any amplifier, voltage clamping prior to the inputs is highly recommended if the application is subject to high transient voltages.

Figure 47 shows a simplified ultrasound transducer interface. A common transducer element serves the dual functions of transmitting and receiving ultrasound energy. During the transmitting phase, high voltage pulses are applied to the ceramic elements. A typical transmit/receive (T/R) switch can consist of four high voltage diodes in a bridge configuration. Although the diodes ideally block transmit pulses from the sensitive receiver input, diode characteristics are not ideal, and the resulting leakage transients imposed on the LI-x inputs can be problematic.

The external input overload protection scheme also contains a pair of back-to-back signal diodes that should be in place prior to the ac coupling capacitors. Keep in mind that all diodes are prone to exhibiting some amount of shot noise. Many types of diodes are available for achieving the desired noise performance. The configuration shown in Figure 47 tends to add 2 nV/√Hz of input-referred noise. Decreasing the 5 kΩ resistor and increasing the 2 kΩ resistor may improve noise contribution, depending on the application. With the diodes shown in Figure 47, clamping levels of ±0.5 V or less significantly enhance the overload performance of the system.

Because ultrasound is a pulse system and time-of-flight is used to determine depth, quick recovery from input overloads is essential. Overload can occur in the preamplifier and in the VGA. Immediately following a transmit pulse, the typical VGA gains are low, and the LNA is subject to overload from T/R switch leakage. With increasing gain, the VGA can become overloaded due to strong echoes that occur near field echoes and acoustically dense materials, such as bone.

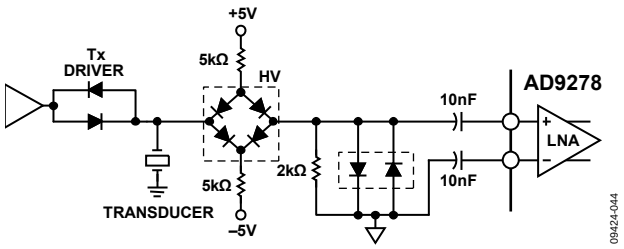

Figure 47. Input Overload Protection

Variable Gain Amplifier (VGA)

The differential X-AMP VGA provides precise input attenuation and interpolation. It has a low input-referred noise of 3.5 nV/√Hz and excellent gain linearity. The VGA is driven by a fully differential input signal from the LNA. The X-AMP architecture produces a linear-in-dB gain law conformance and low distortion levels—only deviating ±0.5 dB or less from the ideal. The gain slope is monotonic with respect to the control voltage and is stable with variations in process, temperature, and supply. The resulting total gain range is 45 dB, which allows for range loss at the endpoints.

The X-AMP inputs are part of a programmable gain feedback amplifier (PGA) that completes the VGA. The PGA in the VGA can be programmed to a gain of 21 dB, 24 dB, 27 dB, or 30 dB. This allows for optimization of channel gain for different imaging modes in the ultrasound system. The VGA bandwidth is approximately 100 MHz. The input stage is designed to ensure excellent frequency response uniformity across the gain setting. For TGC mode, this minimizes time delay variation across the gain range.

Gain Control

The gain control interface, GAIN±, is a differential input. V_{GAIN} varies the gain of all VGAs through the interpolator by selecting the appropriate input stages connected to the input attenuator. For GAIN− at 0.8 V, the nominal GAIN+ range for 28 dB/V is 0 V to 1.6 V, with the best gain linearity from approximately 0.16 V to 1.44 V, where the error is typically less than ±0.5 dB. For GAIN+ voltages greater than 1.44 V and less than 0.16 V, the error increases. The value of GAIN+ can exceed the supply voltage by 1 V without gain foldover.

Gain control response time is less than 750 ns to settle within 10% of the final value for a change from minimum to maximum gain.

There are two ways in which the GAIN+ and GAIN− pins can be interfaced. Using a single-ended method, a Kelvin type of connection to ground can be used, as shown in Figure 48. For driving multiple devices, it is preferable to use a differential method, as shown in Figure 49. In either method, the GAIN+ and GAIN− pins should be dc-coupled and driven to accommodate a 1.6 V full-scale input.

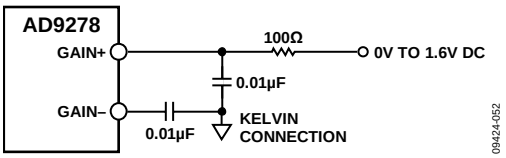

Figure 48. Single-Ended GAIN± Pin Configuration

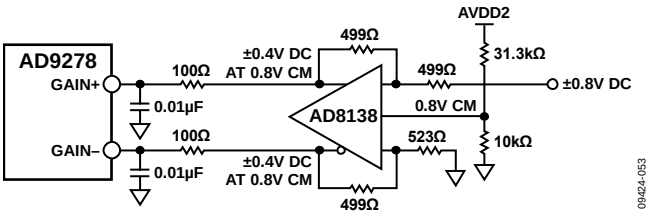

Figure 49. Differential GAIN± Pin Configuration

VGA Noise

In a typical application, a VGA compresses a wide dynamic range input signal to within the input span of an ADC. The input-referred noise of the LNA limits the minimum resolvable input signal, whereas the output-referred noise, which depends primarily on the VGA, limits the maximum instantaneous dynamic range that can be processed at any one particular gain control voltage. This latter limit is set in accordance with the total noise floor of the ADC.

Output-referred noise as a function of GAIN+ is shown in Figure 7, Figure 8, and Figure 10 for the short-circuit input conditions. The input noise voltage is simply equal to the output noise divided by the measured gain at each point in the control range.

The output-referred noise is a flat 50 nV/√Hz (postamp gain = 24 dB) over most of the gain range because it is dominated by the fixed output-referred noise of the VGA. At the high end of the gain control range, the noise of the LNA and of the source prevail. The input-referred noise reaches its minimum value near the maximum gain control voltage, where the input-referred contribution of the VGA is miniscule.

At lower gains, the input-referred noise and, therefore, the noise figure, increases as the gain decreases. The instantaneous dynamic range of the system is not lost, however, because the input capacity increases as the input-referred noise increases. The contribution of the ADC noise floor has the same dependence. The important relationship is the magnitude of the VGA output noise floor relative to that of the ADC.

Gain control noise is a concern in very low noise applications. Thermal noise in the gain control interface can modulate the channel gain. The resultant noise is proportional to the output signal level and is usually evident only when a large signal is present. The gain interface includes an on-chip noise filter, which significantly reduces this effect at frequencies above 5 MHz. Care should be taken to minimize noise impinging at the GAIN± inputs. An external RC filter can be used to remove V_{GAIN} source noise. The filter bandwidth should be sufficient to accommodate the desired control bandwidth.

Antialiasing Filter (AAF)

The filter that the signal reaches prior to the ADC is used to reject dc signals and to band limit the signal for antialiasing. The antialiasing filter is a combination of a single-pole high-pass filter and a second-order low-pass filter. The high-pass filter can be configured at a ratio of the low-pass filter cutoff. This is selectable through the SPI.

The filter uses on-chip tuning to trim the capacitors and, in turn, to set the desired cutoff frequency and reduce variations. The default −3 dB low-pass filter cutoff is 1/3 or 1/4.5 the ADC sample clock rate. The cutoff can be scaled to 0.7, 0.8, 0.9, 1, 1.1, 1.2, or 1.3 times this frequency through the SPI. The cutoff tolerance is maintained from 8 MHz to 18 MHz.

Tuning is normally off to avoid changing the capacitor settings during critical times. The tuning circuit is enabled and disabled through the SPI. Initializing the tuning of the filter must be performed after initial power-up and after reprogramming the filter cutoff scaling or ADC sample rate. Occasional retuning during an idle time is recommended to compensate for temperature drift.

A total of eight SPI-programmable settings allows the user to vary the high-pass filter cutoff frequency as a function of the low-pass cutoff frequency. Two examples are shown in Table 11: one is for an 8 MHz low-pass cutoff frequency, and the other is for an 18 MHz low-pass cutoff frequency. In both cases, as the ratio decreases, the amount of rejection on the low-end frequencies increases. Therefore, making the entire AAF frequency pass band narrow can reduce low frequency noise or maximize dynamic range for harmonic processing.

Table 11. SPI-Selectable High-Pass Filter Cutoff Options

		High-Pass Cutoff Frequency	
SPI Setting	Ratio[1]	Low-Pass Cutoff = 8 MHz	Low-Pass Cutoff = 18 MHz
0	12.00	670 kHz	1.5 MHz
1	8.57	930 kHz	2.1 MHz
2	6.67	1.2 MHz	2.7 MHz
3	5.46	1.47 MHz	3.3 MHz
4	4.62	1.73 MHz	3.9 MHz
5	4.00	2.0 MHz	4.5 MHz
6	3.53	2.27 MHz	5.1 MHz
7	3.16	2.53 MHz	5.7 MHz

[1] Ratio = low-pass filter cutoff frequency/high-pass filter cutoff frequency.

ADC

The AD9278 uses a pipelined ADC architecture. The quantized output from each stage is combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on preceding samples. Sampling occurs on the rising edge of the clock.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and output clocks.

Clock Input Considerations

For optimum performance, the AD9278 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 50 shows the preferred method for clocking the AD9278. A low jitter clock source, such as the Valpey Fisher oscillator, VFAC3-BHL-50 MHz, is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9278 to approximately 0.8 V p-p differential. This helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD9278, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

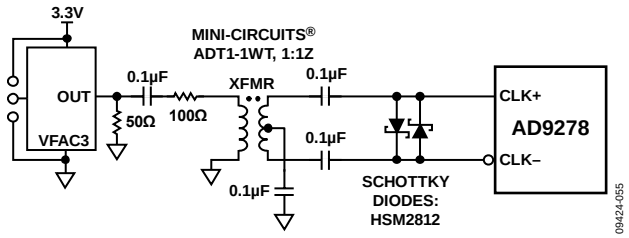

Figure 50. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL signal to the sample clock input pins, as shown in Figure 51. The AD951x family of clock drivers offers excellent jitter performance.

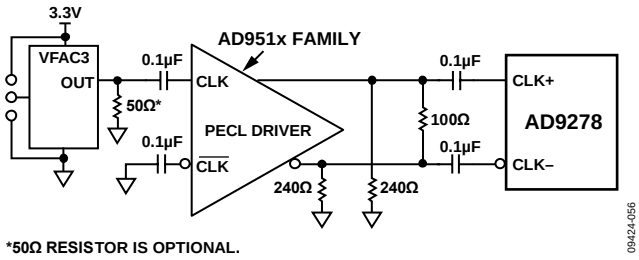

Figure 51. Differential PECL Sample Clock

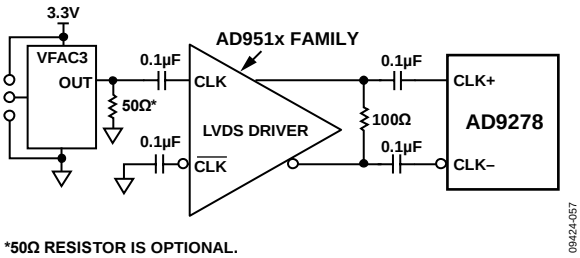

Figure 52. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 53). Although the CLK+ input circuit supply is AVDD1 (1.8 V), this input is designed to withstand input voltages of up to 3.3 V, making the selection of the drive logic voltage very flexible.

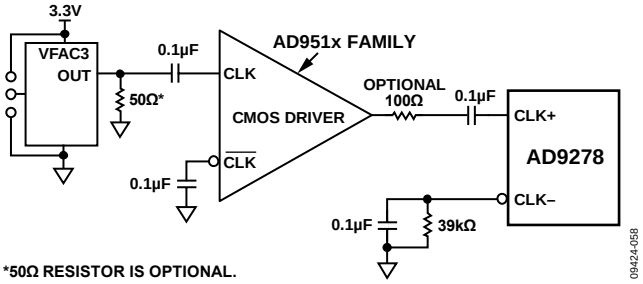

Figure 53. Single-Ended 1.8 V CMOS Sample Clock

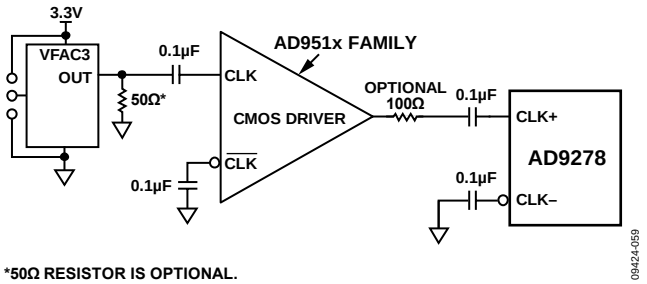

Figure 54. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9278 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9278. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See Table 19 for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated as follows:

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 55).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9278. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources, such as the Valpey Fisher VFAC3 series. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about how jitter performance relates to ADCs (visit www.analog.com).

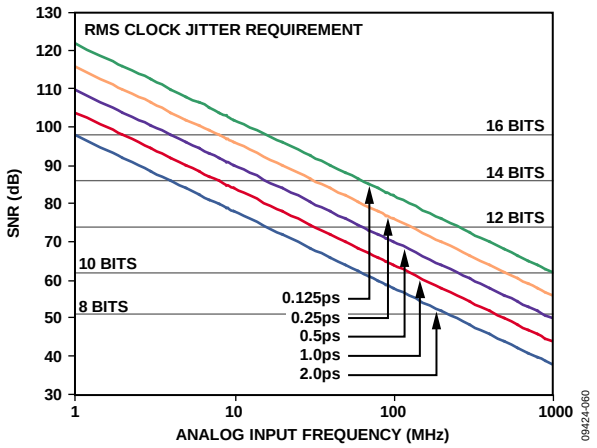

Figure 55. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation and Power-Down Mode

As shown in Figure 56 and Figure 57, the power dissipated by the AD9278 is proportional to its sample rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and the bias current of the LVDS output drivers.

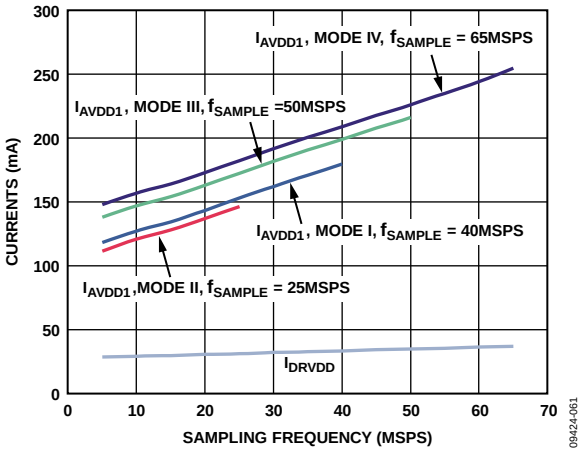

Figure 56. Supply Current vs. f_{SAMPLE} for f_{IN} = 5 MHz

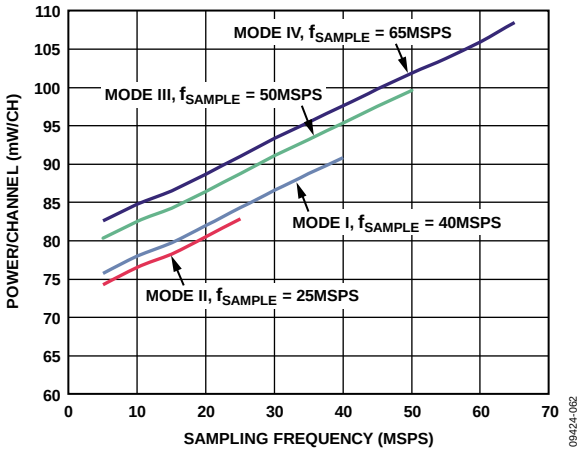

Figure 57. Power per Channel vs. f_{SAMPLE} for f_{IN} = 5 MHz

The AD9278 features scalable LNA bias currents (see Table 19, Register 0x12). The default LNA bias current settings are high. Figure 58 shows the typical reduction of AVDD2 current with each bias setting. It is also recommended that the LNA offset be adjusted using Register 0x10 (see Table 19) when the LNA bias setting is low.

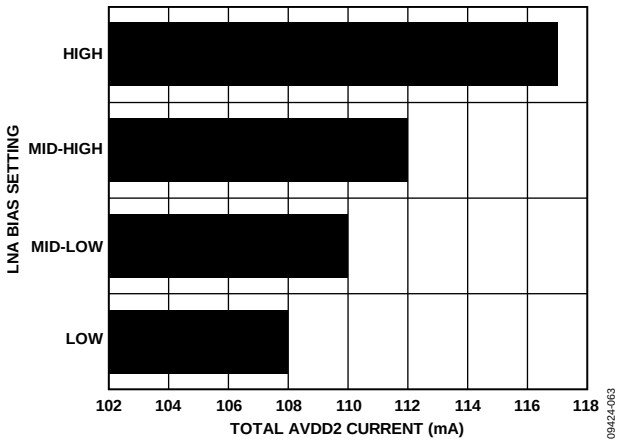

Figure 58. AVDD2 Current at Different LNA Bias Settings, f_{SAMPLE} = 40 MSPS

By asserting the PDWN pin high, the AD9278 is placed into power-down mode. In this state, the device typically dissipates 5 mW. During power-down, the LVDS output drivers are placed into a high impedance state. The AD9278 returns to normal operating mode when the PDWN pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

By asserting the STBY pin high, the AD9278 is placed into a standby mode. In this state, the device typically dissipates 420 mW. During standby, the entire part is powered down except the internal references. The LVDS output drivers are placed into a high impedance state. This mode is well suited for applications that require power savings because it allows the device to be powered down when not in use and then quickly powered up. The time to power the device back up is also greatly reduced. The AD9278 returns to normal operating mode when the STBY pin is pulled low. This pin is both 1.8 V and 3.3 V tolerant.

In power-down mode, low power dissipation is achieved by shutting down the reference, reference buffer, PLL, and biasing networks. The decoupling capacitors on VREF are discharged when entering power-down mode and must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in the power-down mode: shorter cycles result in proportionally shorter wake-up times. To restore the device to full operation, approximately 0.5 ms is required when using the recommended 1 µF and 0.1 µF decoupling capacitors on the VREF pin and the 0.01 µF decoupling capacitors on the GAIN± pins. Most of this time is dependent on the gain decoupling: higher value decoupling capacitors on the GAIN± pins result in longer wake-up times.

A number of other power-down options are available when using the SPI port interface. The user can individually power down each channel or put the entire device into standby mode. This allows the user to keep the internal PLL powered up when fast wake-up times are required. The wake-up time is slightly dependent on gain. To achieve a 1 µs wake-up time when the device is in standby mode, 0.8 V must be applied to the GAIN± pins. See Table 19 for more details on using these features.

Power and Ground Recommendations

When connecting power to the AD9278, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one 1.8 V supply is available, it should be routed to the AVDD1 pin first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD pin. The user should employ several decoupling capacitors on all supplies to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the part, with minimal trace lengths.

A single PCB ground plane should be sufficient when using the AD9278. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance can be easily achieved.

Digital Outputs and Timing

The AD9278 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This can be changed to a low power, reduced signal option similar to the IEEE 1596.3 standard via the SPI, using Register 0x14, Bit 6. This LVDS standard can further reduce the overall power dissipation of the device by approximately 36 mW.

The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver.

The AD9278 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a 100 Ω termination resistor placed as close to the receiver as possible. No far-end receiver termination and poor differential trace routing may result in timing errors. It is recommended that the trace length be no longer than 24 inches and that the differential output traces be kept close together and at equal lengths. An example of the FCO (CH2), DCO (CH1), and data (CH3) stream with proper trace length and position is shown in Figure 59.

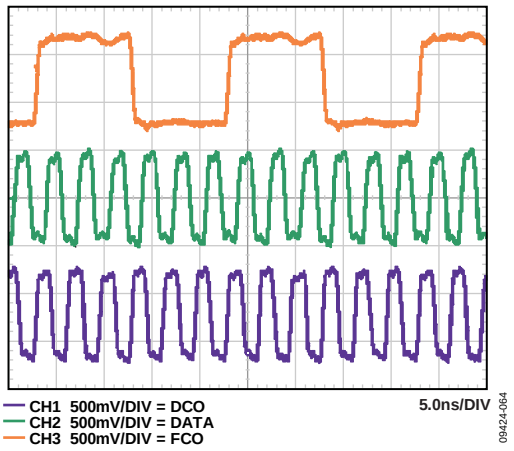

Figure 59. LVDS Output Timing Example in ANSI-644 Mode (Default)

An example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 24 inches on regular FR-4 material is shown in Figure 60. Figure 61 shows an example of the trace lengths exceeding 24 inches on regular FR-4 material. Notice that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position; therefore, the user must determine whether the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches.

Additional SPI options allow the user to further increase the internal termination (and, therefore, increase the current) of all eight outputs to drive longer trace lengths (see Figure 62). Even though this produces sharper rise and fall times on the data edges, is less prone to bit errors, and improves frequency distribution (see Figure 62), the power dissipation of the DRVDD supply increases when this option is used.

In cases that require increased driver strength to the DCO± and FCO± outputs because of load mismatch, Register 0x15 allows the user to double the drive strength. To do this, set the appropriate bit in Register 0x05. Note that this feature cannot be used with Bits[5:4] in Register 0x15 because these bits take precedence over this feature. See Table 19 for more details.

The format of the output data is offset binary by default. Table 12 provides an example of the output coding format. To change the output data format to twos complement, see the Memory Map section.

Table 12. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 2 V p-p (V)	Digital Output Offset Binary (D11 to D0)
4095	+1.00	1111 1111 1111
2048	0.00	1000 0000 0000
2047	−0.000488	0111 1111 1111
0	−1.00	0000 0000 0000

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12 bits times the sample clock rate, with a maximum of 780 Mbps (12 bits × 65 MSPS = 780 Mbps). The lowest typical conversion rate is 10 MSPS, but the PLL can be set up for encode rates as low as 5 MSPS via the SPI if lower sample rates are required for a specific application. See Table 19 for details on enabling this feature.

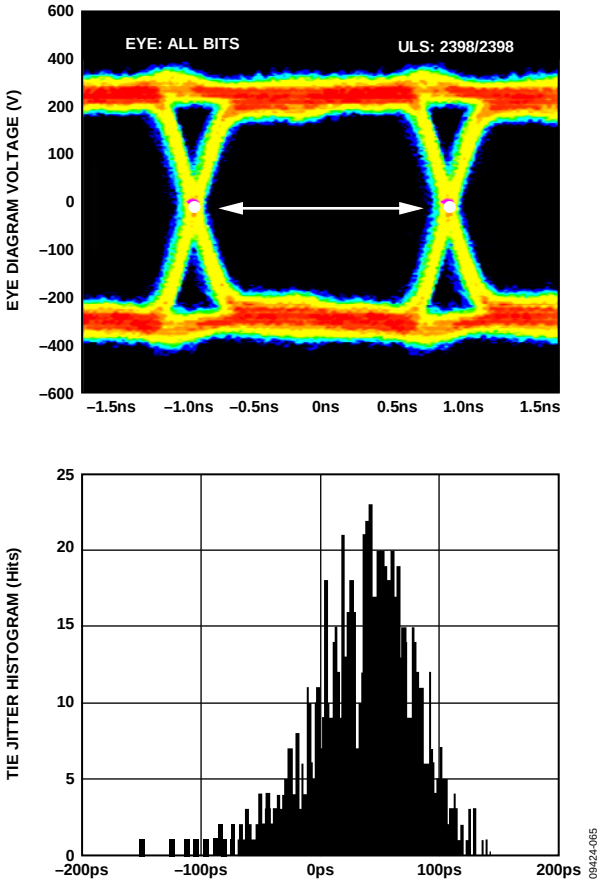

Figure 60. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4

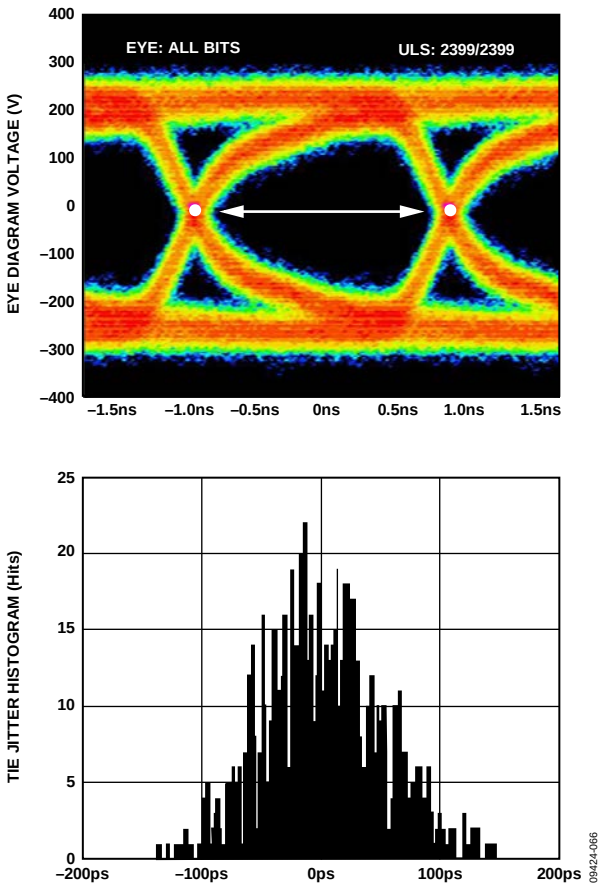

Figure 61. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Greater than 24 Inches on Standard FR-4

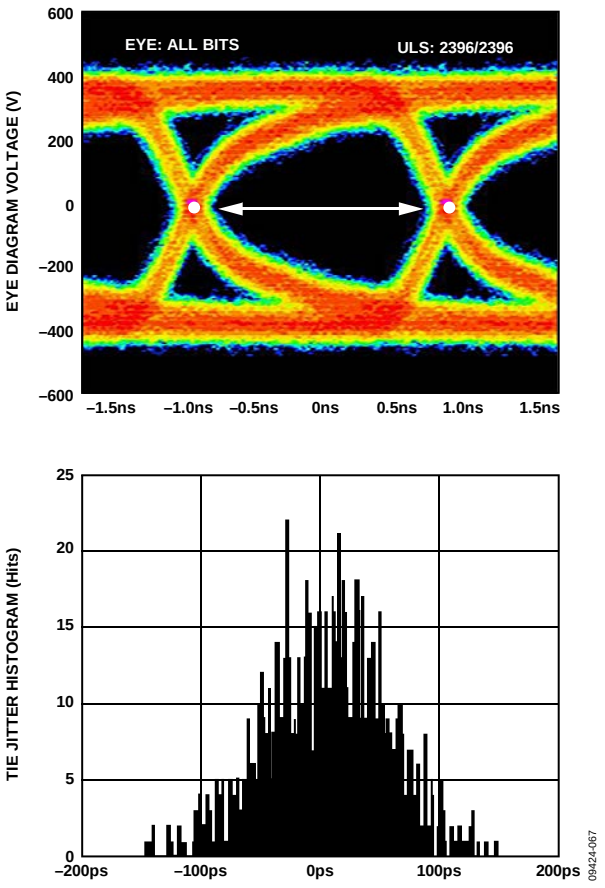

Figure 62. Data Eye for LVDS Outputs in ANSI-644 Mode with 100 Ω Termination On and Trace Lengths of Greater Than 24 Inches on Standard FR-4

Two output clocks are provided to assist in capturing data from the AD9278. DCO± is used to clock the output data and is equal to six times the sampling clock rate. Data is clocked out of the AD9278 and must be captured on the rising and falling edges of DCO±, which supports double data rate (DDR) capturing. The frame clock output (FCO±) is used to signal the start of a new output byte and is equal to the sampling clock rate. See the timing diagram shown in Figure 2 for more information.

When using the serial port interface (SPI), the DCO± phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins if required. The default DCO± timing, as shown in Figure 2, is 90° relative to the output data edge.

An 8-, 10-, or 14-bit serial stream can also be initiated from the SPI. This allows the user to implement different serial streams and to test device compatibility with lower and higher resolution systems. When changing the resolution to an 8- or 10-bit serial stream, the data stream is shortened. When using the 14-bit option, the data stream stuffs two 0s at the end of the normal 12-bit serial data.

When using the SPI, all of the data outputs can also be inverted from their nominal state by setting Bit 2 in the OUTPUT_MODE register (Address 0x14). This is not to be confused with inverting the serial stream to an LSB first mode. In default mode, as shown in Figure 2, the MSB is represented first in the data output serial stream. However, this order this can be inverted so that the LSB is represented first in the data output serial stream (see Figure 3).

There are 12 digital output test pattern options available that can be initiated through the SPI. This feature is useful when validating receiver capture and timing. See Table 13 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen. Note that some patterns may not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the user pattern registers (Address 0x19 through Address 0x1C). All test mode options except PN sequence short and PN sequence long can support 8- to 14-bit word lengths to verify data capture to the receiver.

The PN sequence short pattern produces a pseudo random bit sequence that repeats itself every $2^9 - 1$ bits, or 511 bits. A description of the PN sequence short and how it is generated can be found in Section 5.1 of the ITU-T O.150 (05/96) standard. The only difference is that the starting value is a specific value instead of all 1s (see Table 14 for the initial values).

Table 13. Flexible Output Test Modes[1]

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	1000 0000 0000	Same	Yes
0010	+Full-scale short	1111 1111 1111	Same	Yes
0011	−Full-scale short	0000 0000 0000	Same	Yes
0100	Checkerboard	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long	N/A	N/A	Yes
0110	PN sequence short	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No
1001	1-/0-bit toggle	1010 1010 1010	N/A	No
1010	1× sync	0000 0011 1111	N/A	No
1011	One bit high	1000 0000 0000	N/A	No
1100	Mixed bit frequency	1010 0011 0011	N/A	No

[1] N/A is not applicable.

The PN sequence long pattern produces a pseudo random bit sequence that repeats itself every $2^{23} - 1$ bits, or 8,388,607 bits. A description of the PN sequence long and how it is generated can be found in Section 5.6 of the ITU-T O.150 (05/96) standard. The only differences are that the starting value is a specific value instead of all 1s and that the AD9278 inverts the bit stream with relation to the ITU-T standard (see Table 14 for the initial values).

Table 14. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0DF	0xDF9, 0x353, 0x301
PN Sequence Long	0x29B80A	0x591, 0xFD7, 0x0A3

See the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO Pin

This pin is required to operate the SPI. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. If applications require that this pin be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

SCLK Pin

This pin is required to operate the SPI port interface. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

CSB Pin

This pin is required to operate the SPI port interface. It has an internal 70 kΩ pull-up resistor that pulls this pin high and is both 1.8 V and 3.3 V tolerant.

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor nominally equal to 10.0 kΩ to ground at the RBIAS pin. Using a resistor other than the recommended 10.0 kΩ resistor for RBIAS degrades the performance of the device. Therefore, it is imperative that at least a 1% tolerance on this resistor be used to achieve consistent performance.

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9278. This is gained up internally by a factor of 2, setting VREF to 1.0 V, which results in a full-scale differential input span of 2.0 V p-p for the ADC. VREF is set internally by default, but the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy. However, the AD9278 does not support ADC full-scale ranges below 2.0 V p-p.

When applying the decoupling capacitors to the VREF pin, use ceramic, low ESR capacitors. These capacitors should be close to the reference pin and on the same layer of the PCB as the AD9278. The VREF pin should have both a 0.1 µF capacitor and a 1 µF capacitor connected in parallel to the analog ground. These capacitor values are recommended for the ADC to properly settle and acquire the next valid sample.

The reference settings can be selected using the SPI. The settings allow two options: using the internal reference or using an external reference. The internal reference option is the default setting and has a resulting differential span of 2 V p-p.

Table 15. SPI-Selectable Reference Settings

SPI-Selected Mode	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	N/A	2 × external reference
Internal Reference (Default)	1.0	2.0

CW DOPPLER OPERATION

Each channel of the AD9278 includes a I/Q demodulator. Each demodulator has an individual programmable phase shifter. The I/Q demodulator is ideal for phased array beamforming applications in medical ultrasound. Each channel can be programmed for 16 delay states/360° (or 22.5°/step), selectable via the SPI port. The part has a RESET input used to synchronize the LO dividers of each channel. If multiple AD9278s are used, a common RESET across the array ensures a synchronized phase for all channels. Internal to the AD9278, the individual Channel I and Channel Q outputs are current summed. If multiple AD9278s are used, the I and Q outputs from each AD9278 can be current summed and converted to a voltage using an external transimpedance amplifier.

Quadrature Generation

The internal 0° and 90° LO phases are digitally generated by a divide-by-4 logic circuit. The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals is intrinsically 50% and is unaffected by the asymmetry of the externally connected 4LO input. Furthermore, the divider is implemented such that the 4LO signal reclocks the final flip-flops that generate the internal LO signals and, thereby, minimizes noise introduced by the divide circuitry.

For optimum performance, the 4LO input is driven differentially, as on the AD9278 evaluation board (see the Ordering Guide). The common-mode voltage on each pin is approximately 1.2 V with the nominal 3 V supply. It is important to ensure that the LO source have very low phase noise (jitter), a fast slew rate, and an adequate input level to obtain optimum performance of the CW signal chain.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. A RESET pin is provided to synchronize the LO divider circuits in different AD9278s when they are used in arrays. The RESET pin resets the dividers to a known state after power is applied to multiple AD9278s. Accurate channel-to-channel phase matching can only be achieved via a common pulse on the RESET pin when using more than one AD9278.

I/Q Demodulator and Phase Shifter

The I/Q demodulators consist of double-balanced passive mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability matching the LNA output full scale. These currents are then presented to the mixers, which convert them to baseband (RF − LO) and twice RF (RF + LO). The signals are phase shifted according to the codes programmed into the SPI latch (see Table 16). The phase shift function is an integral part of the overall circuit. The phase shift listed in Column 1 of Table 16 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to a pair of RF inputs to an AD9278, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and that of Channel 2 is 0001, then Channel 2 leads Channel 1 by 22.5°.

Table 16. Phase Select Code for Channel-to-Channel Phase Shift

Φ Shift	I/Q Demodulator Phase (SPI Register 0x2D[3:0])
0°	0000
22.5°	0001
45°	0010
67.5°	0011
90°	0100
112.5°	0101
135°	0110
157.5°	0111
180°	1000
202.5°	1001
225°	1010
247.5°	1011
270°	1100
292.5°	1101
315°	1110
337.5°	1111

Dynamic Range and Noise

Figure 63 is an interconnection block diagram of all eight channels of the AD9278. More channels are easily added to that summation (up to 32 when using an ADA4841 as the summation amplifier) by wire-OR connecting the outputs as shown. In beamforming applications, the I and Q outputs of a number of receiver channels are summed. The dynamic range of the system increases by the factor $10\log_{10}(N)$, where N is the number of channels (assuming random uncorrelated noise). The noise in the 8-channel example of Figure 63 is increased by 9 dB while the signal quadruples (18 dB), yielding an aggregate SNR improvement of (18 − 9) = 9 dB.

The output-referred noise of the CW signal path depends on the LNA gain and the selection of the external summing amplifier and the value of R_{FILT}. To determine the output referred noise, it is important to know the active low-pass filter (LPF) values, R_{FILT}, and C_{FILT}, shown in Figure 63. Typical filter values for a single channel are 2 kΩ for R_{FILT} and 0.8 nF for C_{FILT}; these values implement a 100 kHz single-pole LPF. In the case where eight channels are summed, R_{FILT} and C_{FILT} are 250 Ω and 6.4 nF.

If the RF and LO are offset by 10 kHz, the demodulated signal is 10 kHz and is passed by the LPF. The single-channel mixing gain from the RF input to the ADA4841 output (for example, I1′, Q1′) is approximately the LNA gain for R_{FILT} and C_{FILT} of 2 kΩ and 0.8 nF.

This gain can be increased by increasing the filter resistor while maintaining the corner frequency. The factor limiting the magnitude of the gain is the output swing and drive capability of the op amp selected for the I-to-V converter, in this example, the ADA4841. Because any amplifier has limited drive capability, there is a finite number of channels that can be summed. The channel-summing limit relates directly to the current drive capability of the amplifier used to implement the active low-pass filter and current-to-voltage converter. The maximum sum, when the ADA4841 is used, is 32 channels of the AD9278; that is, four AD9278s (4 × 8 = 32 channels) can be summed in one ADA4841.

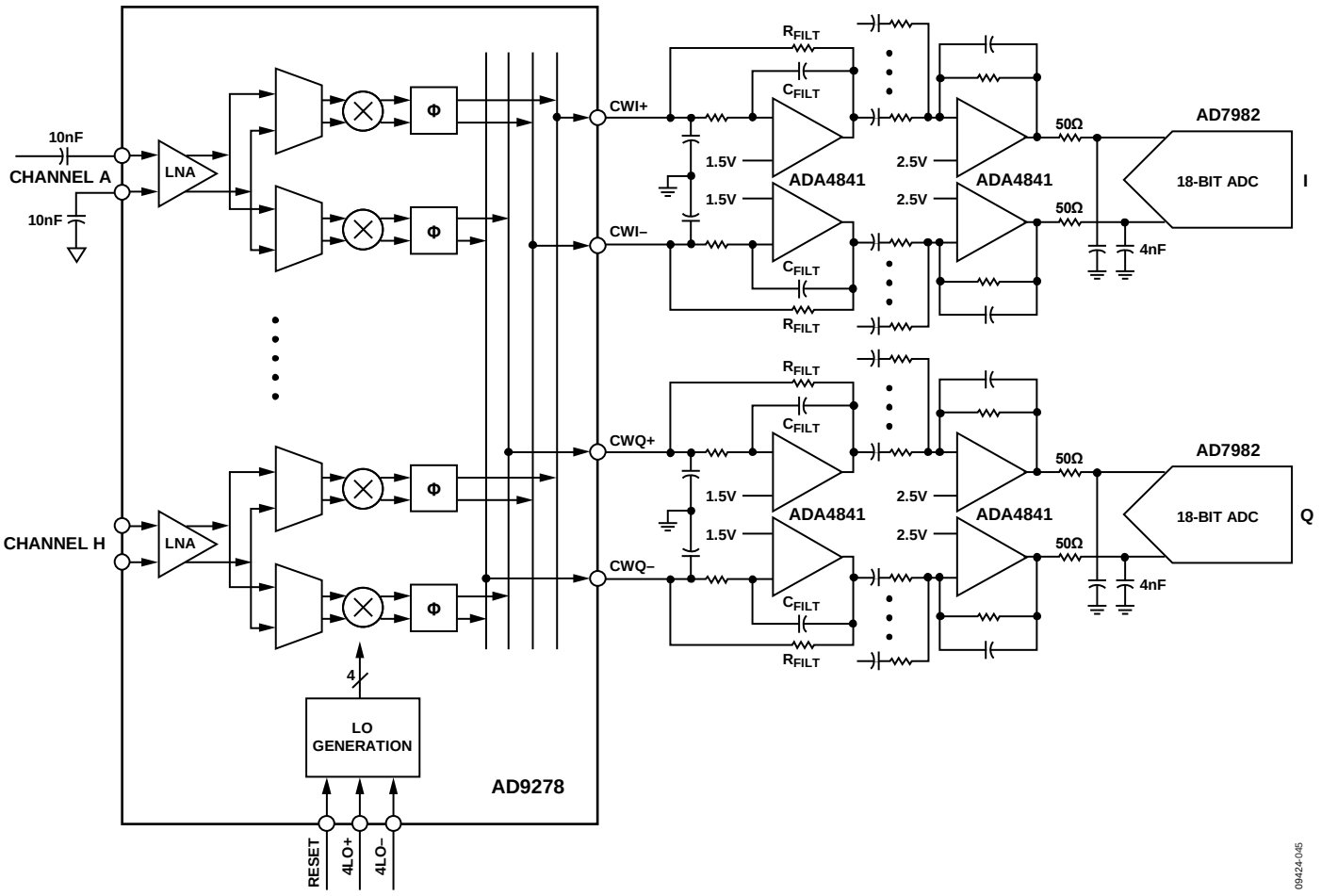

Figure 63. Typical Connection Interface for I/Q Outputs in CW Mode

Phase Compensation and Analog Beamforming

Beamforming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals generated from a common source but received at different times by a multielement ultrasound transducer. Beamforming has two functions: it imparts directivity to the transducer, enhancing its gain, and it defines a focal point within the body from which the location of the returning echo is derived. The primary application for the AD9278 I/Q demodulators is in analog beamforming circuits for ultrasound CW Doppler.

Modern ultrasound machines used for medical applications employ an array of receivers for beamforming, with typical CW Doppler array sizes of up to 64 receiver channels that are phase shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), whereas the noise is increased by the square root of the number of channels. This technique enhances the signal-to-noise performance of the machine. The critical elements in a beamformer design are the means to align the incoming signals in the time domain and the means to sum the individual signals into a composite whole.

In traditional analog beamformers incorporating Doppler, a V-to-I converter per channel and a crosspoint switch precede passive delay lines used as a combined phase shifter and summing circuit. The system operates at the carrier frequency (RF) through the delay line, which also sums the signals from the various channels, and then the combined signal is down-converted by an I/Q demodulator. The dynamic range of the demodulator can limit the achievable dynamic range.

The resultant I and Q signals are filtered and then sampled by two high resolution analog-to-digital converters. The sampled signals are processed to extract the relevant Doppler information.

Alternatively, the RF signal can be processed by downconversion on each channel individually, phase shifting the downconverted signal, and then combining all channels. Because the dynamic range expansion from beamforming occurs after demodulation, the demodulator dynamic range has little effect on the output dynamic range. The AD9278 implements this architecture. The downconversion is done by an I/Q demodulator on each channel, and the summed current output is the same as in the delay line approach. The subsequent filters after the I-to-V conversion and the ADCs are similar.

For CW Doppler operation, the AD9278 integrates the LNA, phase shifter, frequency conversion, and I/Q demodulation into a single package and directly yields the baseband signal. Figure 64 is a simplified diagram showing the concept for four channels. The ultrasound wave (US wave) is received by four transducer elements, TE1 through TE4, in an ultrasound probe and generates signals E1 through E4. In this example, the phase at TE1 leads the phase at TE2 by 45°.

In a real application, the phase difference depends on the element spacing, wavelength (λ), speed of sound, angle of incidence, and other factors. In Figure 64, the signals E1 through E4 are amplified by the low noise amplifiers. For optimum signal-to-noise performance, the output of the LNA is applied directly to the input of the demodulators. To sum the signals E1 through E4, E2 is shifted 45° relative to E1 by setting the phase code in Channel 2 to 0010, E3 is shifted 90° (0100), and E4 is shifted 135° (0110). The phase aligned current signals at the output of the AD9278 are summed in an I-to-V converter to provide the combined output signal with a theoretical improvement in dynamic range of 6 dB for the four channels.

CW Application Information

The RESET pin is used to synchronize the LO dividers in AD9278 arrays. Because they are driven by the same internal LO, the four channels in any AD9278 are inherently synchronous. However, when multiple AD9278s are used, it is possible that their dividers wake up in different phase states. The function of the RESET pin is to phase align all the LO signals in multiple AD9278s.

The 4LO divider of each AD9278 can be initiated in one of four possible states: 0°, 90°, 180°, and 270° relative to other AD9278s. The internally generated I/Q signals of each AD9278 LO are always at a 90° angle relative to each other, but a phase shift can occur during power-up between the dividers of multiple AD9278s used in a common array.

The RESET mechanism also allows the measurement of non-mixing gain from the RF input to the output. The rising edge of the active high RESET pulse can occur at any time; however, the duration should be ≥ 20 ns minimum. When the RESET pulse transitions from high to low, the LO dividers are reactivated on the next rising edge of the 4LO clock. To guarantee synchronous operation of an array of AD9278s, the RESET pulse must go low on all devices before the next rising edge of the 4LO clock.

Therefore, it is best to have the RESET pulse go low on the falling edge of the 4LO clock; at the very least, the t_{SETUP} should be ≥ 5 ns. An optimal timing setup is for the RESET pulse to go high on a 4LO falling edge and to go low on a 4LO falling edge; this gives 15 ns of setup time even at a 4LO frequency of 32 MHz (8 MHz internal LO). Use the following procedure to check the synchronization of multiple AD9278s:

1. Activate at least one channel per AD9278 by setting the appropriate channel enable bit in the serial interface.
2. Set the phase code of all AD9278 channels to the same logic state, for example, 0000.
3. Apply the same test signal to all devices to generate a sine wave in the baseband output and measure the output of one channel per device.
4. Apply a RESET pulse to all AD9278s.
5. Because all phase codes of the AD9278s should be the same, the combined signal of multiple devices should be N times greater than a single channel. If the combined signal is less than N times one channel, one or more of the LO phases of the individual AD9278s are in error.

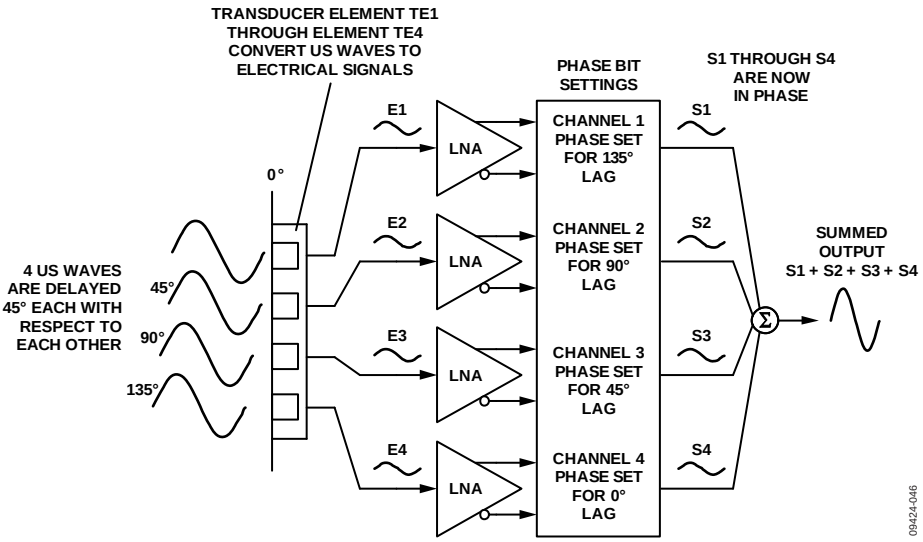

Figure 64. Simplified Example of the AD9278 Phase Shifter

SERIAL PORT INTERFACE (SPI)

The AD9278 serial port interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Three pins define the serial port interface, or SPI: SCLK, SDIO, and CSB (see Table 17). The SCLK (serial clock) pin is used to synchronize the read and write data presented to the device. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent to and read from the internal memory map registers of the device. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 17. Serial Port Pins

Pin	Function
SCLK	Serial clock. Serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. Dual-purpose pin that typically serves as an input or an output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select bar (active low). This control gates the read and write cycles.

The falling edge of CSB in conjunction with the rising edge of SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 66 and Table 18.

During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDIO to execute instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without the need for additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the CSB line can be tied and held high. This places the remainder of the SPI pins in their secondary mode, as defined in the SDIO Pin and SCLK Pin sections. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the CSB line. When operating in 2-wire mode, it is recommended that a 1-, 2-, or 3-byte transfer be used exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or LSB first mode. MSB first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 17 constitute the physical interface between the user's programming device and the serial port of the AD9278. The SCLK and CSB pins function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDIO pins share a common connection, ensure that proper V_{OH} levels are met. Figure 65 shows the number of SDIO pins that can be connected together and the resulting V_{OH} level, assuming the same load for each AD9278.

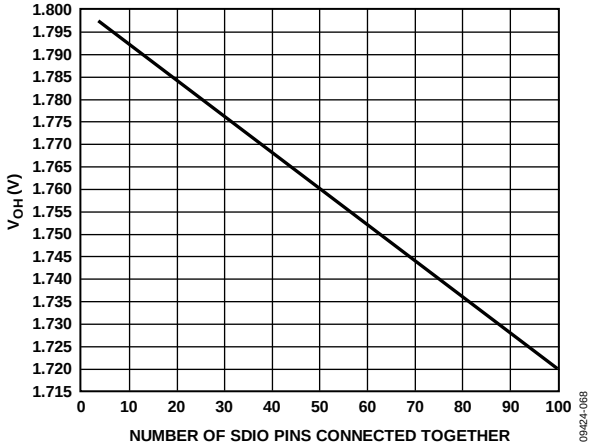

Figure 65. SDIO Pin Loading

This interface is flexible enough to be controlled by either serial PROMs or PIC microcontrollers, providing the user with an alternative method, other than a full SPI controller, for programming the device (see the AN-812 Application Note).

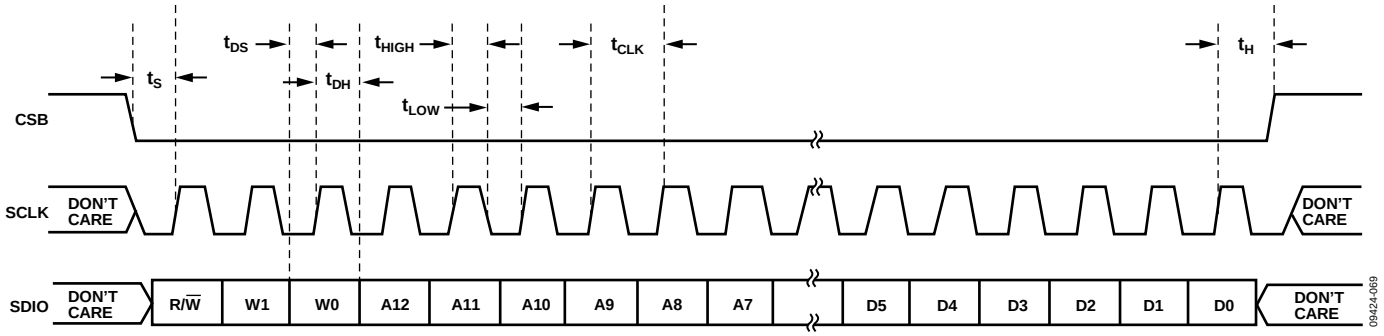

Figure 66. Serial Timing Details

Table 18. Serial Timing Definitions

Parameter	Timing (ns min)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HIGH}	16	Minimum period that SCLK should be in a logic high state
t_{LOW}	16	Minimum period that SCLK should be in a logic low state
t_{EN_SDIO}	10	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 66)
t_{DIS_SDIO}	10	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 66)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration register map (Address 0x00 to Address 0x02), the device index and transfer register map (Address 0x04 to Address 0xFF), and the program register map (Address 0x08 to Address 0x2D).

The leftmost column of the memory map indicates the register address, and the default value is shown in the second rightmost column. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x09, the clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address, followed by 0x01 in Register 0xFF (the transfer bit), the duty cycle stabilizer is turned off. It is important to follow each writing sequence with a transfer bit to update the SPI registers.

All registers except Register 0x00, Register 0x04, Register 0x05, and Register 0xFF are buffered with a master slave latch and require writing to the transfer bit. For more information on this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 19, where an X refers to an undefined feature.

LOGIC LEVELS

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "bit is cleared" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Table 19. AD9278 Memory Map Registers

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
Chip Configuration Registers											
0x00	CHIP_PORT_CONFIG	0	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	Soft reset 1 = on 0 = off (default)	LSB first 1 = on 0 = off (default)	0	0x18	Nibbles should be mirrored so that LSB or MSB first mode is set correctly regardless of shift mode.
0x01	CHIP_ID	Chip ID Bits[7:0] (AD9278 = 0x74), (default)								0x7D	Default is unique chip ID, different for each device. Read-only register.
0x02	CHIP_GRADE	X	X	Speed Mode[5:4] (identify device variants of chip ID) 00: Mode I (40 MSPS) (default) 01: Mode II (25 MSPS) 10: Mode III (50 MSPS) 11: Mode IV (65 MSPS)	X	X	X	X	X	0x0X	Child ID used to differentiate ADC speed power modes.
Device Index and Transfer Registers											
0x04	DEVICE_INDEX_2	X	X	X	X	Data Channel H 1 = on (default) 0 = off	Data Channel G 1 = on (default) 0 = off	Data Channel F 1 = on (default) 0 = off	Data Channel E 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
0x05	DEVICE_INDEX_1	X	X	Clock Channel DCO± 1 = on 0 = off (default)	Clock Channel FCO± 1 = on 0 = off (default)	Data Channel D 1 = on (default) 0 = off	Data Channel C 1 = on (default) 0 = off	Data Channel B 1 = on (default) 0 = off	Data Channel A 1 = on (default) 0 = off	0x0F	Bits are set to determine which on-chip device receives the next write command.
0xFF	DEVICE_UPDATE	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.
Program Function Registers											
0x08	Modes	X	X	X	0	0	Internal power-down mode 000 = chip run (default) 001 = full power-down 010 = standby 011 = reset 100 = CW mode (TGC PDWN)			0x00	Determines generic modes of chip operation (global).
0x09	Clock	X	X	X	X	X	X	X	DCS 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer (DCS) on and off (global).
0x0D	TEST_IO	User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once		Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 13 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = –FS short 0100 = checkerboard output 0101 = PN sequence long 0110 = PN sequence short 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by OUTPUT_MODE)				0x00	When this register is set, the test data is placed on the output pins in place of normal data. (Local, expect for PN sequence.)

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x0E	GPO outputs	X	X	X	X	General-purpose digital outputs				0x00	Values placed on GPO[0:3] pins (global).
0x0F	FLEX_CHANNEL_INPUT	Filter cutoff frequency control 0000 = 1.3 × 1/3 × f_{SAMPLE} 0001 = 1.2 × 1/3 × f_{SAMPLE} 0010 = 1.1 × 1/3 × f_{SAMPLE} 0011 = 1.0 × 1/3 × f_{SAMPLE} (default) 0100 = 0.9 × 1/3 × f_{SAMPLE} 0101 = 0.8 × 1/3 × f_{SAMPLE} 0110 = 0.7 × 1/3 × f_{SAMPLE} 1000 = 1.3 × 1/4.5 × f_{SAMPLE} 1001 = 1.2 × 1/4.5 × f_{SAMPLE} 1010 = 1.1 × 1/4.5 × f_{SAMPLE} 1011 = 1.0 × 1/4.5 × f_{SAMPLE} 1100 = 0.9 × 1/4.5 × f_{SAMPLE} 1101 = 0.8 × 1/4.5 × f_{SAMPLE} 1110 = 0.7 × 1/4.5 × f_{SAMPLE}				X	X	X	X	0x30	Antialiasing filter cutoff (global).
0x10	FLEX_OFFSET	X	X	1	0	0	0	0	0	0x20	Reserved.
0x11	FLEX_GAIN	X	X	X	X	PGA gain 00 = 21 dB 01 = 24 dB (default) 10 = 27 dB 11 = 30 dB		LNA gain 00 = 15.6 dB 01 = 17.9 dB 10 = 21.3 dB (default)		0x06	LNA and PGA gain adjustment (global).
0x12	BIAS_CURRENT	X	X	X	X	1	X	LNA bias 00 = high 01 = mid-high (default) 10 = mid-low 11 = low		0x09	LNA bias current adjustment (global).
0x14	OUTPUT_MODE	X	0 = LVDS ANSI-644 (default) 1 = LVDS low power, (IEEE 1596.3 similar)	X	X	X	Output invert enable 1 = on 0 = off (default)	Data format select 00 = offset binary (default) 01 = twos complement		0x00	Configures the outputs and the format of the data (Bits[7:3] and Bits[1:0] are global; Bit 2 is local).
0x15	OUTPUT_ADJUST	X	X	Output driver termination 00 = none (default) 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		X	X	X	DCO± and FCO± 2× drive strength 1 = on 0 = off (default)	0x00	Determines LVDS or other output properties. Primarily functions to set the LVDS span and common-mode levels in place of an external resistor (Bits[7:1] are global; Bit 0 is local).
0x16	OUTPUT_PHASE	X	X	X	X	Output clock phase adjust 0000 = 0° relative to data edge 0001 = 60° relative to data edge 0010 = 120° relative to data edge 0011 = 180° relative to data edge (default) 0100 = reserved 0101 = 300° relative to data edge 0110 = 360° relative to data edge 0111 = reserved 1000 = 480° relative to data edge 1001 = 540° relative to data edge 1010 = 600° relative to data edge 1011 to 1111 = 660° relative to data edge				0x03	On devices that use global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected. (global)
0x18	FLEX_VREF	X	0 = internal reference 1 = external reference	X	X	X	X	1	1	0x03	Select internal reference (recommended default) or external reference (global).

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Comments
0x19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 1, LSB (global).
0x1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 1, MSB (global).
0x1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-Defined Pattern 2, LSB (global).
0x1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-Defined Pattern 2, MSB (global).
0x21	SERIAL_CONTROL	LSB first 1 = on 0 = off (default)	X	X	X	<10 MSPS, low encode rate mode 1 = on 0 = off (default)	000 = 12 bits (default, normal bit stream) 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 14 bits			0x00	Serial stream control (global).
0x22	SERIAL_CH_STAT	X	X	X	X	X	X	Channel output reset 1 = on 0 = off (default)	Channel power-down 1 = on 0 = off (default)	0x00	Used to power down individual sections of a converter (local).
0x2B	FLEX_FILTER	X	Enable automatic low-pass tuning 1 = on (self-clearing)	X	X	High-pass filter cutoff 0000 = f_{LP}/12.00 0001 = f_{LP}/8.57 0010 = f_{LP}/6.67 0011 = f_{LP}/5.46 0100 = f_{LP}/4.62 0101 = f_{LP}/4.00 0110 = f_{LP}/3.53 0111 = f_{LP}/3.16				0x00	Filter cutoff (global). (f_{LP} = low-pass filter cutoff frequency.)
0x2C	ANALOG_INPUT	X	X	X	X	X	X	LO-x, LOSW-x connection 00 = R_{FB1} 01 = R_{FB1}||$_{RFB2}$ 10 = R_{FB2} 11 = ∞		0x00	LNA active termination/input impedance (global).
0x2D	CW Doppler I/Q demodulator phase	X	X	X	CW Doppler channel enable 1 = on 0 = off	I/Q demodulator phase 0000 = 0° 0001 = 22.5° 0010 = 45° 0011 = 67.5° 0100 = 90° 0101 = 112.5° 0110 = 135° 0111 = 157.5° 1000 = 180° 1001 = 202.5° 1010 = 225° 1011 = 247.5° 1100 = 270° 1101 = 292.5° 1110 = 315° 1111 = 337.5°				0x00	Phase of demodulators (local).

OUTLINE DIMENSIONS

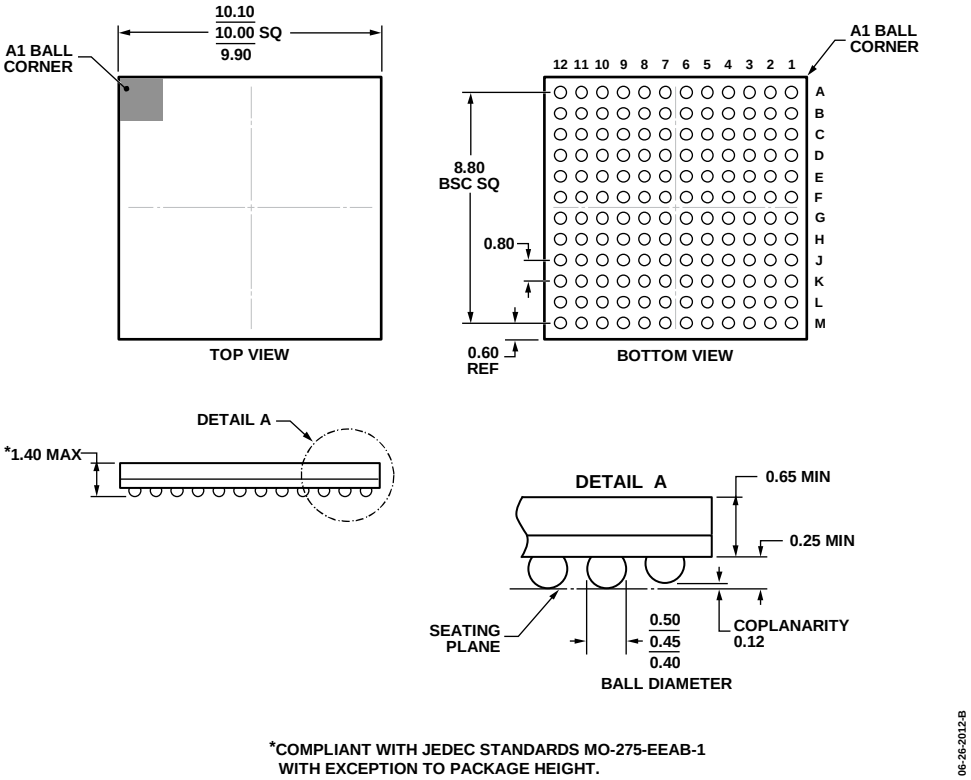

Figure 67. 144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-144-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9278BBCZ	–40°C to +85°C	144-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]	BC-144-1
AD9278-50EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D09424-0-5/12(A)