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Updated Outline Dimensions 13
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Added 14-Lead SOIC_N and 14-Lead TSSOP ..... Universal
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1/2006—Rev. 0 to Rev. A

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9/2005—Revision 0: Initial Version

SPECIFICATIONS

AD8661/AD8662/AD8664 ELECTRICAL CHARACTERISTICS—SOIC, MSOP, AND TSSOP

V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		30	100	µV
AD8661		−40°C < T_A < +85°C			1000	µV
AD8661		−40°C < T_A < +125°C			1400	µV
AD8662		−40°C < T_A < +125°C			1000	µV
AD8664		−40°C < T_A < +125°C			1200	µV
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			−0.1		+3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +3.0 V	85	100		dB
		−40°C < T_A < +125°C	80	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	100	220		V/mV
Offset Voltage Drift	TCV_{OS}					
AD8661		−40°C < T_A < +125°C		3	10	µV/°C
AD8662, AD8664		−40°C < T_A < +125°C		2	9	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.85	4.93		V
		−40°C < T_A < +125°C	4.80			V
Output Voltage Low	V_{OL}	I_L = 1 mA		50	100	mV
		−40°C < T_A < +125°C			110	mV
Short-Circuit Current	I_{SC}			±19		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		50		Ω
POWER SUPPLY						
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		1.15	1.40	mA
		−40°C < T_A < +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_O			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

AD8661/AD8662/AD8664 ELECTRICAL CHARACTERISTICS—SOIC, MSOP, AND TSSOP

V_S = 16.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		50	160	µV
AD8661		−40°C < T_A < +85°C			1000	µV
AD8661		−40°C < T_A < +125°C			1400	µV
AD8662		−40°C < T_A < +125°C			1000	µV
AD8664		−40°C < T_A < +125°C			1200	µV
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			300	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C			20	pA
		−40°C < T_A < +125°C			75	pA
Input Voltage Range			−0.1		+14.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +14.0 V	90	110		dB
		−40°C < T_A < +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 15.5 V	200	360		V/mV
Offset Voltage Drift	TCV_{OS}					
AD8661		−40°C < T_A < +125°C		3	10	µV/°C
AD8662, AD8664		−40°C < T_A < +125°C		2	9	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	15.93	15.97		V
		I_L = 10 mA	15.60	15.70		V
		−40°C < T_A < +125°C	15.50			V
Output Voltage Low	V_{OL}	I_L = 1 mA		24	50	mV
		I_L = 10 mA		190	300	mV
		−40°C < T_A < +125°C			350	mV
Short-Circuit Current	I_{SC}			±140		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 16 V	95	110		dB
		−40°C < T_A < +125°C	95	115		dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		1.25	1.55	mA
		−40°C < T_A < +125°C			2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_O			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

AD8661 ELECTRICAL CHARACTERISTICS—LFCSP ONLY

V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		50	300	µV
		−40°C < T_A < +85°C			2000	µV
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +85°C			50	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C			20	pA
Input Voltage Range			−0.1		+3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +3.0 V	85	100		dB
		−40°C < T_A < +85°C	80	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	100	240		V/mV
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +85°C		4	17	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	4.85	4.93		V
		−40°C < T_A < +85°C	4.80			V
Output Voltage Low	V_{OL}	I_L = 1 mA		50	100	mV
		−40°C < T_A < +85°C			120	mV
Short-Circuit Current	I_{SC}			±19		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		65		Ω
POWER SUPPLY						
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		1.15	1.40	mA
		−40°C < T_A < +85°C			1.8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_O			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

AD8661 ELECTRICAL CHARACTERISTICS—LFCSP ONLY

V_S = 16.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		50	300	µV
		−40°C < T_A < +85°C			2000	µV
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +85°C			50	pA
Input Offset Current	I_{OS}			0.2	0.5	pA
		−40°C < T_A < +85°C			20	pA
Input Voltage Range			−0.1		+14.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +14.0 V	90	110		dB
		−40°C < T_A < +85°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 15.5 V	200	420		V/mV
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +85°C		4	17	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	15.95	15.97		V
		I_L = 10 mA	15.60	15.70		V
		−40°C < T_A < +85°C	15.50			V
Output Voltage Low	V_{OL}	I_L = 1 mA		24	50	mV
		I_L = 10 mA		210	350	mV
		−40°C < T_A < +85°C			400	mV
Short-Circuit Current	I_{SC}			±140		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		45		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 5 V to 16 V	95	110		dB
		−40°C < T_A < +85°C	95	115		dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		1.25	1.55	mA
		−40°C < T_A < +85°C			1.9	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_O			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		2.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	−0.1 V to V_S
Differential Input Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	
R-8, RM-8, R-14, and RU-14	−40°C to +125°C
CP-8-13	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead LFCSP	75[1]	18[1]	°C/W
8-Lead MSOP	142	44	°C/W
14-Lead SOIC	88.2	56.3	°C/W
14-Lead TSSOP	114	23.3	°C/W

[1] Exposed pad soldered to application board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

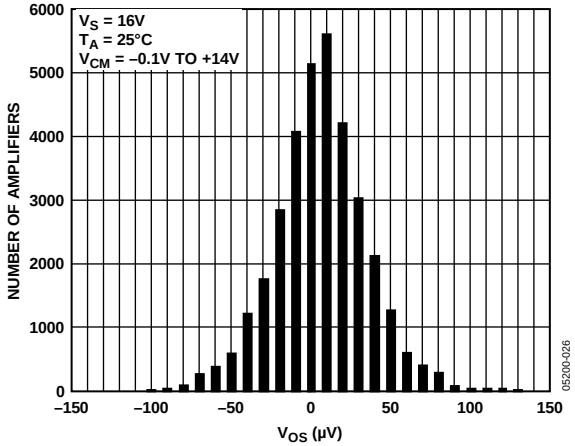


Figure 7. Input Offset Voltage Distribution

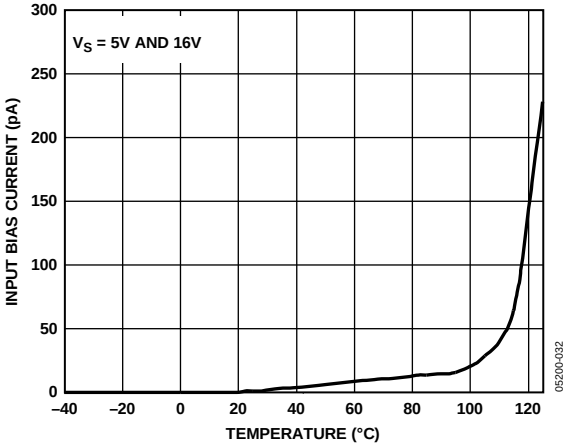


Figure 10. Input Bias Current vs. Temperature

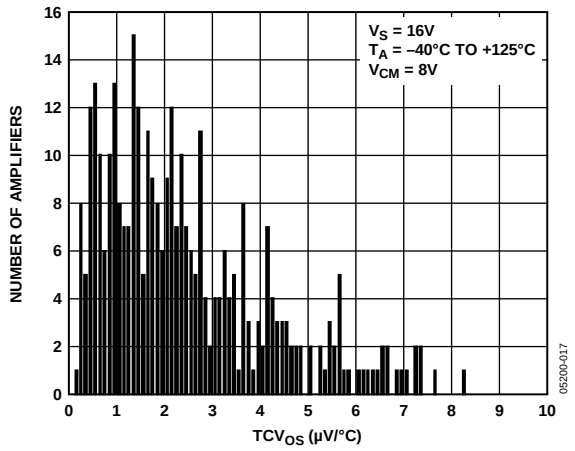


Figure 8. Offset Voltage Drift Distribution

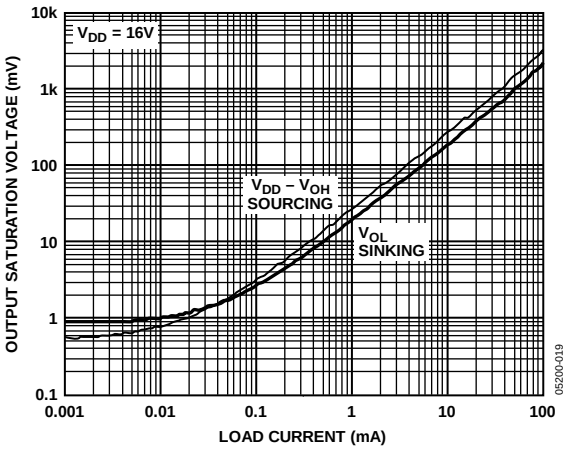


Figure 11. Output Swing Saturation Voltage vs. Load Current

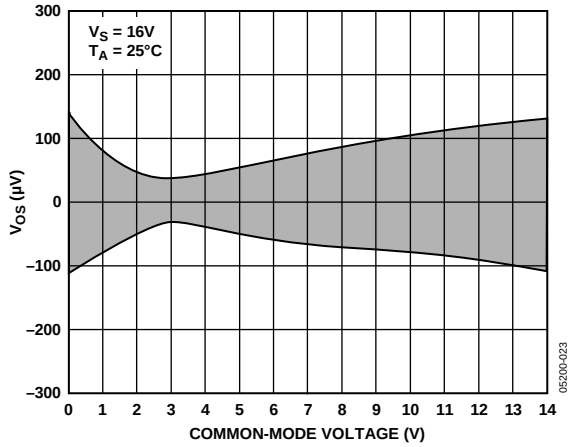


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

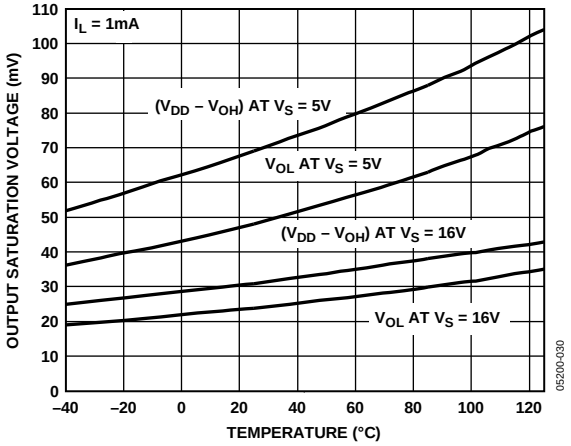


Figure 12. Output Swing Saturation Voltage vs. Temperature, I_L = 1 mA

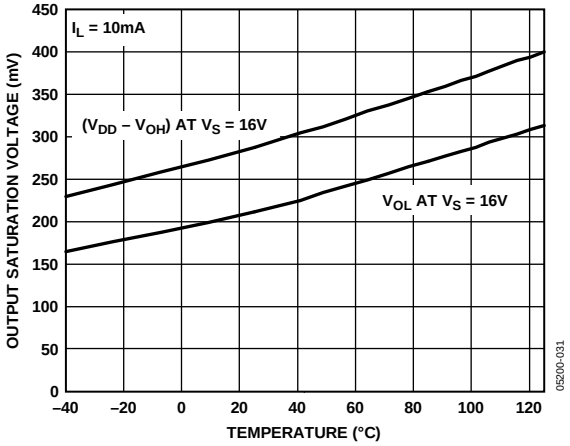


Figure 13. Output Swing Saturation Voltage vs. Temperature, I_L = 10 mA

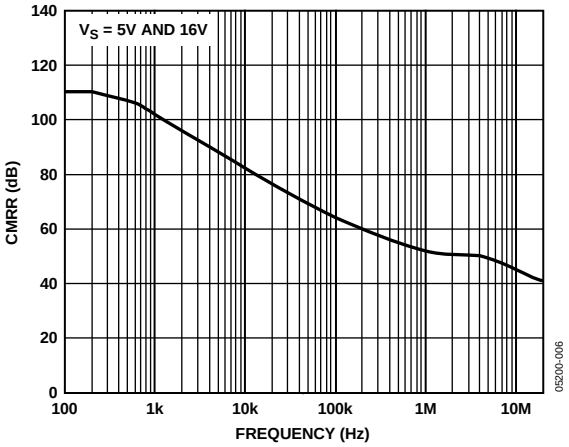


Figure 16. CMRR vs. Frequency

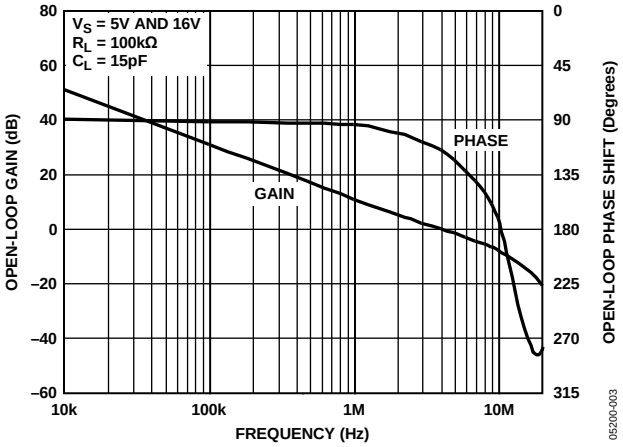


Figure 14. Open-Loop Gain and Phase Shift vs. Frequency

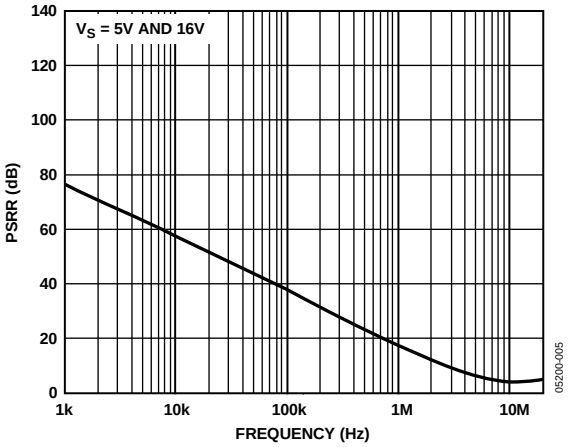


Figure 17. PSRR vs. Frequency

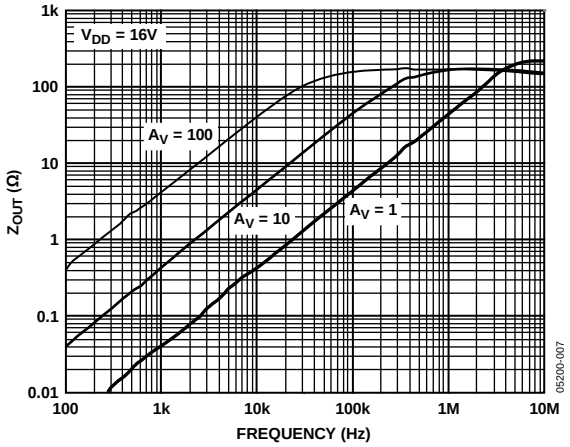


Figure 15. Closed-Loop Output Impedance vs. Frequency

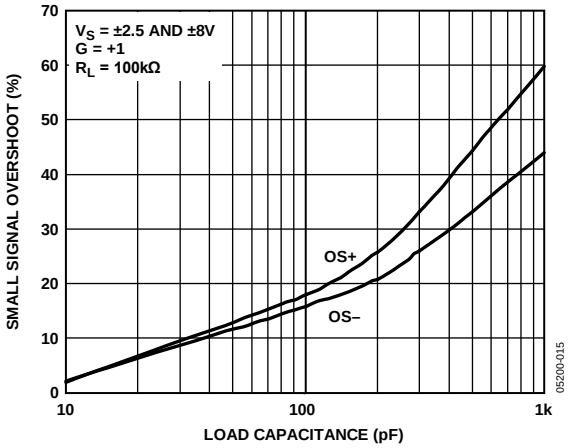


Figure 18. Small Signal Overshoot vs. Load Capacitance

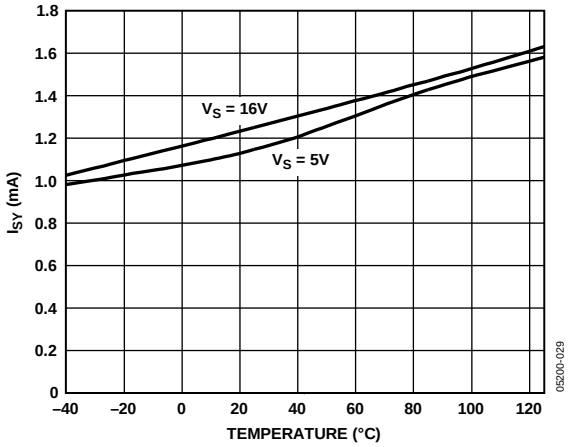


Figure 19. Supply Current vs. Temperature

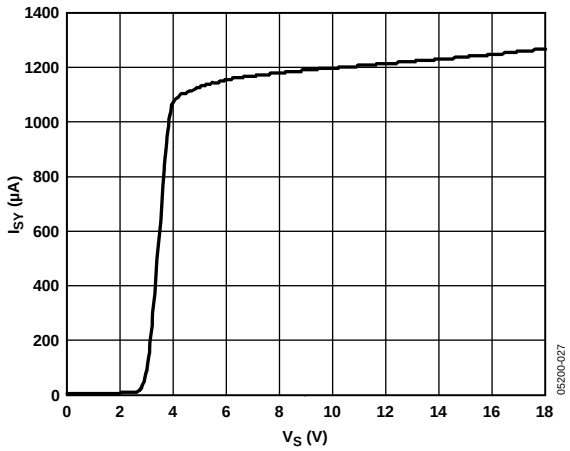


Figure 20. Supply Current vs. Supply Voltage (Dual-Supply Configuration), T_A = 25°C

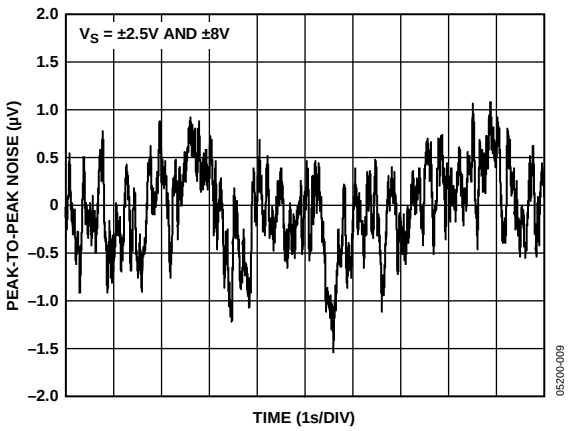


Figure 21. 0.1 Hz to 10 Hz Input Voltage Noise

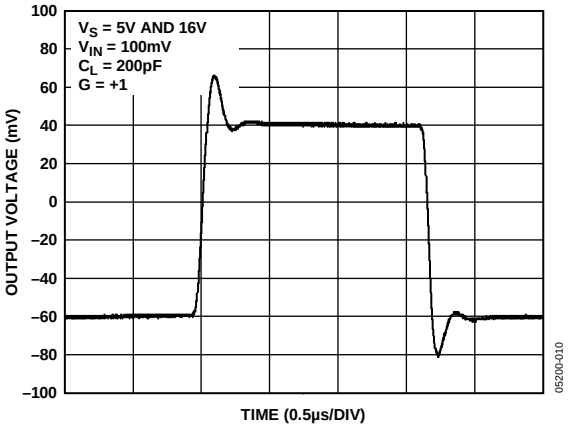


Figure 22. Small Signal Transient Response

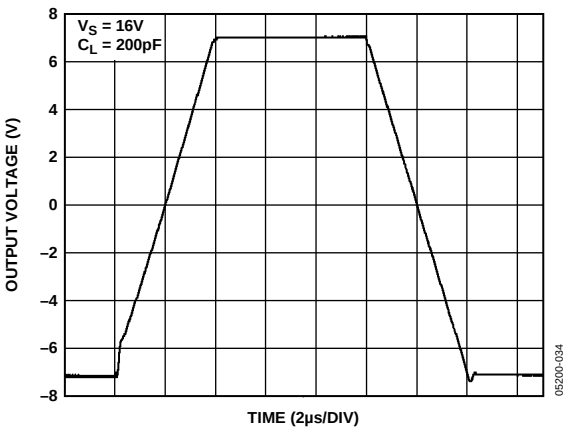


Figure 23. Large Signal Transient Response

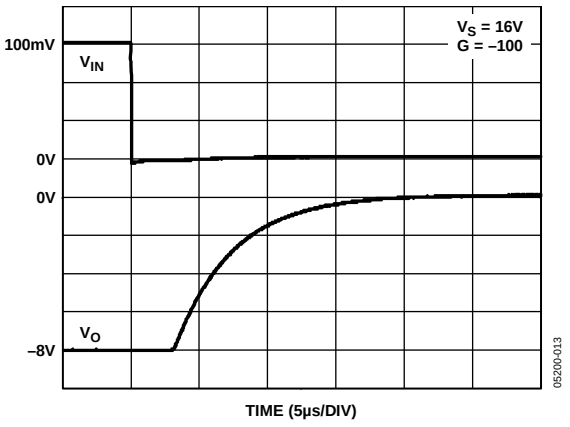


Figure 24. Positive Overload Recovery

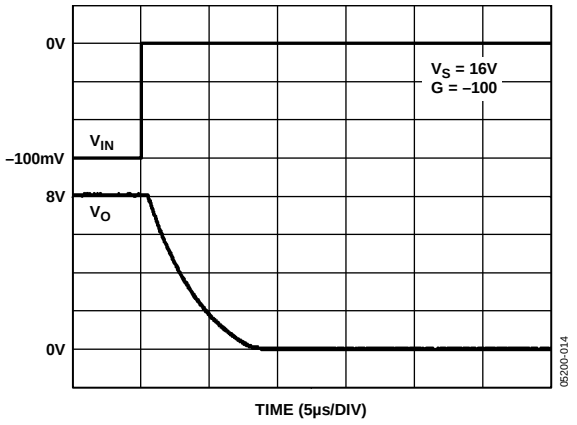


Figure 25. Negative Overload Recovery

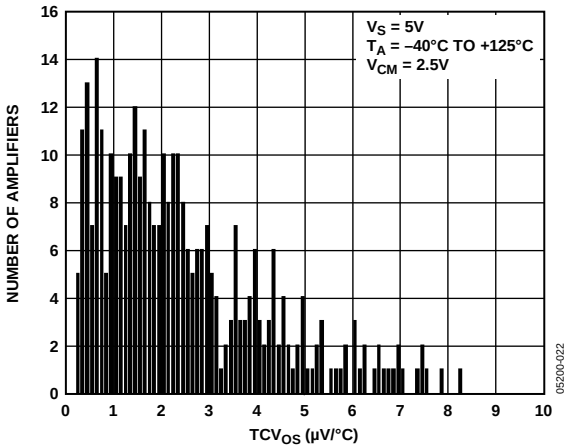


Figure 28. Offset Voltage Drift Distribution

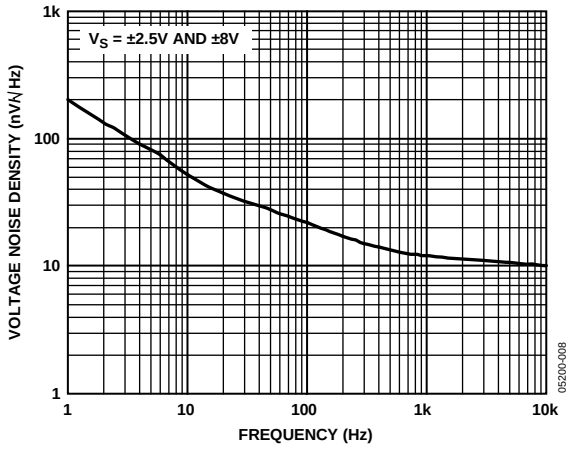


Figure 26. Voltage Noise Density vs. Frequency

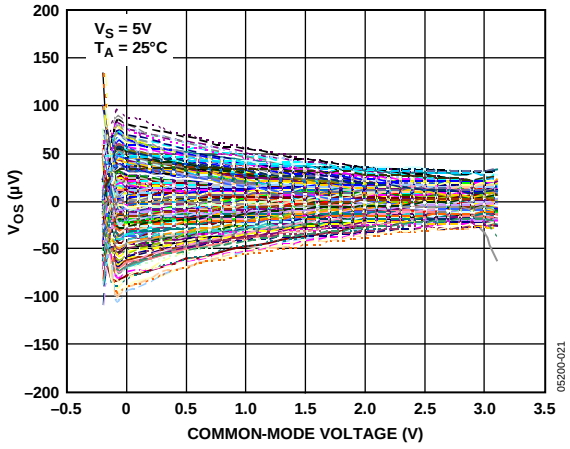


Figure 29. Input Offset Voltage vs. Common-Mode Voltage

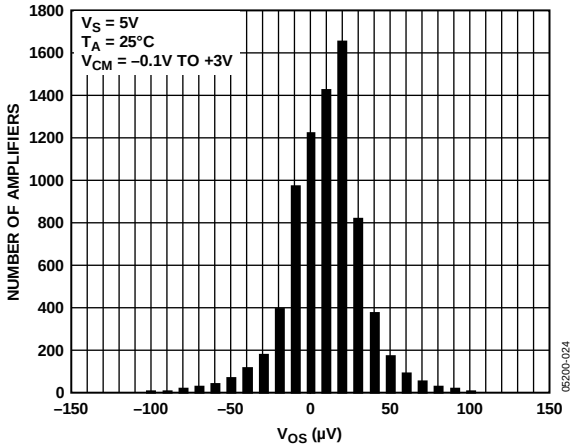


Figure 27. Input Offset Voltage Distribution

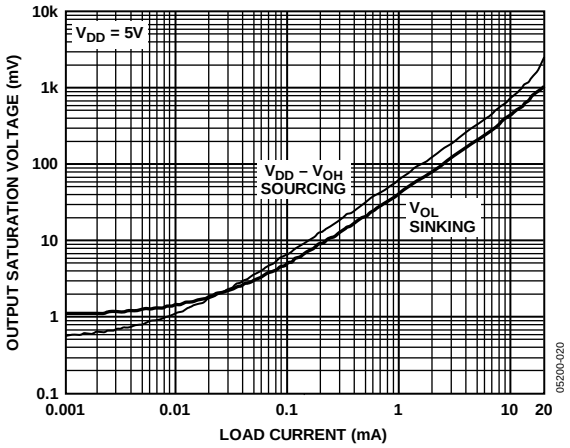


Figure 30. Output Swing Saturation Voltage vs. Load Current

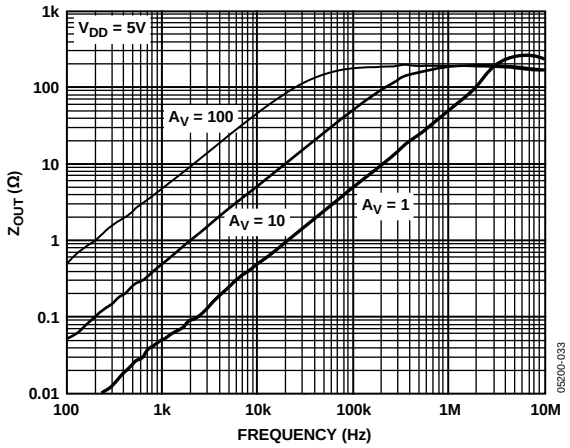


Figure 31. Closed-Loop Output Impedance vs. Frequency

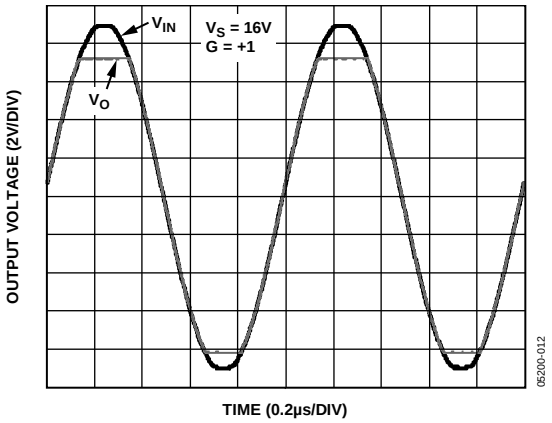


Figure 33. No Phase Reversal

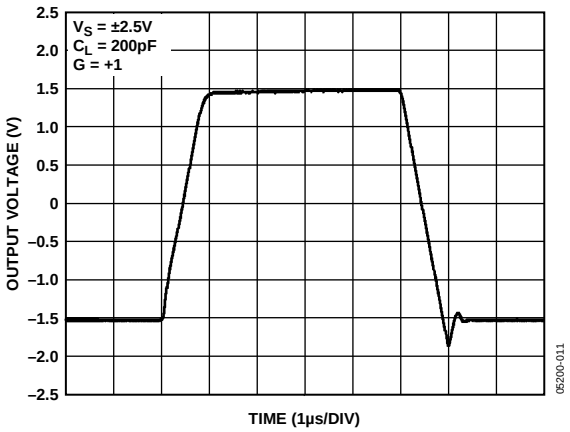


Figure 32. Large Signal Transient Response

OUTLINE DIMENSIONS

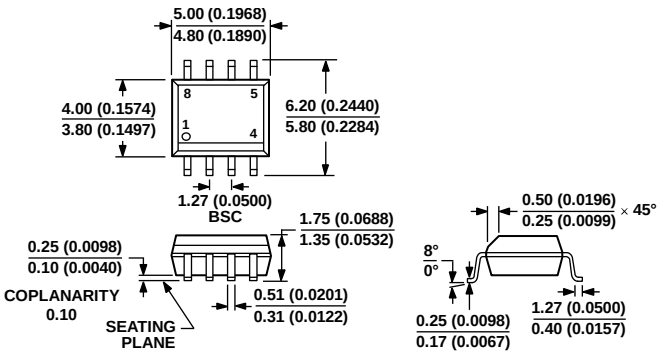


Figure 34. 8-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

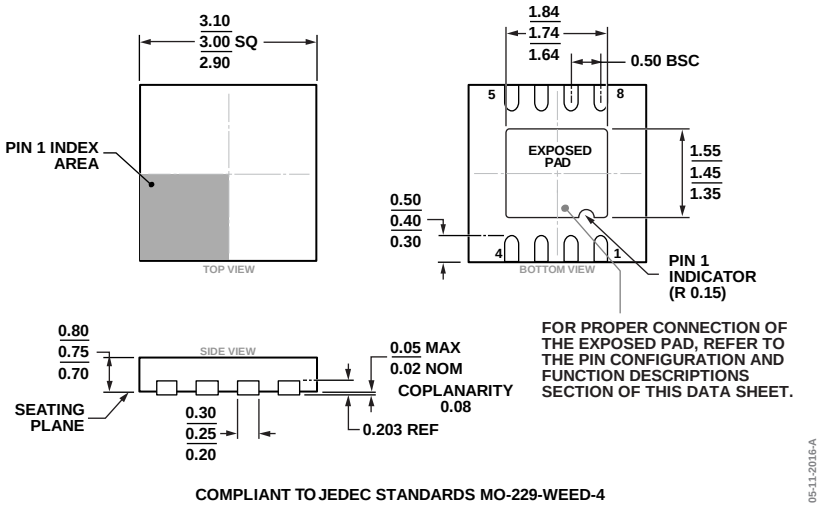
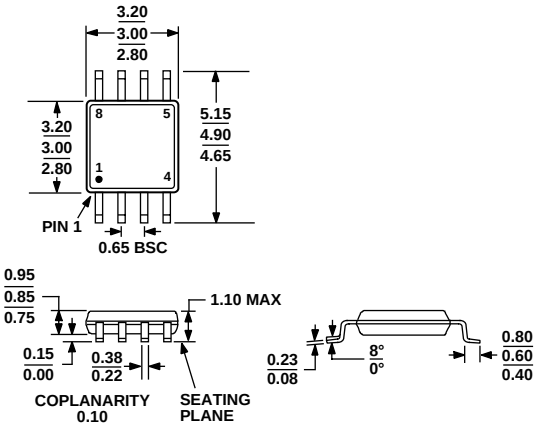
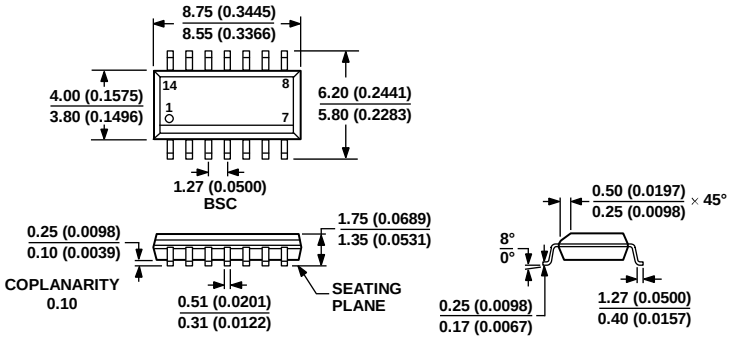


Figure 35. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

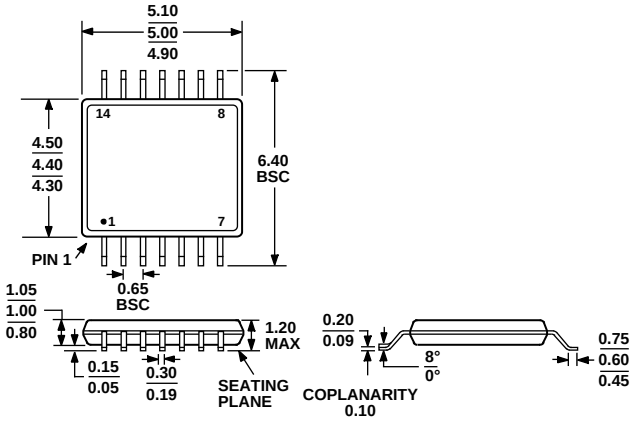
Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 37. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8661ARZ	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8661ARZ-REEL	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8661ARZ-REEL7	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8661ACPZ-R2	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A0M
AD8661ACPZ-REEL7	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	A0M
AD8662ARZ	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8662ARZ-REEL	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8662ARZ-REEL7	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8	
AD8662ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A10
AD8662ARMZ-REEL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A10
AD8664ARZ	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8664ARZ-REEL	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8664ARZ-REEL7	−40°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14	
AD8664ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
AD8664ARUZ-REEL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	

[1] Z = RoHS Compliant Part.

NOTES

D05200-0-7/16(E)