TABLE OF CONTENTS

Features ... 1
Applications ... 1
Connection Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 5
Thermal Resistance ... 5
Maximum Power Dissipation ... 5
ESD Caution ... 5
Pin Configurations and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Test Circuits ... 14
Theory of Operation ... 15
General Design Considerations ... 15
Achieving Very Flat Gain Response at High Frequency ... 15
Choice of Feedback Resistor ... 15
Printed Circuit Board Layout ... 15
Quality of Coaxial Cable ... 15
Power Supply Bypassing ... 15
Power Supply Operating Range ... 15
Offset Nulling ... 16
Disable Mode ... 16
Applications Information ... 17
Capacitive Loads ... 17
Operation As a Video Line Driver ... 18
2:1 Video Multiplexer ... 19
4:1 Multiplexer ... 20
Outline Dimensions ... 21
Ordering Guide ... 22

REVISION HISTORY

5/2019—Rev. A to Rev. B

Updated Format ... Universal
Changed V_O to V_{OUT} and AD810S to 5962-9313201MPA ... Throughout
Deleted Closed-Loop Gain and Phase vs. Frequency Plot and Differential Gain and Phase vs. Supply Voltage Plot ... 1
Changes to General Description Section ... 1
Changes to Table 1 ... 3
Deleted Figure 2; Renumbered Sequentially ... 4
Changes to Table 2, Maximum Power Dissipation Section ... 5
Added Thermal Resistance Section and Table 3; Renumbered Sequentially ... 5
Added Pin Configurations and Function Descriptions Section, Figure 3, Figure 4, Figure 5, and Table 4; Renumbered Sequentially ... 6
Changes to Figure 6 Caption and Figure 7 Caption ... 7
Changes to Figure 14 Caption and Figure 16 ... 8
Changes to Figure 19 ... 9
Added Test Circuits Section ... 14
Moved Figure 45 and Figure 46 ... 14
Changed Choice of Feedback and Gain Resistor Section to Choice of Feedback Resistor Section ... 15
Changes to Achieving Very Flat Gain Response at High Frequency Section, Choice of Feedback Resistor Section, and Power Supply Bypassing Section ... 15
Moved Figure 45 ... 16
Changes to Disable Mode Section ... 16
Added Applications Information Section ... 17
Moved Capacitive Loads Section and Figure 48 to Figure 51 ... 17
Changes to Figure 48 and Figure 50 ... 17
Moved Operation As a Video Line Driver Section and Figure 52 to Figure 56 ... 18
Change to Figure 54 ... 18
Moved 2:1 Video Multiplexer Section and Figure 57 to Figure 60 ... 19
Changes to Figure 58 ... 19
Moved 4:1 Multiplexer Section and Figure 61 to Figure 63 ... 20
Changes to 4:1 Multiplexer Section ... 20
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 22

10/1992—Rev. 0 to Rev. A

SPECIFICATIONS

T_A = 25°C, supply voltage (V_S) = ±15 V dc, load resistance (R_L) = 150 Ω, unless otherwise noted.

Table 1.

		AD810A			5962-9313201MPA[1]			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	G = +2, feedback resistor (R_F) = 715 Ω, V_S = ±5 V	40	50		40	50		MHz
	G = +2, R_F = 715 Ω, V_S = ±15 V	55	75		55	75		MHz
	G = +1, R_F = 1000 Ω, V_S = ±15 V	40	80		40	80		MHz
	G = +10, R_F = 270 Ω, V_S = ±15 V	50	65		50	65		MHz
0.1 dB Bandwidth	G = +2, R_F = 715 Ω, V_S = ±5 V	13	22		13	22		MHz
	G = +2, R_F = 715 Ω, V_S = ±15 V	15	30		15	30		MHz
Full Power Bandwidth	Output voltage (V_{OUT}) = 20 V p-p							
	R_L = 400 Ω		16		8	16		MHz
Slew Rate[2]	R_L = 150 Ω, V_S = ±5 V		350		175	350		V/µs
	R_L = 400 Ω, V_S = ±15 V		1000		500	1000		V/µs
Settling Time to 0.1%	10 V step, G = −1		50			50		ns
Settling Time to 0.01%	10 V step, G = −1		125			125		ns
Differential Gain	f = 3.58 MHz, V_S = ±15 V		0.02	0.05		0.02	0.05	%
	f = 3.58 MHz, V_S = ±5 V		0.04	0.07		0.04	0.07	%
Differential Phase	f = 3.58 MHz, V_S = ±15 V		0.04	0.07		0.04	0.07	Degrees
	f = 3.58 MHz, V_S = ±5 V		0.045	0.08		0.045	0.08	Degrees
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 2 V p-p							
	R_L = 400 Ω, G = +2		−61			−61		dBc
INPUT OFFSET VOLTAGE	V_S = ±5 V and ±15 V		1.5	6		1.5	6	mV
	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		2	7.5		4	15	mV
Offset Voltage Drift			7			15		µV/°C
INPUT BIAS CURRENT								
Negative Input	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		0.7	5		0.8	5	µA
Positive Input	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		2	7.5		2	10	µA
OPEN-LOOP TRANSRESISTANCE	T_{MIN} to T_{MAX}							
	V_{OUT} = ±10 V, R_L = 400 Ω, V_S = ±15 V	1.0	3.5		1.0	3.5		MΩ
	V_{OUT} = ±2.5 V, R_L = 100 Ω, V_S = ±5 V	0.3	1.2		0.2	1.0		MΩ
OPEN-LOOP DC VOLTAGE GAIN	T_{MIN} to T_{MAX}							
	V_{OUT} = ±10 V, R_L = 400 Ω, V_S = ±15 V	86	100		80	100		dB
	V_{OUT} = ±2.5 V, R_L = 100 Ω, V_S = ±5 V	76	88		72	88		dB
COMMON-MODE REJECTION	T_{MIN} to T_{MAX}							
Offset Voltage (V_{OS})	Common-mode voltage (V_{CM}) = ±12 V, V_S = ±15 V	56	64		56	64		dB
	V_{CM} = ±2.5 V, V_S = ±5 V	52	60		50	60		dB
Input Bias Current	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		0.1	0.4	−0.4	0.1	+0.4	µA/V
POWER SUPPLY REJECTION								
V_{OS}	T_{MIN} to T_{MAX}, V_S = ±4.5 V to ±18 V	65	72		60	72		dB
Input Bias Current	T_{MIN} to T_{MAX}		0.05	0.3	−0.3	0.05	+0.3	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz, V_S = ±5 V and ±15 V		2.9			2.9		nV/√Hz
INPUT CURRENT NOISE	Negative input current ($-I_{IN}$), f = 1 kHz, V_S = ±5 V and ±15 V		13			13		pA/√Hz
	Positive input current ($+I_{IN}$), f = 1 kHz, V_S = ±5 V and ±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE	V_S = ±5 V	±2.5	±3.0		±2.5	±3		V
	V_S = ±15 V	±12	±13		±12	±13		V

Parameter	Test Conditions/Comments	AD810A Min	AD810A Typ	AD810A Max	5962-9313201MPA[1] Min	5962-9313201MPA[1] Typ	5962-9313201MPA[1] Max	Unit
OUTPUT CHARACTERISTICS								
Output Voltage Swing[3]	R_L = 150 Ω, T_{MIN} to T_{MAX}, V_S = ±5 V	±2.5	±2.9		±2.5	±2.9		V
	R_L = 400 Ω, V_S = ±15 V	±12.5	±12.9		±12.5	±12.9		V
	R_L = 400 Ω, T_{MIN} to T_{MAX}, V_S = ±15 V	±12			±12			V
Short-Circuit Current			150			150		mA
Output Current	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V	40	60		30	60		mA
OUTPUT RESISTANCE	Open loop (5 MHz)		15			15		Ω
INPUT CHARACTERISTICS								
Input Resistance	Positive input	2.5	10		2.5	10		MΩ
	Negative input		40			40		Ω
Input Capacitance	Positive input		2			2		pF
DISABLE CHARACTERISTICS[4]								
Off Isolation	f = 5 MHz, see Figure 59		64			64		dB
Off Output Resistance	See Figure 15, R_G is gain resistor		(R_F + R_G)||13 pF			(R_F + R_G)||13 pF		Ω
Turn On Time[5]	Output impedance (Z_{OUT}) = low, see Figure 59		170			170		ns
Turn Off Time	Z_{OUT} = high		100			100		ns
$\overline{\text{DISABLE}}$ Pin Current	$\overline{\text{DISABLE}}$ pin = 0 V, V_S = ±5 V		50	75		50	75	µA
	$\overline{\text{DISABLE}}$ pin = 0 V, V_S = ±15 V		290	400		290	400	µA
Minimum $\overline{\text{DISABLE}}$ Pin Current to Disable	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		30		10	30	40	µA
POWER SUPPLY								
Operating Range	25°C to T_{MAX}	±2.5		±18	±2.5		±18	V
	T_{MIN}	±3.0		±18	±3.5		±18	V
Quiescent Current	V_S = ±5 V		6.7	7.5		6.7	7.5	mA
	V_S = ±15 V		6.8	8.0		6.8	8.0	mA
	T_{MIN} to T_{MAX}, V_S = ±5 V and ±15 V		8.3	10.0		9	11.0	mA
Power-Down Current	V_S = ±5 V		1.8	2.3		1.8	2.3	mA
	V_S = ±15 V		2.1	2.8		2.1	2.8	mA
TEMPERATURE								
Operating Range (T_{MIN} to T_{MAX})		−40		+85	−55		+125	°C

[1] See the Analog Devices military data sheet for 883B specifications.
[2] Slew rate measurement is based on 10% to 90% rise time with the amplifier configured for a gain of −10.
[3] Voltage swing is defined as useful operating range, not the saturation range.
[4] Disable guaranteed break before make.
[5] Turn on time is defined with ±5 V supplies using complementary output CMOS to drive the disable pin.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	See Figure 2
Output Short-Circuit Duration[1]	See Figure 2
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±6 V
Storage Temperature Range	
PDIP	−65°C to +125°C
CERDIP	−65°C to +150°C
SOIC_N	−65°C to +125°C
Operating Temperature Range	
AD810A	−40°C to +85°C
5962-9313201MPA	−55°C to +125°C
Junction Temperature	
AD810A	145°C
5962-9313201MPA	175°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Internal short-circuit protection may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one-cubic foot sealed enclosure.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
N-8	90	°C/W
Q-8	110	°C/W
R-8	150	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD810 is limited by the associated rise in junction temperature. To ensure proper operation, it is important to observe the derating curves in Figure 2.

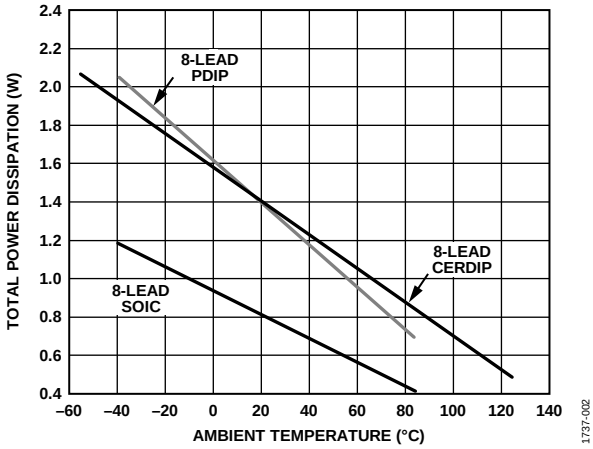


Figure 2. Total Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

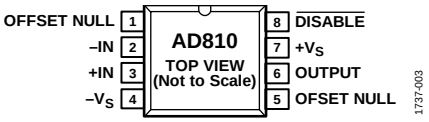


Figure 3. 8-Lead PDIP Pin Configuration

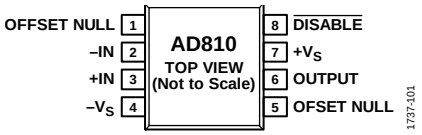


Figure 5. 8-Lead SOIC Pin Configuration

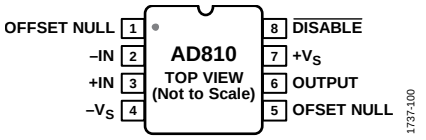


Figure 4. 8-Lead CERDIP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5	OFFSET NULL	Inverting Input Offset Null Connection. See Figure 47.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply Voltage.
6	OUTPUT	Output.
7	$+V_S$	Positive Supply Voltage.
8	$\overline{\text{DISABLE}}$	Disable (Active Low).

TYPICAL PERFORMANCE CHARACTERISTICS

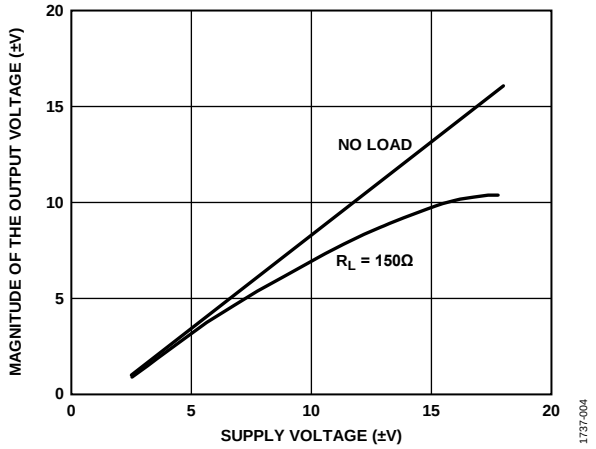


Figure 6. Magnitude of the Output Voltage vs. Supply Voltage

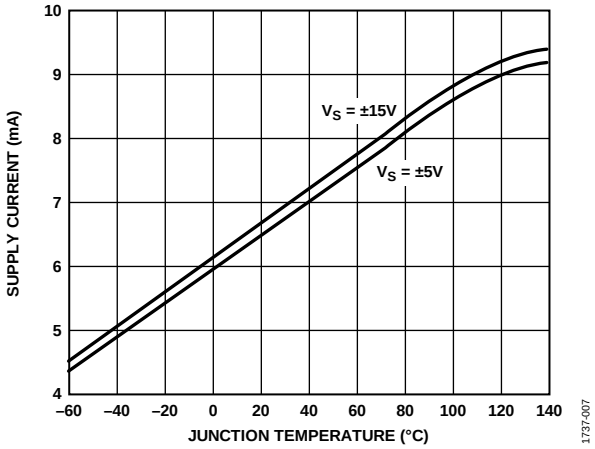


Figure 9. Supply Current vs. Junction Temperature

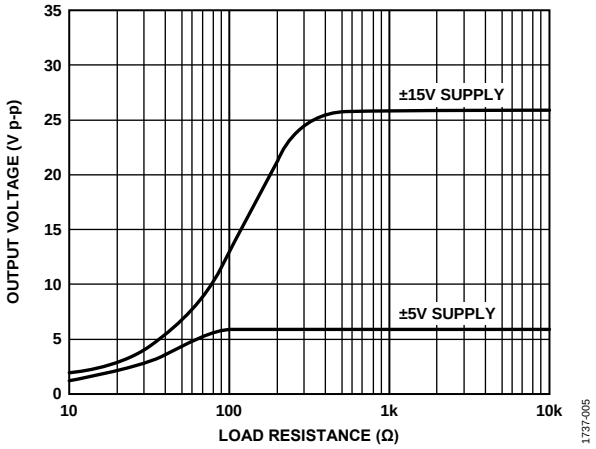


Figure 7. Output Voltage vs. Load Resistance

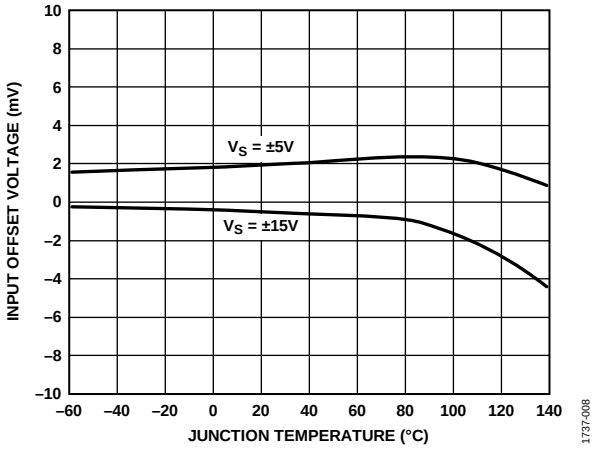


Figure 10. Input Offset Voltage vs. Junction Temperature

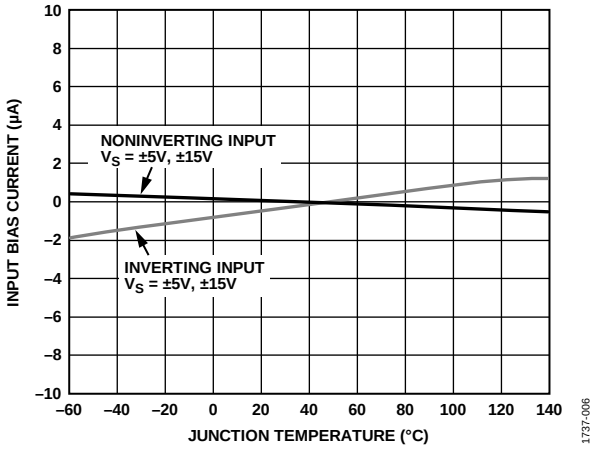


Figure 8. Input Bias Current vs. Junction Temperature

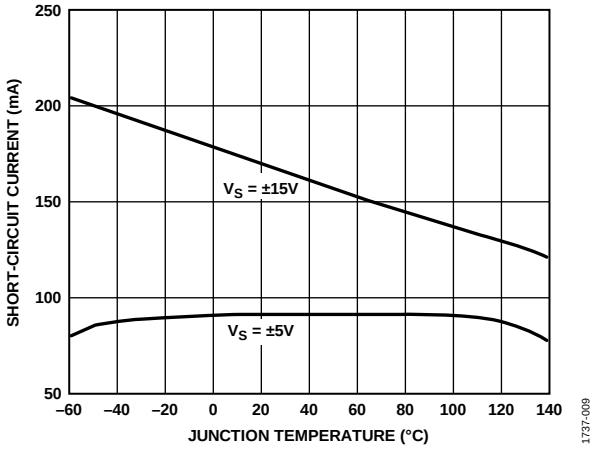


Figure 11. Short-Circuit Current vs. Junction Temperature

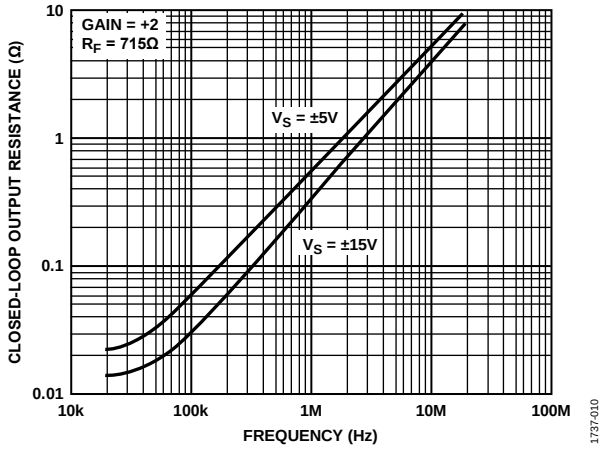


Figure 12. Closed-Loop Output Resistance vs. Frequency

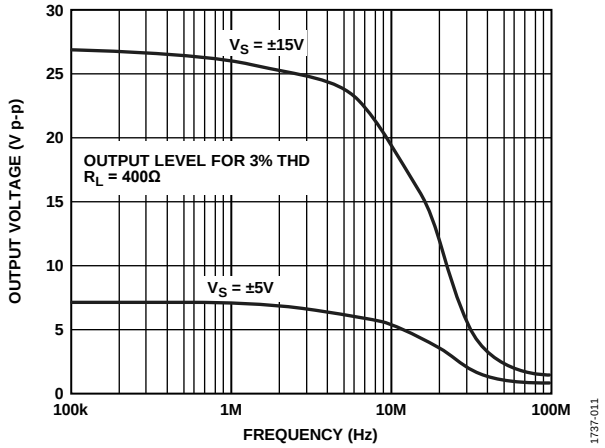


Figure 13. Large Signal Frequency Response

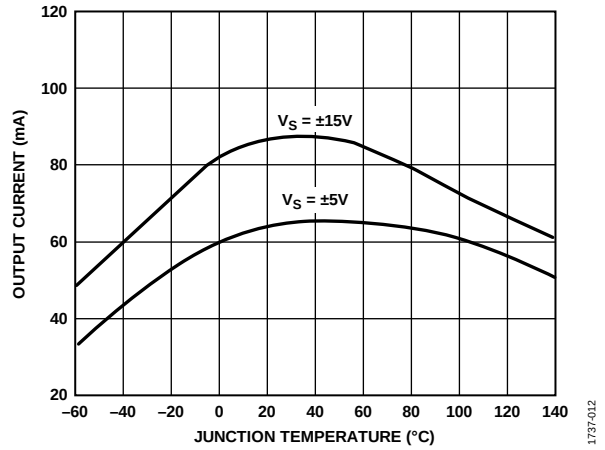


Figure 14. Output Current vs. Junction Temperature

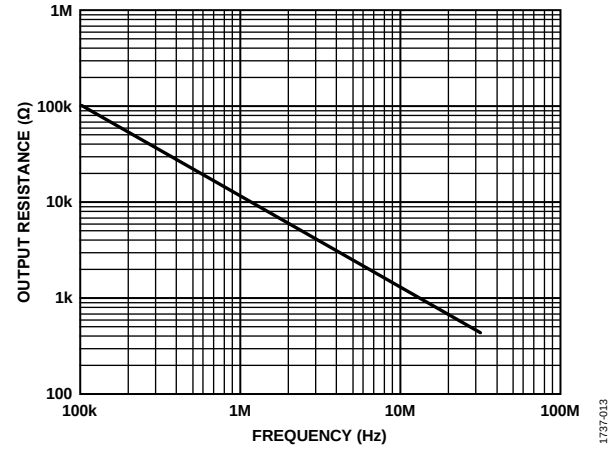


Figure 15. Output Resistance vs. Frequency, Disabled State

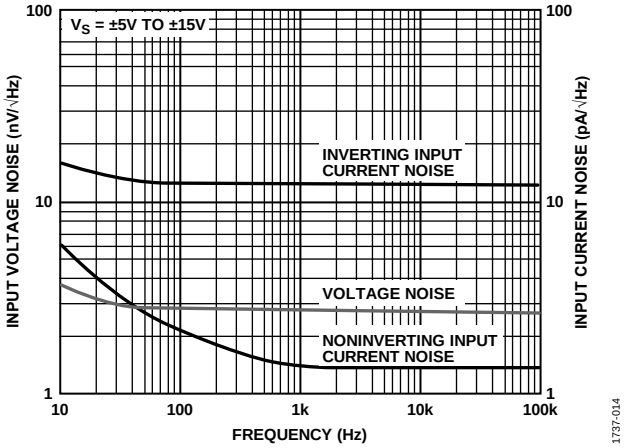


Figure 16. Input Voltage Noise and Input Current Noise vs. Frequency

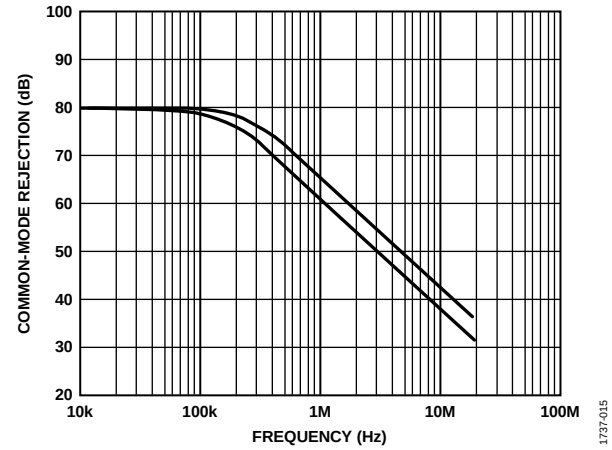


Figure 17. Common-Mode Rejection vs. Frequency

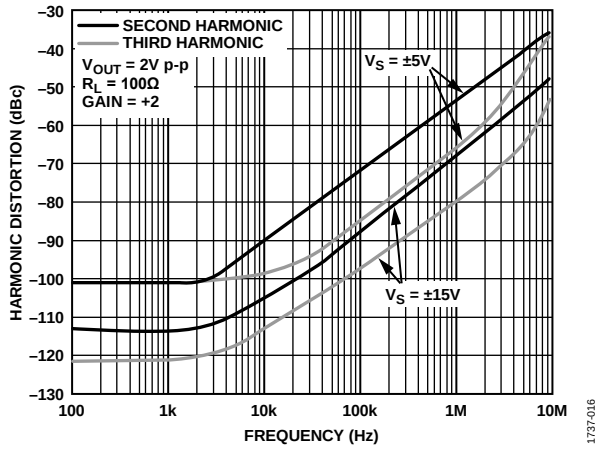


Figure 18. Harmonic Distortion vs. Frequency (R_L = 100 Ω)

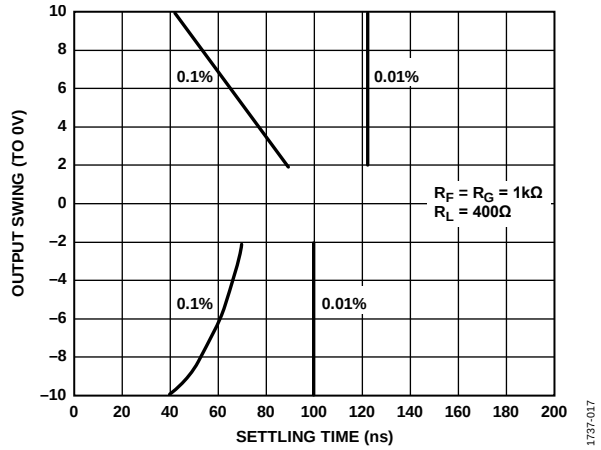


Figure 19. Output Swing (to 0 V) vs. Settling Time at Various Error Levels

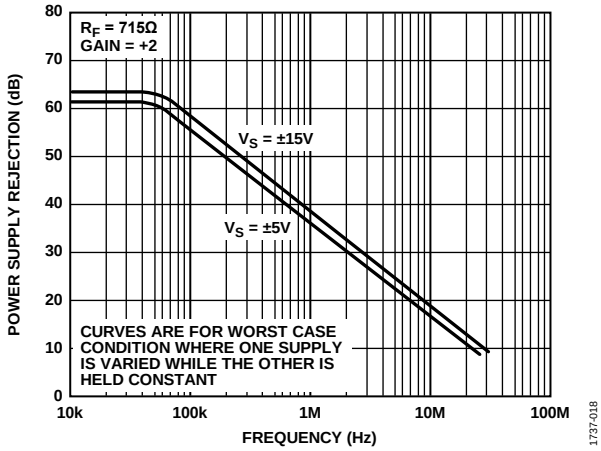


Figure 20. Power Supply Rejection vs. Frequency

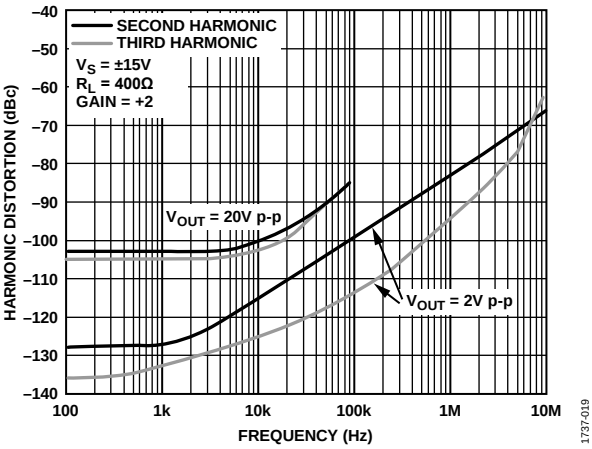


Figure 21. Harmonic Distortion vs. Frequency (R_L = 400 Ω)

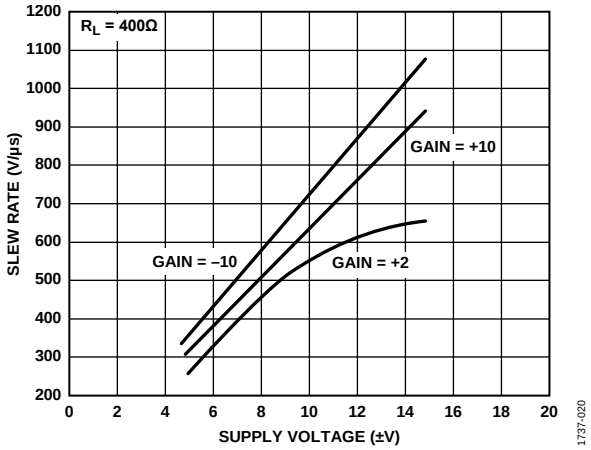


Figure 22. Slew Rate vs. Supply Voltage

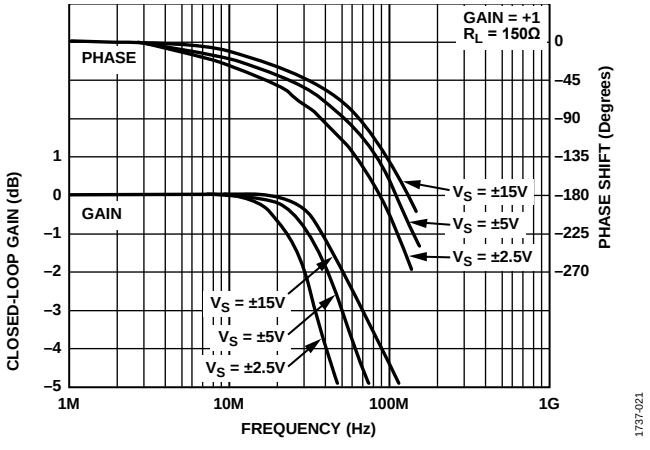


Figure 23. Closed-Loop Gain and Phase Shift vs. Frequency, G= +1, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V and ±2.5 V

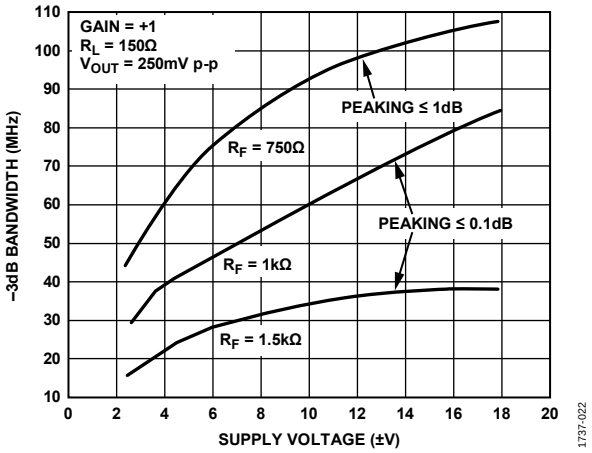


Figure 24. –3 dB Bandwidth vs. Supply Voltage, Gain = +1, R_L = 150 Ω

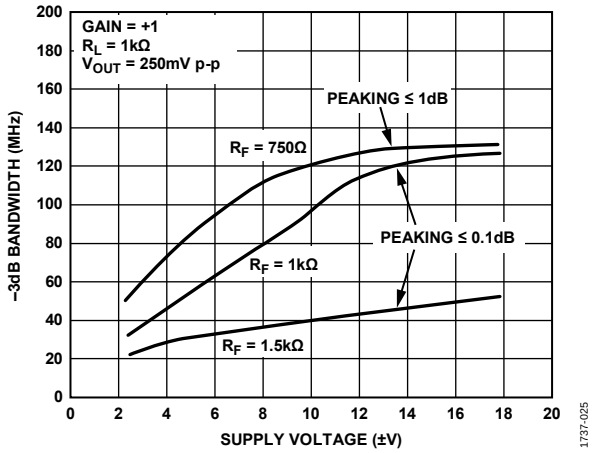


Figure 27. –3 dB Bandwidth vs. Supply Voltage, G = +1, R_L = 1 kΩ

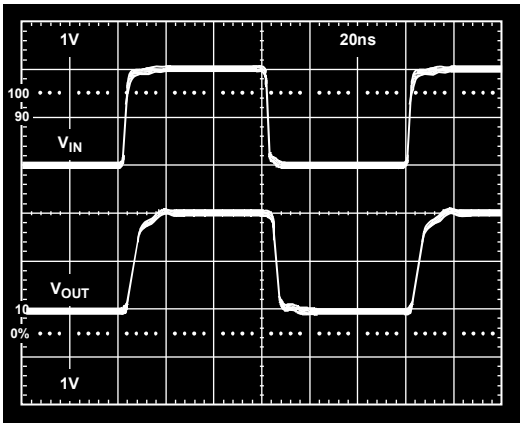


Figure 25. Small Signal Pulse Response, Gain = +1, R_F = 1 kΩ, R_L = 150 Ω, V_S = ±15 V

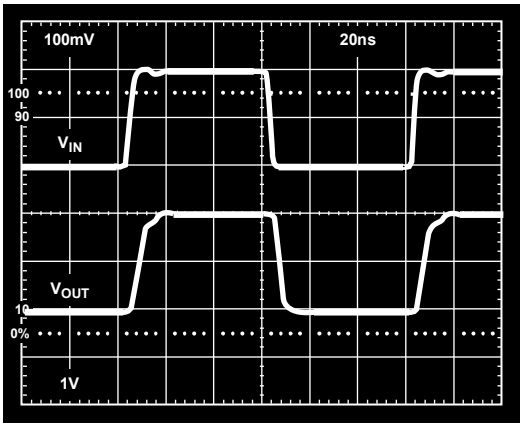


Figure 28. Small Signal Pulse Response, Gain = +10, R_F = 442 Ω, R_L = 150 Ω, V_S = ±15 V

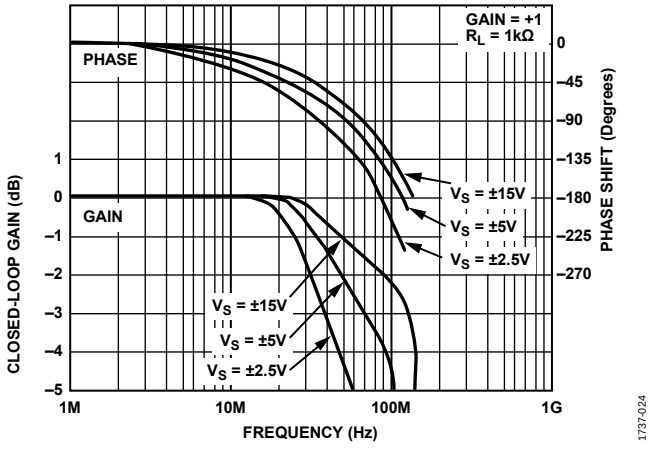


Figure 26. Closed-Loop Gain and Phase Shift vs. Frequency, G= +1, R_F = 1 kΩ for ±15 V, 910 Ω for ±5 V and ±2.5 V

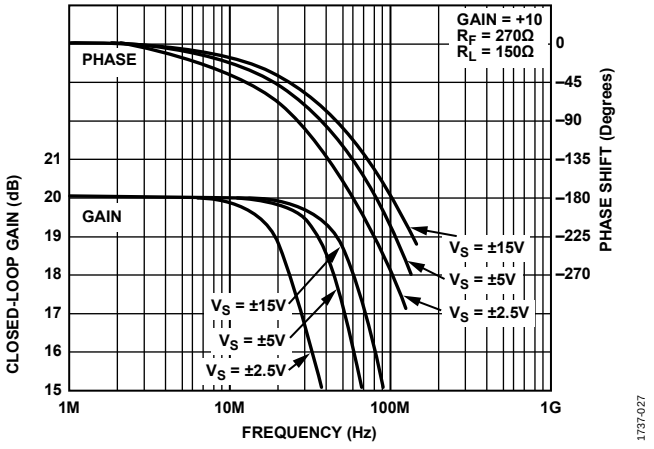


Figure 29. Closed-Loop Gain and Phase Shift vs. Frequency, G = +10, R_L = 150 Ω

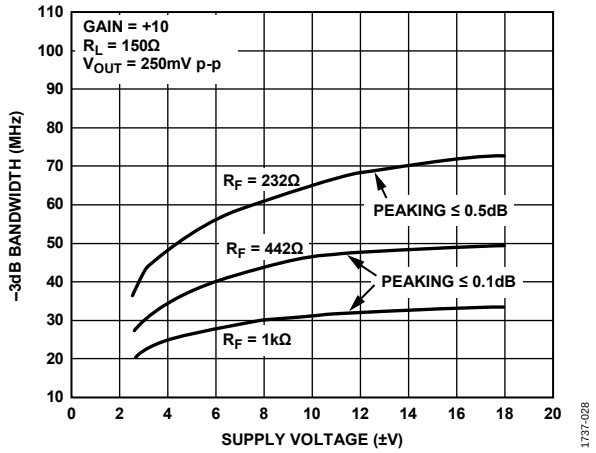


Figure 30. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 150 Ω

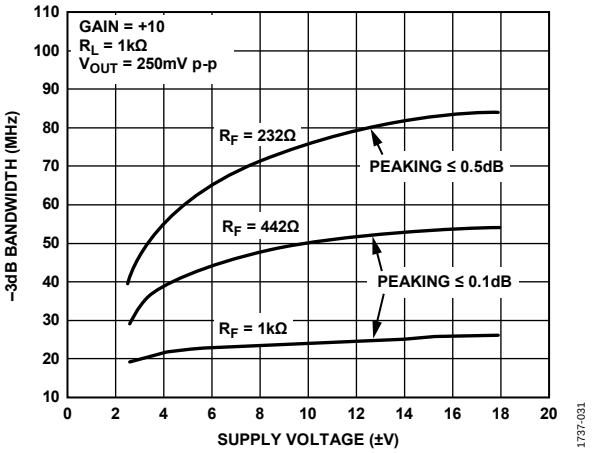


Figure 33. –3 dB Bandwidth vs. Supply Voltage, Gain = +10, R_L = 1 kΩ

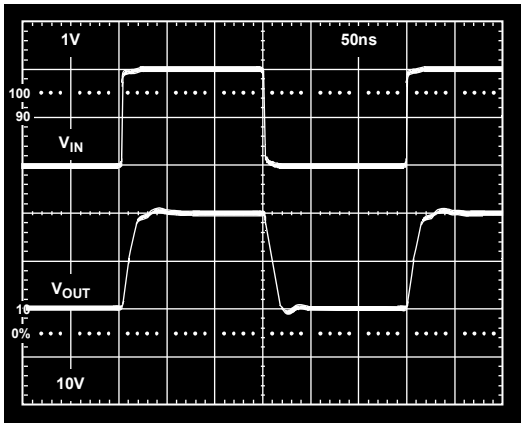


Figure 31. Large Signal Pulse Response, Gain = +10, R_F = 442 Ω, R_L = 400 Ω, V_S = ±15 V

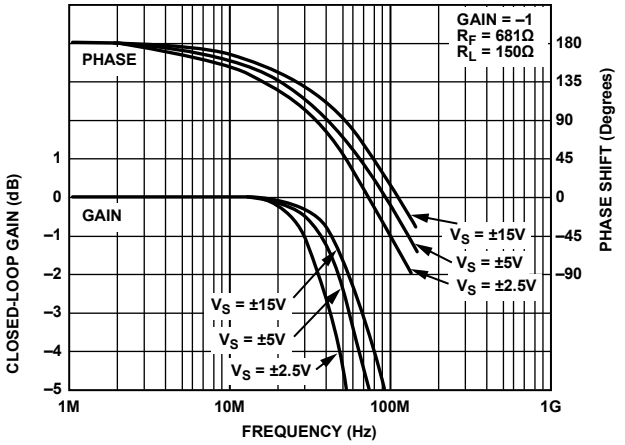


Figure 34. Closed-Loop Gain and Phase Shift vs. Frequency G = –1, R_L = 150 Ω, R_F = 681 Ω for ±15 V, 620 Ω for ±5 V and ±2.5 V

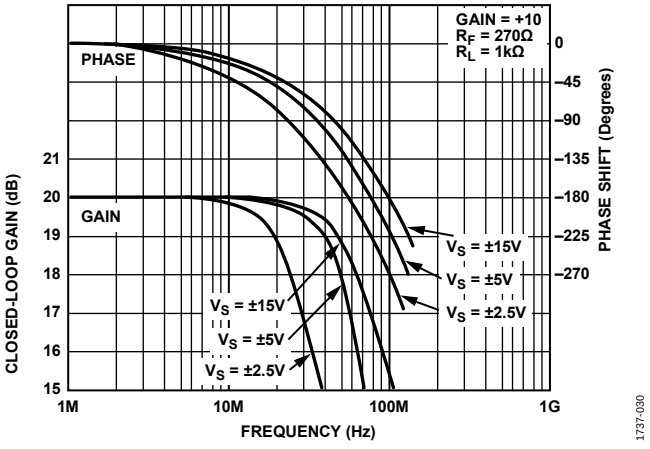


Figure 32. Closed-Loop Gain and Phase Shift vs. Frequency, G = +10, R_L = 1 kΩ

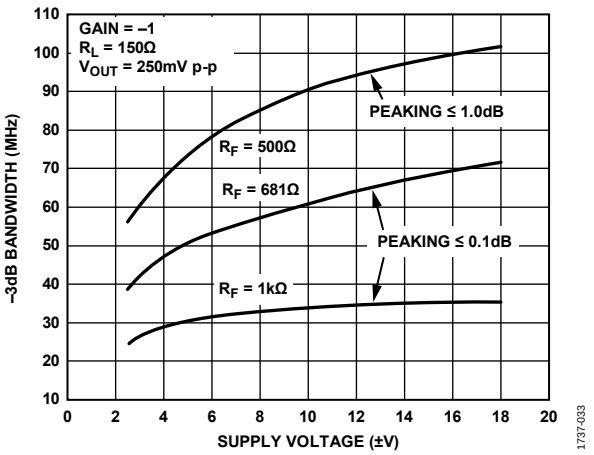


Figure 35. –3 dB Bandwidth vs. Supply Voltage, Gain = –1, R_L = 150 Ω

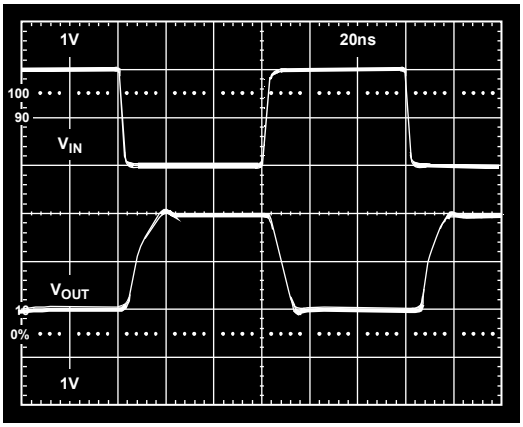


Figure 36. Small Signal Pulse Response, Gain = −1, R_F = 681 Ω, R_L = 150 Ω, V_S = ±5 V

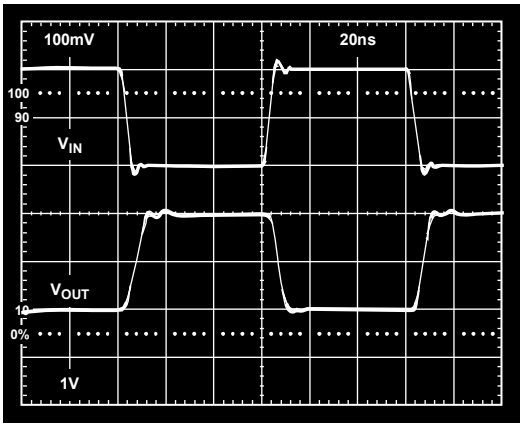


Figure 39. Small Signal Pulse Response, Gain = −10, R_F = 442 Ω, R_L = 150 Ω, V_S = ±15 V

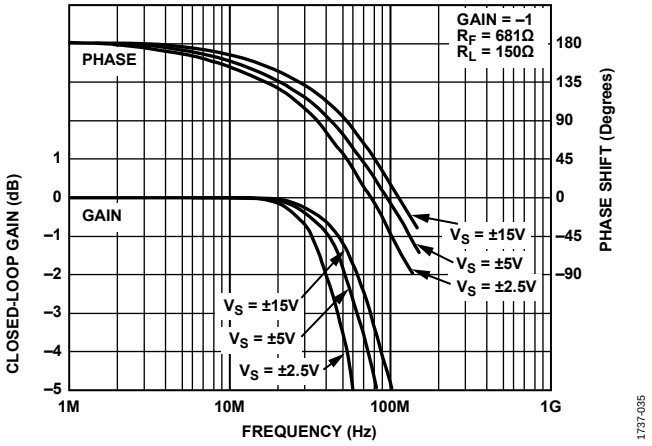


Figure 37. Closed-Loop Gain and Phase Shift vs. Frequency, G = −1, R_L = 1 kΩ, R_F = 681 Ω for V_S = ±15 V, 620 Ω for ±5 V and ±2.5 V

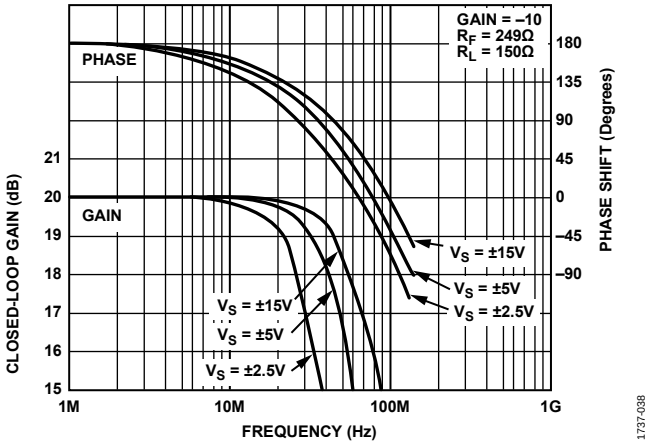


Figure 40. Closed-Loop Gain and Phase Shift vs. Frequency, G = −10, R_L = 150 Ω

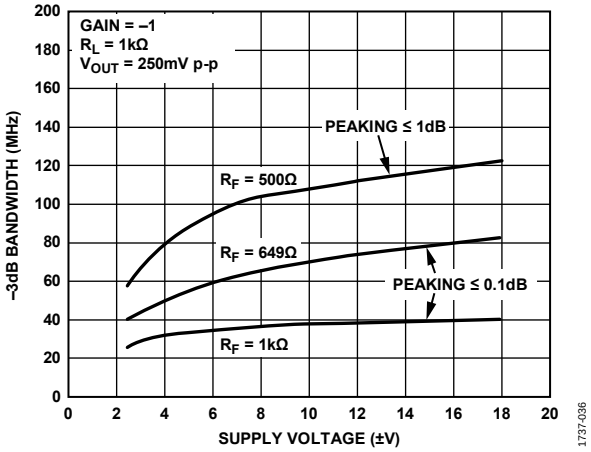


Figure 38. −3 dB Bandwidth vs. Supply Voltage, Gain = −1, R_L = 1 kΩ

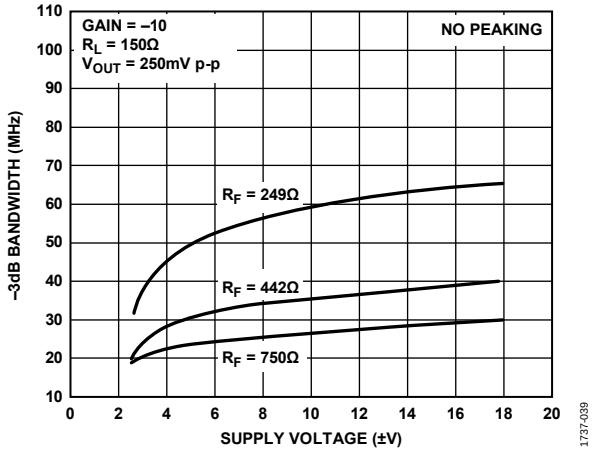


Figure 41. −3 dB Bandwidth vs. Supply Voltage, G = −10, R_L = 150 Ω

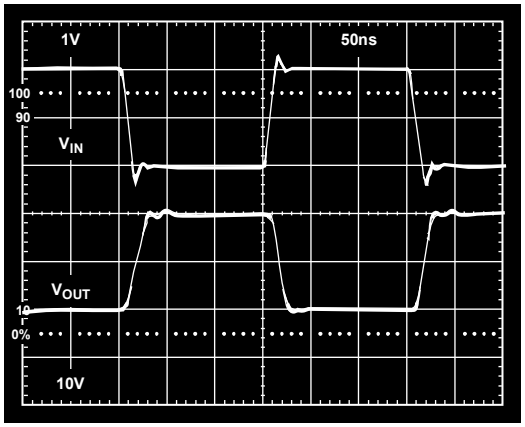


Figure 42. Large Signal Pulse Response, Gain = −10, R_F = 442 Ω, R_L = 400 Ω, V_S = ±15 V

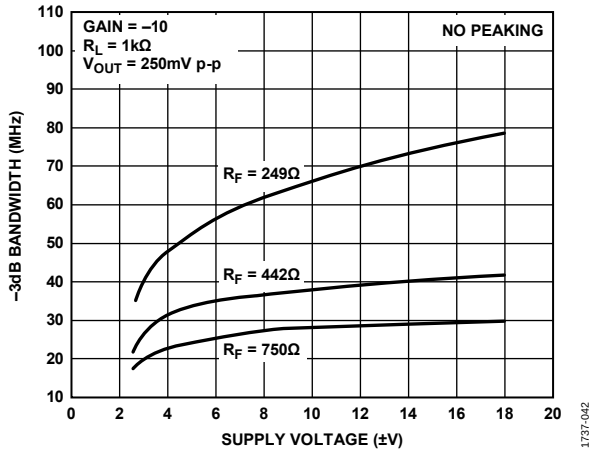


Figure 44. −3 dB Bandwidth vs. Supply Voltage, G = −10, R_L = 1 kΩ

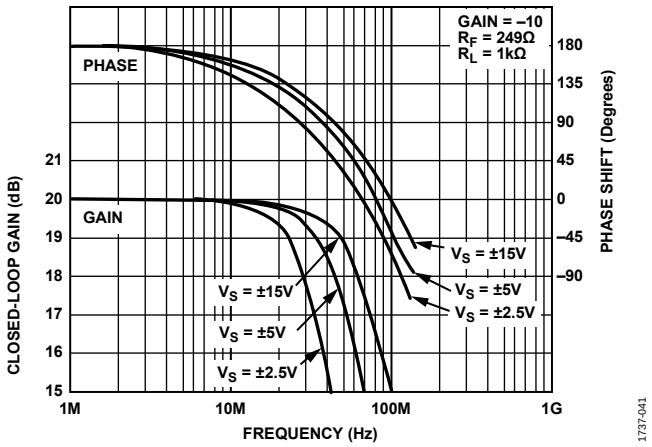


Figure 43. Closed-Loop Gain and Phase Shift vs. Frequency, G = −10, R_L = 1 kΩ

TEST CIRCUITS

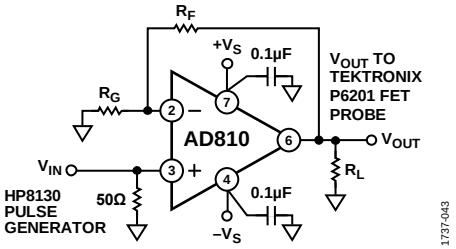


Figure 45. Noninverting Amplifier Connection

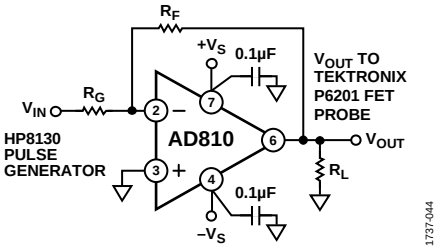


Figure 46. Inverting Amplifier Connection

THEORY OF OPERATION

GENERAL DESIGN CONSIDERATIONS

The AD810 is a current feedback amplifier optimized for use in high performance video and data acquisition systems. Because the AD810 uses a current feedback architecture, its closed-loop bandwidth depends on the value of the feedback resistor. Table 5 and Table 6 list recommended resistor values for some useful closed-loop gains and supply voltages. As shown in Table 5 and Table 6, the closed-loop bandwidth is not a strong function of gain, as it is for a voltage feedback amplifier. The recommended resistor values results in maximum bandwidths with less than 0.1 dB of peaking in the gain vs. frequency response.

The −3 dB bandwidth is also somewhat dependent on the power supply voltage. Lowering the supplies increases the values of internal capacitances, reducing the bandwidth. To compensate for this reduction, smaller values of feedback resistor are sometimes used at lower supply voltages. The characteristic curves in Figure 23 and Figure 24 illustrate that bandwidths of over 100 MHz on 30 V total supplies and over 50 MHz on 5 V total supplies can be achieved.

Table 5. −3 dB Bandwidth vs. Closed-Loop Gain and Resistance Values (R_L = 150 Ω), V_S = ±15 V

Closed-Loop Gain	R_F	R_G	−3 dB Bandwidth (MHz)
+1	1 kΩ	Open	80
+2	715 Ω	715 Ω	75
+10	270 Ω	30 Ω	65
−1	681 Ω	681 Ω	70
−10	249 Ω	24.9 Ω	65

Table 6. −3 dB Bandwidth vs. Closed-Loop Gain and Resistance Values (R_L = 150 Ω), V_S = ±5 V

Closed-Loop Gain	R_F	R_G	−3 dB Bandwidth (MHz)
+1	910 Ω	Open	50
+2	715 Ω	715 Ω	50
+10	270 Ω	30 Ω	50
−1	620 Ω	620 Ω	55
−10	249 Ω	24.9 Ω	50

ACHIEVING VERY FLAT GAIN RESPONSE AT HIGH FREQUENCY

Achieving and maintaining gain flatness of less than 0.1 dB above 10 MHz is not difficult if the recommended resistor values are used. Additionally, consider feedback resistor selection, PCB layout, coaxial cable quality, power supply bypassing and operating range, and offset nulling to ensure consistently optimal results.

CHOICE OF FEEDBACK RESISTOR

Because the 3 dB bandwidth depends on the feedback resistor, the fine scale flatness varies to some extent with feedback resistor tolerance. It is recommended that resistors with a 1% tolerance be used to maintain exceptional flatness through high volume production.

PRINTED CIRCUIT BOARD LAYOUT

As with all wideband amplifiers, PCB parasitics can affect the overall closed-loop performance. Most important are stray capacitances at the output and inverting input nodes. (An added capacitance of 2 pF between the inverting input and ground adds about 0.2 dB of peaking in the gain of 2 response, and increase the bandwidth to 105 MHz). Leave space (3/16 inches is sufficient) around the signal lines to minimize coupling. Also, keep signal lines connecting the feedback and gain resistors short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than ¼ inches are recommended.

QUALITY OF COAXIAL CABLE

Optimum flatness when driving a coaxial cable is possible only when the driven cable is terminated at each end with a resistor matching its characteristic impedance. With an ideal coaxial cable, the resulting flatness is not affected by the length of the cable. Although outstanding results can be achieved using inexpensive cables, some variation in flatness due to varying cable lengths is to be expected.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can contribute to resonant circuits that produce peaking in the amplifier response. Although the recommended 0.1 µF power supply bypass capacitors are sufficient in most applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases. In addition, if large current transients must be delivered to the load, bypass capacitors (typically greater than 1 µF) are required to optimize settling time and lowest distortion.

POWER SUPPLY OPERATING RANGE

The AD810 operates with supplies from ±18 V down to about ±2.5 V. On ±2.5 V supplies, the low distortion output voltage swing is greater than 1 V p-p. Single-supply operation can be achieved by biasing the input common-mode voltage at the supply midpoint.

OFFSET NULLING

A 10 kΩ potentiometer connected between Pin 1 and Pin 5, with its wiper connected to $+V_S$ can be used to trim out the inverting input current (with about ±20 μA of range). For closed-loop gains above about 5, this configuration may not be sufficient to trim the output offset voltage to zero. Tie the potentiometer wiper to ground through a large value resistor (50 kΩ for ±5 V supplies, 150 kΩ for ±15 V supplies) to trim the output to zero at high closed-loop gains.

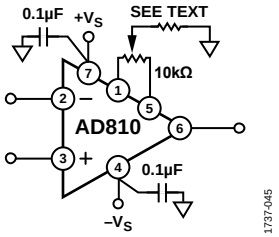


Figure 47. Offset Null Configuration

DISABLE MODE

By pulling the voltage on Pin 8 to ground (0 V), the AD810 can be put into a disabled state. In this condition, the supply current drops to less than 2.8 mA, the output becomes high impedance, and there is a high level of isolation from input to output. In the case of a line driver, for example, the output impedance is about the same as for a 1.5 kΩ resistor (the feedback plus gain resistors) in parallel with a 13 pF capacitor (due to the output) and the input to output isolation is greater than 65 dB at 1 MHz.

Leaving the disable pin disconnected (floating) keeps the AD810 operational in the enabled state.

The input impedance of the disable pin is about 35 kΩ in parallel with a few pF. When grounded, about 50 μA flows out of the $\overline{\text{DISABLE}}$ pin for ±5 V supplies. If driven by complementary output CMOS logic, the disable time (until the output goes high impedance) is about 100 ns and the enable time (to low impedance output) is about 170 ns on ±5 V supplies. The enable time can be extended to about 750 ns by using open-drain logic.

When operated on ±15 V supplies, the AD810 disable pin can be driven by open-drain logic. In this case, adding a 10 kΩ pull-up resistor from the $\overline{\text{DISABLE}}$ pin to the positive supply decreases the enable time to about 150 ns. If there is a nonzero voltage present on the amplifier output at the time the device is switched to the disabled state, some additional decay time is required for the output voltage to decrease to zero. The total time for the output to go to zero is generally about 250 ns and is somewhat dependent on the load impedance.

In cases where the amplifier is driving a high impedance load, the input to output isolation decreases significantly if the input signal is greater than about 1.2 V p-p. The isolation can be restored back to the 65 dB level by adding an extra load (for example, 150 Ω) at the amplifier output. This additional load attenuates the feedthrough signal. (This decreased isolation is not an issue for multiplexer applications where the outputs of multiple AD810 devices are tied together as long as at least one channel is in the on state.)

APPLICATIONS INFORMATION

CAPACITIVE LOADS

When used with the appropriate feedback resistor, the AD810 can drive capacitive loads exceeding 1000 pF directly without oscillation. By using the curves in Figure 50 to choose the resistor value, less than 1 dB of peaking can easily be achieved without sacrificing much bandwidth. Note that the curves in Figure 50 were generated for the case of a 10 kΩ load resistor. For smaller load resistances, the peaking is less than indicated by Figure 50.

Another method of compensating for large load capacitances is to insert a resistor in series (R_S) with the loop output, as shown in Figure 48. In most cases, less than 50 Ω is all that is needed to achieve an extremely flat gain response.

Figure 49 to Figure 51 illustrate the outstanding performance that can be achieved when driving a 1000 pF capacitor.

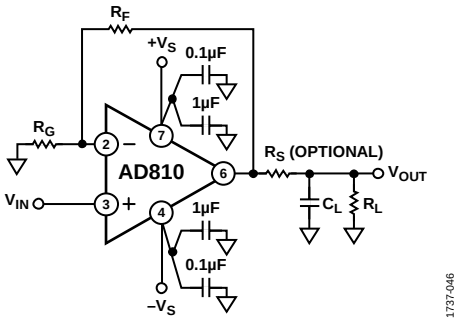


Figure 48. Circuit Options for Driving a Large Capacitive Load

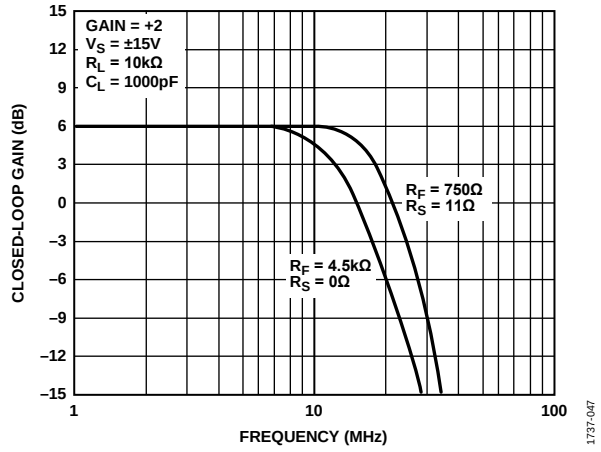


Figure 49. Performance Comparison of Two Methods for Driving a Large Capacitive Load

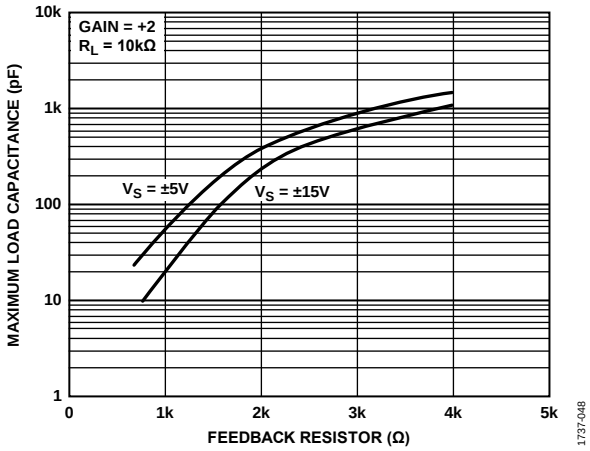


Figure 50. Maximum Load Capacitance vs. Feedback Resistor, Peaking < 1 dB

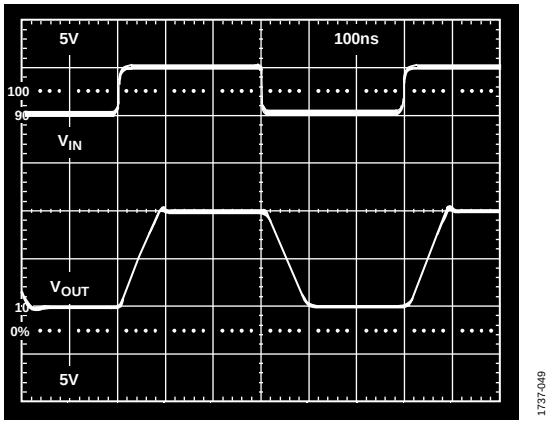


Figure 51. AD810 Driving a 1000 pF Load, Gain = +2, R_F = 750 Ω, R_S = 11 Ω, R_L = 10 kΩ

OPERATION AS A VIDEO LINE DRIVER

The AD810 is designed to offer outstanding performance at closed-loop gains of 1 or greater. At a gain of 2, the low differential gain and phase errors and wide −0.1 dB bandwidth are nearly independent of supply voltage and load (as shown in Figure 53 through Figure 55) making the AD810 an excellent video line driver.

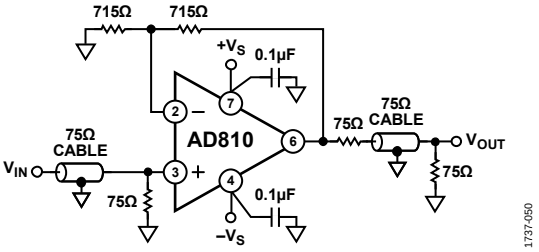


Figure 52. Video Line Driver Operating at Gain = +2

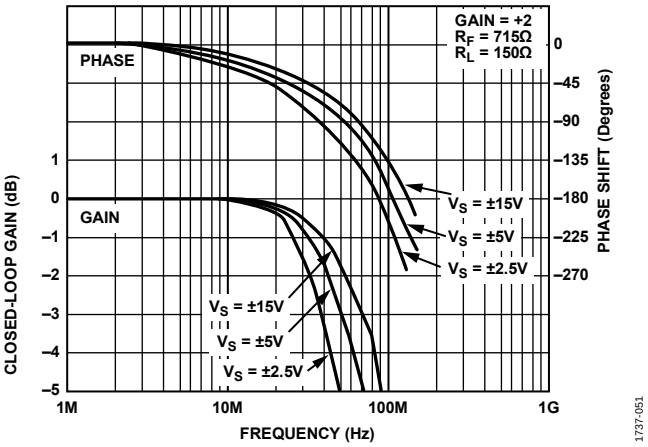


Figure 53. Closed-Loop Gain and Phase Shift vs. Frequency, G = +2, R_L = 150 Ω, R_F = 715 Ω

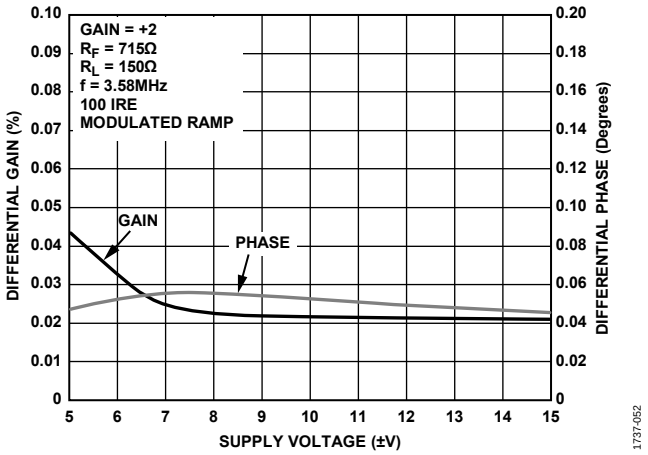


Figure 54. Differential Gain and Differential Phase vs. Supply Voltage

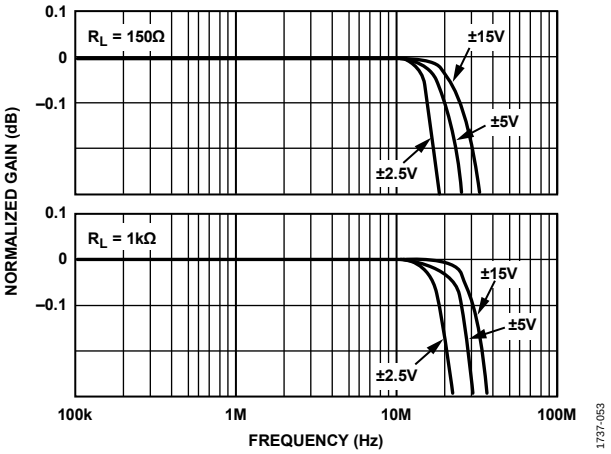


Figure 55. Normalized Gain vs. Frequency for Various Supply Voltages, Gain = +2, R_F = 715 Ω

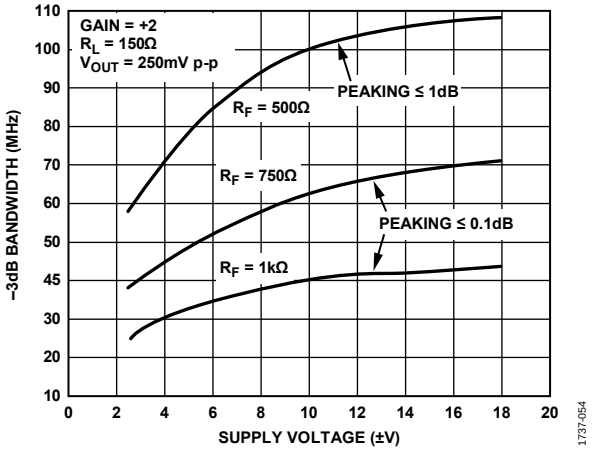


Figure 56. −3 dB Bandwidth vs. Supply Voltage, G = +2, R_L = 150 Ω

2:1 VIDEO MULTIPLEXER

The outputs of two AD810 devices can be wired together to form a 2:1 mux without degrading the flatness of the gain response. Figure 59 shows a recommended configuration that results in −0.1 dB bandwidth of 20 MHz and off channel isolation of 77 dB at 10 MHz on ±5 V supplies. The time to switch between channels is about 0.75 µs when the $\overline{\text{DISABLE}}$ pins are driven by open-drain output logic. Adding pull-up resistors to the logic outputs or using complementary output logic (such as the 74HC04) reduces the switching time to about 180 ns. The switching time is only slightly affected by the signal level.

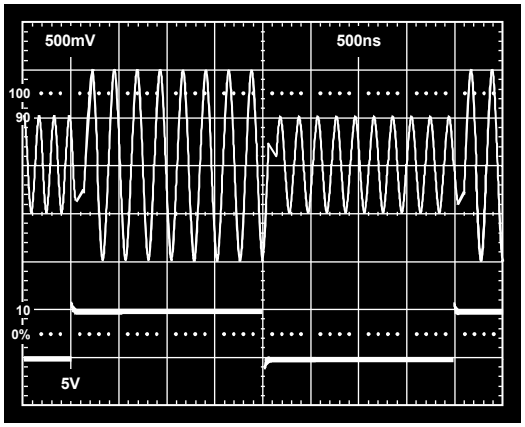


Figure 57. Channel Switching Time for the 2:1 Mux

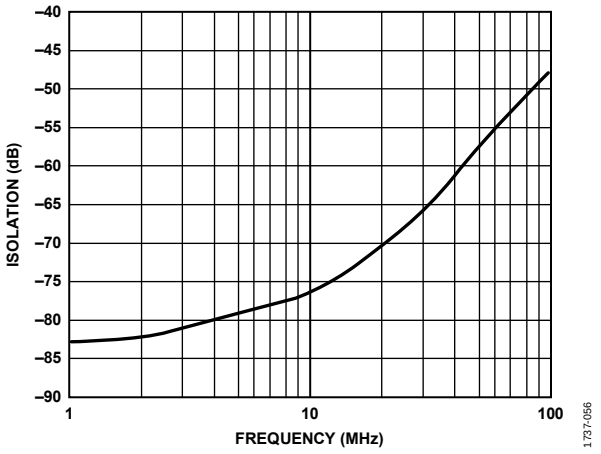


Figure 58. Isolation vs. Frequency for 2:1 Mux, Off Channel

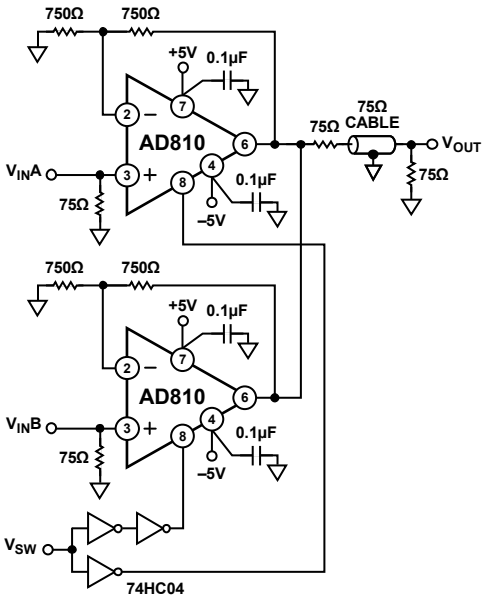


Figure 59. A Fast Switching 2:1 Video Mux

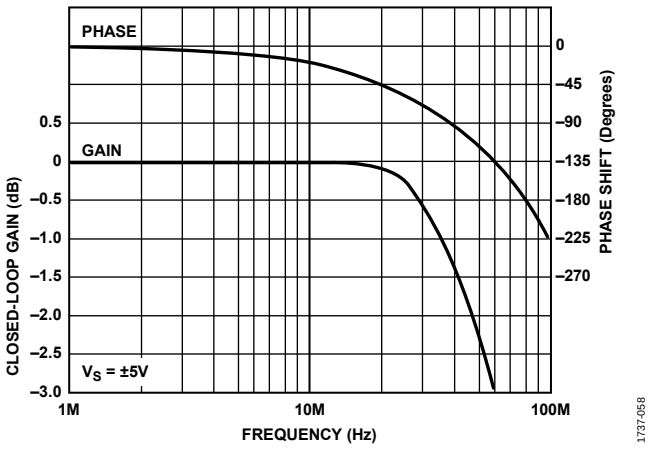


Figure 60. Closed-Loop Gain and Phase Shift vs. Frequency for 2:1 Mux, On Channel

4:1 MULTIPLEXER

A multiplexer of arbitrary size can be formed by combining the desired number of AD810 devices together with the appropriate selection logic. The schematic in Figure 63 shows a recommendation for a 4:1 mux, which can be useful for driving a high impedance such as the input to a video ADC. The output series resistors effectively compensate for the combined output capacitance of the off channels plus the input capacitance of the ADC while maintaining wide bandwidth. In the case illustrated in Figure 63, the −0.1 dB bandwidth is about 20 MHz with no peaking. Switching time and off channel isolation (for the 4:1 mux) are about 250 ns and 60 dB at 10 MHz, respectively.

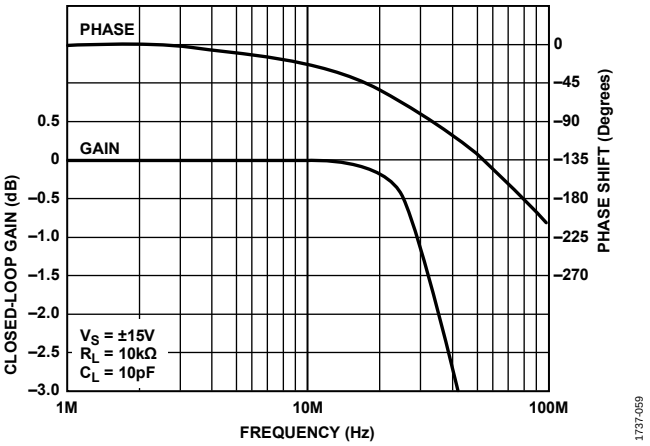


Figure 61. Closed-Loop Gain and Phase Shift vs. Frequency for 4:1 Mux, On Channel

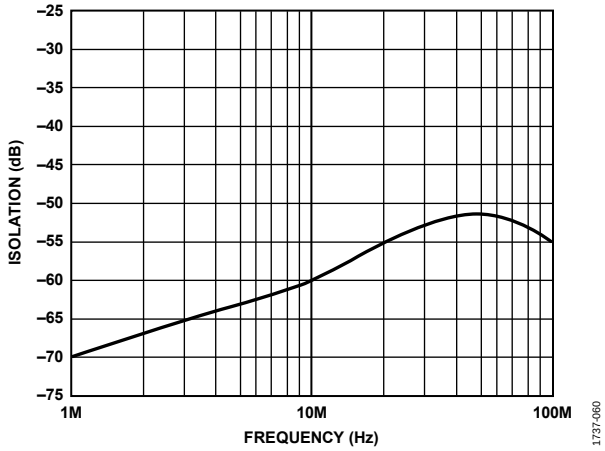


Figure 62. Isolation vs. Frequency for 4:1 Mux, Off Channel

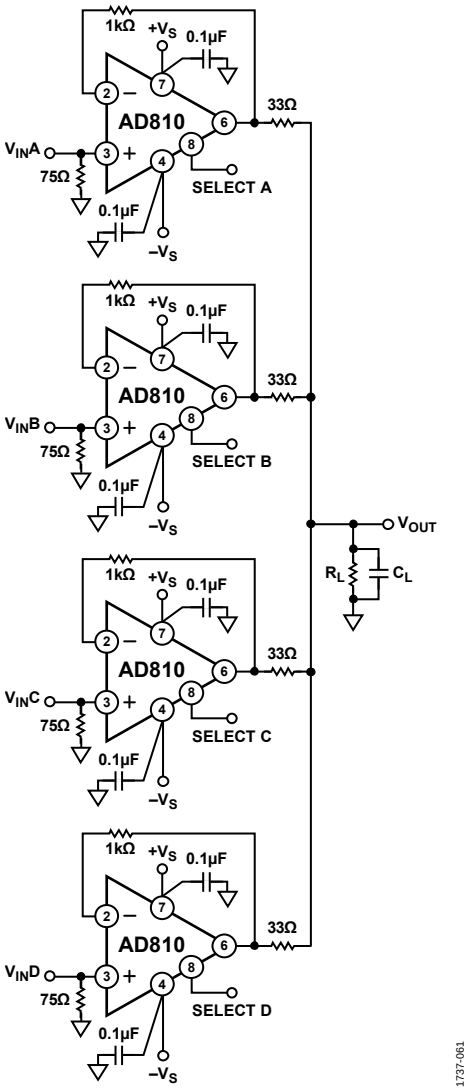
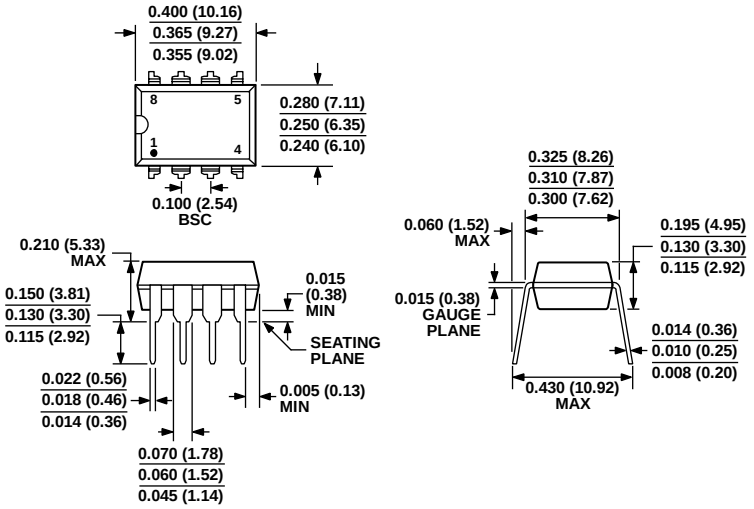


Figure 63. 4:1 Multiplexer Driving a High Impedance

OUTLINE DIMENSIONS

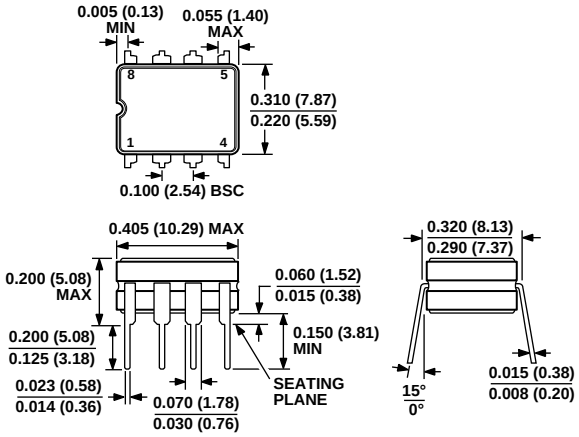


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 64. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 65. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)

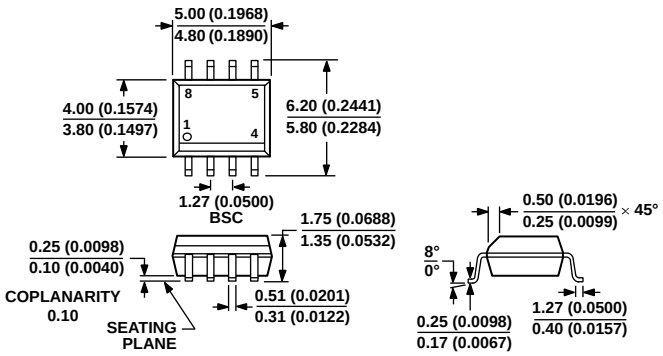


Figure 66. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD810ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD810ARZ	−40°C to +85°C	8-Lead Plastic Standard Small Outline Package [SOIC_N]	R-8
AD810ARZ-REEL	−40°C to +85°C	8-Lead Plastic Standard Small Outline Package [SOIC_N]	R-8
AD810ARZ-REEL7	−40°C to +85°C	8-Lead Plastic Standard Small Outline Package [SOIC_N]	R-8
5962-9313201MPA	−55°C to +125°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8

[1] Z = RoHS Compliant Part.