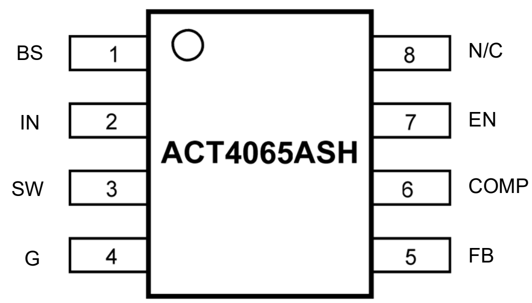
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4065ASH-T	-40°C to 85°C	SOP-8	8	TAPE & REEL

PIN CONFIGURATION



SOP-8

PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION
1	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF between this pin and SW.
2	IN	Input Supply. Bypass this pin to G with a low ESR capacitor. See *Input Capacitor* in *Application Information* section.
3	SW	Switch Output. Connect this pin to the switching end of the inductor.
4	G	Ground.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.808V. Connect to the resistor divider between output and ground to set output voltage.
6	COMP	Compensation Pin. See *Compensation Techniques* in *Application Information* section.
7	EN	Enable Input. When higher than 0.8V, this pin turns the IC on. When lower than 0.8V, this pin turn the IC off. Output voltage is discharged when the IC is off. This pin has a small internal pull-up current to a high level voltage when pin is not connected. Do not allow EN pin to exceed 6V.
8	N/C	Not Connected.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN Supply Voltage	-0.3 to 30	V
SW Voltage	-1 to V_{IN} + 1	V
BS Voltage	V_{SW} - 0.3 to V_{SW} + 7	V
EN, FB, COMP Voltage	-0.3 to 6	V
Continuous SW Current	Internally limited	A
Maximum Power Dissipation	0.76	W
Junction to Ambient Thermal Resistance (θ_{JA})	105	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

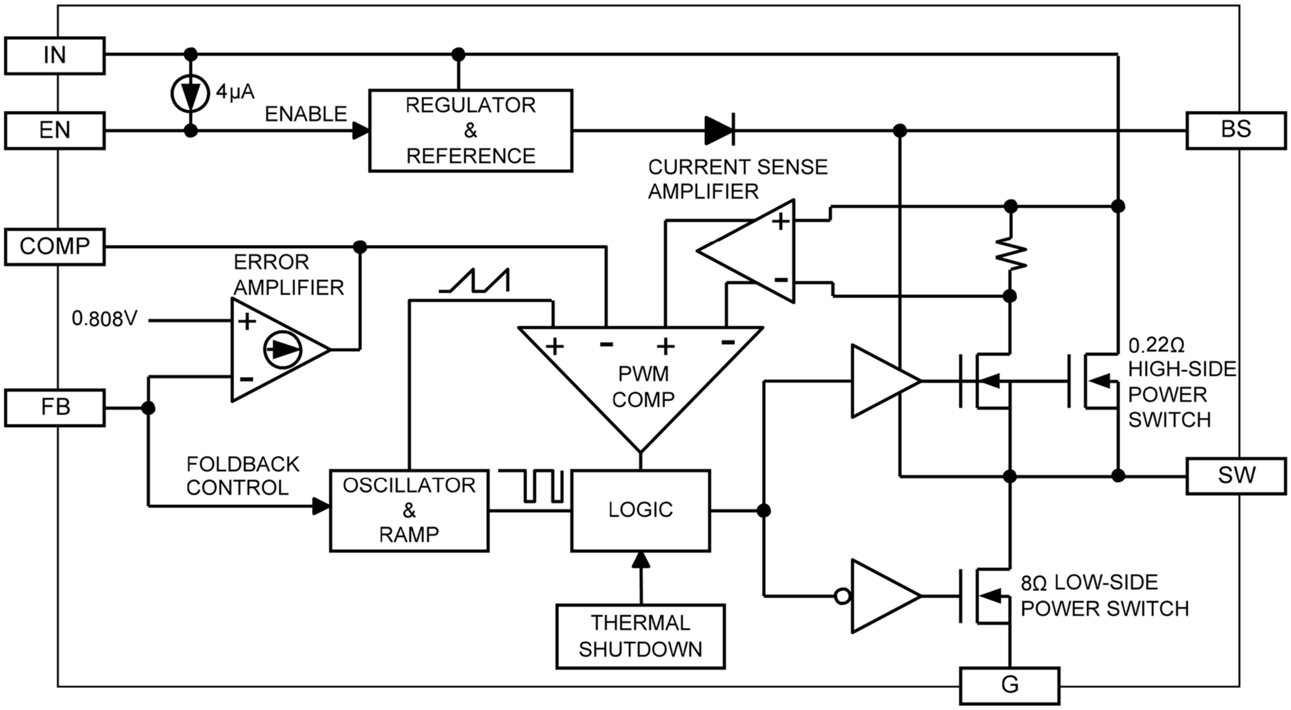
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = 25˚C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{OUT} = 5V, I_{LOAD} = 1A	6		30	V
Feedback Voltage	V_{FB}	V_{COMP} = 1.5V	0.792	0.808	0.824	V
High-Side Switch On Resistance	R_{ONH}			0.22		Ω
Low-Side Switch On Resistance	R_{ONL}			8		Ω
SW Leakage		V_{EN} = 0		1	10	µA
High-Side Switch Current Limit	I_{LIM}	Duty = 50%		3.5		A
COMP to Current Limit Transconductance	G_{COMP}			3.4		A/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10µA		650		µA/V
Error Amplifier DC Gain	A_{VEA}			4000		V/V
Switching Frequency	f_{SW}		190	210	240	kHz
Short Circuit Switching Frequency		V_{FB} = 0		30		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V		88		%
Minimum Duty Cycle		V_{FB} = 1.0V			0	%
Enable Threshold Voltage		Hysteresis = 0.1V	0.75	0.8	0.85	V
Enable Pull-Up Current		Pin pulled up to 4.5V typically when left unconnected		4		µA
Supply Current in Shutdown		V_{EN} = 0		75	100	µA
IC Supply Current in Operation		V_{EN} = 3V, V_{FB} = 1.0V		0.75		mA
Thermal Shutdown Temperature		Hysteresis = 10°C		155		°C

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As seen in, *Functional Block Diagram*, the ACT4065A is a current mode pulse width modulation (PWM) converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in its magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP volt- age, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the Low-Side Power Switch turns on. At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to the output. This state continues until the cycle starts again.

The High-Side Power Switch is driven by logic using the BS bootstrap pin as the positive rail. This pin is charged to V_{SW} + 5V when the Low-Side Power Switch turns on.

The COMP voltage is the integration of the error between the FB input and the internal 0.808V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Current limit happens when COMP reaches its maximum clamp value of 2.0V.

The Oscillator normally switches at 210kHz. However, if the FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a minimum of 30kHz at V_{FB} = 0.15V.

Shutdown Control

The ACT4065A has an enable input EN for turning the IC on or off. When EN is less than 0.7V, the IC is in 8μA low current shutdown mode. When EN is higher than 0.8V, the IC is in normal operation mode. EN is internally pulled up with a 4μA current source and can be left unconnected for always-on operation. EN should never be directly connected to IN.

Thermal Shutdown

The ACT4065A automatically turns off when its junction temperature exceeds 155°C.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:
Output Voltage Setting

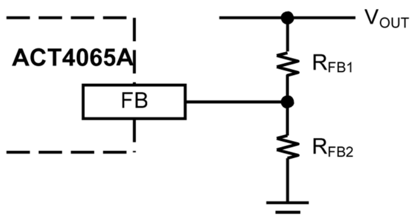


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Typically, use $R_{FB2} \approx 10k\Omega$ and determine R_{FB1} from the output voltage:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.808\ V} - 1\right) \quad (1)$$

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, I_{OUTMAX}\, K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{OUTMAX} is the maximum output current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum output current.

With this inductor value (Table 1), the peak inductor current is $I_{OUT} \times (1 + K_{RIPPLE} / 2)$. Make sure that this peak inductor current is less that the 3A current limit. Finally, select the inductor core size so that it does not saturate at 3A.

Table 1.
Typical Inductor Values

V_{OUT}	1.5V	1.8V	2.5V	3.3V	5V
L	10µH	10µH	15µH	22µH	33µH

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since a large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with shortest possible traces. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX}\, K_{RIPPLE}\left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (3)$$

where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, RESR is the ESR resistance of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, C_{OUT} is the output capacitance, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic type, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

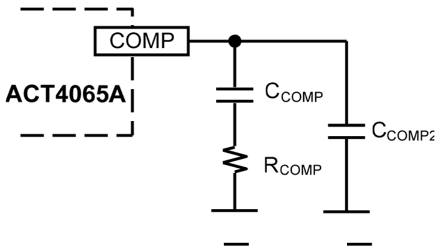
For ceramic output type, typically choose a capacitance of about 22µF. For tantalum or electrolytic type, choose a capacitor with less than 50mΩ ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and the reverse voltage rating higher than the maximum input voltage.

Stability Compensation

Figure 2:
Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitors

The feedback system of the IC is stabilized by the components at COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808\,V}{I_{OUT}} A_{VEA}\, G_{COMP} \quad (4)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi\, A_{VEA}\, C_{COMP}} \quad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi\, V_{OUT}\, C_{OUT}} \quad (6)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi\, R_{COMP}\, C_{COMP}} \quad (7)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi\, R_{COMP}\, C_{COMP2}} \quad (8)$$

Follow the following steps to compensate the IC:

STEP 1. Set the cross over frequency at 1/5 of the switching frequency via RCOMP:

$$R_{COMP} = \frac{2\pi\, V_{OUT}\, C_{OUT}\, f_{SW}}{10\, G_{EA}\, G_{COMP} \times 0.808\,V} = 2.75 \times 10^{8}\, V_{OUT}\, C_{OUT} \quad (\Omega) \quad (9)$$

but limit R_{COMP} to 15kΩ maximum.

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{1.8 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (10)$$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.1/ ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 1.2 \times 10^{-5}\, V_{OUT}\, C_{OUT} \quad (F) \quad (11)$$

STEP 3. If the output capacitors ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESROUT} \geq Min\left(\frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012\, V_{OUT}\right) \quad (\Omega) \quad (12)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT}\, R_{ESROUT}}{R_{COMP}} \quad (13)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 2 shows some calculated results based on the compensation method above

Table 2:
Typical Compensation for Different Output voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2} ①
2.5V	22μF Ceramic	12kΩ	2.2nF	None
3.3V	22μF Ceramic	12kΩ	1.5 nF	None
5V	22μF Ceramic	15kΩ	2.2 nF	None
2.5V	47μF SP Cap	15kΩ	1.5 nF	None
3.3V	47μF SP Cap	15kΩ	1.8 nF	None
5V	47μF SP Cap	15kΩ	2.7 nF	None
2.5V	470μF/6.3V/30mΩ	15kΩ	1.5 nF	47pF
3.3V	470μF/6.3V/30mΩ	15kΩ	2.2 nF	47pF
5V	470μF/10V/30mΩ	15kΩ	2.7 nF	47pF

①: C_{COMP2} is needed only for high ESR output capacitors

Figure 3 shows a sample ACT4065A application circuit generating a 2.5V/2A output.

Figure 3:
Typical Application Circuit for 5V/2A Car Charge

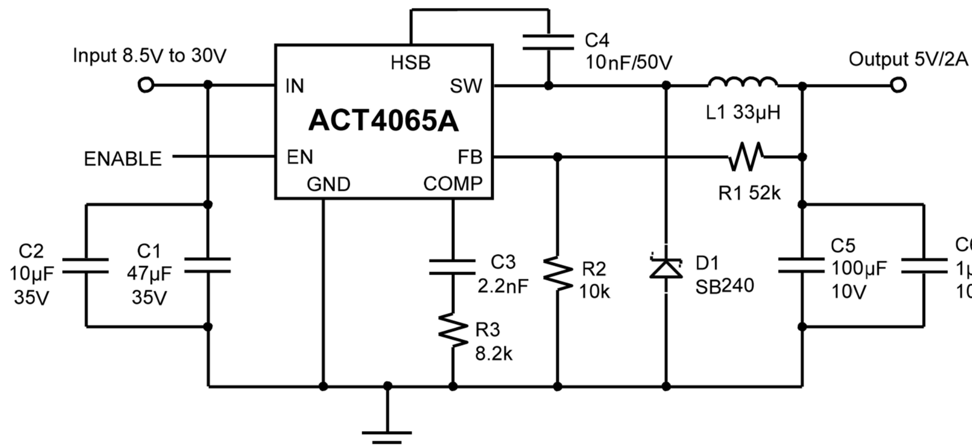
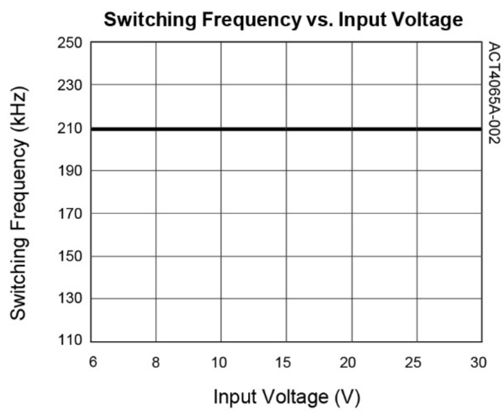


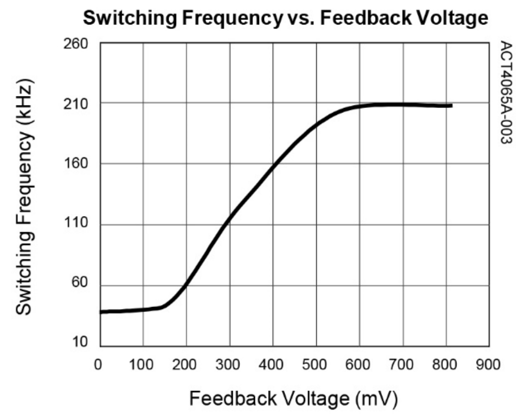
Table 3:
BOM List for 5V/2A Car Charger

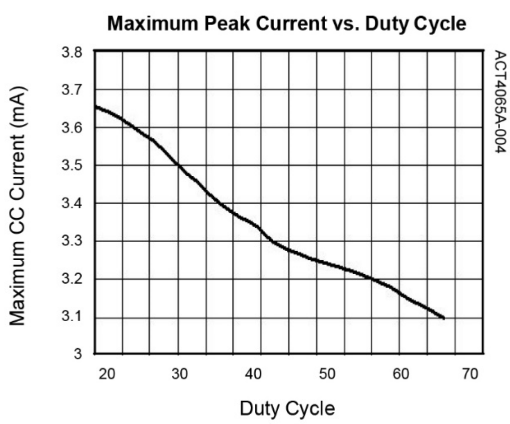
ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4065ASH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47µF/35V, 6.3x7mm	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10µF/35V, 1210, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 2.2nF/6.3V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 10nF/50V, 0603, SMD	Murata, TDK	1
6	C5	Capacitor, Electrolytic, 100µF/10V, 6.3x7mm	Murata, TDK	1
7	C6	Capacitor, Ceramic, 1µF/10V, 0603, SMD	Murata, TDK	1
8	L1	Inductor,33µH, 3.0A	Sumida	1
9	D1	Diode, Schottky, 40V/2A, SB240	Diodes	1
10	R1	Chip Resistor, 52kΩ, 0603, 1%	Murata, TDK	1
11	R3	Chip Resistor, 8.2kΩ, 0603, 5%	Murata, TDK	1
12	R2	Chip Resistor, 10kΩ, 0603, 1%	Murata, TDK	1

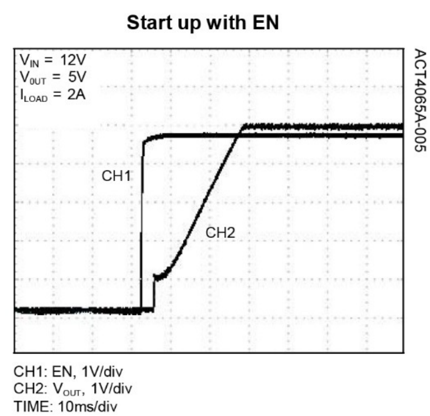
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 3, unless otherwise specified.)

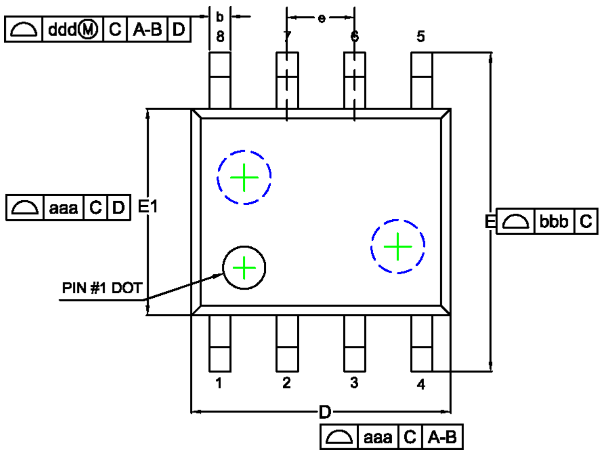




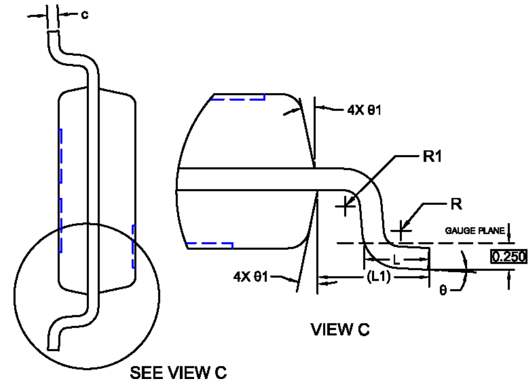




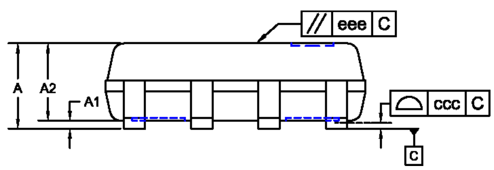
PACKAGE OUTLINE AND DIMENSIONS



Top View



Side View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	1.450	--	1.750
A1	0.100	--	0.250
A2	1.350	--	1.550
b	0.330	--	0.510
c	0.170	--	0.250
D	4.900BSC		
E	6.000BSC		
E1	3.900BSC		
e	1.270 BSC		
L	0.400	--	1.270
L1	1.040REF.		
R	0.070	--	--
R1	0.070	--	--
θ	0°	--	8°
θ1	5°	--	15°
Tol. of Form&Position			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

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Email: customer.support@qorvo.com

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