

2K-bit TTL bipolar PROM (512 x 4)

82S130

82S131

DC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
			Min	Typ ⁵	Max	
Input voltage						
V _{IL} V _{IH} V _{IK}	Low High Clamp	V _{CC} = 4.5V, I _I = -18mA	2.0	0.8	-1.2	V V V
Output voltage						
V _{OL} V _{OH}	Low High (82S131)	CE = Low I _O = 16mA V _{CC} = 4.5V, I _O = -2mA	2.4		0.5	V V
Input current						
I _{IL} I _{IH}	Low High	V _{CC} = 5.5V V _I = 0.45V V _I = 5.5V			-150 40	μA μA
Output current ¹						
I _{OLK} I _{OZ} I _{OS}	Leakage (82S130) Hi-Z state (82S131) Short circuit (82S131) ³	V _{CC} = 5.5V CE = High, V _O = 5.5V CE = High, V _O = 5.5V CE = High, V _O = 0.5V V _{CC} = 5.5V, CE = Low, V _O = 0V, High stored	-15		40 40 -40 -85	μA μA μA mA
Supply current						
I _{CC}		CE = High, V _{CC} = 5.5V			130	mA
Capacitance ⁶						
C _{IN} C _{OUT}	Input Output	CE = High, V _{CC} = 5.0V V _I = 2.0V V _O = 2.0V		5 8	10 13	pF pF

AC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{\text{CC}} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ⁵	Max	
t_{AA}	Access time ⁴	Output	Address			60	ns
t_{CE}	Access time ⁴	Output	Chip Enable			30	ns
t_{CD}	Disable time	Output	Chip Disable			30	ns

NOTES:

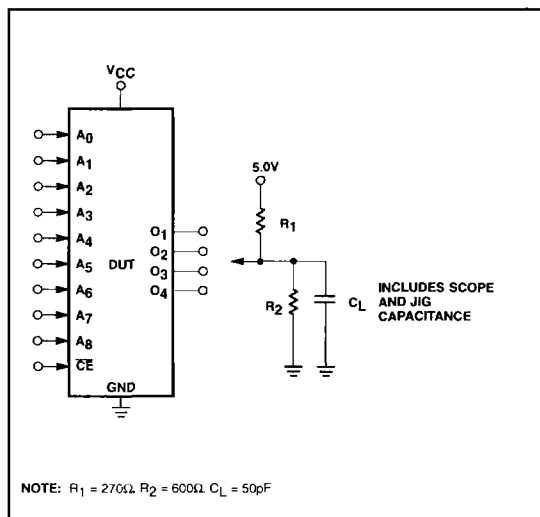
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of $1\mu\text{s}$.
5. Typical values are at $V_{\text{CC}} = 5\text{V}$, $T_A = +25^{\circ}\text{C}$.
6. Guaranteed, but not tested.

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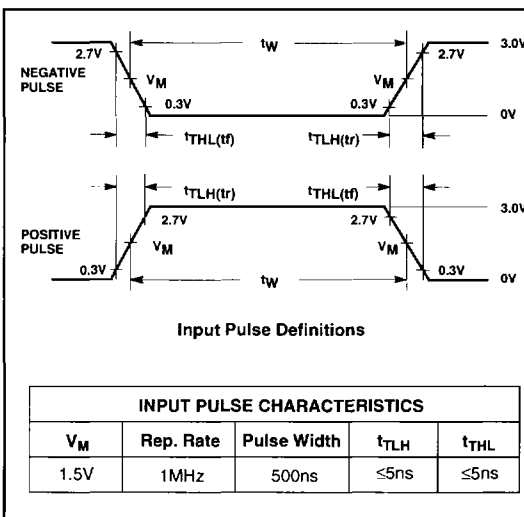
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TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



TIMING DIAGRAMS

