Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN}..........-0.3V to 43V

V_{CC}..........-0.3V to 6.0V

BST..........-0.3V to 48V(1)

BST-SW..........-0.3V to 6V

SW, ILIM..........-1V to 43V(1, 2)

ALL other pins..........-0.3V to VCC+0.3V

Storage Temperature..........-65°C to +150°C

Junction Temperature..........150°C

Power Dissipation..........Internally Limited

Lead Temperature (Soldering, 10 sec)..........300°C

ESD Rating (HBM - Human Body Model)..........2kV

Operating Conditions

PV_{IN}..........5V to 40V

V_{IN}..........5V to 40V

SW, ILIM..........-1V to 40V(1)

PGOOD, V_{CC}, T_{ON}, SS, EN, FB..........-0.3V to 5.5V

Switching Frequency..........100kHz to 800kHz(3)

Junction Temperature Range..........-40°C to +125°C

XR76203 JEDEC51 Package Thermal Resistance, θ_{JA}..........28°C/W

XR76205 JEDEC51 Package Thermal Resistance, θ_{JA}..........26°C/W

XR76208 JEDEC51 Package Thermal Resistance, θ_{JA}..........25°C/W

XR76203 Package Power Dissipation at 25°C..........3.6W

XR76205 Package Power Dissipation at 25°C..........3.8W

XR76208 Package Power Dissipation at 25°C..........4.0W

Note 1: No external voltage applied.

Note 2: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.

Note 3: Recommended frequency

Electrical Characteristics

Unless otherwise noted: T_J= 25°C, V_{IN}=24V, BST=V_{CC}, SW=AGND=PGND=0V, C_{VCC}=4.7uF. Limits applying over the full operating temperature range are denoted by a "•"

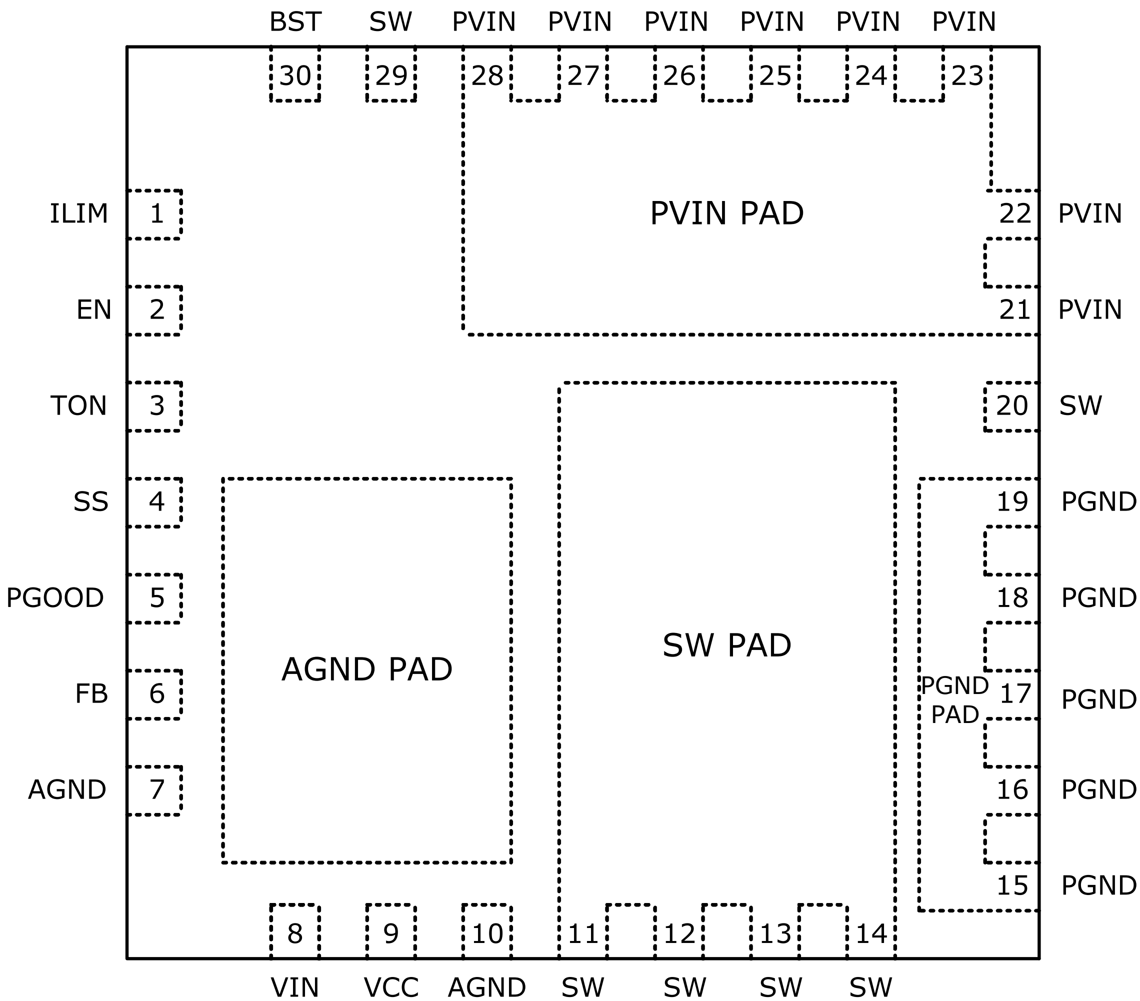
Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input Voltage Range	VCC regulating	•	5.5		40	V
I_{VIN}	VIN Input Supply Current	Not switching, V_{IN} = 24V, V_{FB} = 0.7V	•		0.7	2	mA
I_{VIN}	VIN Input Supply Current (XR76203)	f=300kHz, R_{ON}=215k, VFB=0.58V			12		mA
I_{VIN}	VIN Input Supply Current (XR76205)	f=300kHz, R_{ON}=215k, VFB=0.58V			15		mA
I_{VIN}	VIN Input Supply Current (XR76208)	f=300kHz, R_{ON}=215k, VFB=0.58V			19		mA
I_{OFF}	Shutdown Current	Enable = 0V, V_{IN} = 12V			1		µA
Enable and Under-Voltage Lock-Out UVLO							
$V_{IH\_EN\_1}$	EN Pin Rising Threshold		•	1.8	1.9	2.0	V
$V_{EN\_H\_1}$	EN Pin Hysteresis				70		mV
$V_{IH\_EN\_2}$	EN Pin Rising Threshold for DCM/ CCM operation		•	2.8	3.0	3.1	V
$V_{EN\_H\_2}$	EN Pin Hysteresis				100		mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO Start Threshold, Rising Edge		•	4.00	4.25	4.40	V
	VCC UVLO Hysteresis				230		mV
Reference Voltage							
V_{REF}	Reference Voltage	V_{IN} = 5.5V to 40V, VCC regulating		0.596	0.600	0.604	V
		V_{IN} = 5.5V to 40V, VCC regulating	•	0.594	0.600	0.606	V
	DC Line Regulation	CCM, closed loop, V_{IN}=5.5V-40V, applies to any C_{OUT}			±0.33		%
	DC Load Regulation	CCM, closed loop, applies to any C_{OUT}			±0.39		%
Programmable Constant On-Time							
T_{ON1}	On-Time 1	R_{ON} = 237k, V_{IN} = 40V	•	1570	1840	2120	ns
	f Corresponding to On-Time 1	V_{OUT}= 24V, V_{IN} = 40V, R_{ON} = 237k	•	283	326	382	kHz
$T_{ON(MIN)}$	Minimum Programmable On-Time	R_{ON} = 14k, V_{IN} = 40V			120		ns
T_{ON2}	On-Time 2	R_{ON} = 14k, V_{IN} = 24V	•	174	205	236	ns
T_{ON3}	On-Time 3	R_{ON} = 35.7k, V_{IN} = 24V	•	407	479	550	ns
	f Corresponding to On-Time 3	V_{OUT} = 3.3V, V_{IN} = 24V, R_{ON} = 35.7k	•	250	287	338	kHz
	f Corresponding to On-Time 3	V_{OUT} = 5.0V, V_{IN} = 24V, R_{ON} = 35.7k	•	379	435	512	kHz
	Minimum Off-Time		•		250	350	ns
Diode Emulation Mode							
	Zero Crossing Threshold	DC value measured during test			-2		mV
Soft-start							
	SS Charge Current		•	-14	-10	-6	µA
	SS Discharge Current	Fault present	•	1			mA
VCC Linear Regulator							
	VCC Output Voltage	V_{IN} = 6V to 40V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5V, I_{LOAD} = 0 to 20mA	•	4.51	4.7		V
Power Good Output							
	Power Good Threshold			-10	-6.9	-5	%
	Power Good Hysteresis				1.6	4	%
	Power Good Sink Current			1			mA
Protection: OCP, OTP, Short-Circuit							
	Hiccup Timeout				110		ms
	ILIM Pin Source Current			45	50	55	µA
	ILIM Current Temperature Coefficient				0.4		%/°C
	OCP Comparator Offset		•	-8	0	+8	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Current Limit Blanking	GL rising>1V			100		ns
	Thermal Shutdown Threshold[1]	Rising temperature			150		°C
	Thermal Hysteresis[1]				15		°C
	VSCTH Feedback Pin Short-Circuit Threshold	Percent of V_{REF}, short circuit is active after PGOOD is asserted	•	50	60	70	%
XRP76203 Output Power Stage							
R_{DSON}	High-Side MOSFET R_{DSON}	I_{DS} = 1A			115	160	mΩ
	Low-Side MOSFET R_{DSON}				40	59	mΩ
I_{OUT}	Maximum Output Current		•	3A			A
XRP76205 Output Power Stage							
R_{DSON}	High-Side MOSFET R_{DSON}	I_{DS} = 2A			42	59	mΩ
	Low-Side MOSFET R_{DSON}				40	59	mΩ
I_{OUT}	Maximum Output Current		•	5A			A
XRP76208 Output Power Stage							
R_{DSON}	High-Side MOSFET R_{DSON}	I_{DS} = 2A			42	59	mΩ
	Low-Side MOSFET R_{DSON}				16.2	21.5	mΩ
I_{OUT}	Maximum Output Current		•	8A			A

Note 1: Guaranteed by design

Pin Configuration, Top View

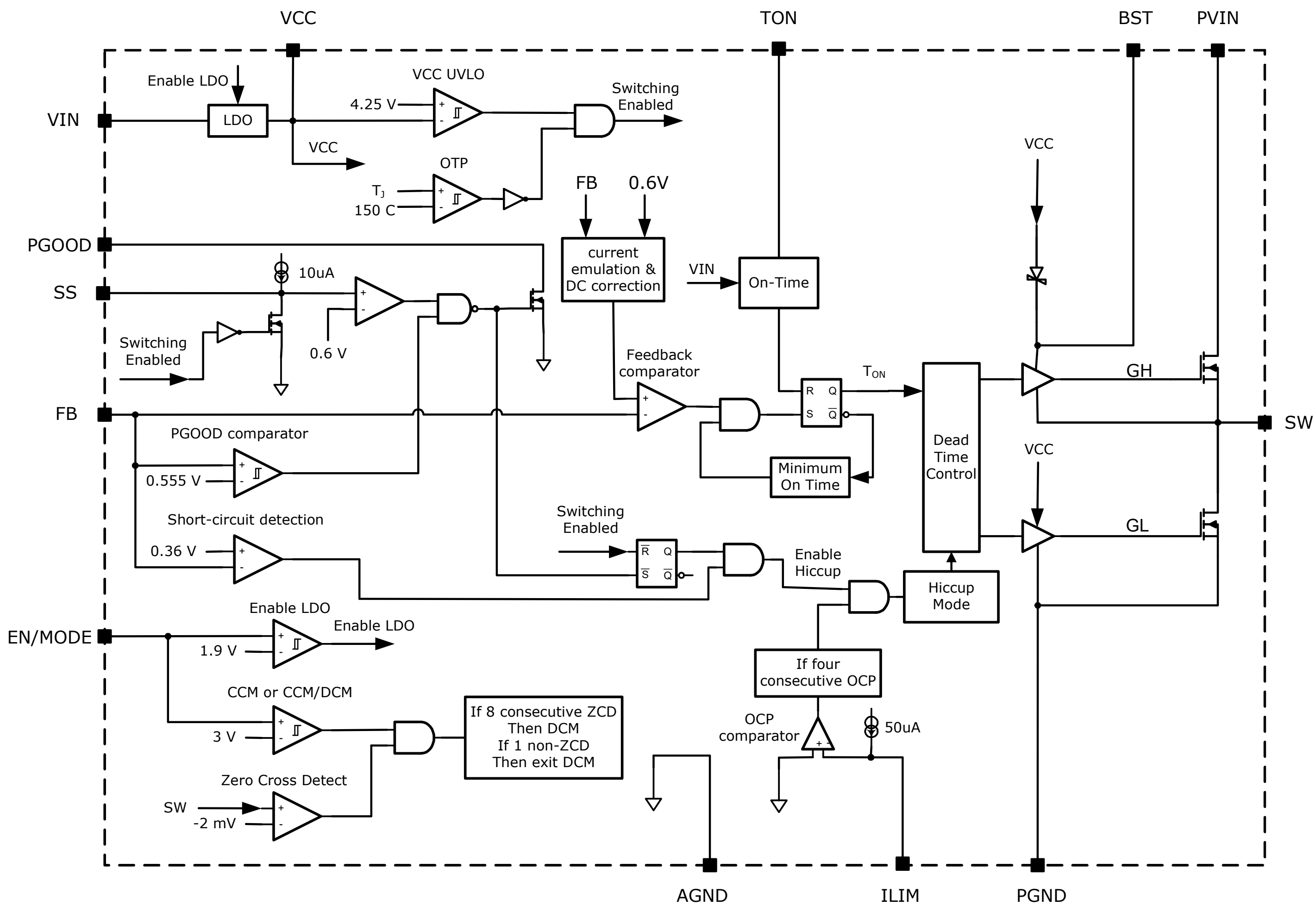


Pin Assignments

Pin No.	Pin Name	Type	Description
1	ILIM	A	Over-current protection programming. Connect with a resistor to SW.
2	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the regulator on and it will operate in CCM. If the voltage is raised above 3.0V then the regulator will operate in DCM/CCM depending on load
3	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
4	SS	A	Soft-Start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10uA internal source current.
5	PGOOD	O, OD	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
6	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program V_{OUT}.
7, 10, AGND Pad	AGND	A	Signal ground for control circuitry. Connect AGND Pad with a short trace to pins 7 and 10.
8	VIN	A	Supply input for the regulator's LDO. Normally it is connected to PVIN.
9	VCC	A	The output of regulator's LDO. For operation using a 5V rail, VCC should be shorted to VIN.
11-14, 20, 29, SW Pad	SW	PWR	Switch node. Drain of the low-side N-channel MOSFET. Source of the high-side MOSFET is wire-bonded to the SW Pad. Pins 20 and 29 are internally connected to SW pad.
15-19, PGND Pad	PGND	PWR	Ground of the power stage. Should be connected to the system's power ground plane. Source of the low-side MOSFET is wire-bonded to PGND Pad.
21-28, PVIN Pad	PVIN	PWR	Input voltage for power stage. Drain of the high-side N-channel MOSFET.
30	BST	A	High-side driver supply pin. Connect a bootstrap capacitor between BST and pin 29.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT}=3.3V, I_{OUT}=8A, f=400kHz, T_A = 25°C. Schematic from the application information section.

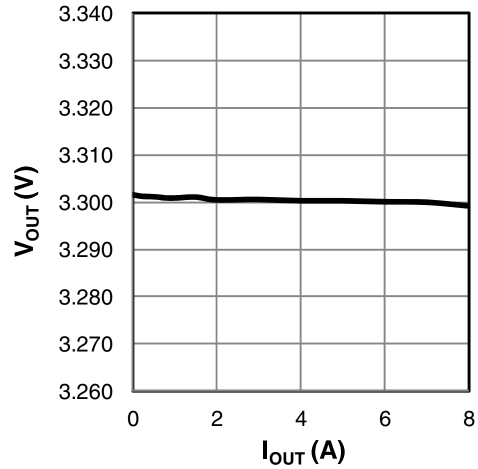


Figure 1: Load Regulation

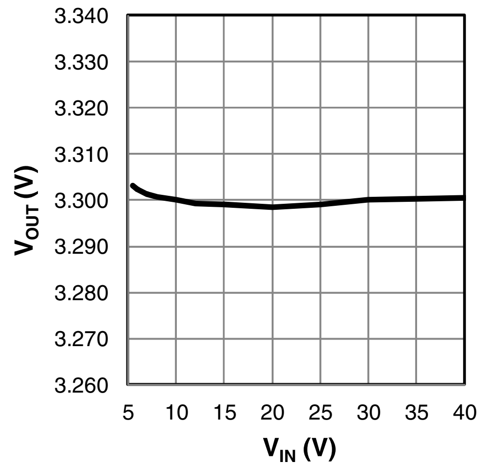


Figure 2: Line regulation

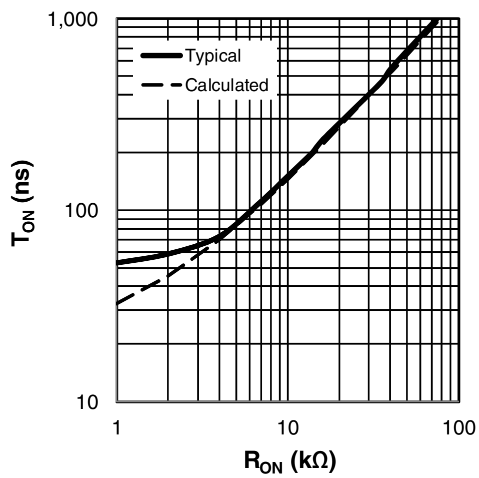


Figure 3: T_{ON} versus R_{ON}

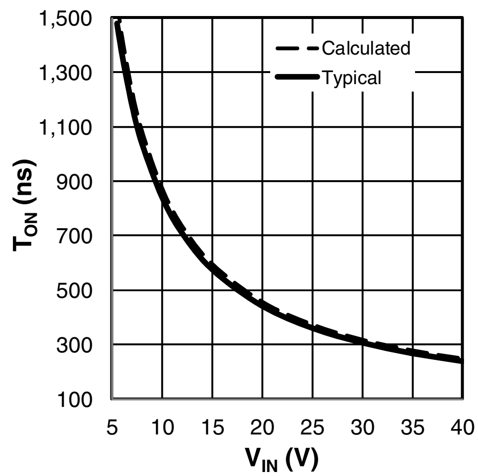


Figure 4: T_{ON} versus V_{IN}, R_{ON}=27.4k

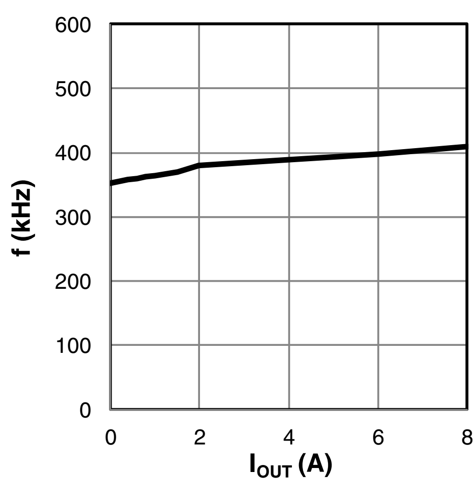


Figure 5: frequency versus I_{OUT}

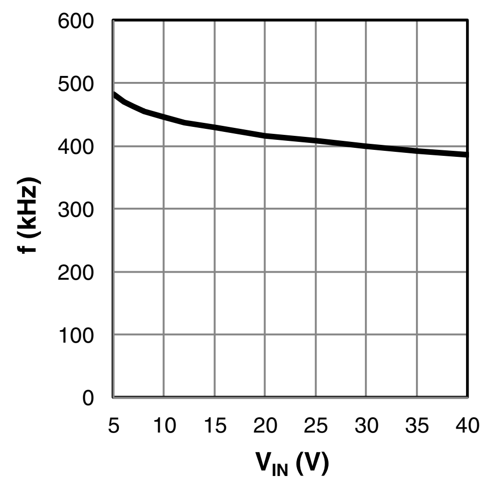


Figure 6: frequency versus V_{IN}

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT}=3.3V, I_{OUT}=8A, f=400kHz, T_A = 25°C. Schematic from the application information section.

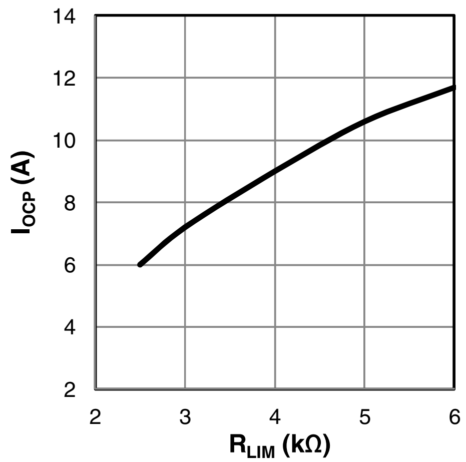


Figure 7: XR76208 I_{OCP} versus R_{LIM}

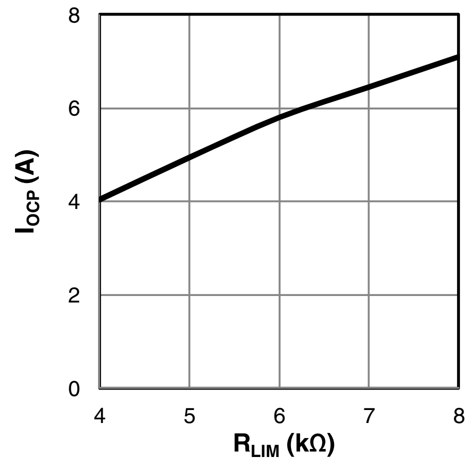


Figure 8: XR76205 I_{OCP} versus R_{LIM}

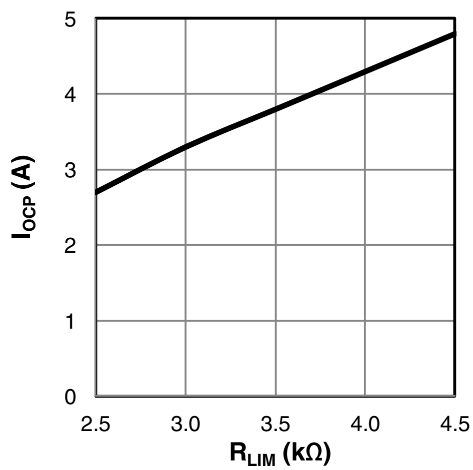


Figure 9: XR76203 I_{OCP} versus R_{LIM}

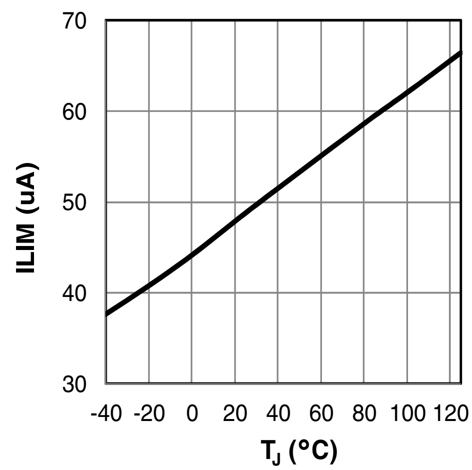


Figure 10: I_{LIM} versus temperature

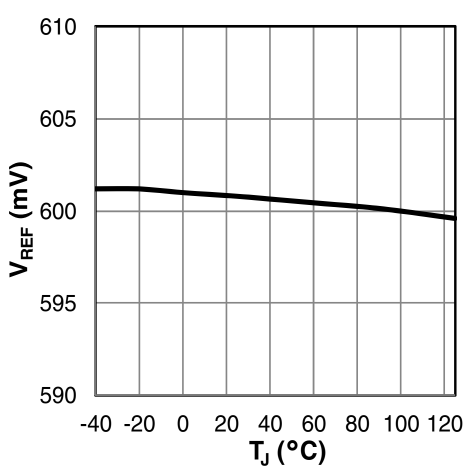


Figure 11: V_{REF} versus temperature

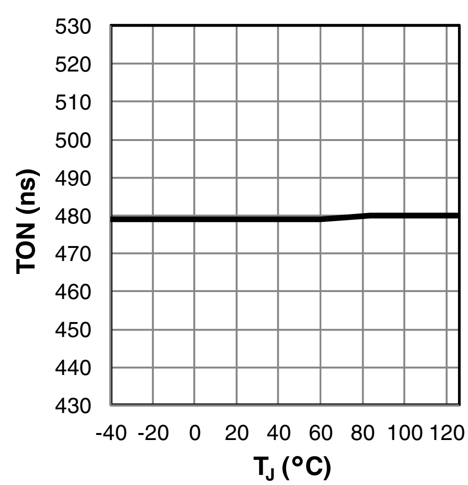


Figure 12: T_{ON} versus temperature, R_{ON}=35.7kΩ

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT}=3.3V, I_{OUT}=8A, f=400kHz, T_A = 25°C. Schematic from the application information section.

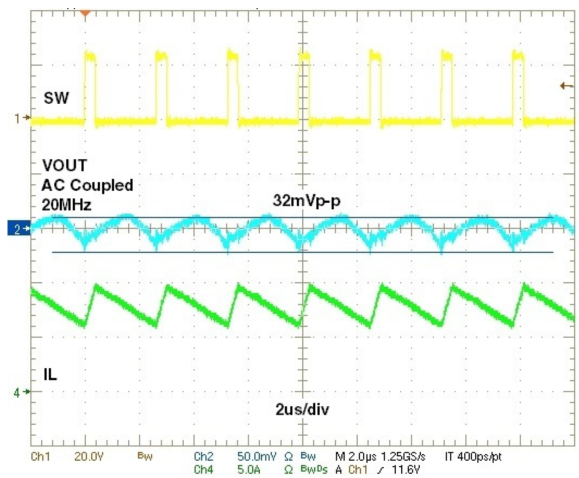


Figure 13: Steady state, I_{OUT}=8A

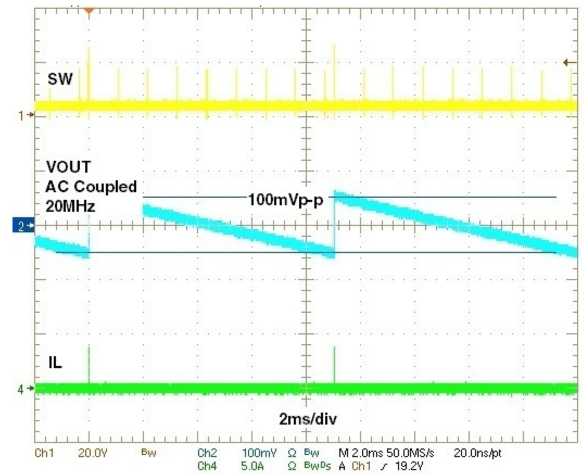


Figure 14: Steady state, DCM, I_{OUT}=0A

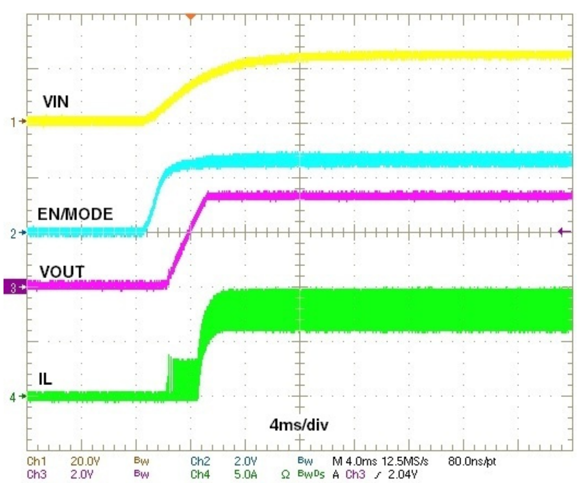


Figure 15: Power up, Forced CCM

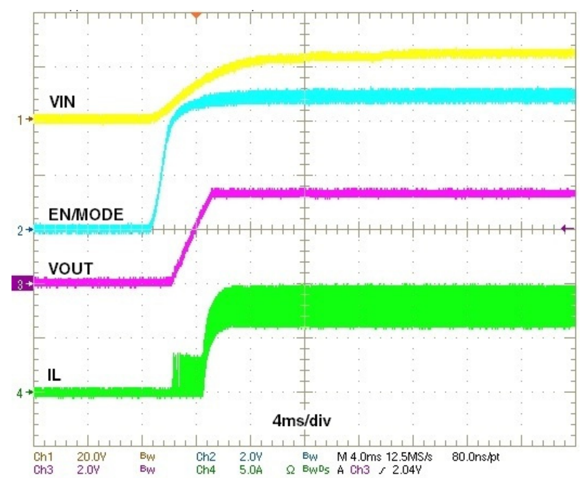


Figure 16: Power up, DCM/CCM

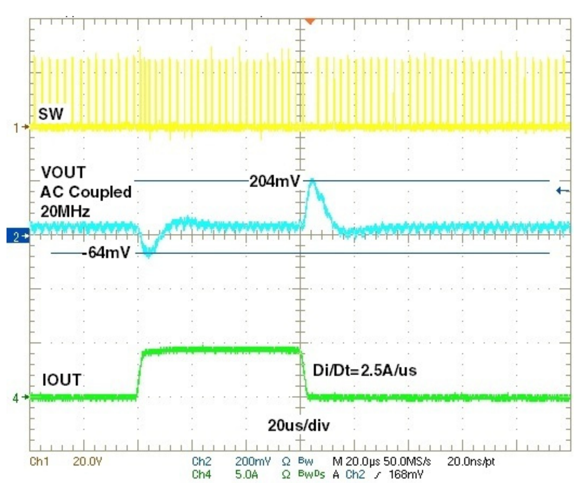


Figure 17: Load step, Forced CCM, 0A-4A-0A

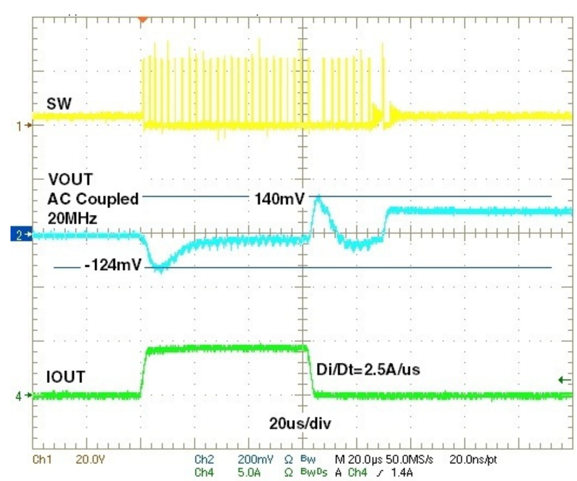


Figure 18: Load step, DCM/CCM, 0A-4A-0A

Efficiency

Unless otherwise noted: $T_{AMBIENT}$ = 25°C, No Air flow, f=400kHz, Inductor losses are included, Schematic from the application information section.

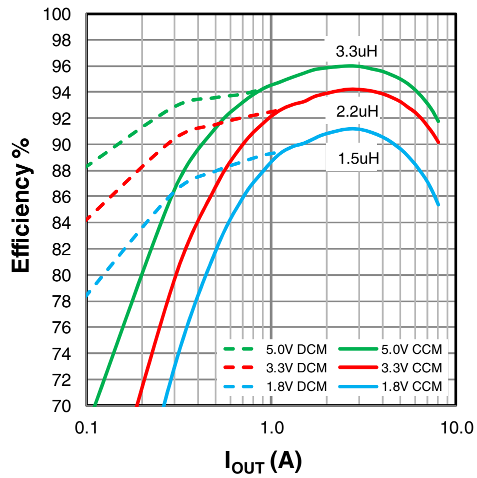


Figure 19: XR76208 efficiency, V_{IN}=12V

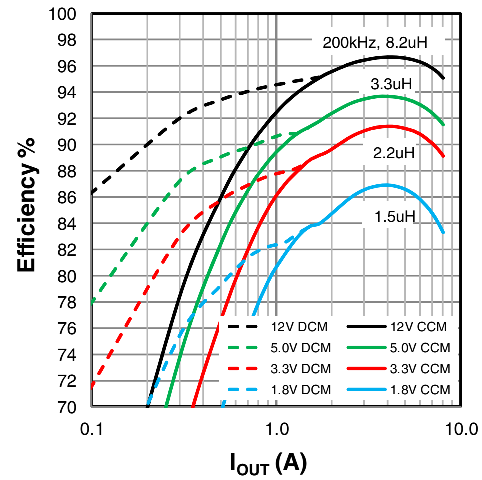


Figure 20: XR76208 efficiency, V_{IN}=24V

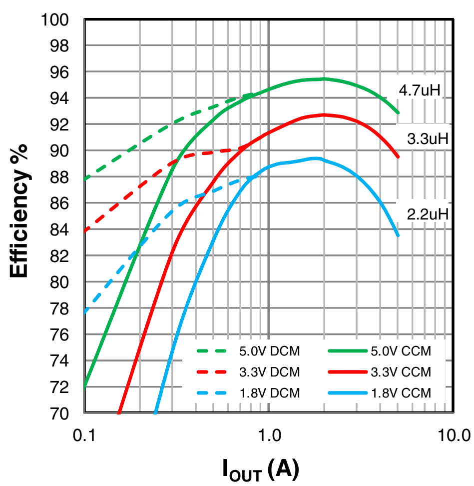


Figure 21: XR76205 efficiency, V_{IN}=12V

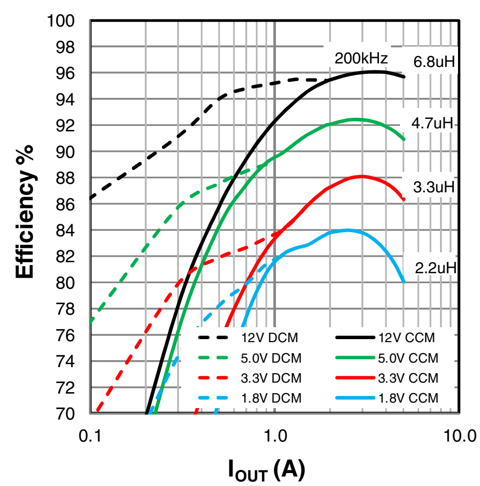


Figure 22: XR76205 efficiency, V_{IN}=24V

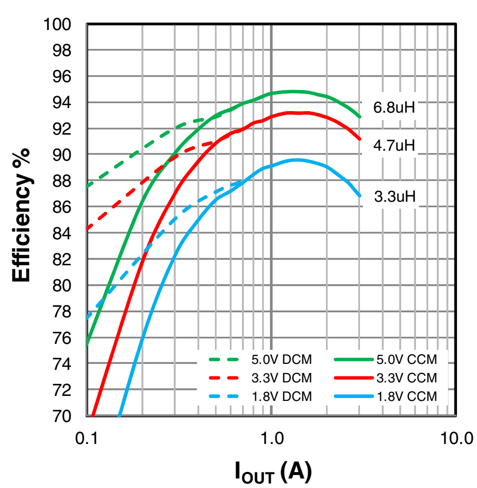


Figure 23: XR76203 efficiency, V_{IN}=12V

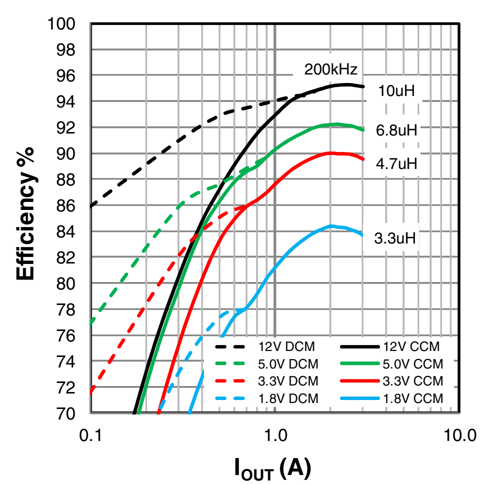


Figure 24: XR76203 efficiency, V_{IN}=24V

Thermal Derating

Unless otherwise noted: No Air flow, f=400kHz, Schematic from the application information section.

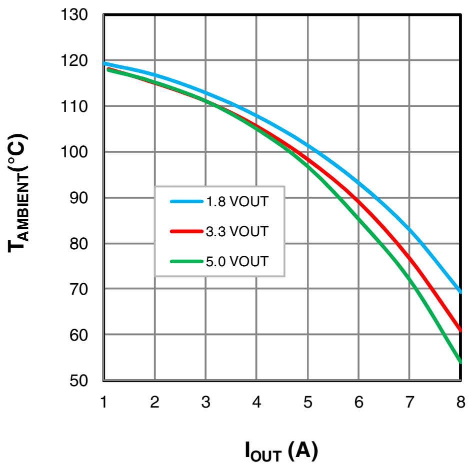


Figure 25: XR76208, V_{IN}=12V

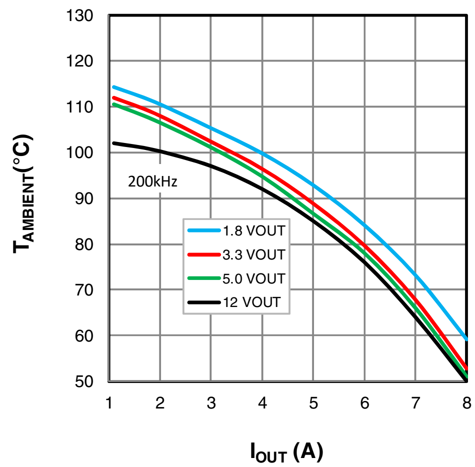


Figure 26: XR76208, V_{IN}=24V

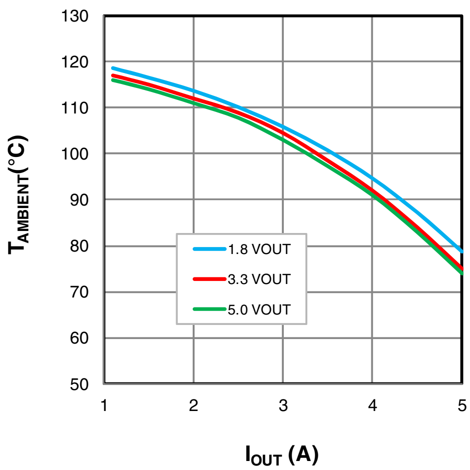


Figure 27: XR76205, V_{IN}=12V

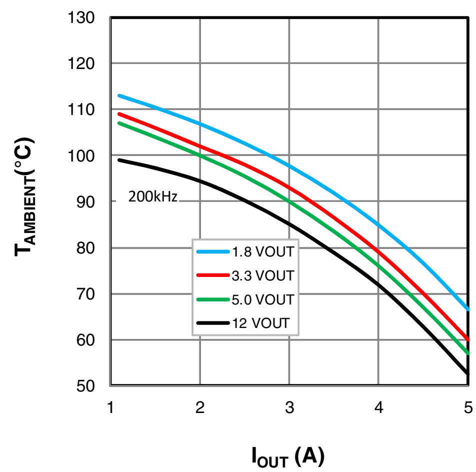


Figure 28: XR76205, V_{IN}=24V

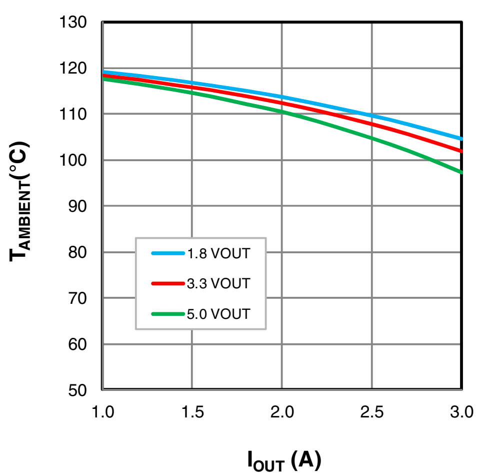


Figure 29: XR76203, V_{IN}=12V

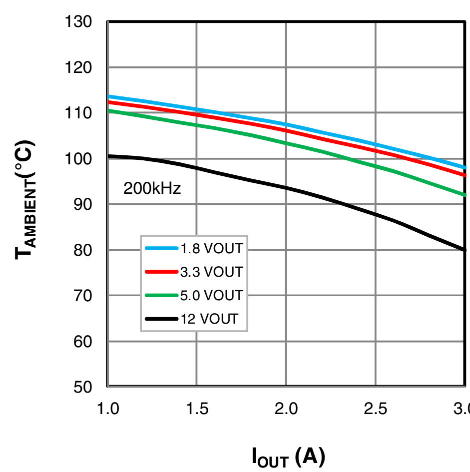


Figure 30: XR76203, V_{IN}=24V

Functional Description

XR76203, XR76205 and XR76208 are synchronous step-down proprietary emulated current-mode Constant On-Time (COT) regulators. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with GH signal turning on the high-side (control) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the minimum off-time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable/Mode Input (EN/MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on/off. It also selects between two modes of operation: 'Forced CCM' and 'DCM/CCM'. If EN is pulled below 1.8V, the Regulator shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM mode which will run the Regulator in continuous conduction at all times. A voltage higher than 3.1V selects the DCM/CCM mode which will run the Regulator in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the Regulator to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 31 can be used to generate the required voltage. Note that at V_{IN} of 5.5V and 40V the nominal Zener voltage is 4.0V and 5.0V respectively. Therefore for V_{IN} in the range of 5.5V to 40V, the circuit shown in Figure 31 will generate V_{EN} required for Forced CCM.

Selecting the DCM/CCM Mode

In order to set the Regulator operation to DCM/CCM, a voltage between 3.1V and 5.5V must be applied to EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 32 can be used to generate the required voltage.

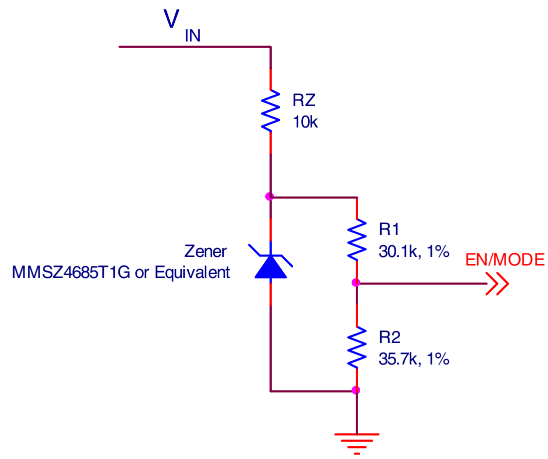


Figure 31: Selecting Forced CCM by deriving EN/MODE from V_{IN}

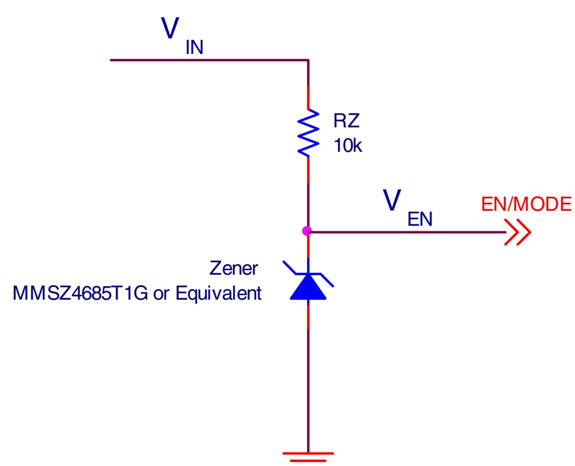


Figure 32: Selecting DCM/CCM by deriving EN/MODE from V_{IN}

Programming the On-Time

The On-Time T_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON} - (25 \times 10^{-9})]}{3.05 \times 10^{-10}}$$

where T_{ON} is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff}$$

where:

f is the desired switching frequency at nominal I_{OUT}

Eff is the Regulator efficiency corresponding to nominal I_{OUT} shown in Figures 19-24

Substituting for T_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{f \times Eff}\right) - [(25 \times 10^{-9}) \times V_{IN}]}{3.05 \times 10^{-10}}$$

Over-Current Protection (OCP)

If load current exceeds the programmed over-current, I_{OCP}, for four consecutive switching cycles, the Module enters hiccup mode of operation. In hiccup, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The Module will remain in hiccup mode until load current is reduced below the programmed I_{OCP} . In order to program the over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current threshold to be programmed

RDS is the MOSFET rated On Resistance; XR76208=21.5mΩ, XR76205=59mΩ, XR76203=59mΩ

8mV is the OCP comparator maximum offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C (Figure 10). This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. Graph of typical I_{OCP} versus RLIM is shown in Figure 7-9. Maximum allowable RLIM for XR76205 is 8.06kΩ.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the Module will enter hiccup mode. Hiccup will persist until short-circuit is removed. SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the Application Circuit to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

where R2 has a nominal value of 2kΩ.

Programming the Soft-start

Place a capacitor CSS between the SS and AGND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left(\frac{10\mu A}{0.6V}\right)$$

Feed-Forward Capacitor (C_{FF})

A feed-forward capacitor (C_{FF}) may be necessary depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used for C_{OUT} then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}$$

where:

R1 is the resistor that C_{FF} is placed in parallel with

f_{LC} is the frequency of output filter double-pole

f_{LC} frequency must be less than 11kHz when using ceramic C_{OUT}. If necessary, increase L and/or C_{OUT} in order to meet this constraint.

When using capacitors with higher ESR, such as PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 11kHz.

2. The frequency of ESR Zero $f_{Zero,ESR}$ should be at least five times larger than f_{LC}.

Note that if $f_{Zero,ESR}$ is less than $5xf_{LC}$, then it is recommended to set the f_{LC} at less than 2kHz. CFF is still not required.

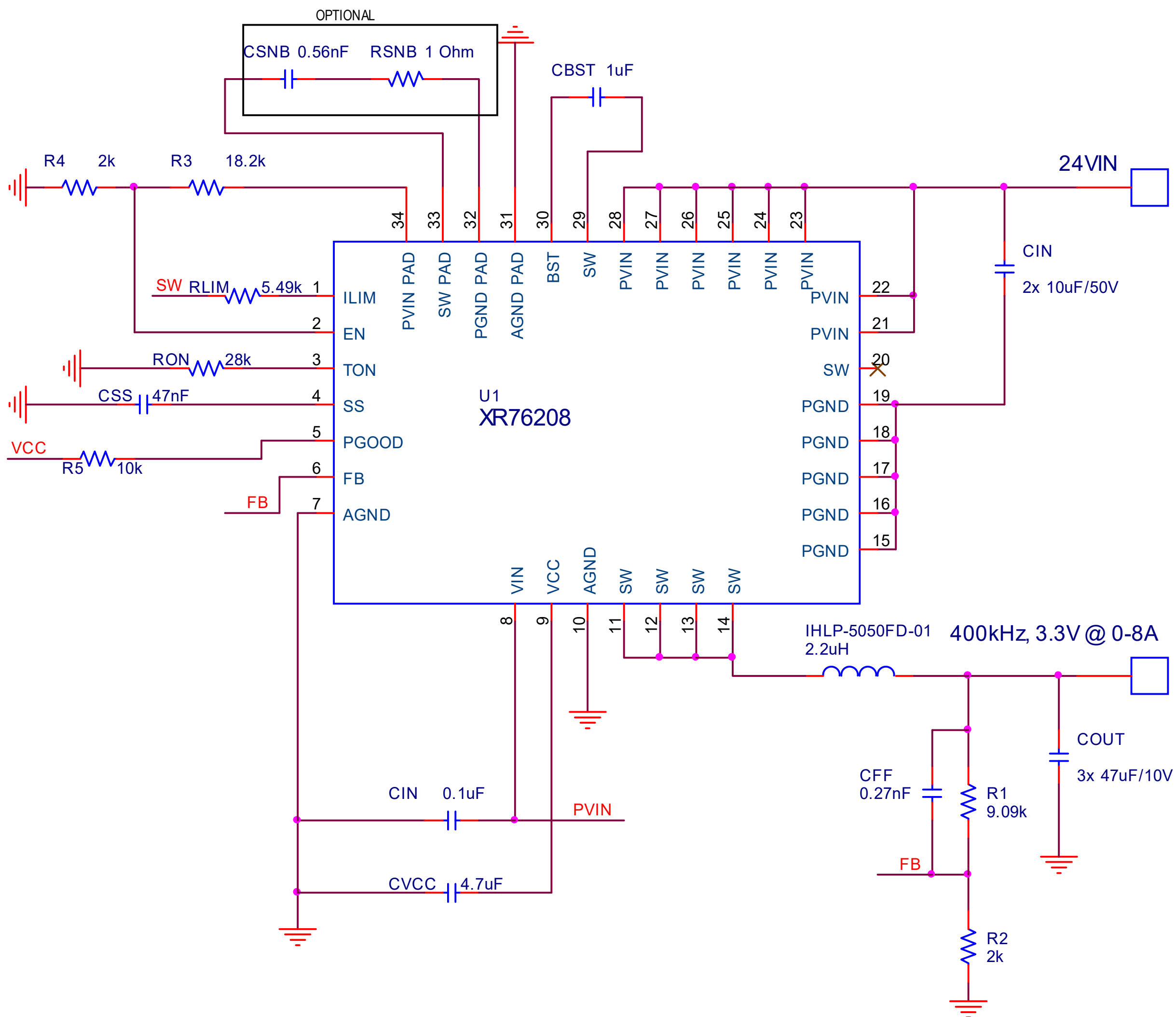
Maximum Allowable Voltage Ripple at FB pin

Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the Regulator to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

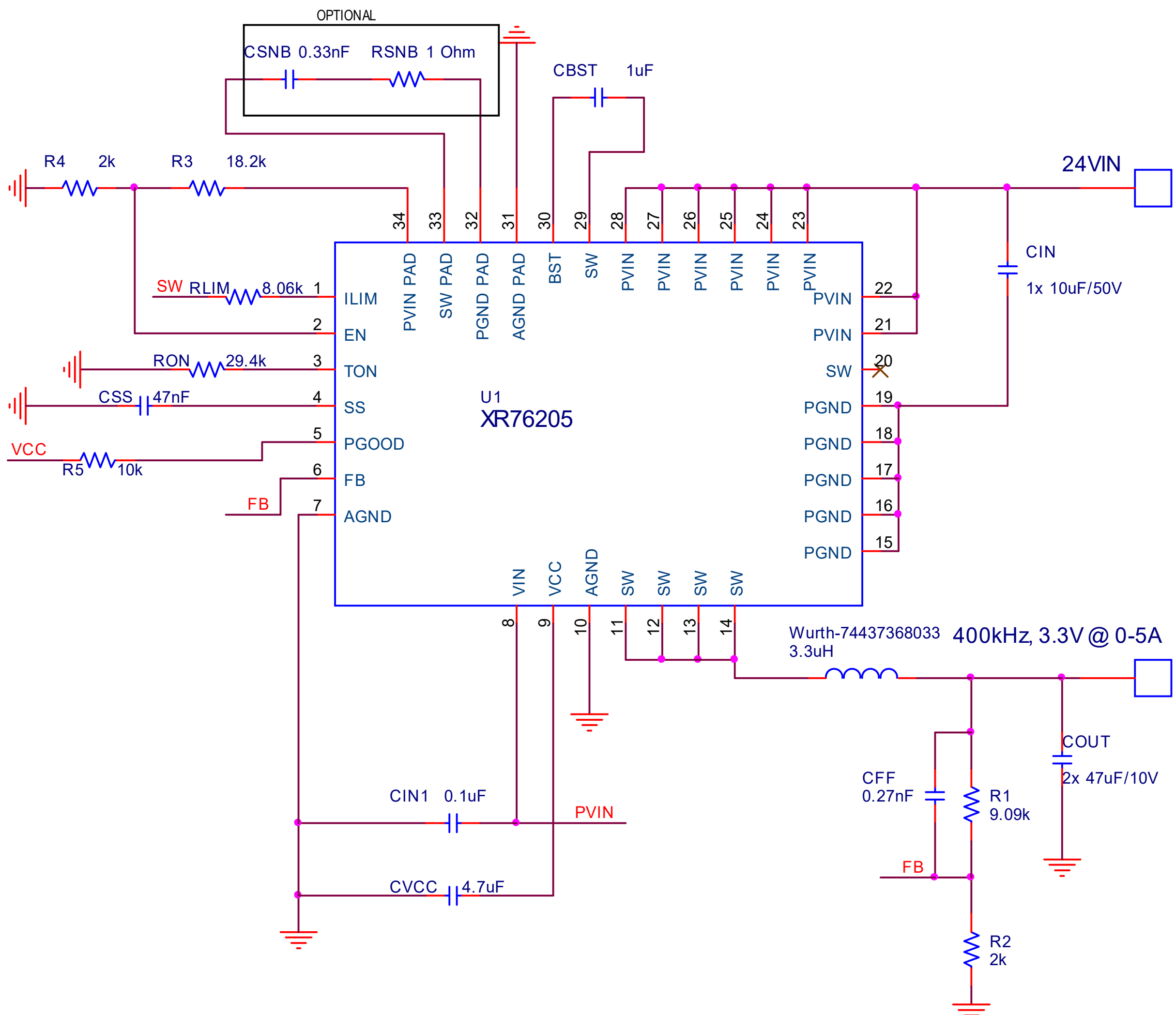
Feed-Forward Resistor (R_{FF})

Poor PCB layout can cause FET switching noise at the output and may couple to the FB pin via $C_{FF.}$ Excessive noise at FB will cause poor load regulation. To solve this problem place a resistor R_{FF} in series with C_{FF}. R_{FF} value up to 2% of R1 is acceptable.

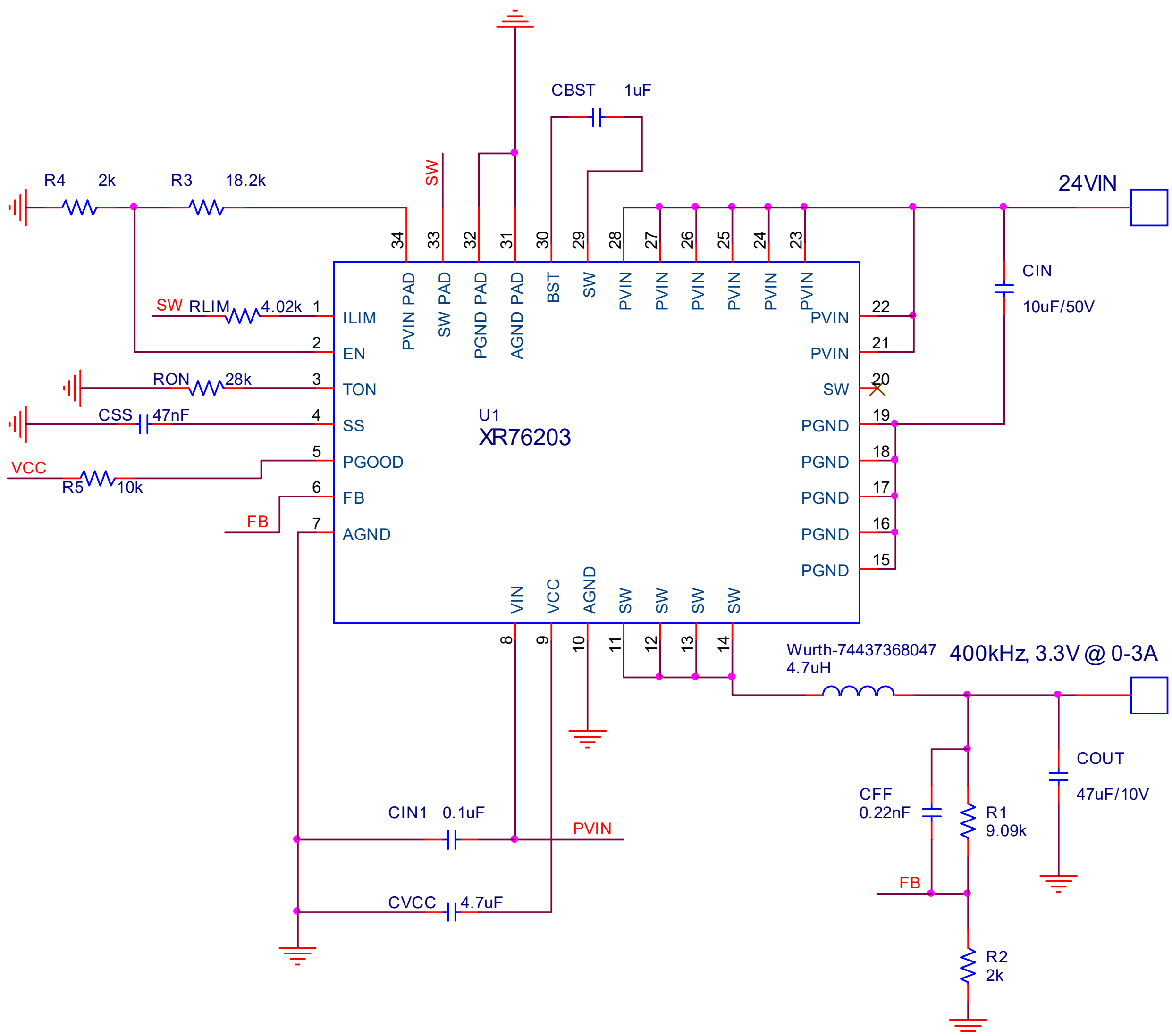
Application Circuit, XR76208



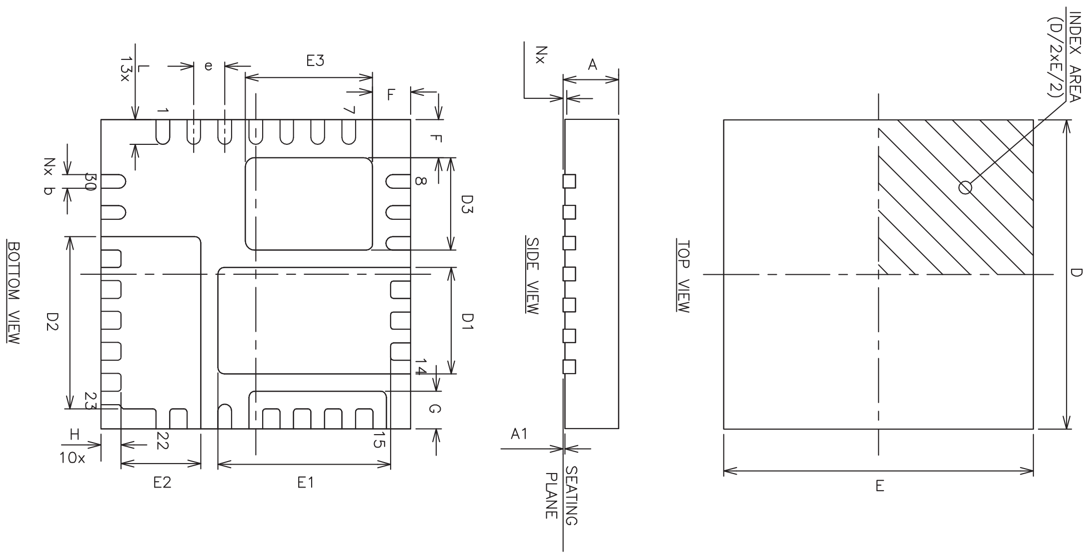
Application Circuit, XR76205

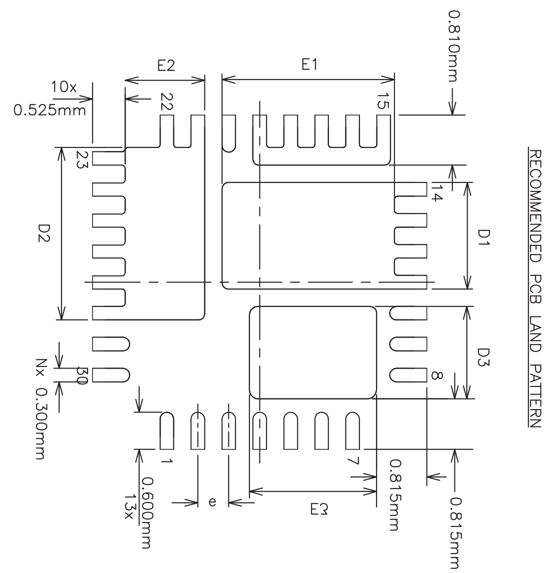


Application Circuit, XR76203



Mechanical Dimensions





30LD 5x5mm QFN 0.50 PITCH						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.800	0.900	1.000	0.031	0.035	0.039
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.180	0.250	0.300	0.007	0.010	0.012
D		5.000 BSC			0.200 BSC	
E		5.000 BSC			0.200 BSC	
e		0.500 BSC			0.020 BSC	
F		0.615 REF			0.024 REF	
G		0.610 REF			0.024 REF	
H		0.325 REF			0.013 REF	
D1	1.570	1.720	1.820	0.062	0.068	0.072
E1	2.635	2.785	2.885	0.104	0.110	0.113
D2	2.635	2.785	2.885	0.104	0.110	0.113
E2	1.135	1.285	1.385	0.045	0.050	0.054
D3	1.345	1.495	1.595	0.053	0.059	0.063
E3	1.903	2.053	2.153	0.075	0.081	0.085
L	0.300	0.400	0.500	0.012	0.016	0.020
N		30			30	

Drawing No: POD-00000018
Revision: A

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR76208EL-F	-40°C to +125°C	Yes[2]	5x5mm QFN	Tray
XR76208ELTR-F				Tape and Reel
XR76208ELMTR-F				Mini Tape and Reel
XR76208EVB	XR76208 Evaluation Board			
XR76205EL-F	-40°C to +125°C	Yes[2]	5x5mm QFN	Tray
XR76205ELTR-F				Tape and Reel
XR76205ELMTR-F				Mini Tape and Reel
XR76205EVB	XR76205 Evaluation Board			
XR76203EL-F	-40°C to +125°C	Yes[2]	5x5mm QFN	Tray
XR76203ELTR-F				Tape and Reel
XR76203ELMTR-F				Mini Tape and Reel
XR76203EVB	XR76203 Evaluation Board			

NOTES:
1. Refer to www.exar.com/XR76203, www.exar.com/XR76205, www.exar.com/XR76208 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	February 2015	Initial release
1B	June 2018	Update to MaxLinear logo. Update format and Ordering Information table.

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