**Figure 2. Block Diagram**

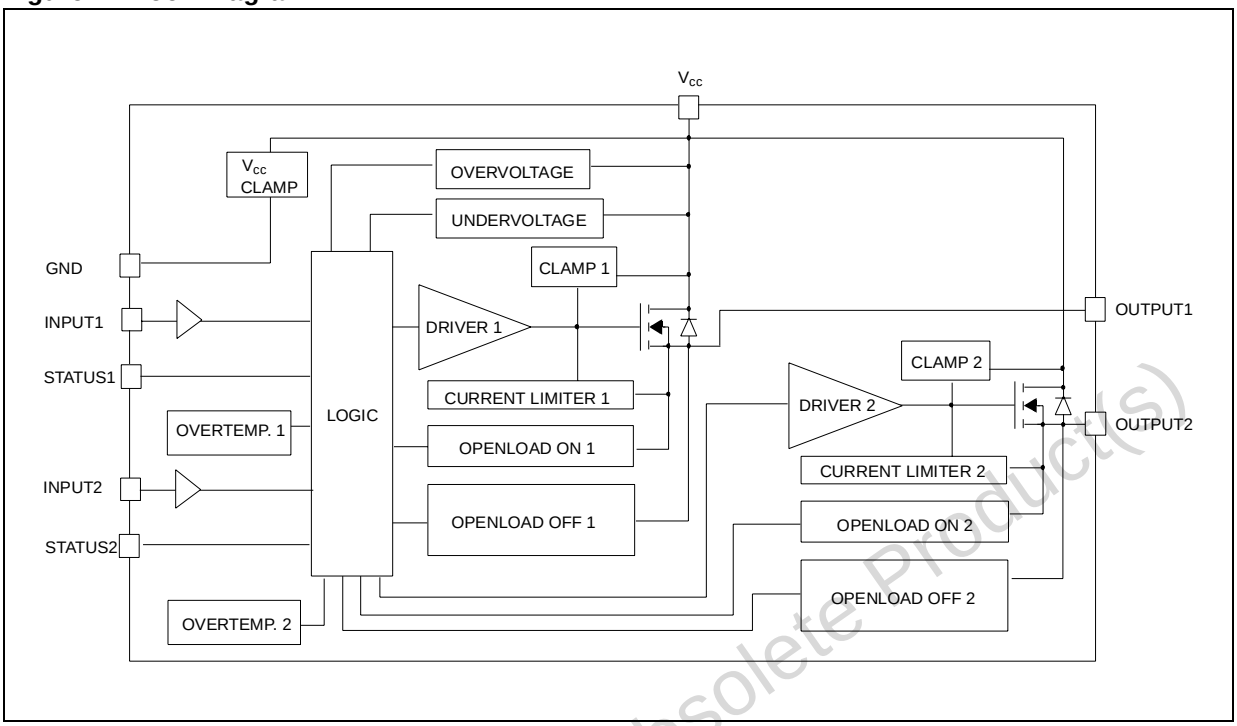


**Table 3. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | 41 | V |
| - $V_{CC}$ | Reverse DC Supply Voltage | - 0.3 | V |
| - $I_{GND}$ | DC Reverse Ground Pin Current | - 200 | mA |
| $I_{OUT}$ | DC Output Current | Internally Limited | A |
| - $I_{OUT}$ | Reverse DC Output Current | - 6 | A |
| $I_{IN}$ | DC Input Current | +/- 10 | mA |
| $I_{stat}$ | DC Status Current | +/- 10 | mA |
| $V_{ESD}$ | Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)<br>- INPUT<br>- STATUS<br>- OUTPUT<br>- $V_{CC}$ | <br>4000<br>4000<br>5000<br>5000 | <br>V<br>V<br>V<br>V |
| $E_{MAX}$ | Maximum Switching Energy (L=1.5mH; $R_L$=0Ω; $V_{bat}$=13.5V; $T_{jstart}$=150ºC; $I_L$=5A) | 26 | mJ |
| $P_{tot}$ | Power Dissipation $T_C$=25°C | 8.3 | W |
| $T_j$ | Junction Operating Temperature | Internally Limited | °C |
| $T_c$ | Case Operating Temperature | - 40 to 150 | °C |
| $T_{stg}$ | Storage Temperature | - 55 to 150 | °C |

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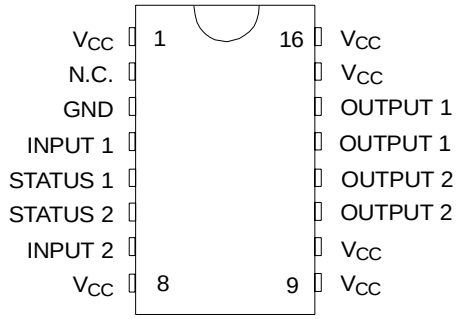
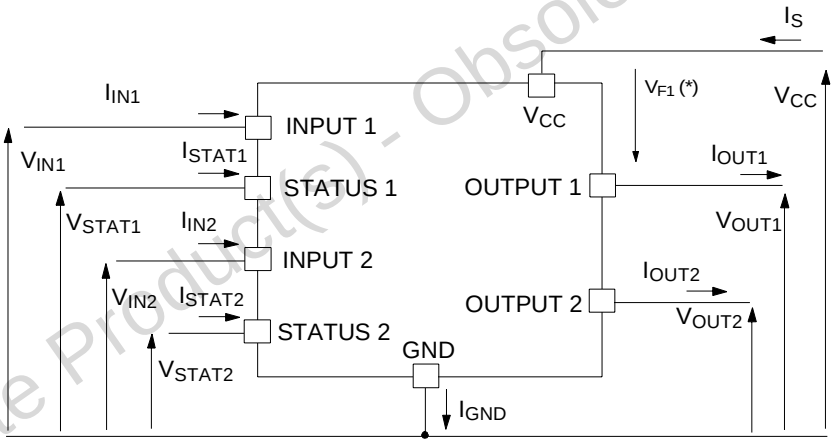
**Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins**




| Connection / Pin | Status | N.C. | Output | Input |
|---|---|---|---|---|
| Floating | X | X | X | X |
| To Ground | | X | | Through 10KΩ resistor |

**Figure 4. Current and Voltage Conventions**




(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

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**Table 4. Thermal Data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}lead}$ | Thermal Resistance Junction-lead | 15 | | °C/W |
| $R_{thj\text{-}amb}$ | Thermal Resistance Junction-ambient | 77 (1) | 57 (2) | °C/W |

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm$^2$ of Cu (at least 35µm thick) connected to all $V_{CC}$ pins. Horizontal mounting and no artificial air flow.

Note: 2. When mounted on a standard single-sided FR-4 board with 4cm$^2$ of Cu (at least 35µm thick) connected to all $V_{CC}$ pins. Horizontal mounting and no artificial air flow.



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## ELECTRICAL CHARACTERISTICS

(8V<$V_{CC}$<36V; -40°C < $T_j$ <150°C, unless otherwise specified)
(Per each channel)

### Table 5. Power Output

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ (**) | Operating Supply Voltage | | 5.5 | 13 | 36 | V |
| $V_{USD}$ (**) | Undervoltage Shut-down | | 3 | 4 | 5.5 | V |
| $V_{OV}$ (**) | Overvoltage Shut-down | | 36 | | | V |
| $R_{ON}$ | On State Resistance | $I_{OUT}$=1A; $T_j$=25°C<br>$I_{OUT}$=1A; $V_{CC}$>8V | | | 160<br>320 | mΩ<br>mΩ |
| $I_S$ (**) | Supply Current | Off State; $V_{CC}$=13V; $V_{IN}$=$V_{OUT}$=0V<br>Off State; $V_{CC}$=13V; $V_{IN}$=$V_{OUT}$=0V; $T_j$=25°C<br>On State; $V_{CC}$=13V; $V_{IN}$=5V; $I_{OUT}$=0A | | 12<br>12<br>5 | 40<br>25<br>7 | µA<br>µA<br>mA |
| $I_{L(off1)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V | 0 | | 50 | µA |
| $I_{L(off2)}$ | Off State Output Current | $V_{IN}$=0V; $V_{OUT}$=3.5V | -75 | | 0 | µA |
| $I_{L(off3)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13V; $T_j$ =125°C | | | 5 | µA |
| $I_{L(off4)}$ | Off State Output Current | $V_{IN}$=$V_{OUT}$=0V; $V_{CC}$=13V; $T_j$ =25°C | | | 3 | µA |

Note: (**) Per device.

### Table 6. Protection (see note 1)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{TSD}$ | Shut-down Temperature | | 150 | 175 | 200 | °C |
| $T_R$ | Reset Temperature | | 135 | | | °C |
| $T_{hyst}$ | Thermal Hysteresis | | 7 | 15 | | °C |
| $t_{SDL}$ | Status Delay in Overload Conditions | $T_j$>$T_{TSD}$ | | | 20 | µs |
| $I_{lim}$ | Current limitation | <br>5.5V<$V_{CC}$<36V | 3.5 | 5 | 7.5<br>7.5 | A<br>A |
| $V_{demag}$ | Turn-off Output Clamp Voltage | $I_{OUT}$=1A; L=6mH | $V_{CC}$-41 | $V_{CC}$-48 | $V_{CC}$-55 | V |

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

### Table 7. $V_{CC}$ - Output Diode

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_F$ | Forward on Voltage | -$I_{OUT}$=0.5A; $T_j$=150°C | | | 0.6 | V |

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## ELECTRICAL CHARACTERISTICS (continued)

### Table 8. Status Pin

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{STAT}$ | Status Low Output Voltage | $I_{STAT}$= 1.6 mA | | | 0.5 | V |
| $I_{LSTAT}$ | Status Leakage Current | Normal Operation; $V_{STAT}$= 5V | | | 10 | µA |
| $C_{STAT}$ | Status Pin Input Capacitance | Normal Operation; $V_{STAT}$= 5V | | | 100 | pF |
| $V_{SCL}$ | Status Clamp Voltage | $I_{STAT}$= 1mA<br>$I_{STAT}$= - 1mA | 6 | 6.8<br>-0.7 | 8 | V<br>V |

### Table 9. Switching ($V_{CC}$=13V)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on Delay Time | $R_L$=13Ω from $V_{IN}$ rising edge to $V_{OUT}$=1.3V | | 30 | | µs |
| $t_{d(off)}$ | Turn-off Delay Time | $R_L$=13Ω from $V_{IN}$ falling edge to $V_{OUT}$=11.7V | | 30 | | µs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on Voltage Slope | $R_L$=13Ω from $V_{OUT}$=1.3V to $V_{OUT}$=10.4V | | See relative diagram | | V/µs |
| $dV_{OUT}/dt_{(off)}$ | Turn-off Voltage Slope | $R_L$=13Ω from $V_{OUT}$=11.7V to $V_{OUT}$=1.3V | | See relative diagram | | V/µs |

### Table 10. Openload Detection

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OL}$ | Openload ON State Detection Threshold | $V_{IN}$=5V | 20 | 40 | 80 | mA |
| $t_{DOL(on)}$ | Openload ON State Detection Delay | $I_{OUT}$=0A | | | 200 | µs |
| $V_{OL}$ | Openload OFF State Voltage Detection Threshold | $V_{IN}$=0V | 1.5 | 2.5 | 3.5 | V |
| $t_{DOL(off)}$ | Openload Detection Delay at Turn Off | | | | 1000 | µs |

### Table 11. Logic Input

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Level | | | | 1.25 | V |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 1.25V | 1 | | | µA |
| $V_{IH}$ | Input High Level | | 3.25 | | | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = 3.25V | | | 10 | µA |
| $V_{I(hyst)}$ | Input Hysteresis Voltage | | 0.5 | | | V |
| $V_{ICL}$ | Input Clamp Voltage | $I_{IN}$ = 1mA<br>$I_{IN}$ = -1mA | 6 | 6.8<br>-0.7 | 8 | V<br>V |

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**Figure 5.**

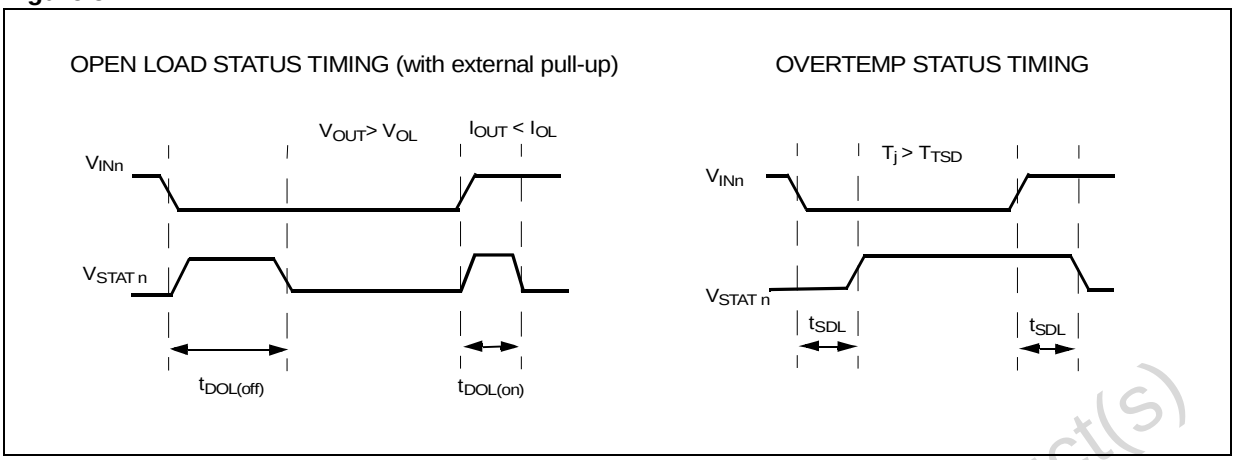


**Table 12. Truth Table**

| CONDITIONS | INPUT | OUTPUT | SENSE |
|---|---|---|---|
| Normal Operation | L<br>H | L<br>H | H<br>H |
| Current Limitation | L<br>H<br>H | L<br>X<br>X | H<br>($T_j < T_{TSD}$) H<br>($T_j > T_{TSD}$) L |
| Overtemperature | L<br>H | L<br>L | H<br>L |
| Undervoltage | L<br>H | L<br>L | X<br>X |
| Overvoltage | L<br>H | L<br>L | H<br>H |
| Output Voltage > $V_{OL}$ | L<br>H | H<br>H | L<br>H |
| Output Current < $I_{OL}$ | L<br>H | L<br>H | H<br>L |

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**Figure 6. Switching Time Waveforms**

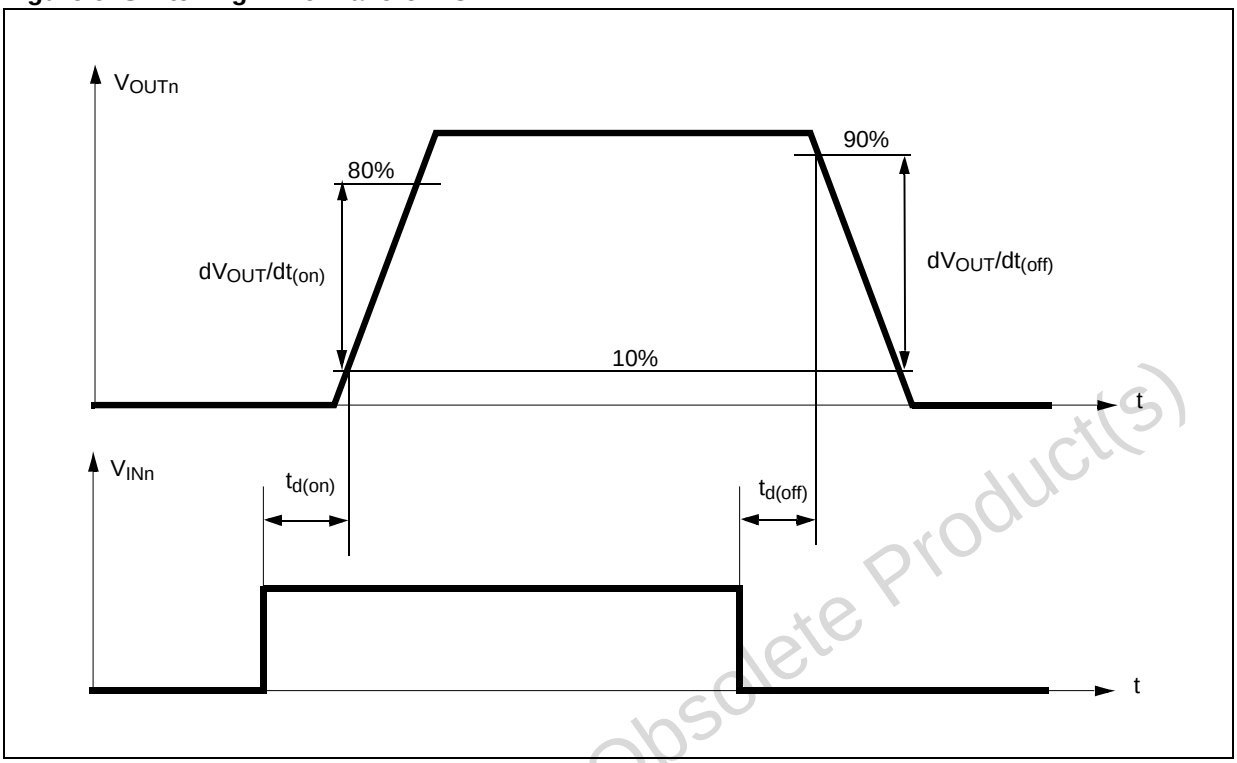


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**Table 13. Electrical Transient Requirements On $V_{CC}$ Pin**

| ISO T/R 7637/1 Test Pulse | TEST LEVELS | | | | |
|---|---|---|---|---|---|
| | I | II | III | IV | Delays and Impedance |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 µs 50 Ω |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 µs 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |
| 5 | +26.5 V | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 Ω |

| ISO T/R 7637/1 Test Pulse | TEST LEVELS RESULTS | | | |
|---|---|---|---|---|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

| CLASS | CONTENTS |
|---|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device. |



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**Figure 7. Waveforms**

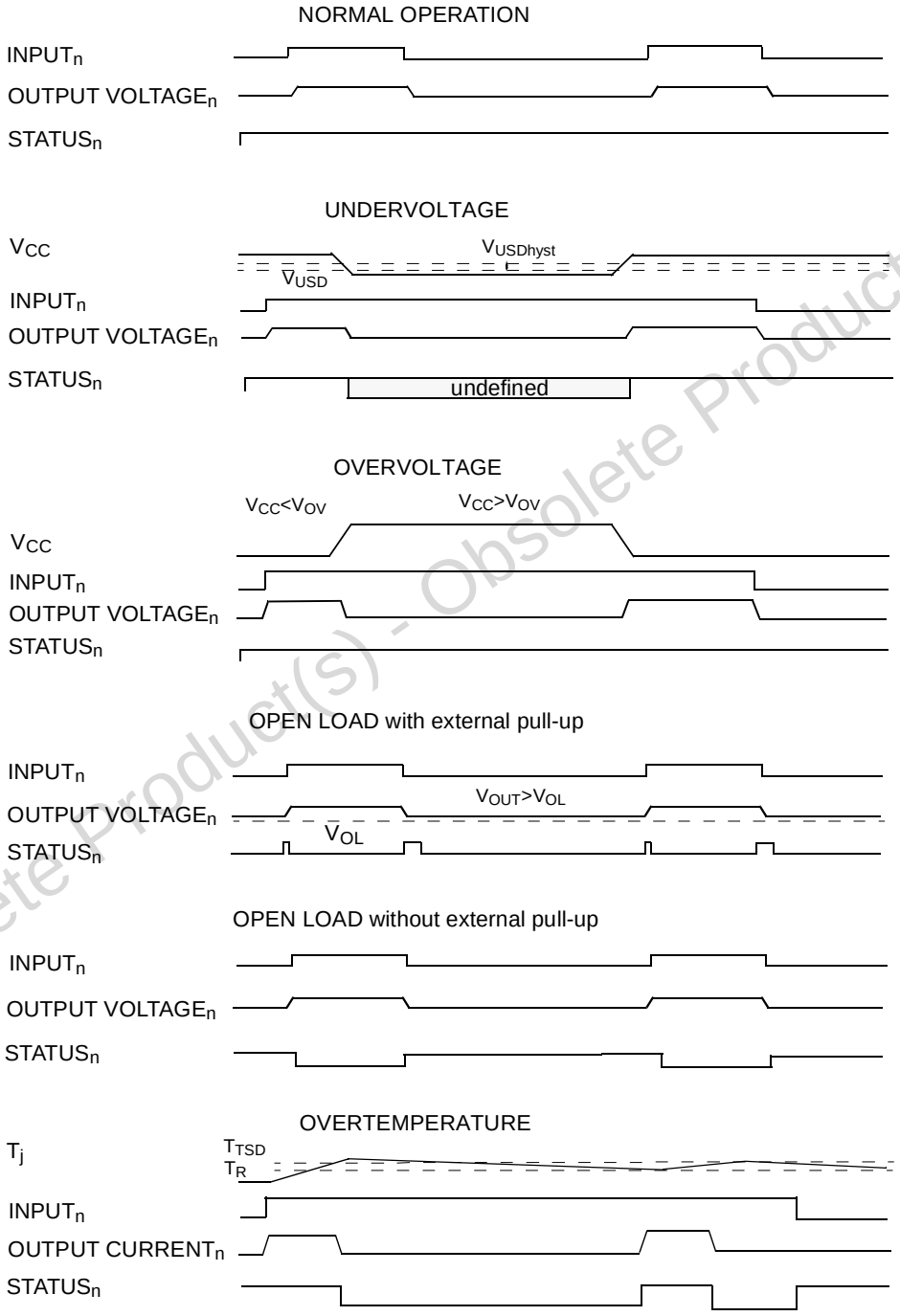


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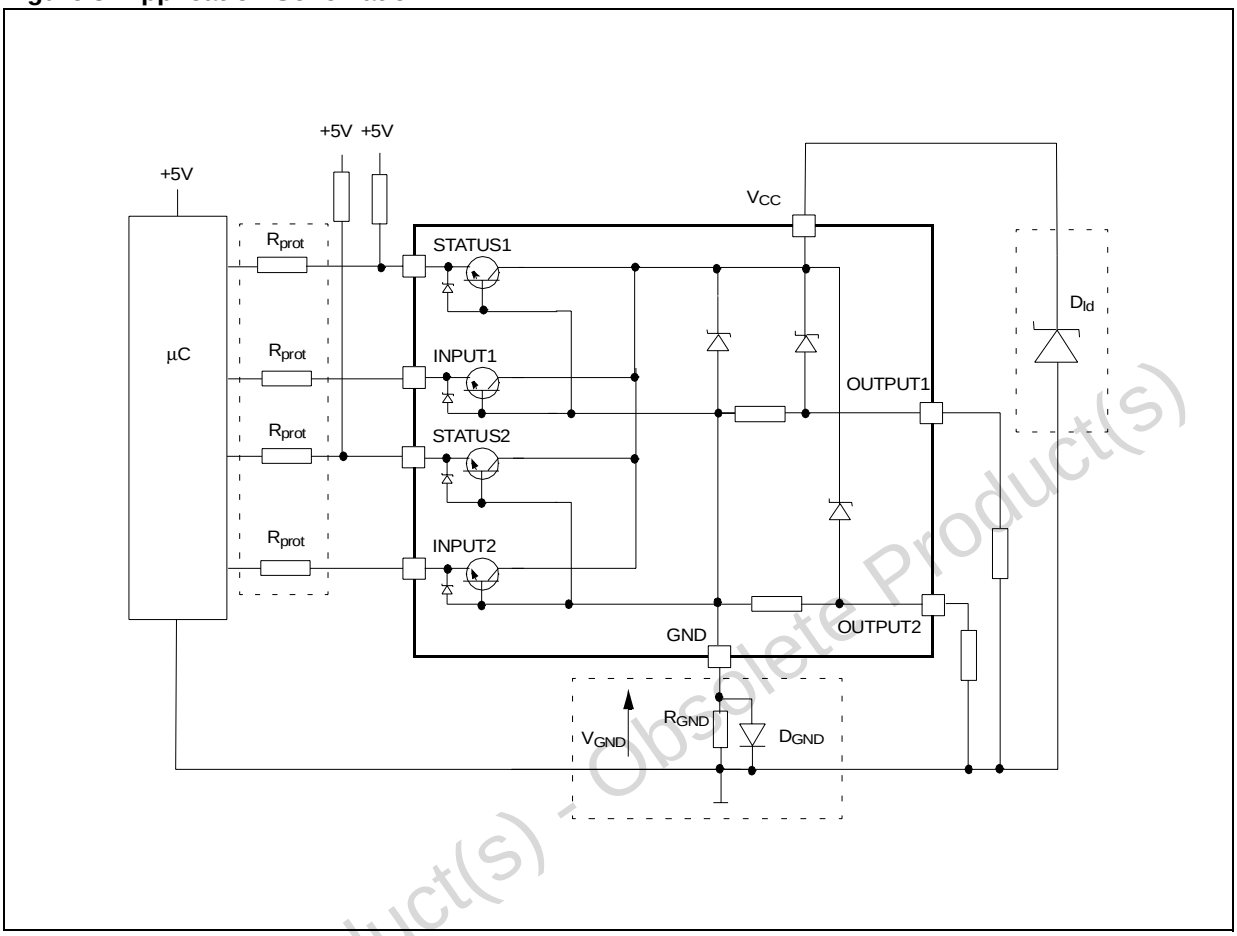
**Figure 8. Application Schematic**

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## GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line ($R_{GND}$ only). This can be used with any type of load.

The following is an indication on how to dimension the $R_{GND}$ resistor.

1) $R_{GND} \leq 600mV / I_{S(on)max}$.
2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in $R_{GND}$ (when $V_{CC}<0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the $R_{GND}$ will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same $R_{GND}$.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode ($D_{GND}$) in the ground line.

A resistor ($R_{GND}$=1kΩ) should be inserted in parallel to $D_{GND}$ if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## LOAD DUMP PROTECTION

$D_{Id}$ is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds $V_{CC}$ max DC rating. The same applies if the device will be subject to transients on the $V_{CC}$ line that are greater than the ones shown in the ISO T/R 7637/1 table.



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## µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the $V_{CC}$ line, the control pins will be pulled negative. ST suggests to insert a resistor ($R_{prot}$) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For $V_{CCpeak}$= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ $R_{prot}$ ≤ 65kΩ.

Recommended $R_{prot}$ value is 10kΩ.

## OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor ($R_{PU}$) connected between OUTPUT pin and a positive supply voltage ($V_{PU}$) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1) no false open load indication when load is connected: in this case we have to avoid $V_{OUT}$ to be higher than $V_{OLmin}$; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{OLmin}$.
2) no misdetection when load is disconnected: in this case the $V_{OUT}$ has to be higher than $V_{OLmax}$; this results in the following condition $R_{PU}<(V_{PU}–V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if $V_{out}$ is pulled high (up to several mA), the pull-up resistor $R_{PU}$ should be connected to a supply that is switched OFF when the module is in standby.

The values of $V_{OLmin}$, $V_{OLmax}$ and $I_{L(off2)}$ are available in the Electrical Characteristics section.

**Figure 9. Open Load detection in off state**

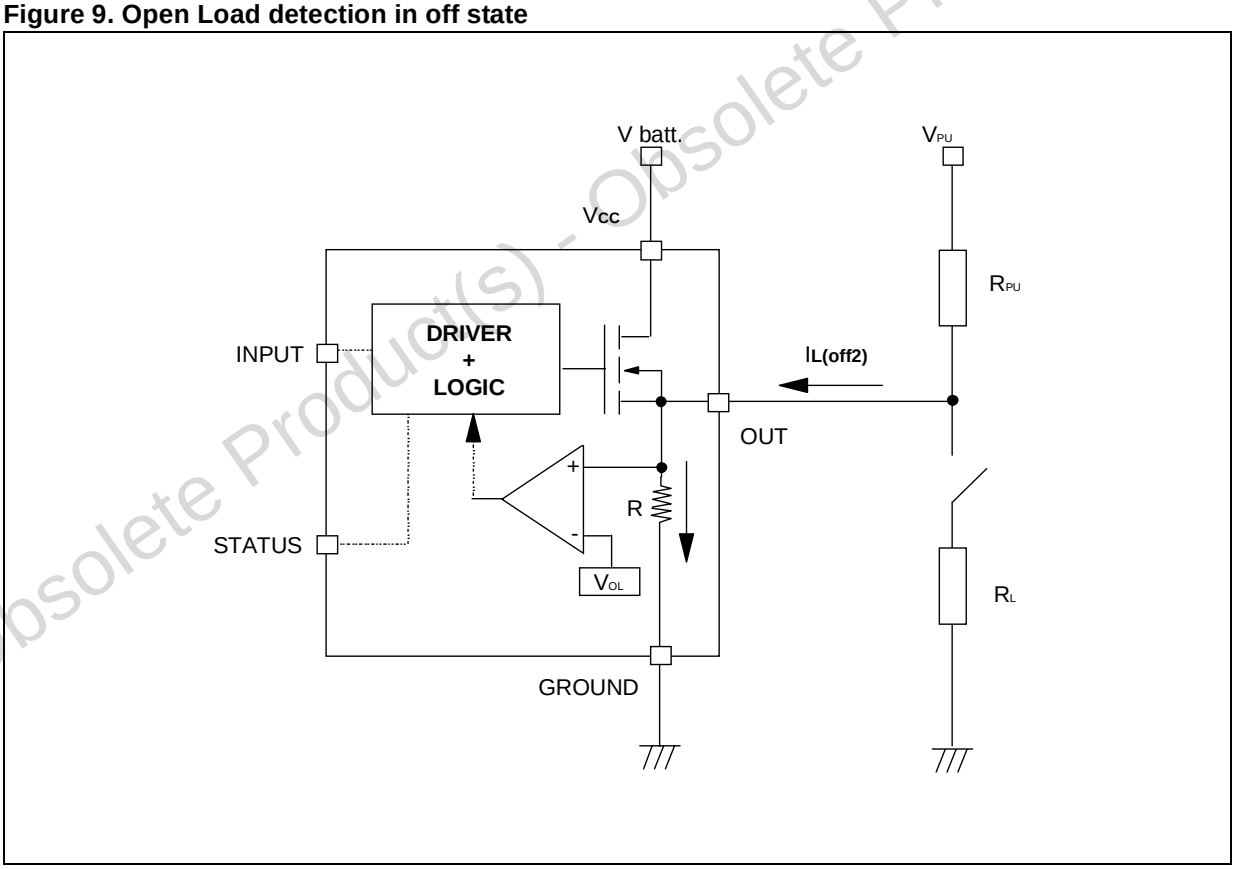


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**Figure 10. Off State Output Current**

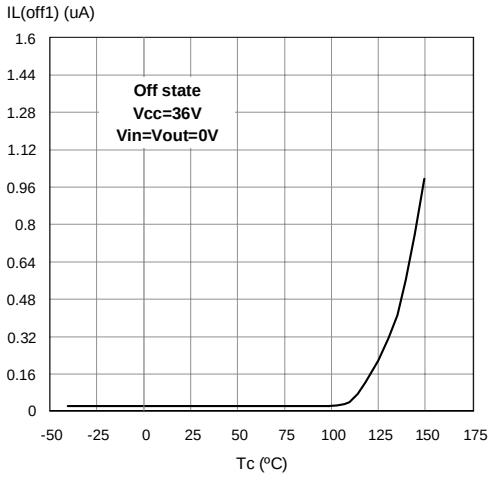


**Figure 11. Input Clamp Voltage**

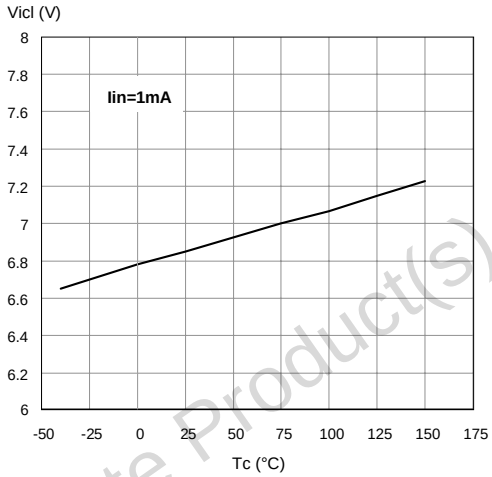


**Figure 12. Status Low Output Voltage**

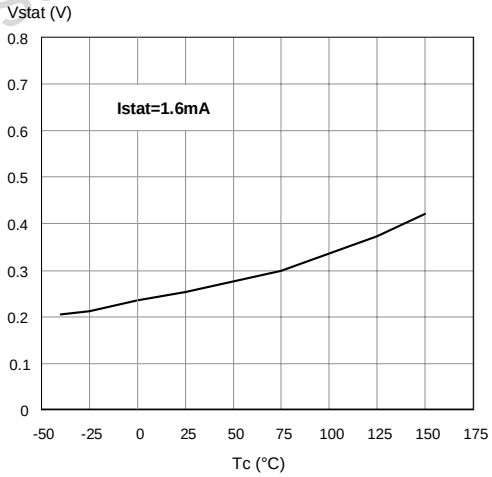


**Figure 13. High Level Input Current**

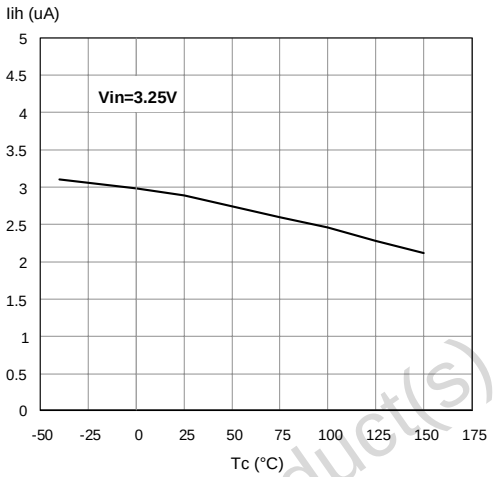


**Figure 14. Status Leakage Current**

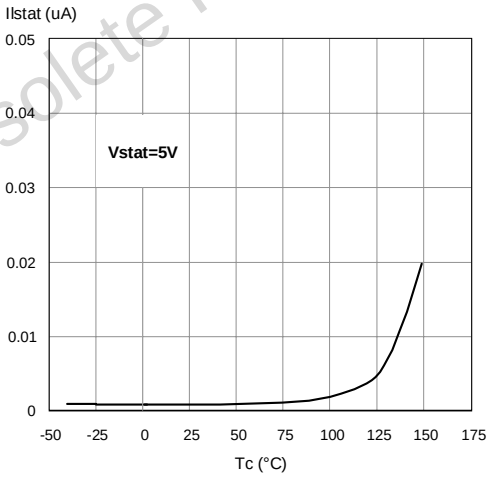


**Figure 15. Status Clamp Voltage**

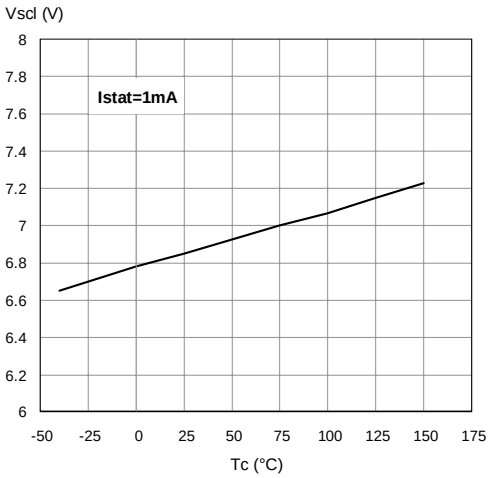


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**Figure 16. On State Resistance Vs $T_{case}$**

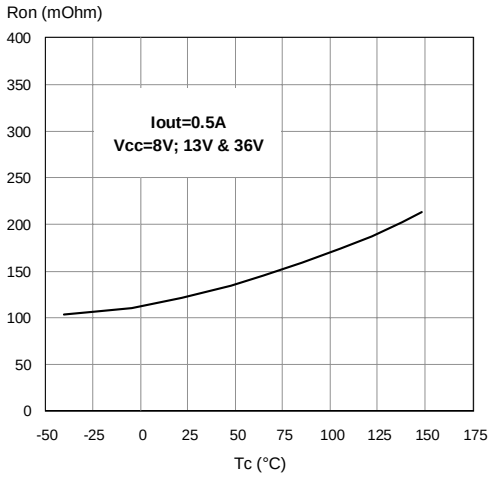


**Figure 17. Openload On State Detection Threshold**

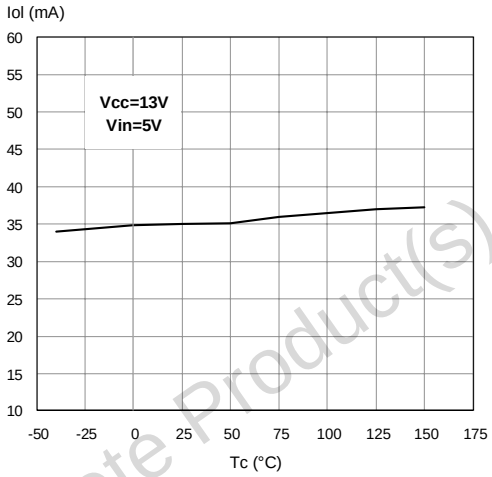


**Figure 18. Input High Level**

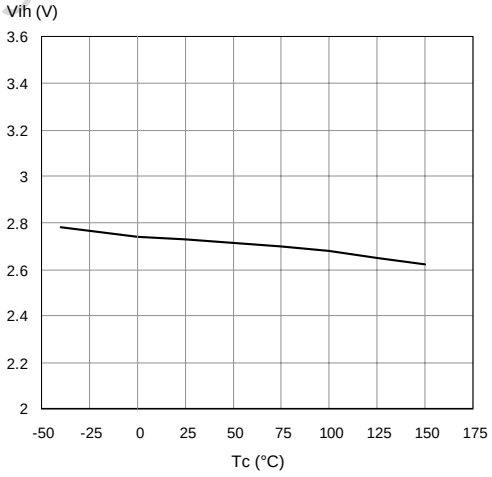


**Figure 19. On State Resistance Vs $V_{CC}$**

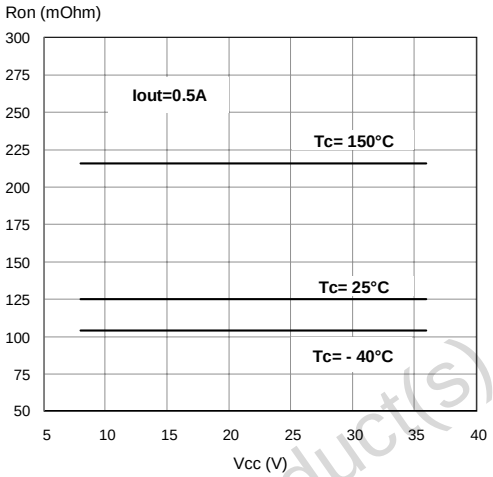


**Figure 20. Openload Off State Detection Threshold**

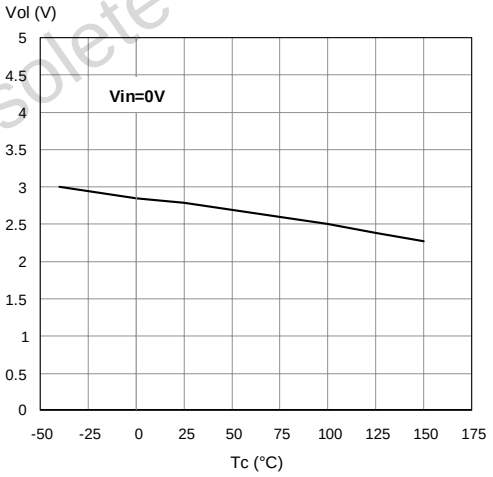


**Figure 21. Input Low Level**

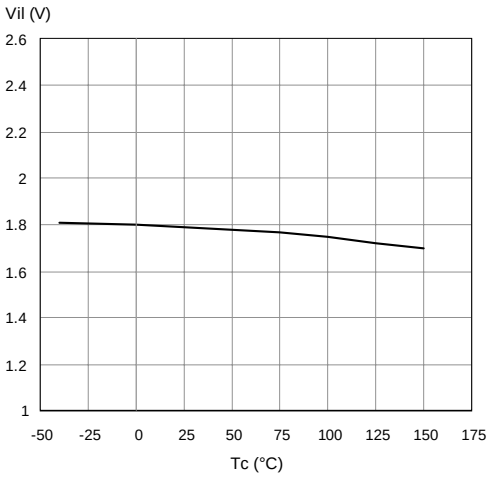


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**Figure 22. Input Hysteresis Voltage**

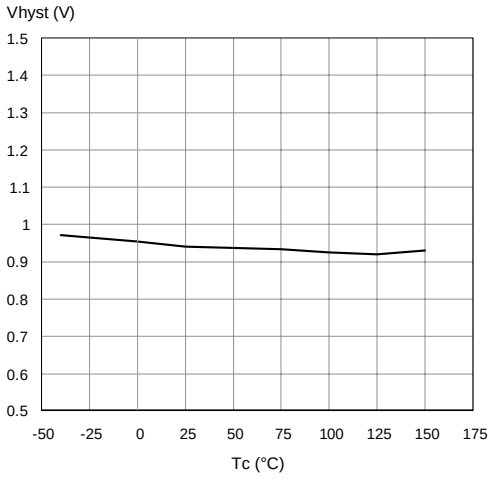


**Figure 23. Turn-on Voltage Slope**

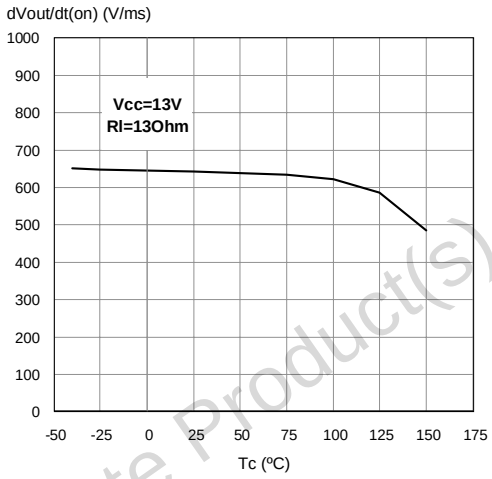


**Figure 24. $I_{LIM}$ Vs $T_{case}$**

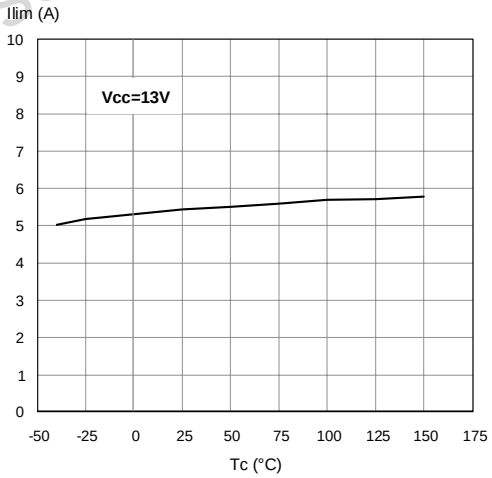


**Figure 25. Overvoltage Shutdown**

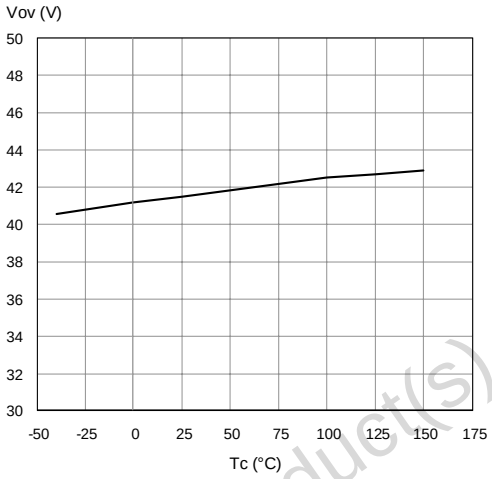


**Figure 26. Turn-off Voltage Slope**

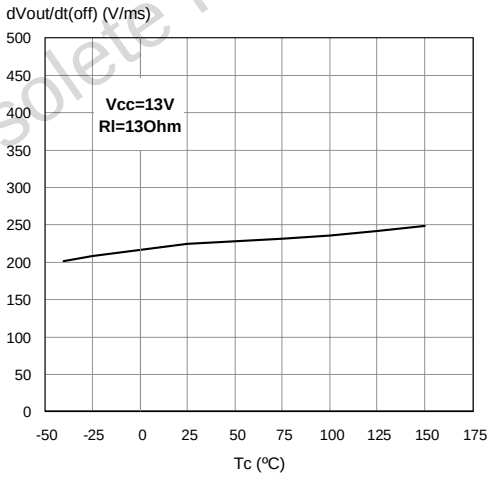


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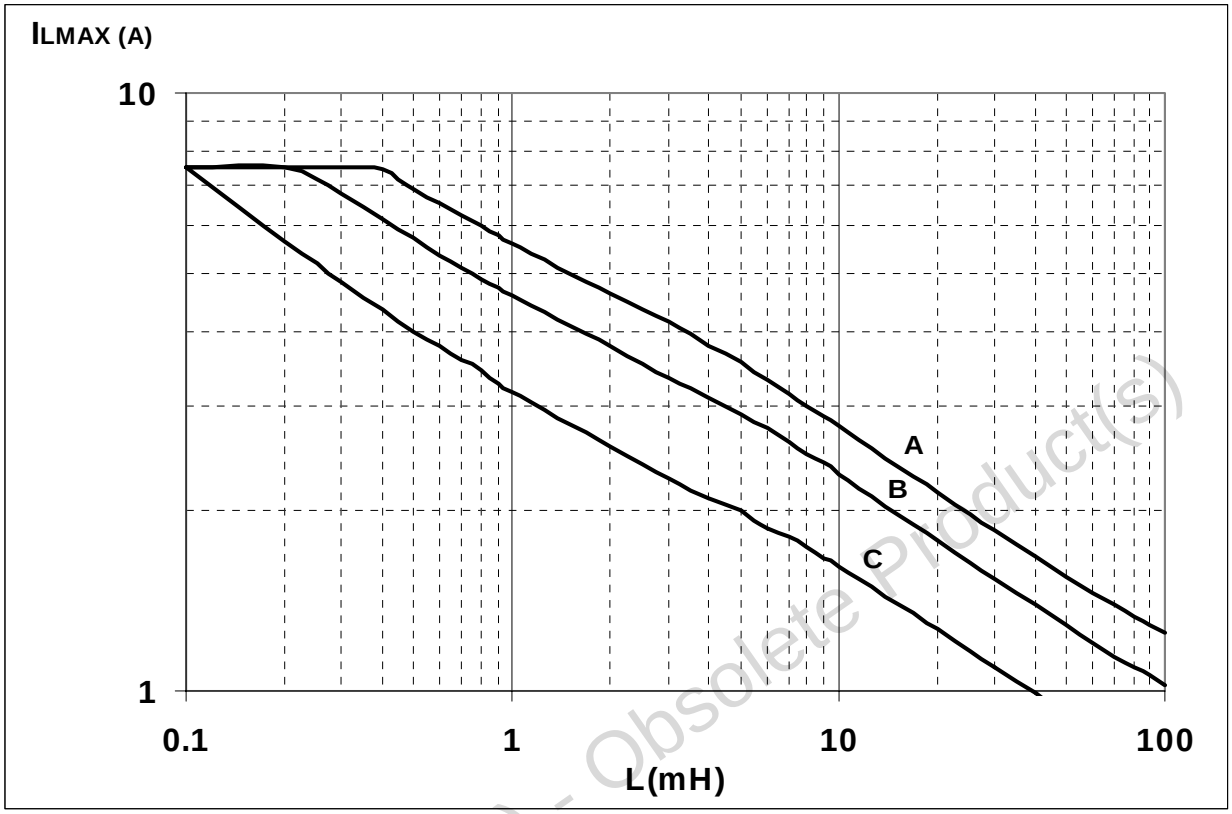
**Figure 27. Maximum turn off current versus load inductance**




A = Single Pulse at $T_{Jstart}$=150ºC
B= Repetitive pulse at $T_{Jstart}$=100ºC
C= Repetitive Pulse at $T_{Jstart}$=125ºC

Conditions:
$V_{CC}$=13.5V

Values are generated with $R_L$=0Ω

In case of repetitive pulses, $T_{jstart}$ (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

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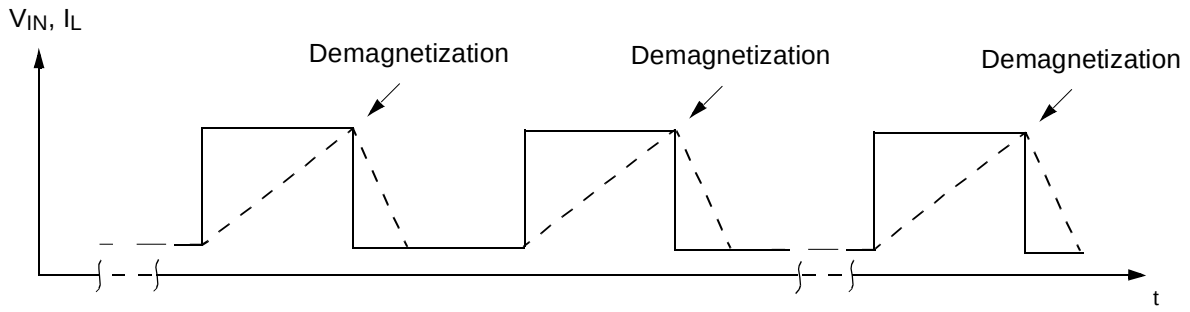




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## PowerSO-10™ Thermal Data

**Figure 28. SO-16 PC Board**

Layout condition of $R_{th}$ and $Z_{th}$ measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=1.6mm, Cu thickness=35µm, Copper areas: 0.26cm$^2$, 4cm$^2$).

**Figure 29. $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition**

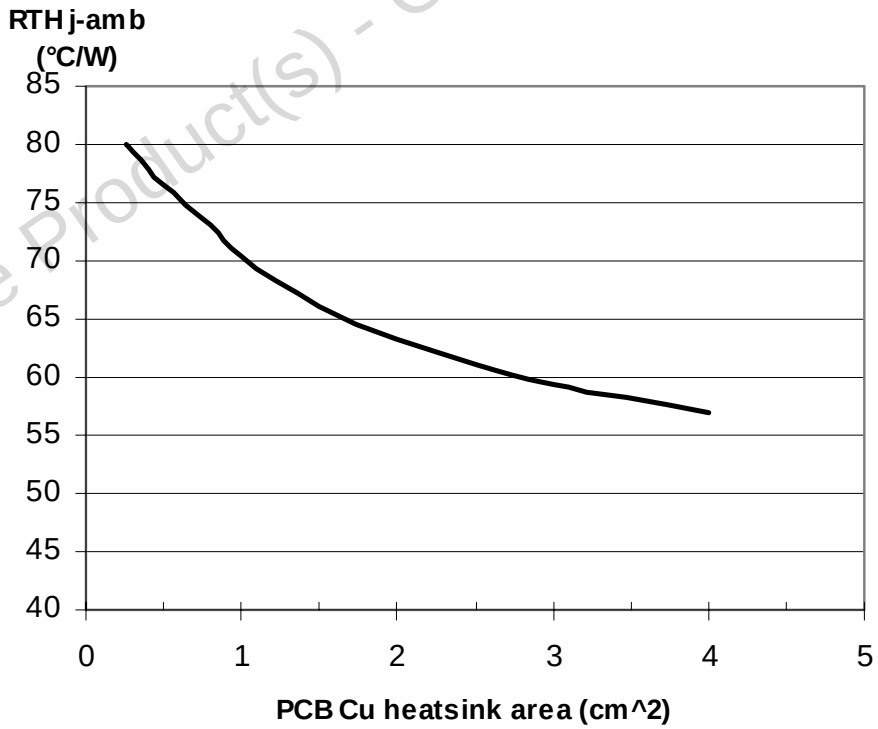


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**Figure 30. SO-16 Thermal Impedance Junction Ambient Single Pulse**

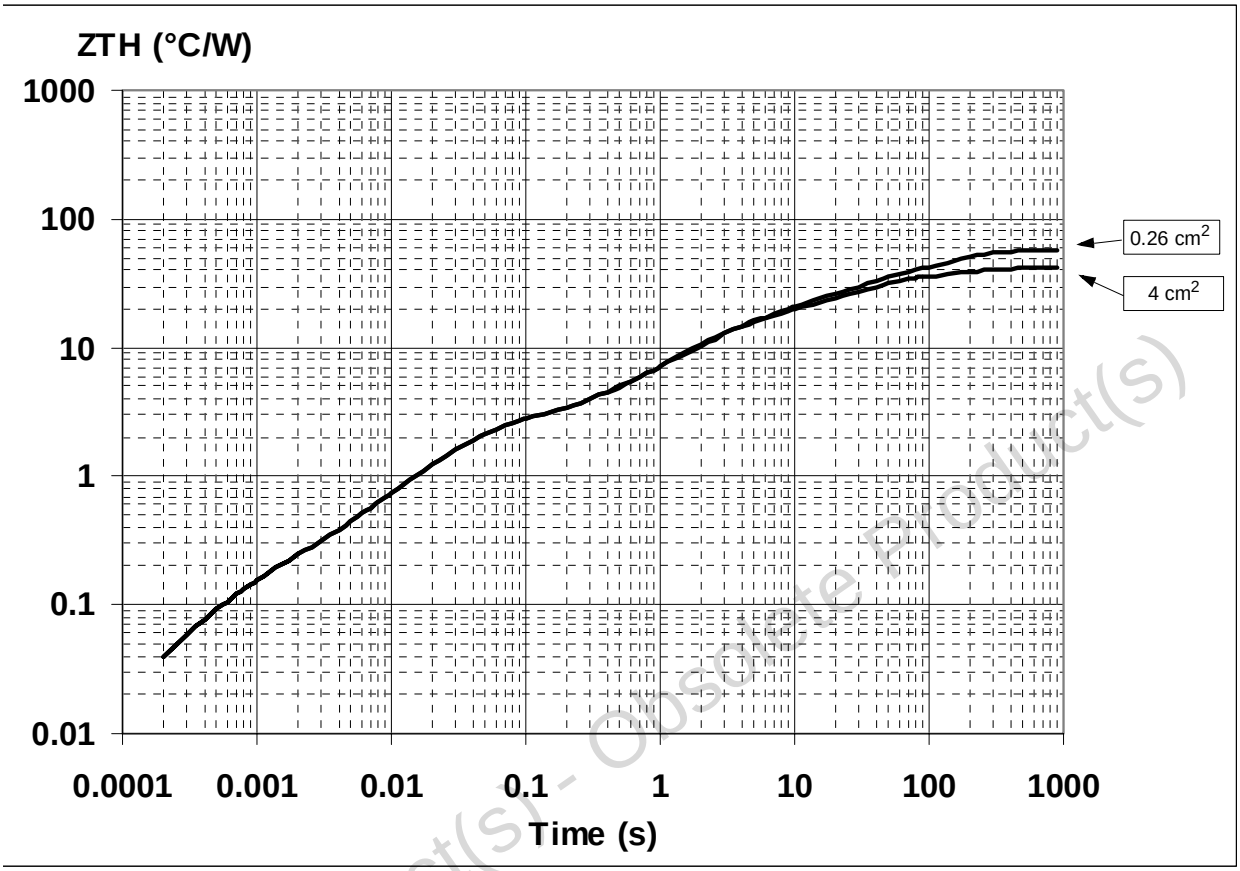


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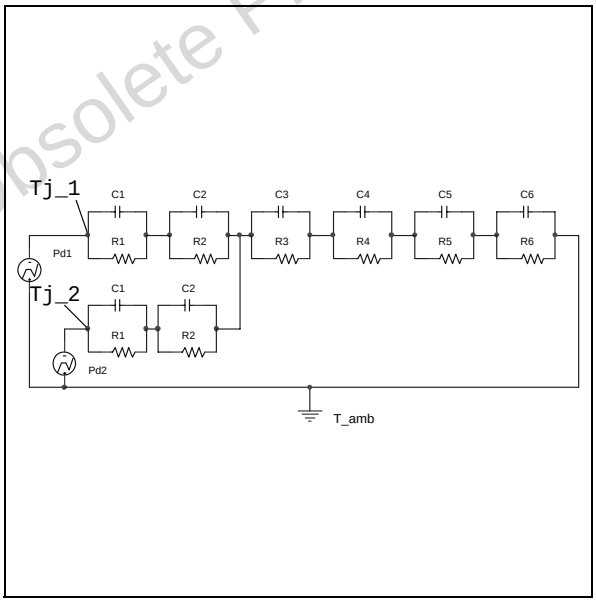
**Figure 31. Thermal fitting model of a double channel HSD in SO-16**




**Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

**Table 14. Thermal Parameter**

| Area/island ($cm^2$) | 0.5 | 4 |
|---|---|---|
| R1 (°C/W) | 0.35 | |
| R2 (°C/W) | 1.8 | |
| R3 ( °C/W) | 4.5 | |
| R4 (°C/W) | 10 | |
| R5 (°C/W) | 16 | |
| R6 (°C/W) | 48 | 25 |
| C1 (W.s/°C) | 0.0001 | |
| C2 (W.s/°C) | 7.00E-04 | |
| C3 (W.s/°C) | 6.00E-03 | |
| C4 (W.s/°C) | 0.2 | |
| C5 (W.s/°C) | 0.7 | |
| C6 (W.s/°C) | 2 | 4 |



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## PACKAGE MECHANICAL

**Table 15. SO-16 Mechanical Data**

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | | | 1.75 |
| a1 | 0.1 | | 0.2 |
| a2 | | | 1.65 |
| b | 0.35 | | 0.46 |
| b1 | 0.19 | | 0..25 |
| C | | 0.5 | |
| c1 | | 45° (typ.) | |
| D | 9.8 | | 10 |
| E | 5.8 | | 6.2 |
| e | | 1.27 | |
| e3 | | 8.89 | |
| F | 3.8 | | 4.0 |
| G | 4.6 | | 5.3 |
| L | 0.5 | | 1.27 |
| M | | | 0.62 |
| S | | 8° (max.) | |

**Figure 32. SO-16 Package Dimensions**

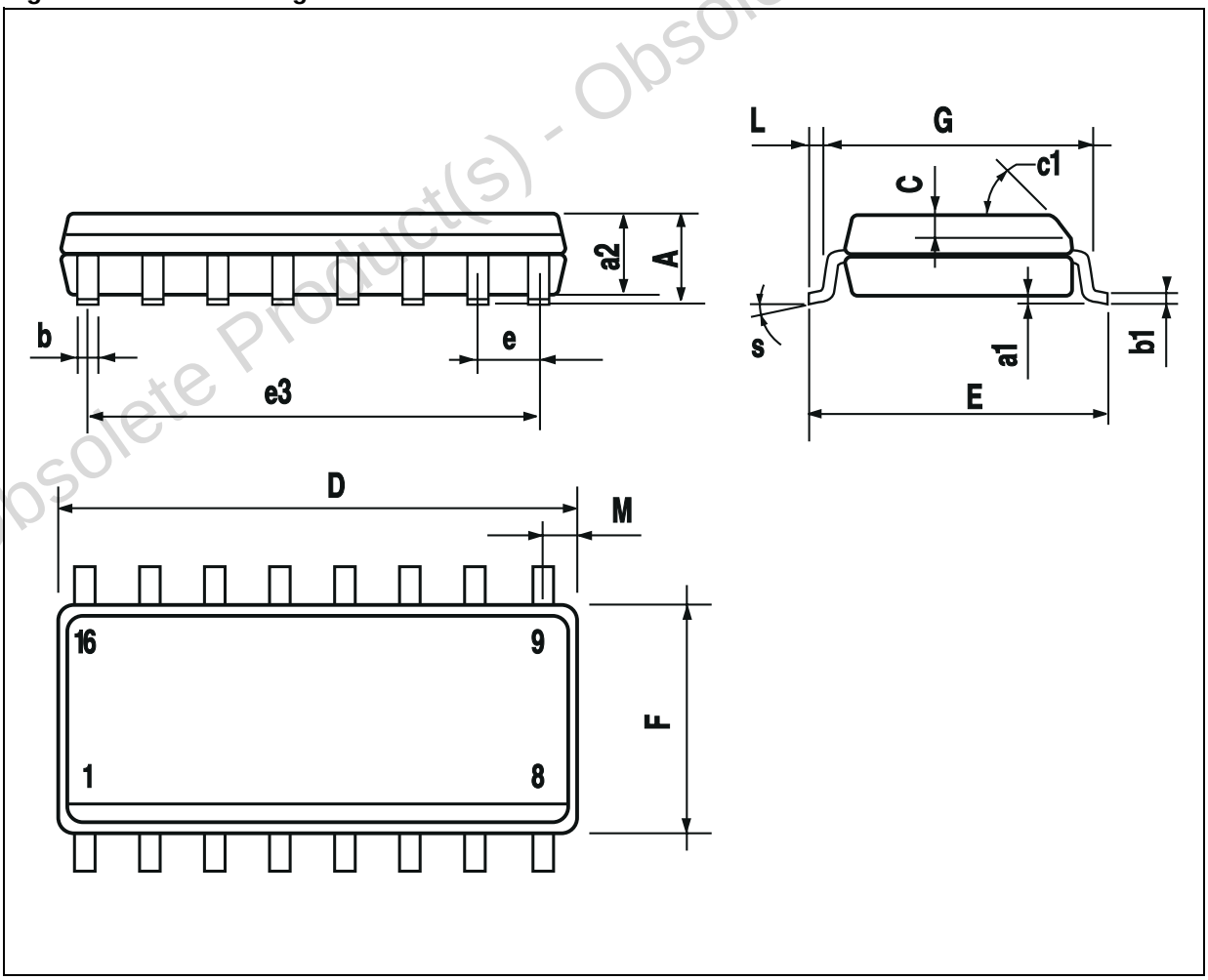


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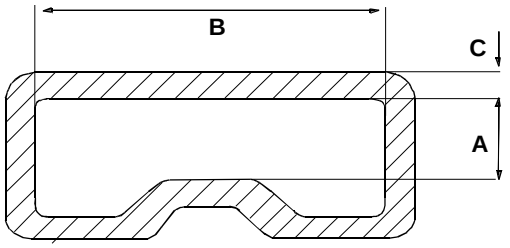
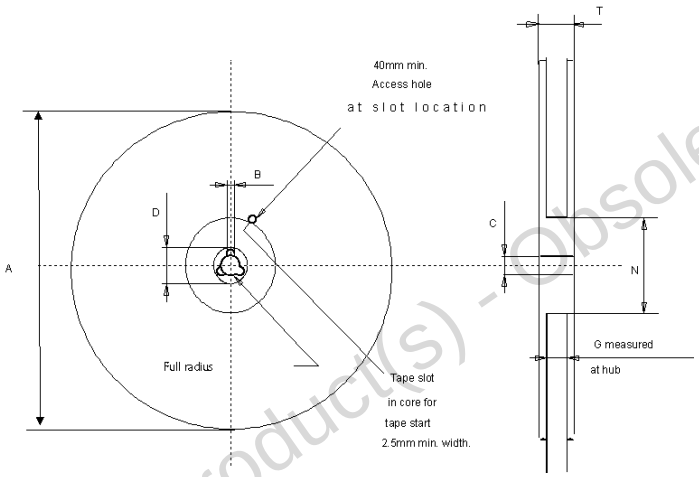
**Figure 33. SO-16 Suggested Pad Layout And Tube Shipment (no suffix)**




| | |
|---|---|
| **Base Q.ty** | 50 |
| **Bulk Q.ty** | 1000 |
| **Tube length (± 0.5)** | 532 |
| **A** | 3.2 |
| **B** | 6 |
| **C (± 0.1)** | 0.6 |

All dimensions are in mm.

**Figure 34. Tape And Reel Shipment (suffix "TR")**




**REEL DIMENSIONS**

.All dimensions are in mm.

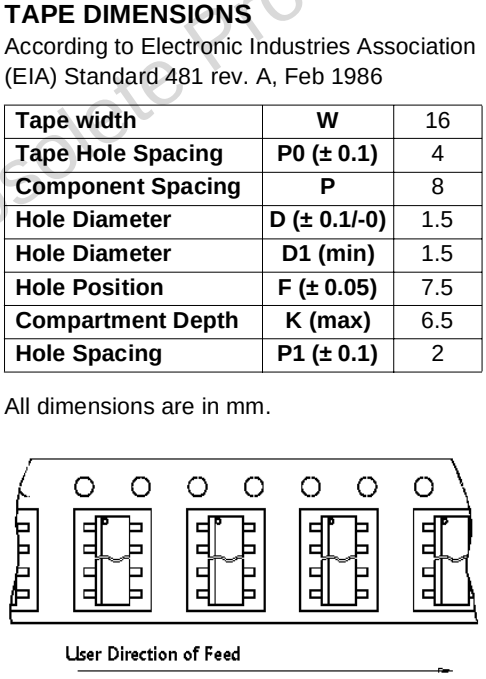
| | |
|---|---|
| **Base Q.ty** | 1000 |
| **Bulk Q.ty** | 1000 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (± 0.2)** | 13 |
| **F** | 20.2 |
| **G (+ 2 / -0)** | 16.4 |
| **N (min)** | 60 |
| **T (max)** | 22.4 |

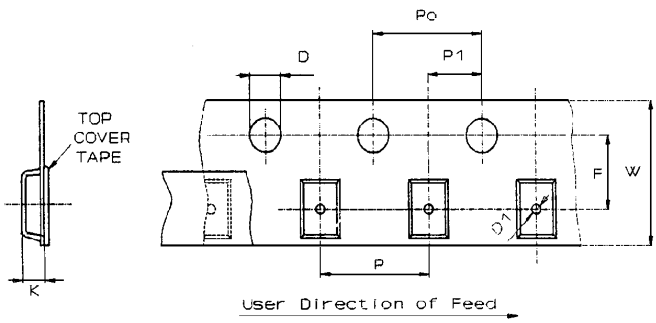
**TAPE DIMENSIONS**

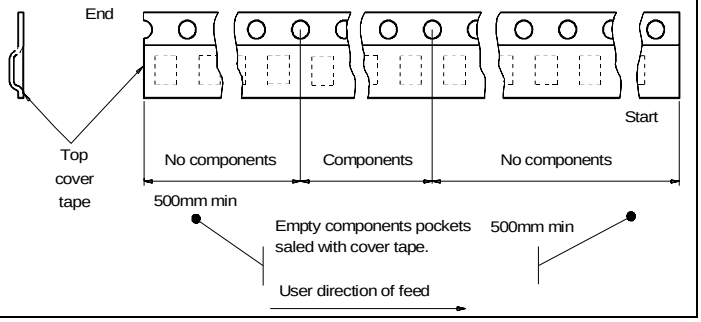
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

| | | |
|---|---|---|
| **Tape width** | **W** | 16 |
| **Tape Hole Spacing** | **P0 (± 0.1)** | 4 |
| **Component Spacing** | **P** | 8 |
| **Hole Diameter** | **D (± 0.1/-0)** | 1.5 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (± 0.05)** | 7.5 |
| **Compartment Depth** | **K (max)** | 6.5 |
| **Hole Spacing** | **P1 (± 0.1)** | 2 |

All dimensions are in mm.

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## REVISION HISTORY

| Date | Revision | Description of Changes |
|---|---|---|
| Oct. 2004 | 1 | - First Issue |

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