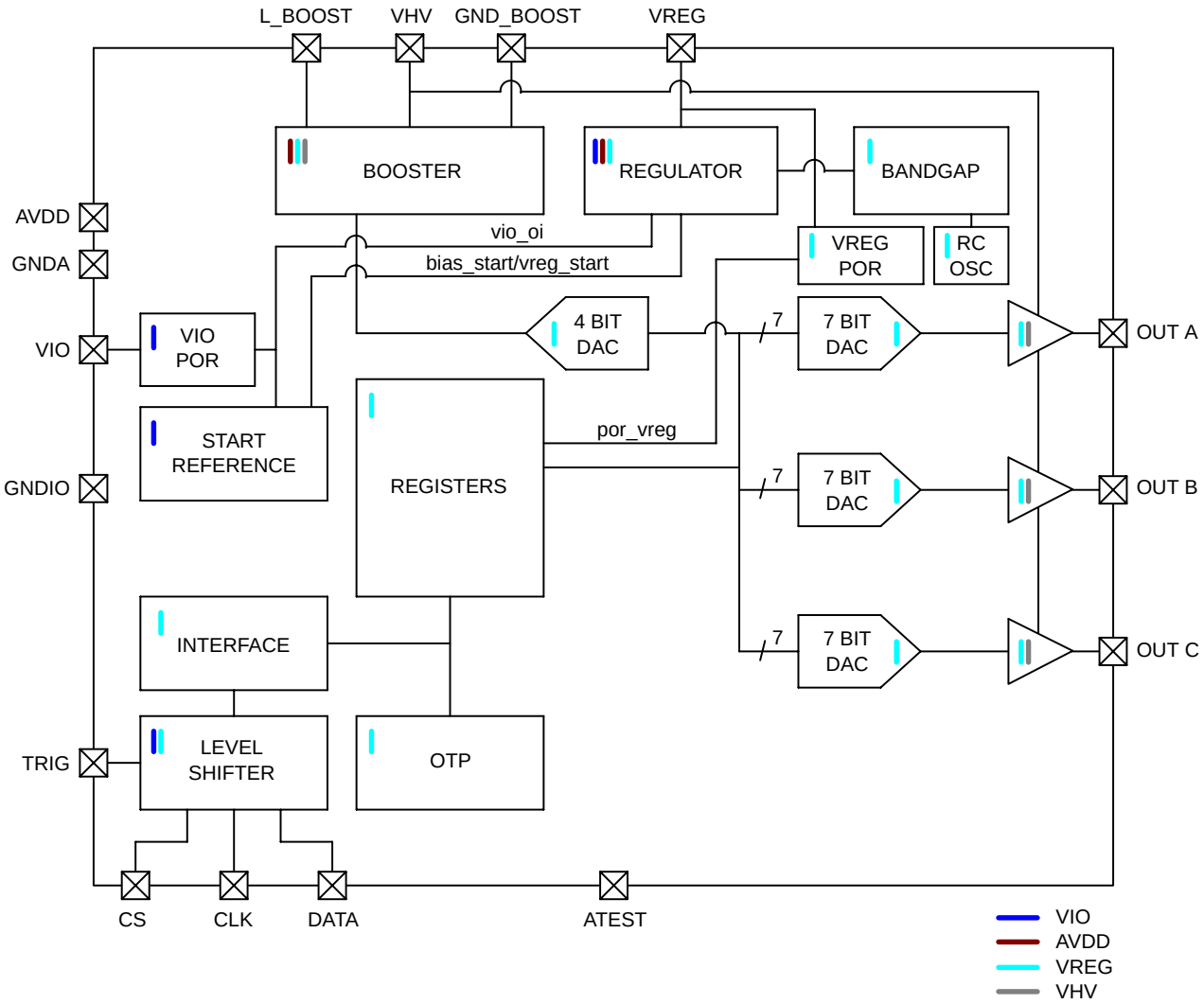


Figure 1. HVDAC Functional Block Diagram

RDL Pin Out

Table 1. PIN FUNCTION DESCRIPTIONS

Bump	Name	Type	Description
A1	VREG	Analog Output	VREG Capacitor
A2	ATEST	Analog Output	Test Pin (Ground in Application)
A3	GND_BOOST	Power	Boost Ground
A4	VHV	Analog HV I/O	Boost High Voltage Output
B1	OUTB	Analog HV Output	High Voltage Output B
B2	OUTC	Analog HV Output	High Voltage Output C
B3	AVDD	Power	Analog Supply
B4	L_BOOST	Analog HV Output	Boost Inductor
C1	OUTA	Analog HV Output	High Voltage Output A
C2	GND_DIG	Power	Digital Ground
C3	TRIG	Digital I/O	Trigger Signal Input (Note 1)
C4	GND_REF	Power	Analog Ground
D1	VIO	Power	IO Reference Supply
D2	DATA	Digital I/O	RFFE SDATA/SPI_DATA
D3	CLK	Digital Input	RFFE SCLK/SPI CLK
D4	CS	Digital Input	SPI_CS (Ground for MIPI RFFE)

1. To be grounded when not in use.

RDL Ball Array Package Footprint

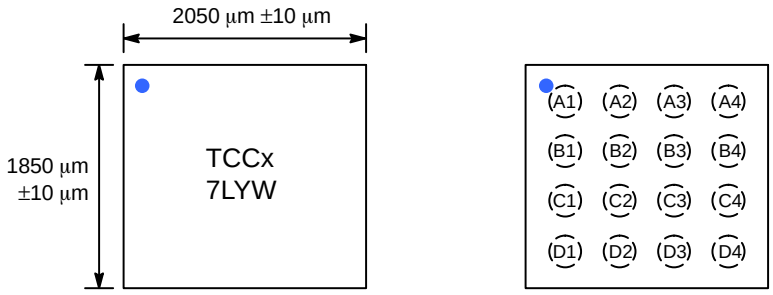


Figure 2. Ball Array Footprint − Top View

Electrical Performance Specifications

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
AVDD	Analog Supply Voltage	−0.3 to +6.0	V
VIO	IO Reference Supply Voltage	−0.3 to +3.6	V
$V_{I/O}$	Input Voltage Logic Lines (DATA, CLK, CS)	−0.3 to VIO +0.3	V
VHV	VHV Maximum Voltage	−0.3 to 30	V
$V_{ESD\ (HBM)}$	Human Body Model, JESD22-A114, All I/O	2,000	V
$V_{ESD\ (MM)}$	Machine Model, JESD22-A115	200	V
T_{STG}	Storage Temperature	−55 to +150	°C
$T_{AMB\_OP\_MAX}$	Max Operating Ambient Temperature without Damage	+110	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating			Unit
		Min	Typ	Max	
T_{AMB_OP}	Operating Ambient Temperature	−30	−	+85	°C
T_{J_OP}	Operating Junction Temperature	−30	−	+125	°C
AVDD	Analog Supply Voltage	2.3	−	5.5	V
VIO	IO Reference Supply Voltage	1.1	−	3.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC CHARACTERISTICS

(T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Shutdown Mode						
I_{AVDD}	AVDD Supply Current	−	−	0.8	μA	VIO Supply is Low
I_{L_BOOST}	L_BOOST Leakage	−	−	1	μA	VIO Supply is Low
I_{BATT}	Battery Current	−	−	1	μA	VIO Supply is Low
I_{VIO}	VIO Supply Current	−1	−	1	μA	VIO Supply is Low
I_{CLK}	CLK Leakage	−1	−	1	μA	VIO Supply is Low
I_{DATA}	DATA Leakage	−1	−	1	μA	VIO Supply is Low
Active Mode						
I_{BATT}	Average Battery Current, 3 Outputs Actively Switching 16 V for 1205 μs to 2 V for 1705 μs to 8V for 1705 μs	−	980	1,290	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS0}	Average Battery Current, 3 Outputs @ 0 V Steady State	−	590	830	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS2}	Average Battery Current, 3 Outputs @ 2 V Steady State	−	610	860	μA	At VHV = 20 V AVDD = 3.3 V
I_{BATT_SS16}	Average Battery Current, 3 Outputs @ 20 V Steady State	−	780	1,020	μA	At VHV = 20 V AVDD = 3.3 V
I_{L_BOOST}	Average Inductor Current, 3 Outputs Actively Switching 20 V for 1205 μs to 2 V for 1705 μs to 8 V for 1705 μs	−	730	1,000	μA	At VHV = 20 V AVDD = 3.3 V
$I_{L\_BOOST\_SS0}$	Average Inductor Current, 3 Outputs @ 0 V Steady State	−	350	550	μA	At VHV = 20 V AVDD = 3.3 V
$I_{L\_BOOST\_SS2}$	Average Inductor Current, 3 Outputs @ 2 V Steady State	−	380	570	μA	At VHV = 20 V AVDD = 3.3 V

Table 4. DC CHARACTERISTICS (continued)
(T_A = −30 to +85°C; V_{OUTX} = 15 V for each output; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; R_{LOAD} = equivalent series load of 5.6 kΩ and 2.7 nF; C_{HV} = 22 nF; L_{BOOST} = 15 μH; TRIG pin grounded; unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Active Mode (continued)						
$I_{L\_BOOST\_SS16}$	Average Inductor Current, 3 Outputs @ 20 V Steady State	−	550	750	μA	At VHV = 20 V AVDD = 3.3 V
I_{VIO_INACT}	VIO Average Inactive Current	−	−	3	μA	VIO is High, No Bus Activity
I_{VIO_ACTIVE}	VIO Average Active Current	−	−	250	μA	VIO = 1.8 V, Master Sending Data at 26 MHz
V_{VREG}		2.05	−	2.3	V	No External Load Allowed
Low Power Mode						
I_{AVDD}	AVDD Supply Current	−	−	7	μA	
I_{L_BOOST}	L_BOOST Leakage	−	−	3	μA	
I_{BATT}	Battery Current	−	−	10	μA	I_{AVDD} + I_{L_BOOST}
I_{VIO}	VIO Supply Current	−	−	3	μA	No Bus Activity
V_{VREG}		2.0	−	3.3	V	No External Load Allowed

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. BOOST CONVERTER CHARACTERISTICS
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; T_A = –30 to +85°C; C_{HV} = 22 nF; L_{BOOST} = 15 μH; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VHV_min	Minimum Programmable Output Voltage (Average), DAC Boost = 0h	Active Mode	−	9	−	V
VHV_max	Maximum Programmable Output Voltage (Average), DAC Boost = Fh	Active Mode		24		V
Resolution	Boost Voltage Resolution	4−bit DAC	−	1	−	V
$R_{DS(ON)}$	n-Channel MOSFET On-Resistance	I_{L_BOOST} = 10 mA	−	1.3	−	Ω
$I_{L\_BOOST\_LIMIT}$	Inductor Current Limit		−	100	−	mA

Table 6. ANALOG OUTPUTS (OUT A, OUT B, OUT C)
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; VHV = 24 V; T_A = −30 to +85°C; R_{LOAD} = ∞ unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
Shutdown Mode						
Z_{OUT}	OUT A, OUT B, OUT C Output Impedance	7	−	−	MΩ	DAC Disabled
Active Mode						
V_{OH}	Maximum Output Voltage	22.0	−	−	V	DAC A, B or C = FFh, DAC Boost = Fh, I_{OH} < 10 μA
V_{OL}	Minimum Output Voltage	−	−	1	V	DAC A, B or C = 01h, DAC Boost = 0h to Fh, I_{OH} < 10 μA
Slew Rate		−	6.5	10	μs	2 V to 20 V Step, Measured at V_{OUT} = 15.2 V, R_{LOAD} = Equivalent Series Load of 5.6 kΩ and 2.7 nF, Turbo Enabled
R_{PD}	OUT A, OUT B, OUT C Set In Pull−Down Mode	−	−	800	Ω	DAC A, B or C = 00h, DAC Boost = 0h to Fh, Selected Output(s) is Disabled
Resolution	Voltage Resolution (1−bit)	−	188	−	mV	(1 LSB = 1 Bit)
V_{OFFSET}	Zero Scale, Least Squared Best Fit	-1	−	+1	LSB	
Error		-3.0	−	+3.0	$\%V_{OUT}$	Over 2 V – 18 V V_O Range
DNL	Differential Non-linearity Least Squared Best Fit	-0.9	−	+0.9	LSB	Over 2 V – 18 V V_O Range
INL	Integral Non-linearity Least Squared Best Fit	-1	−	+1	LSB	Over 2 V – 18 V V_O Range
I_{SC}	Over Current Protection	−	35	65	mA	Any DAC Output to Ground
V_{RIPPLE}	Output Ripple with All Outputs at Steady State	−	−	10	mV RMS	Over 2 V – 18 V V_O Range, VHV = 20 V

Theory of Operation

Overview

The control IC outputs are directly controlled by programming the three DACs (DAC A, DAC B, and DAC C) through the digital interface. The DACs are 8-bit DACs used in a 7-bit format.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high-voltage amplifier supplied from the boost converter (see Control IC block diagram − Figure 1).

The control IC output voltages are scaled from 0 to 24 V, with 128 steps of 188 mV (2×24 V/255 = 0.188235 V). The nominal control IC output can be approximated to 188 mV × (DAC value).

For performance optimization the boost output voltage (VHV) can be programmed to levels between 9 V and 24 V via the DAC_boost register (4 bits with 1 V steps). The startup default level for the boosted voltage is VHV = 20 V.

For proper operation and to avoid saturation of the output devices and noise issues it is recommended to operate the boosted VHV voltage at least 2 V above the highest programmed V_{OUT} voltage of any of the three outputs.

When the DAC output value is set to 00h the corresponding output is disabled and the output is pulled to GND through an effective impedance of less than 800 Ω.

Operating Modes

The following operating modes are available:

1. **Shutdown Mode:** All circuit blocks are off, the DAC outputs are disabled and placed in high Z state and current consumption is limited to minimal leakage current. The shutdown mode is entered upon initial application of AVDD or upon VIO being placed in the low state. The contents of the registers are not maintained in shutdown mode.
2. **Startup Mode:** Startup is only a transitory mode. Startup mode is entered upon a VIO high state. In startup mode all registers are reset to their default states, the digital interface is functional, the boost converter is activated, outputs OUT A, OUT B, and OUT C are disabled and the DAC outputs are placed in a high Z state. Control software can request a full hardware and register reset of the TCC−103 by sending an appropriate PWR_MODE command to direct the chip from either the active mode or the low power mode to the startup mode. From the startup mode the device automatically proceeds to the Active mode.
3. **Active Mode:** All blocks of the TCC−103 are activated and the DAC outputs are fully controlled through the digital interface. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. Active mode is automatically entered from the startup mode. Active mode can also be entered from the low power mode under control software command.
4. **Low Power Mode**: In low power mode the serial interface is enabled, the DAC outputs are disabled and are placed in a high Z state and the boost voltage circuit is disabled. Control software can request to enter the low power mode from the active mode by sending an appropriate PWR_MODE command. The contents of all registers are maintained in the low power mode.

AVDD Power-On Reset

Upon application of AVDD the TCC−103 will be in shutdown mode. All circuit blocks are off and the chip draws only minimal leakage current.

VIO Power-On Reset and Startup Conditions

A high level on VIO places the chip in startup mode which provides a power on reset (POR) to the TCC−103. POR resets all registers to their default settings as described in Table 7. VIO POR also resets the serial interface circuitry. POR is **not** a brown-out detector and VIO needs to be brought back to a low level to enable the POR to trigger again.

Table 7. VIO POWER-ON RESET AND STARTUP

Register	Default State for VIO POR	Comment
DAC Boost	[1011]	VHV = 20 V
Power Mode	[01] > [00]	Transitions from SHUTDOWN to STARTUP and then Automatically to ACTIVE Mode
DAC Enable	[000]	V_{OUT} A, B and C Disabled
DAC A		Output in High-Z Mode
DAC B		Output in High-Z Mode
DAC C		Output in High-Z Mode

VIO Shutdown

A low level at any time on VIO places the chip in shutdown mode in which all circuit blocks are off. The contents of the registers are not maintained in shutdown mode.

Table 8. VIO THRESHOLDS
(AVDD from 2.3 V to 5.5 V; T_A = –30 to +85°C unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
VIORST	VIO Low Threshold	−	−	0.2	V	When VIO is lowered below this threshold level the chip is reset and placed into the Shutdown mode.

Power Supply Sequencing

The AVDD input is typically directly supplied from the battery and thus is the first on. After AVDD is applied and before VIO is applied to the chip all circuits are in the shutdown state and draw minimum leakage currents. Upon application of VIO the chip automatically starts up using default settings and is placed in the active state waiting for a command via the serial interface.

Table 9. TIMING
(AVDD from 2.3 V to 5.5 V; VIO from 1.1 V to 3.0 V; T_A = –30 to +85°C; OUT A, OUT B & OUT C; CHV = 22 nF; L_{BOOST} = 15 μH; VHV = 20 V; Turbo-Charge mode off unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
T_{POR_VREG}	Internal bias settling time from Shutdown to Active mode	−	50	120	μs	For Info Only
T_{BOOST_START}	Time to charge CHV @ 95% of set VHV	−	130	−	μs	For Info Only
$T_{SD\_TO\_ACT}$	Startup time from Shutdown to Active mode	−	180	250	μs	
T_{SET+}	Output A, B, C positive settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 2 V to 20 V; 0Bh (11d) to 55h (85d)	−	50	60	μs	Voltage Settling Time Connected on V_{OUT} A, B, C
T_{SET-}	Output A, B, C negative settling time to within 5% of the delta voltage, equivalent series load of 5.6 kΩ and 2.7 nF, V_{OUT} from 20 V to 2 V; 55h (85d) to 0Bh (11d)	−	50	60	μs	Voltage Settling Time Connected on V_{OUT} A, B, C

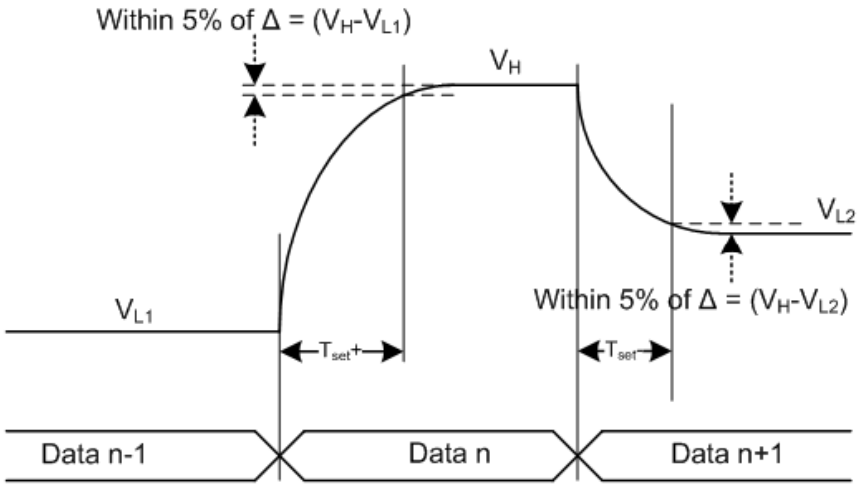


Figure 3. Output Setting Diagram

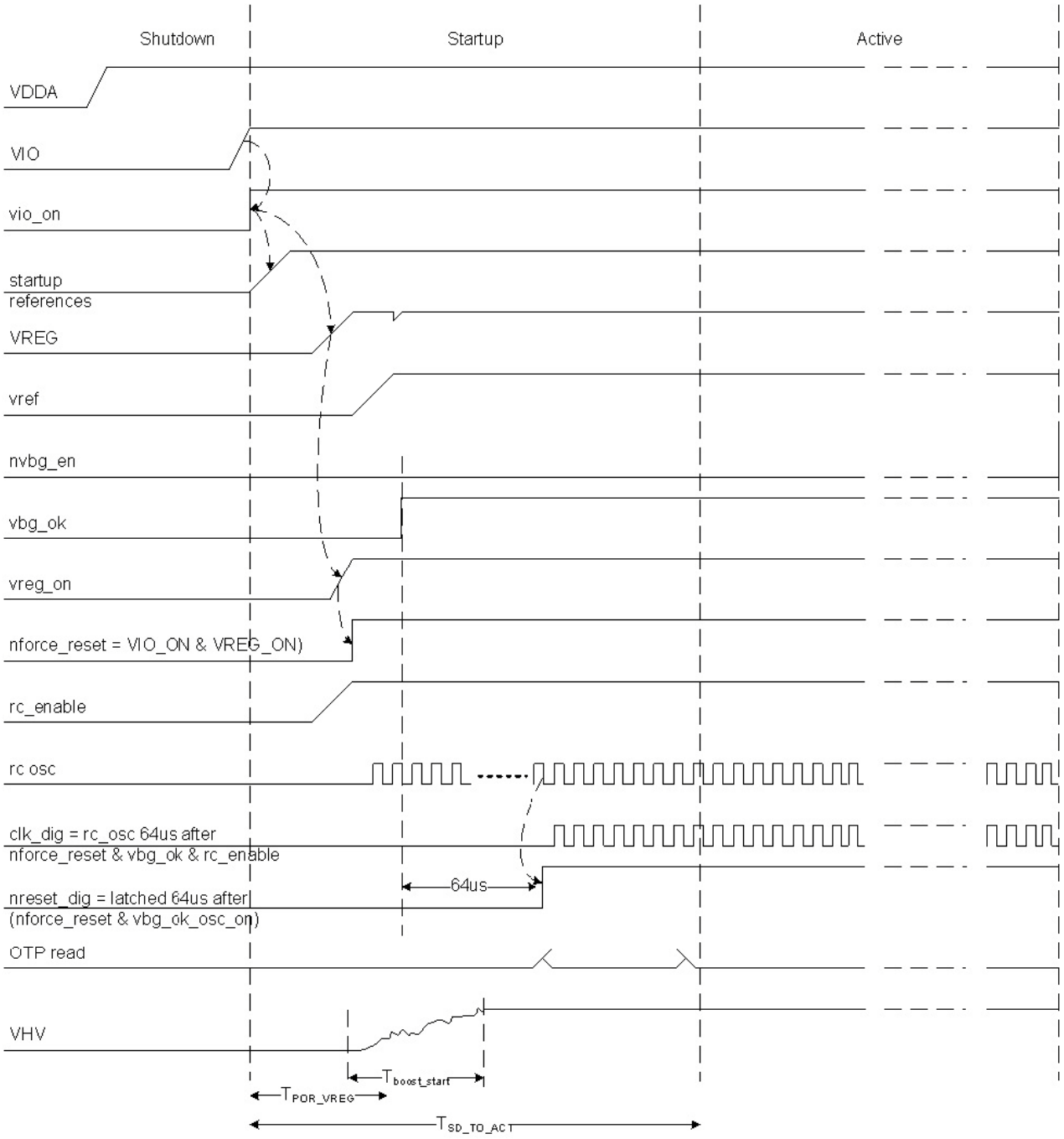


Figure 4. Startup Timing Diagram

Boost Control

The TCC−103 integrates an asynchronous current control boost converter. It operates in a discontinuous mode and features spread-spectrum circuitry for Electro-Magnetic Interference (EMI) reduction. The average boost clock is 2 MHz and the clock is spread between 0.8 MHz and 3.2 MHz.

Boost Output Voltage (VHV) Control Principle

The asynchronous control starts the boost converter as soon as the VHV voltage drops below the reference set by the 4-bit DAC and stops the boost converter when the VHV voltage rises above the reference again.

Due to the slow response time of the control loop, the VHV voltage may drop below the set voltage before the control loop compensates for it. In the same manner, VHV can rise higher than the set value. This effect may reduce the maximum output voltage available. Please refer to Figure 5 below.

The asynchronous control reduces switching losses and improves the output (VHV) regulation of the DC/DC converter under light load, particularly in the situation where the TCC−103 only maintains the output voltages to fixed values.

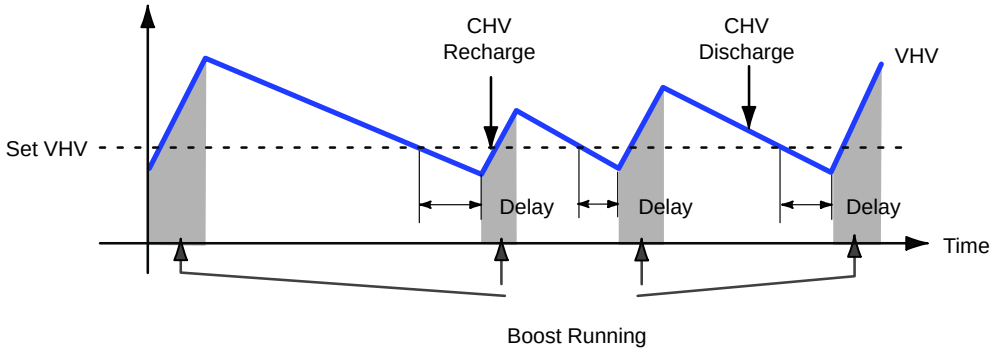


Figure 5. VHV Voltage Waveform

High Impedance (High Z) Feature

In Shutdown mode the OUT pins are set to a high impedance mode (high Z).

Following is the principle of operation for the control IC:

1. The output voltage V_{OUT} is defined by:

$$V_{OUT} = \frac{\text{DAC code}}{255} \times 24\ V \times 2 \qquad \text{(eq. 1)}$$

2. The voltage VHV defines the maximum supply voltage of the output regulator and is set by the 4−bit DAC.
3. The maximum DC output voltage V_{OUT} is limited to (VHV − 2 V).
4. The minimum output voltage V_{OUT} is 1.0 V MAX.

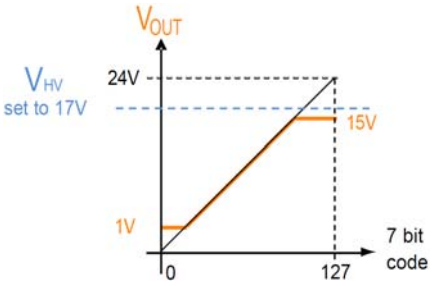


Figure 6. DAC Output Range Example A

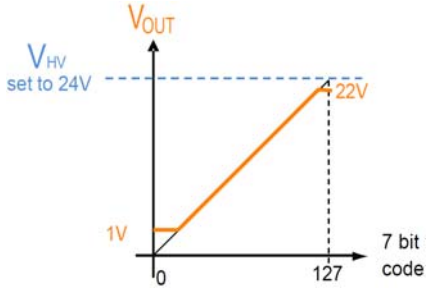


Figure 7. DAC Output Range Example B

Digital Interface

The control IC is fully controlled through a digital interface (DATA, CLK, CS). The digital interface automatically detects and responds to MIPI RFFE interface commands, 3-wire 30-bit Serial Interface commands or 3-wire 32-bit Serial Interface commands. Auto-detection is accomplished on a frame by frame basis. The digital interface is further described in the next sections of this document.

3-wire Serial Interface

The 3-wire serial interface operates in a synchronous write-only 3-wire slave mode. 30-bit or 32-bit message length is automatically detected for each frame. If CS changes state before all bits are received then all data bits are ignored. Data is transmitted most significant bit first and DATA is latched on the rising edge of CLK. Commands are latched on the falling edge of CS.

Table 10. 3-WIRE SERIAL INTERFACE SPECIFICATION

(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 3.0 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
F_{CLK}	Clock Frequency	−	−	26	MHz	
T_{CLK}	Clock Period	38.4	−	−	ns	
N_{BIT}	Bits Number	−	30/32	−	bits	Auto-detection 30-bit or 32-bit
T_{HIGH}	Clock High Time	13	−	−	ns	
T_{LOW}	Clock Low Time	13	−	−	ns	
TCS_{SETUP}	CS Set-up Time	5	−	−	ns	70% Rising Edge of CS to 30% Rising Edge of First Clock Cycle
TCS_{HOLD}	CS Hold Time	5	−	−	ns	30% Falling Edge of Last Clock Cycle to 70% Falling Edge of CS
TD_{SETUP}	Data Set-up Time	4	−	−	ns	Relative to 30% of CLK Rising Edge
TD_{HOLD}	Data Hold Time	4	−	−	ns	Relative to 70% of CLK Rising Edge
T_{SUCC}	CS Low Time between Successive Writes	38.4	−	−	ns	70% Falling Edge of CS to 70% Rising Edge of CS
T_{SUCC}	CS Low Time between Successive DAC Update Writes	1,500	−	−	ns	Time between Groups of DAC Update Reg [00000] & [00001] Writes
C_{CLK}	Input Capacitance	−	−	5	pF	CLK Pin
C_{DATA}	Input Capacitance	−	−	8.3	pF	DATA Pin
C_{CS}	Input Capacitance	−	−	5	pF	CS Pin
C_{TRIG}	Input Capacitance	−	−	10	pF	TRIG Pin
V_{IH}	Input Logic Level High	0.7 × VIO	−	VIO + 0.3	V	DATA, CLK, CS
V_{IL}	Input Logic Level Low	−0.3	−	0.3 × VIO	V	DATA, CLK, CS
I_{IH_DATA}	Input Current High	−2	−	10	μA	DATA
I_{IL_DATA}	Input Current Low	−2	−	1	μA	DATA
$I_{IH\_CLK,CS}$	Input Current High	−1	−	10	μA	CLK, CS
$I_{IL\_CLK,CS}$	Input Current Low	−1	−	1	μA	CLK, CS
V_{TP_TRIG}	Positive Going Threshold Voltage	0.4 × VIO	−	0.7 × VIO	V	TRIG
V_{TN_TRIG}	Negative Going Threshold Voltage	0.3 × VIO	−	0.6 × VIO	V	TRIG
V_{H_TRIG}	Hysteresis Voltage ($V_{TP} – V_{TN}$)	0.1 × VIO	−	0.4 × VIO	V	TRIG
I_{IH_TRIG}	TRIG Input Current High	−2	−	10	μA	TRIG = 0.8 × VIO
I_{IL_TRIG}	TRIG Input Current Low	−2	−	1	μA	TRIG = 0.2 × VIO

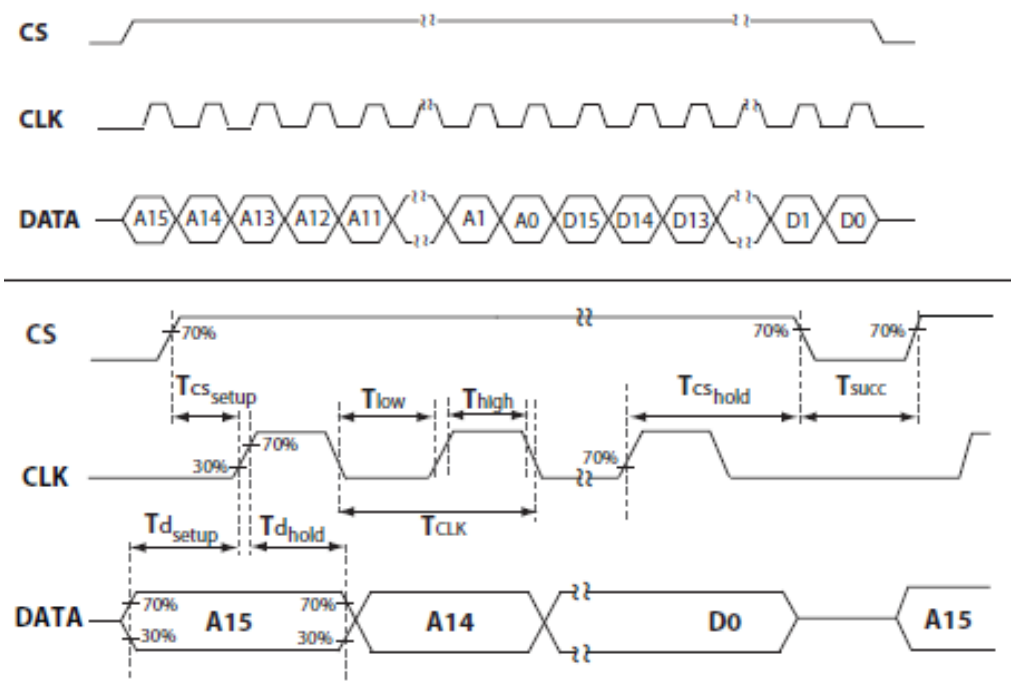


Figure 8. SPI 3-wire Serial Interface Signal Timing

SPI Frame Length Decoding

30-bit or 32-bit frame length is automatically detected. The length of the frame is defined by the number of Clock rising edges while CS is kept high. The TCC−103 will not respond to a SPI command if the length of the frame is not exactly 30 bits or 32 bits. SPI registers are write only.

SPI Frame Structure

Table 11. 32 BITS FRAME: ADDRESS DECODING (1 OR 2 OR 3 OUTPUTS)

H0	H1	R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	1	0	0	1	0	0	X	X	X	X	X
ON Semiconductor Header		R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 12. 30 BITS FRAME: ADDRESS DECODING (1 OR 2 OR 3 OUTPUTS)

R/W	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	1	0	0	X	X	X	X	X
R/W	Device ID			Specific Device ID					Register Address for Operation				

Table 13. 3-WIRE SERIAL INTERFACE ADDRESS MAP

A4	A3	A2	A1	A0	Data [15:8]	Data [7:0]
0	0	0	0	0	Turbo Charge Settings for DAC A, B, C	DAC C
0	0	0	0	1	DAC B	DAC A
0	0	1	0	0	Turbo-Charge Delay Parameters for DAC A, B, C	Turbo Threshold Delay Settings for A, B, C
1	0	0	0	0	Mode Select + Control IC Setup	
1	0	0	1	0	Reserved	Reserved
To						
1	1	1	1	1		

Turbo-Charge Mode

The TCC−103A control IC has a Turbo-Charge mode that significantly shortens the system settling time when changing programming voltages. In Turbo-Charge mode the DAC output target voltage is temporarily set to either a delta voltage above or a delta voltage below the actual desired target for the TCDLY time. It is recommended that VHV be set to 24 V when using Turbo-Charge mode. For more details about programming the part in Turbo-Charge mode, refer to application note XXXX (coming soon).

RF Front-End Control Interface (MIPI RFFE Interface)

The TCC−103 is a write-only slave device which is fully compliant to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE) Version 1.10.00 26 July 2011. This device is rated at Full-Speed operation for 1.65 V < VIO < 1.95 V and at Half-Speed operation for 1.1 V < VIO < 1.65 V. When using the MIPI RFFE interface the CS pin is grounded.

Table 14. MIPI RFFE INTERFACE SPECIFICATION

(T_A = −30 to +85°C; 2.3 V < AVDD < 5.5 V; 1.1 V < VIO < 1.95 V; unless otherwise specified)

Parameter	Description	Min	Typ	Max	Unit	Comment
F_{SCLK}	Clock Full-Speed Frequency	0.032	−	26	MHz	Full-Speed Operation: 1.65 V < VIO < 1.95 V
T_{SCLK}	Clock Full-Speed Period	0.038	−	32	μs	Full-Speed Operation: 1.65 V < VIO < 1.95 V
T_{SCLKIH}	CLK Input High Time	11.25	−	−	ns	Full-Speed
T_{SCLKIL}	CLK Input Low Time	11.25	−	−	ns	Full-Speed
F_{SCLK_HALF}	Clock Half-Speed Frequency	0.032	−	13	MHz	
T_{SCLK_HALF}	Clock Half-Speed Period	0.077	−	32	μs	
T_{SCLKIH}	CLK Input High Time	24	−	−	ns	Half-Speed
T_{SCLKIL}	CLK Input Low Time	24	−	−	ns	Half-Speed
V_{TP}	Positive Going Threshold Voltage	0.4 × VIO	−	0.7 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_{TN}	Negative Going Threshold Voltage	0.3 × VIO	−	0.6 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
V_H	Hysteresis Voltage ($V_{TP} – V_{TN}$)	0.1 × VIO	−	0.4 × VIO	V	CLK, DATA, TRIG, 1.2 or 1.8 V Bus
I_{IH}	Input Current High	−2	−	+10	μA	TRIG, SDATA = 0.8 × VIO
		−1	−	+10	μA	SCLK = 0.8 × VIO
I_{IL}	Input Current Low	−2	−	+1	μA	TRIG, SDATA = 0.2 × VIO
		−1	−	+1	μA	SCLK = 0.2 × VIO
C_{CLK}	Input Capacitance	−	−	5	pF	CLK Pin
C_{DATA}	Input Capacitance	−	−	8.3	pF	DATA Pin
C_{TRIG}	Input Capacitance	−	−	10	pF	TRIG Pin
TD_{SETUP}	DATA Setup Time	1	−	−	ns	Full-Speed
TD_{HOLD}	DATA Hold Time	5	−	−	ns	Full-Speed
TD_{SETUP}	DATA Setup Time	2	−	−	ns	Half-Speed
TD_{HOLD}	DATA Hold Time	5	−	−	ns	Half-Speed
T_{SUCC}	Time between Successive DAC Update Writes	1,500	−	−	ns	

The control IC contains twenty−four 8−bit registers. Register content is described in Table 15. Some additional registers, implement as provision, are not described in this document.

Table 15. MIPI RFFE ADDRESS MAP

Register Address	Description	Purpose	Access Type	Size (Bits)
0x00	DAC Configuration (Enable Mask)	High Voltage Output Enable Mask	Write	7
0x01	Turbo Register DAC A, B & C	Turbo-Charge Configuration DAC A, B & C	Write	8
0x02	DAC A Register	Used to Set Up OUT A	Write	8
0x03	DAC B Register	Used to Set Up OUT B	Write	8
0x04	DAC C Register	Used to Set Up OUT C	Write	8
0x10	DAC Boost (VHV)	Settings for the Boost High Voltage	Write	8
0x11	Trigger Register	Trigger Configuration	Write	8
0x12	Turbo-Charge Delay DAC A, B, C	Turbo-Charge Delay Steps DAC A, B, C	Write	8
0x13	Turbo-Charge Delay DAC A, B, C	Turbo-Charge Delay Multiplication DAC A, B, C	Write	8
0x1C	Power Mode and Trigger Register	Power Mode & Trigger Control PWR_MODE [7:6] TRIG_REG [5:0]	Write	8
0x1D	Product ID Register	Product Number * Hard Coded into ASIC	(Write)	8
0x1E	Manufacturer ID Register	MN (10 Bits Long) Manufacturer ID[7:0] Hard Coded into ASIC	(Write)	8
0x1F	Unique Slave Identifier Register (USID)	Spare [7:6] [5,4] = Manufacturer ID [9:8] USID [3:0]	Write	8

*The two least significant bits are programmed in OTP during manufacture.

Command Sequences

- **Register 0 Write** (used to access the Register 0 DAC Configuration - Enable Mask). Register 0 can be also be accessed using Register Write or/and Extended Register Write.
- **Register Write** (used to access only one register at the time)
- **Extended Register Write** (used to access a group of contiguous registers with one command bursting up to 16 bytes)

Register 0 Write Command Sequence

The Command Sequence starts with a Sequence Start Condition (SSC) which is followed by the Register 0 Write Command Frame. This Frame contains the Slave address, a logic one, and the seven bit word that will be written to Register 0. The Command Sequence is depicted below.

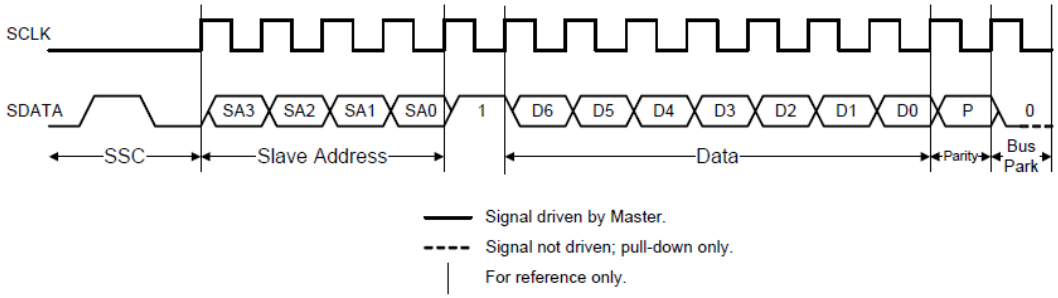


Figure 9. Register 0 Write Command Sequence

Table 16. MIPI RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										BP
SSE & DAC Configuration	1	0	SA [3,0]	1	SSE	0	0	DAC_A	DAC_B	DAC_C	0	P	BP

Register Write Command Sequence

The Write Register command sequence may be used to access each register (addresses 0-31).

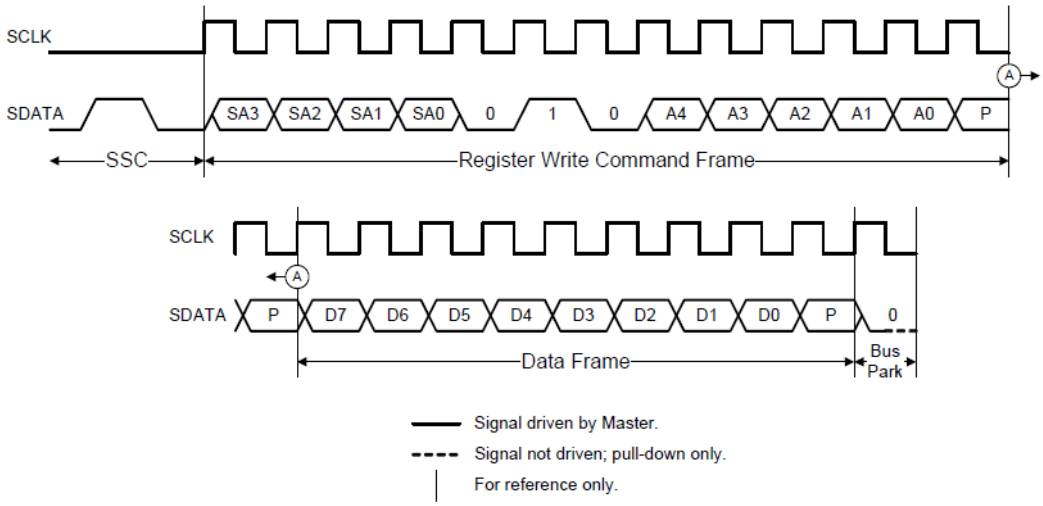


Figure 10. Register Write Command Sequence

Table 17. MIPI RFFE COMMAND FRAME FOR REGISTER 0 WRITE COMMAND SEQUENCE

Description	SSC		Command Frame										Data Frame		BP
Turbo Charge Settings	1	0	SA [3,0]	0	1	0	0	0	0	0	1	P	Turbo Charge [7:0]	P	BP
Register Write DAC A	1	0	SA [3,0]	0	1	0	0	0	0	1	0	P	TC [8] & DAC_A [6:0]	P	BP
Register Write DAC B	1	0	SA [3,0]	0	1	0	0	0	0	1	1	P	TC [9] & DAC_B [6:0]	P	BP
Register Write DAC C	1	0	SA [3,0]	0	1	0	0	0	1	0	0	P	TC [10] & DAC_C [6:0]	P	BP

Extended Register Write Command Sequence

In order to access more than one register in one sequence this message could be used. Most commonly it will be used for loading three DAC registers at the same time. The four LSBs of the Extended Register Write Command Frame determine the number of bytes that will be written by the Command Sequence. A value of 0b0000 would write one byte and a value of 0b1111 would write sixteen bytes.

If more than one byte is to be written, the register address in the Command Sequence contains the address of the first extended register that will be written to and the Slave's local extended register address shall be automatically incremented by one for each byte written up to address 0x1F, starting from the address indicated in the Address Frame.

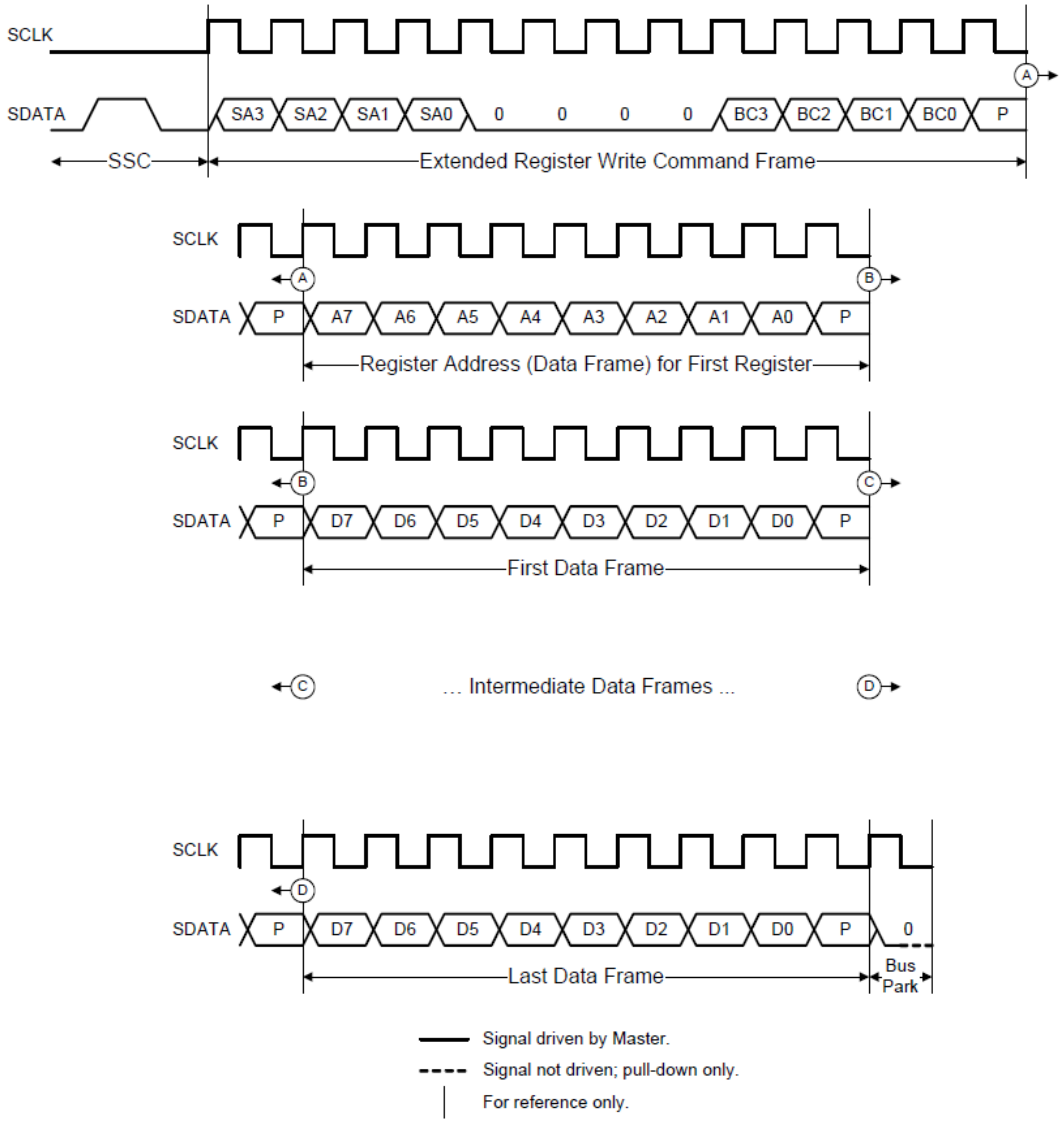


Figure 11. Extended Register Write Command Sequence

Table 18. EXTENDED REGISTER WRITE

Description	SSC		Command Frame										Address Frame								
Extended Register Write							Op Code				<Byte Count>			P	<Starting Address>								P
Turbo Charge & DAC	1	0	SA [3,0]				0	0	0	0	0	0	1	1	P	0	0	0	0	0	0	0	1	P

Data Frame		Data Frame		Data Frame		Data Frame		BP
<Data-8 Bit>	P	<Data-8 Bit>	P	<Data-8 Bit>	P	<Data-8 Bit>	P	BP
Turbo Charge	P	DAC_A [7,0]	P	DAC_B [7,0]	P	DAC_C [7,0]	P	BP

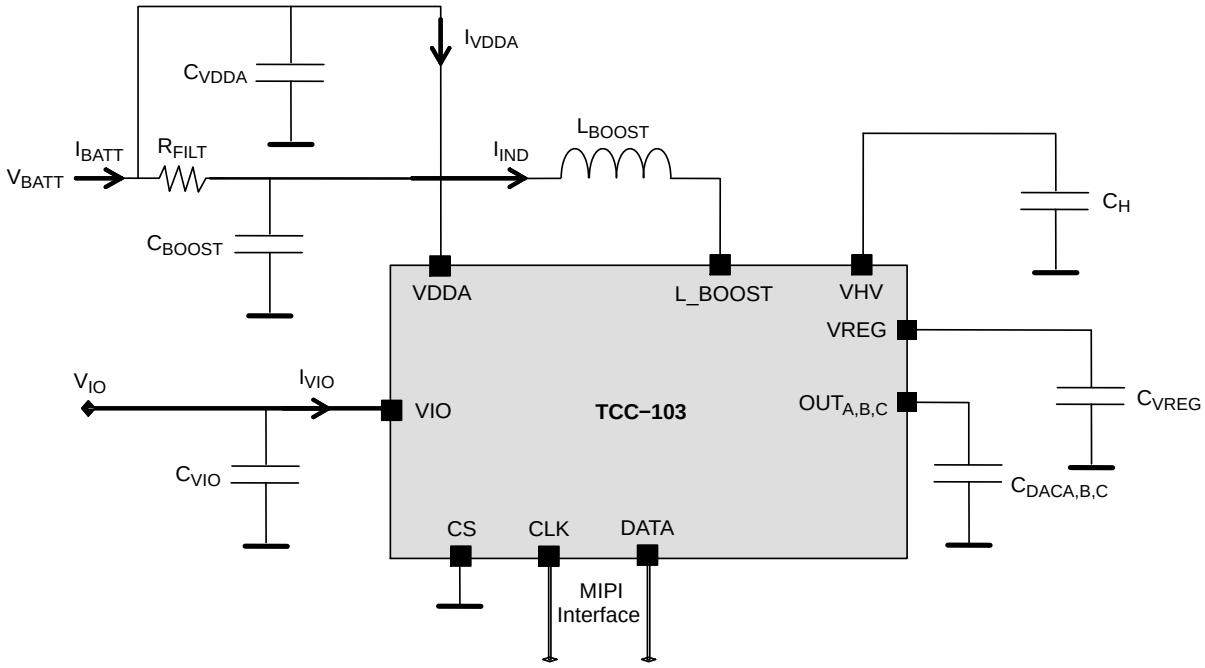


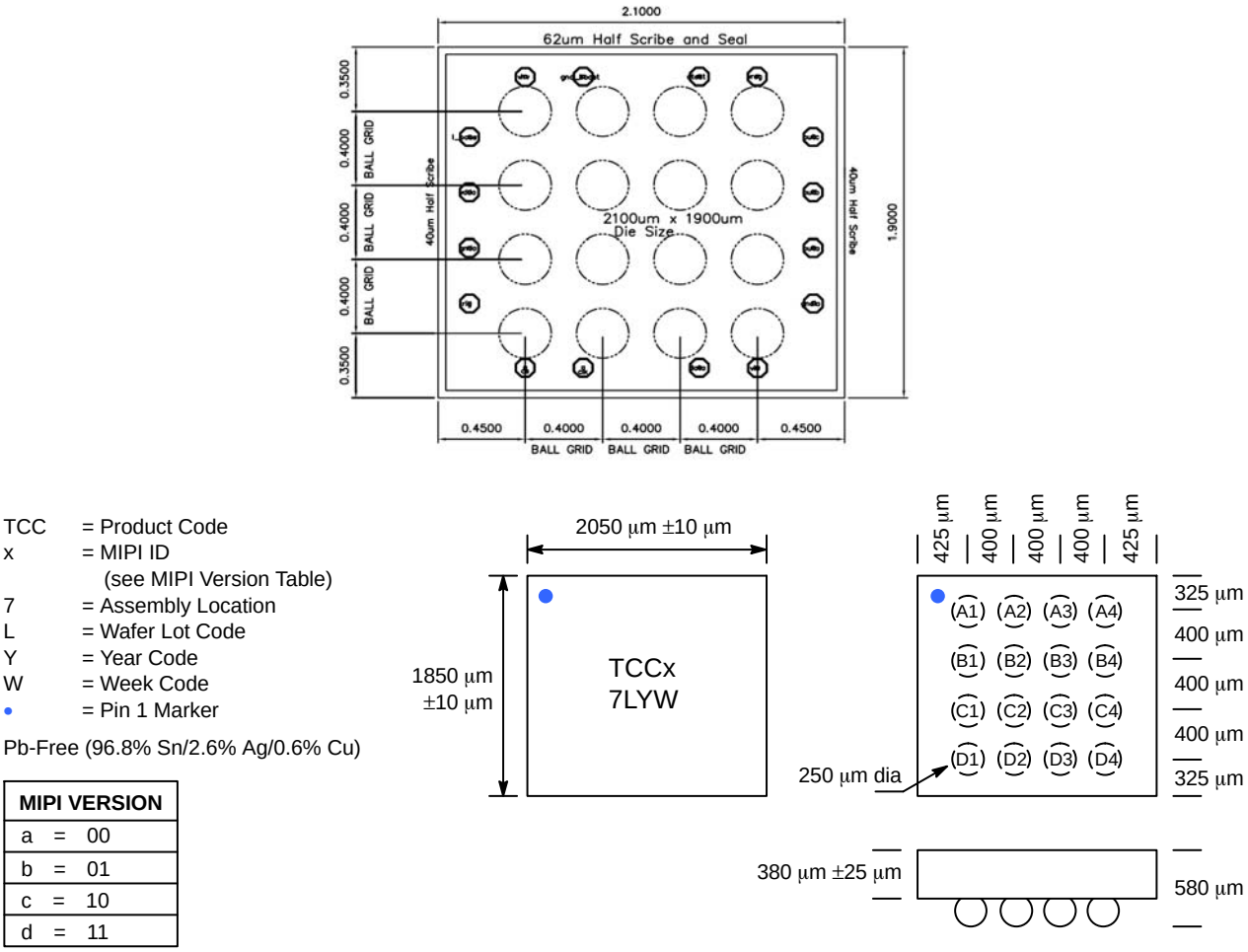
Figure 12. Recommended MIPI RFFE Interface Application Schematic

Table 19. RECOMMENDED EXTERNAL BOM

Component	Description	Nominal Value	Package (Inch)	Recommended P/N
C_{BOOST}	Boost Supply Capacitor, 10 V	1 μF	0402	TDK: C1005X5R1A105K
L_{BOOST}	Boost Inductor	15 μH	0603	TDK: VLS2010ET-150M
R_{FILT}	Decoupling Resistor, 5%	3.3 Ω	0402	Vishay: CRCW04023R30JNED
C_{VIO}	V_{IO} Supply Decoupling, 10 V	100 nF	0201	Murata: GRM033R61A104ME15D
C_{AVDD}	V_{AVDD} Supply Decoupling, 10 V	1 μF	0402	TDK: C1005X5R1A105K
C_{VREG}	V_{VREG} Supply Decoupling, 10 V	220 nF	0201	TDK: C0603X5R1A224M
C_{HV}	Boost Output Capacitor, 50 V	22 nF	0402	Murata: GRM155R71H223KA12
C_{dacA} C_{dacB} C_{dacC}	Decoupling Capacitor, 50 V (Note 2)	100 pF	0201	Murata: GRM0335C1H101JD01D

2. Recommended for noise reduction only− not essential.

MECHANICAL DESCRIPTION



MIPI VERSION		
a	=	00
b	=	01
c	=	10
d	=	11

Figure 13. Ball Array Package

NOTE: Die dimensions include an assumed 50 µm wide sawing kerf, this kerf width is subject to change without notice.

TAPE & REEL DIMENSIONS

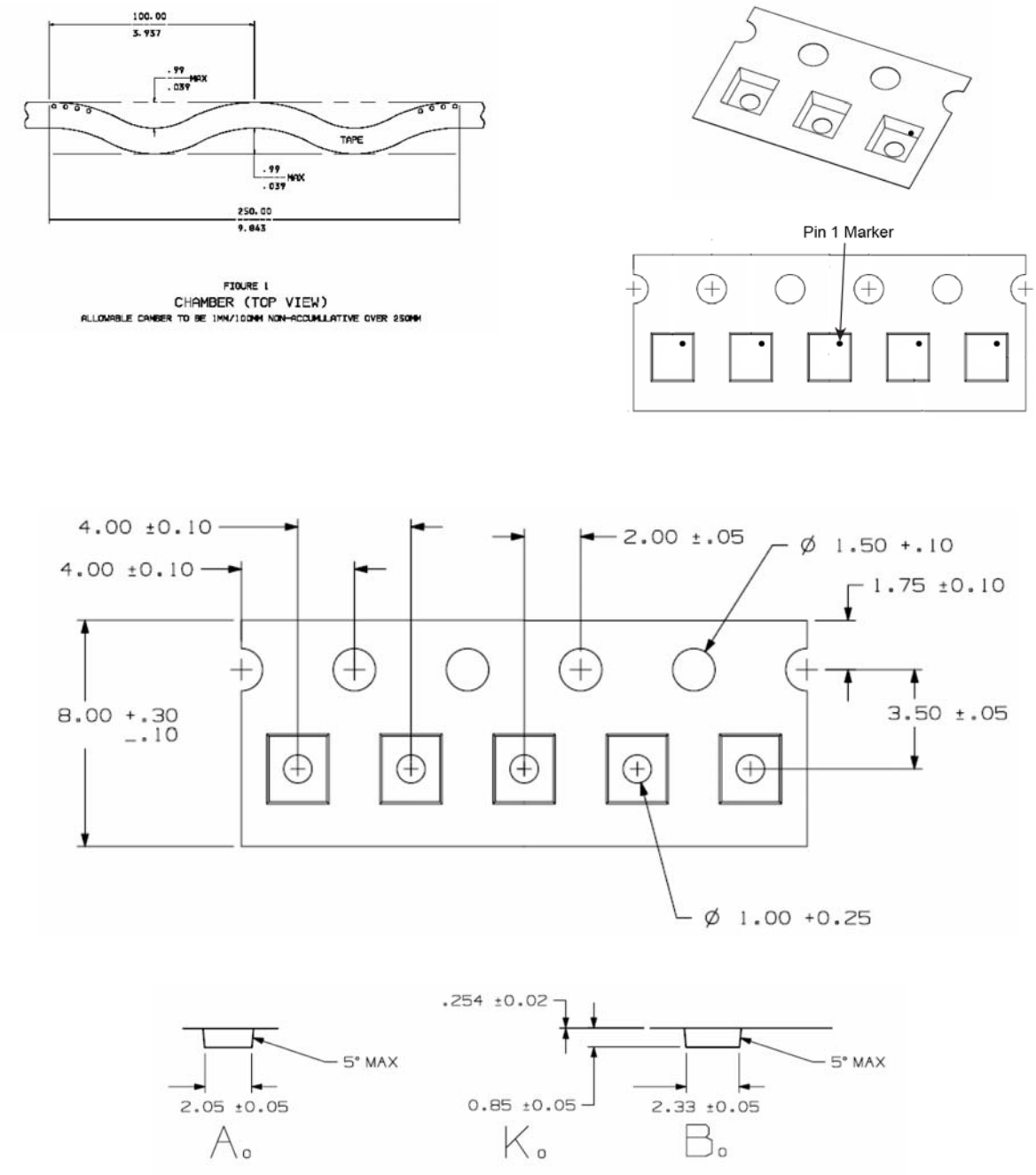


Figure 14. WLCSP Carrier Tape Drawings

Table 20. ORDERING INFORMATION

Device	Package	Shipping†
TCC−103A−RT	RDL (Pb-Free)	3000 / Tape & Reel
TCC−103B−RT	RDL (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

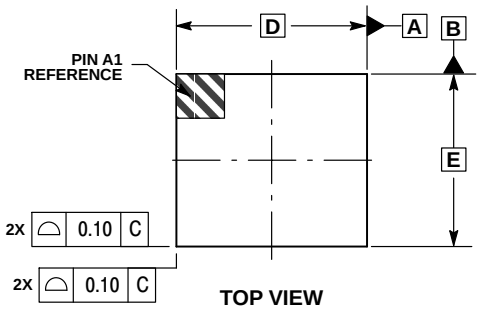
Assembly Instructions

Note: It is recommended that under normal circumstances, this device and associated components should be located in a shielded enclosure.

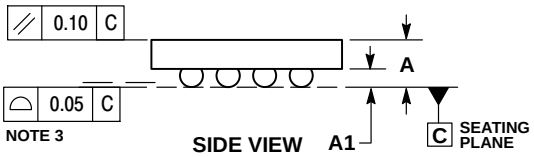
TCC−103

PACKAGE DIMENSIONS

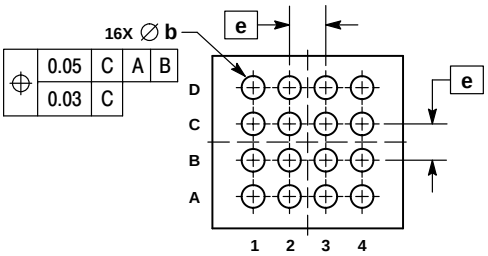
CSP16, 2.1x1.90
CASE 568AE
ISSUE O



TOP VIEW



SIDE VIEW

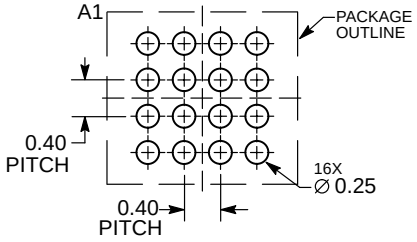


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MAX
A	−−−	0.62
A1	0.18	0.22
b	0.24	0.30
D	2.10 BSC	
E	1.90 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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