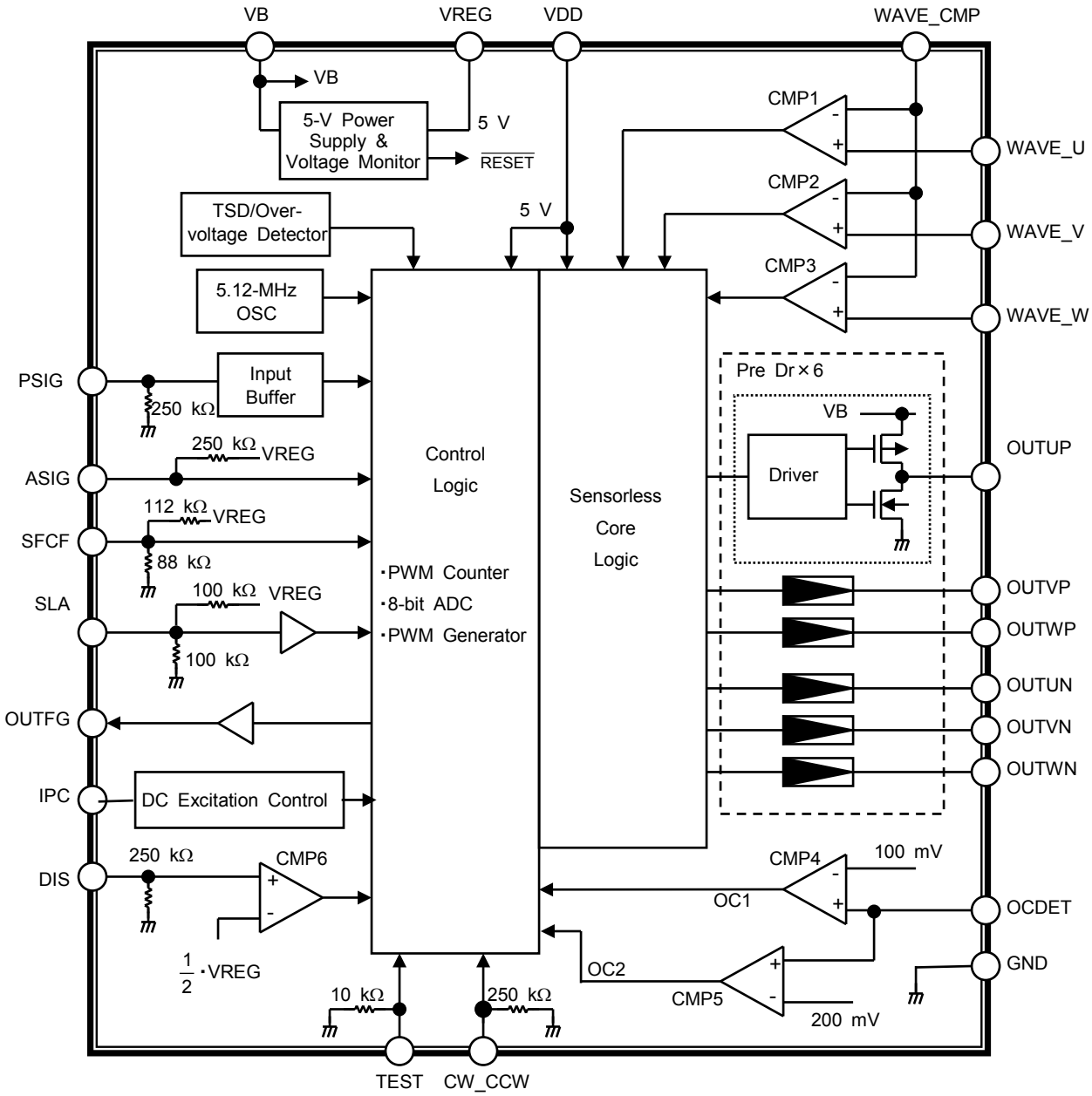
Block Diagram



Note: Some of the functional blocks, circuits, or constants in the block diagram are omitted or simplified to clarify the descriptions of the relevant features.

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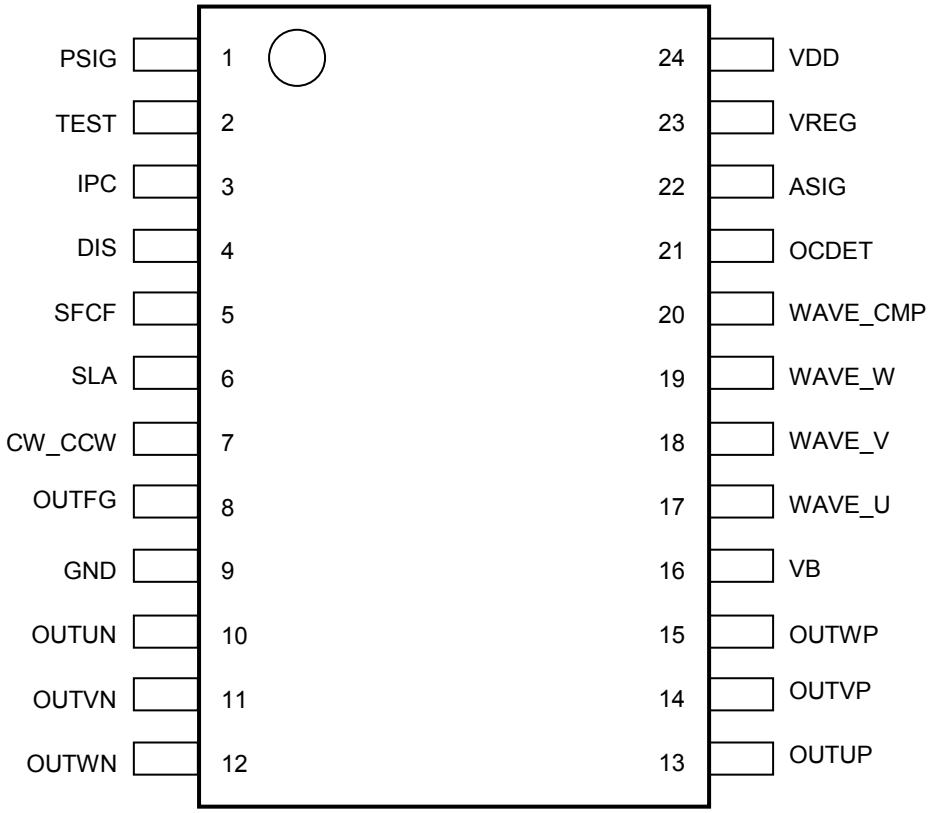
Pin Assignment



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Pin Description

Pin No.	Symbol	Description
1	PSIG	External PWM signal input The PWM signal period is measured by the counter, and converted into output control PWM signal. Built-in pull-down resister. When Duty cycle is set to 0% this pin is connected to GND.
2	TEST	Test mode setting pin Low: User mode. Built-in pull-down resister. Please connect this pin to GND in your application.
3	IPC	Input to set 1-phase DC excitation time at start up. Any value can be set according to the value of external capacitance.
4	DIS	Disable pin (active Low) Setting this pin High puts the pre-driver output into the high-impedance state. Built-in pull-down resistor. The output is active when this pin is open.
5	SFCF	Forced commutation frequency select pin According to the input voltage, user can select 8-level frequencies from 391 rpm up to 25,000 rpm. Built-in voltage dividing resistors. 1,563 rpm is selected when this pin is open.
6	SLA	Lead angle select pin User ca select lead angle (LA) from three levels: 7.5, 15, or 30 °. Low: LA = 7.5 ° ; High: LA = 15 ° ; Middle or open: LA = 30 °
7	CW_CCW	Input to select motor's rotating direction. Low: Clockwise rotation (CW); High: Counterclockwise rotation (CCW). Built-in pull-down resister of 250 kΩ.
8	OUTFG	Rotation signal output
9	GND	Ground pin
10	OUTUN	Nch MOSFET gate drive pin for phase U
11	OUTVN	Nch MOSFET gate drive pin for phase V
12	OUTWN	Nch MOSFET gate drive pin for phase W
13	OUTUP	Pch MOSFET gate drive pin for phase U
14	OUTVP	Pch MOSFET gate drive pin for phase V
15	OUTWP	Pch MOSFET gate drive pin for phase W
16	VB	Power supply pin This pin incorporates the overvoltage detection feature. Upon detection of an overvoltage condition, motor rotation is stopped.
17	WAVE_U	U phase induced voltage signal input
18	WAVE_V	V phase induced voltage signal input
19	WAVE_W	W phase induced voltage signal input
20	WAVE_CMP	Reference voltage input for the voltage comparison with induced voltage.
21	OCDET	Overcurrent input detection pin Connected to two internal comparators, one of which has 100 mV threshold and the other has 200 mV threshold.
22	ASIG	External analog voltage input pin Analog voltage is input to ADC and converted into PWM signal. Built-in pull-up resister. Duty cycle is set to 100% when this pin is open.
23	VREG	5 V constant-voltage output It is used as power supply for the logic circuit by being connected to VDD. The current capability is 10 mA (max). This pin has an automatic reset function for resetting the IC upon detecting an undervoltage condition.
24	VDD	Logic power supply pin

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Functional Description

1. Overview

The user inputs PWM signal to this IC. A 3-phase motor is driven by the PWM output signals with the duty cycle determined by that of the input PWM. The user can input PWM signal under the following conditions.

- Frequency: 10 Hz up to 1 kHz
- PWM duty cycle: 0% up to 100%
- Voltage amplitude: 0 V up to VB

This input PWM signal is measured, calculated, and corrected in the logic circuit. The TB9061AFNG generates a 20-kHz PWM signal (PWMint) according to its result. The TB9061AFNG inputs PWMint into the Sensorless Core Logic and outputs sensorless driving signal for a 3-phase brushless motor.

2. Sensorless drive

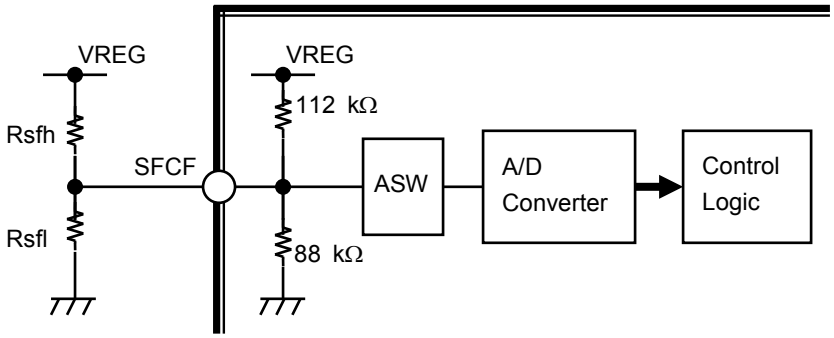
On receipt of a start instruction, which is generated upon completion of 1-cycle counting of a linear voltage at ASIG or PWM signal at PSIG, turn-on signal for forced commutation (commutation irrespective of the motor's rotor position) is driven onto the OUTxx pins, and the motor starts to rotate. The motor's rotation causes an induced voltage on winding wire for each phase. The TB9061AFNG detects the change of the induced voltage using comparators and receives it as a position signal. Then the TB9061AFNG changes the commutation signal automatically from the one for forced commutation to the one based on a position signal and starts sensorless drive of a 3-phase blushless motor.

3. Selection of forced commutation frequency

The user can select forced commutation frequency by changing the input voltage to the SFCF pin. The relation between the frequency and input voltage is shown in the table below. The TB9061AFNG receives the voltage at the SFCF pin through the ADC (upper 3-bit data of the 8-bit ADC) and decides the forced commutation frequency. Please set an appropriate frequency according to motor and load for the user application.

The sum of the external resistor values Rsfh and Rsfl, which are used for setting the SFCF pin voltage, is recommended to be less than 10kΩ. When the SFCF pin is open, the voltage is determined to be (VREG*44%) by internal resisters and the frequency of 1563 rpm is selected.

Input Voltage to the SFCF Pin			Rotational frequency (Forced Commutation Frequency :Electrical Angle) fosc = 5.12 MHz
Vsfcf (VREG = 5 V)	Rate	ADC output	
5.00 to 4.375 V	100 to 87.5%	111xxxxx	25,000 rpm (417 Hz)
4.375 to 3.75 V	87.5 to 75%	110xxxxx	12,500 rpm (208 Hz)
3.75 to 3.125 V	75 to 62.5%	101xxxxx	6,250 rpm (104 Hz)
3.125 to 2.50 V	62.5 to 50%	100xxxxx	3,125 rpm (52 Hz)
2.50 to 1.875 V	50 to 37.5%	011xxxxx	1,563 rpm (26 Hz)
1.875 to 1.25 V	37.5 to 25%	010xxxxx	781 rpm (13 Hz)
1.25 to 0.625 V	25 to 12.5%	001xxxxx	391 rpm (6.5 Hz)
0.625 to 0.0 V	12.5 to 0%	000xxxxx	9,375 rpm (156 Hz)



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Note1 : The forced commutation frequency function at the time of start and function of low PWM input duty can be adjusted using inertia of the motor and load.

- The forced commutation frequency should be set higher as the number of magnetic pole increases.
- The forced commutation frequency should be set lower as the inertia of the load increases.

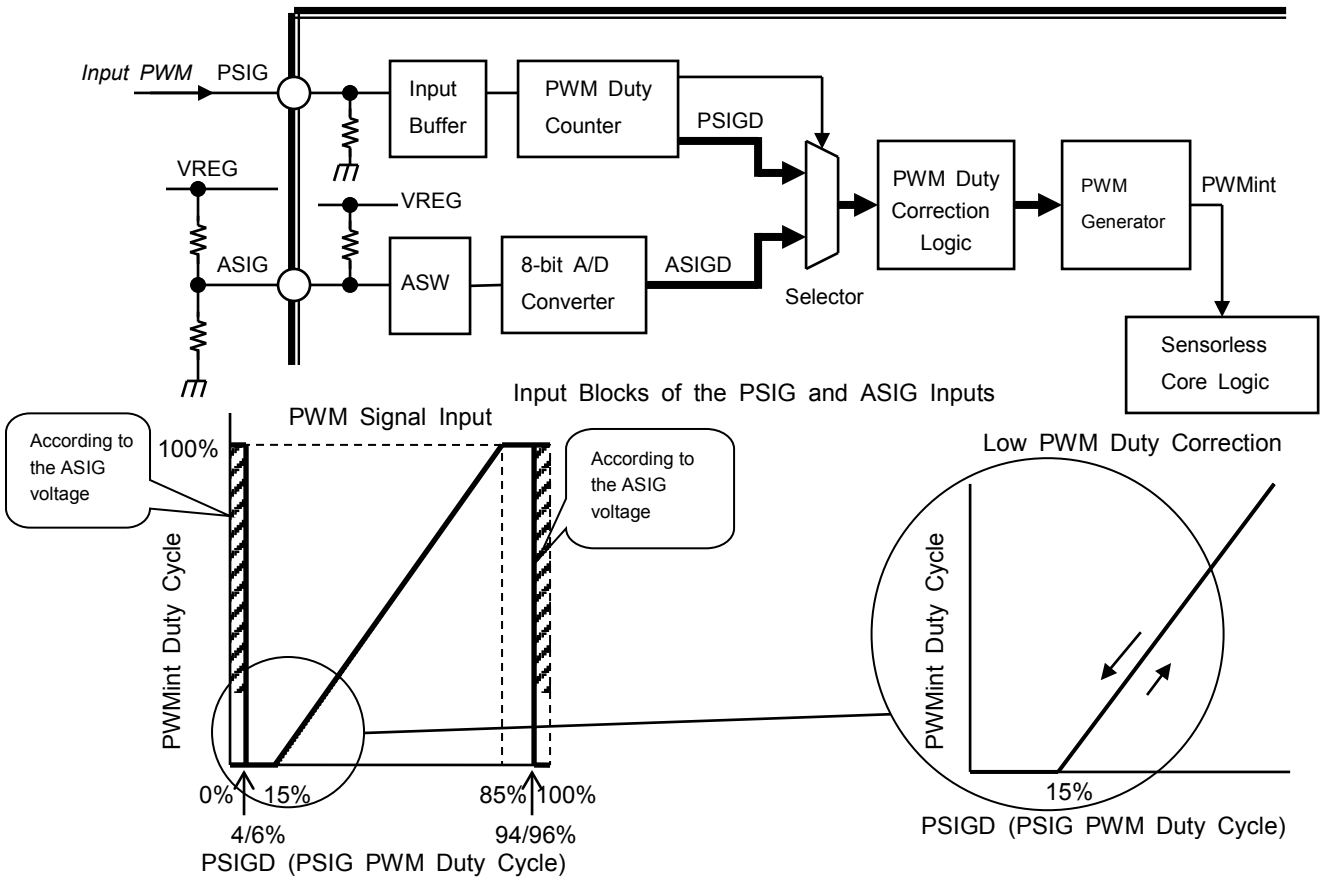
Note2: The IC may cause to step out when the motor is driven by low PWM input duty.
Please use it by PWM input duty that takes an enough margin.
Please conform minimum PWM input DUTY to which the motor can drive and do an enough evaluation according to an external motor.

Note3: It is not possible to make the motor work by a frequency that is lower than the forced commutation frequency.

Functional Description

4. Relation between the PSIG input and internal PWM (PWMint) signals

The relation between the PSIG input signal and the internal PWM signal (PWMint) which is generated in the TB9061AFNG and input to the Sensorless Core Logic is described below.
In the case that the PWM Duty Counter value is within the range between 6% and 94%, the PSIGD input (PSIG PWM duty cycle) is selected and input to the PWM Duty Correction Logic. In the case that the PWM Duty Counter value is ≤ 4% or ≥ 96%, the ASIG voltage is selected.
A hysteresis of 2% is provided for switching between PSIGD and ASIGD.
All PWM signals are active-High. (Setting these signals High turns on the corresponding external N-ch MOSFET.)
The noise filter is built in at the PWM Duty Counter to eliminate 10-μs and shorter pulses.



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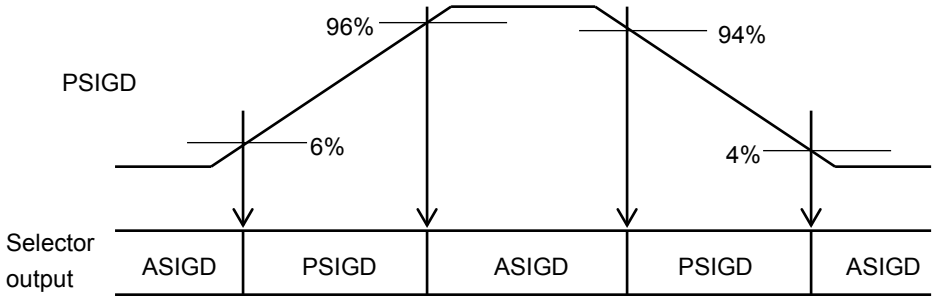
Relation between the Input PWM Duty (PSIGD) and the Selector Output



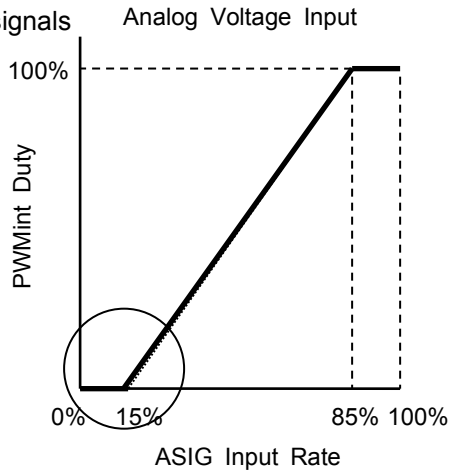
Note1: Slow, low duty driven in the rotation of the motor becomes unstable and can't detect the induced voltage of the motor rotation speed. Please decide the input PWM Duty to evaluate and verify sufficient conditions for your application, the drive motor is stable.

Note2: In case of low PWM input duty, the generation voltage may not be detected with low duty by the output delay of external FET and the rotation of the motor may become discontinuous function.

Functional Description

4. Relation between the PSIG input and internal PWM (PWMint) signals

The graph on the right shows the relation between the analog voltage input to ASIG (shown as rate of voltage divider) and the PWMint duty cycle when the Selector is set to ASIGD. The same correction as that of PSID is executed for the low PWM duty cycle.



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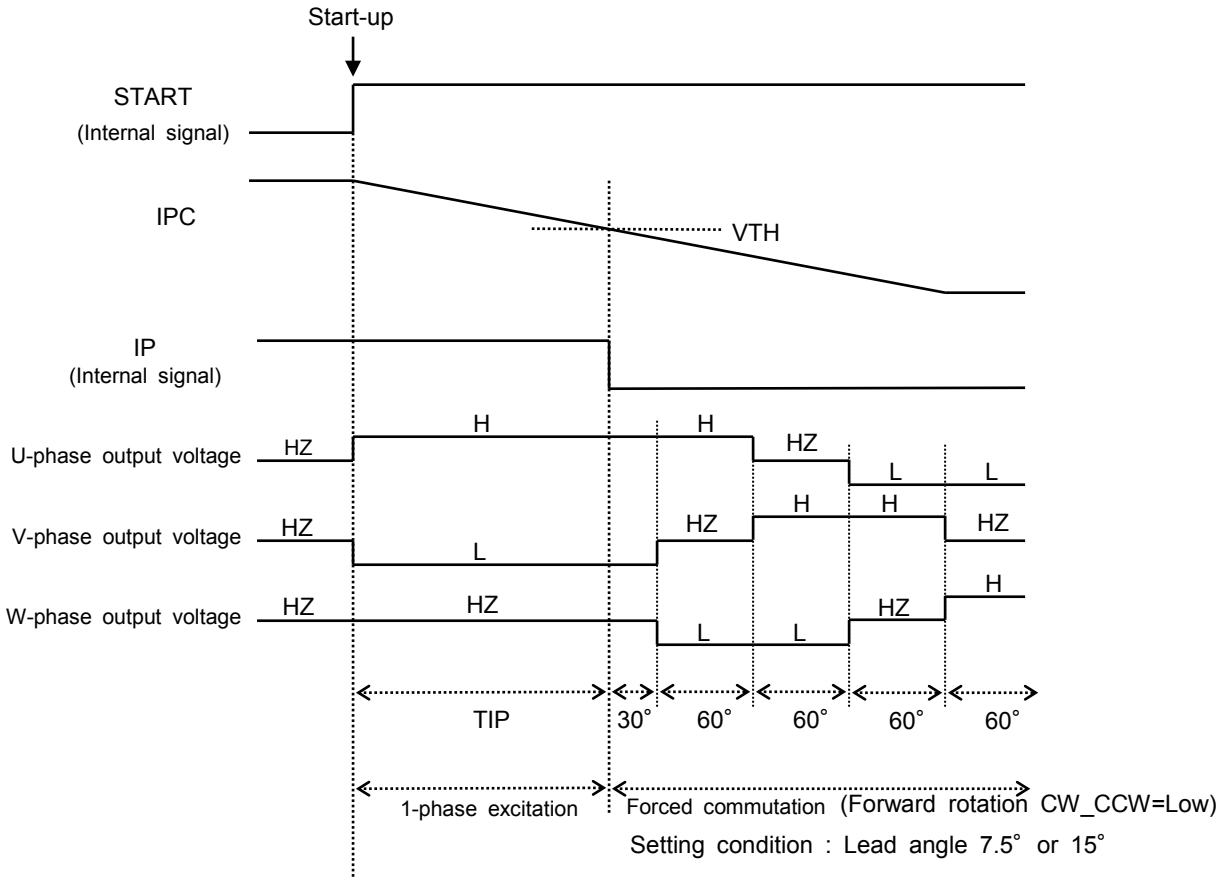
5. Start-up operation

5-1. DC excitation

At start-up, forced commutation signal rotates a motor to generate an induced voltage. For motors with big inertia, it is effective for smoother starting to apply DC excitation signal for certain time in order to fix phase then start the forced commutation. The user can set an arbitrary time for DC excitation (TIP) by connecting a capacitor (CIP) to the IPC pin.

If the user doesn't need DC excitation, a capacitor is not necessary and the IPC pin should be shorted to the GND pin.



TIP = 200 × CIP (ms)

*CIP is an external capacitor connected to IPC. (Unit: μF) HZ: High-Impedance

Note1: The motor current might rush to the FET nearly motor lock current during the DC excitation.
Please decide the DC excitation time setting for un-break-ness or not deterioration by the heat of external FET.

Note2 : In case of lead angle 30°,the first electric angle 60° pattern of forced commutation is different pattern.

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Functional Description

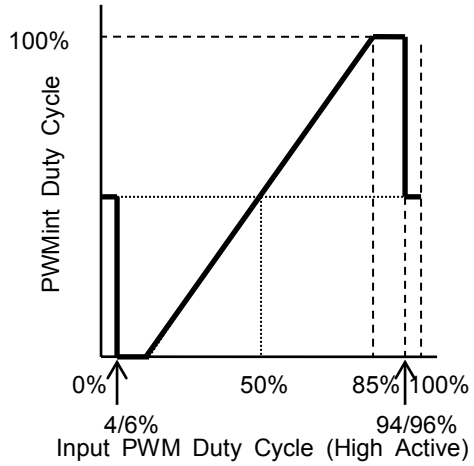
5. Start-up operation (continued)

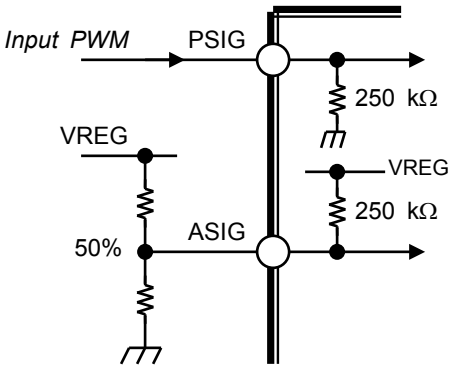
5-2. PWM input control

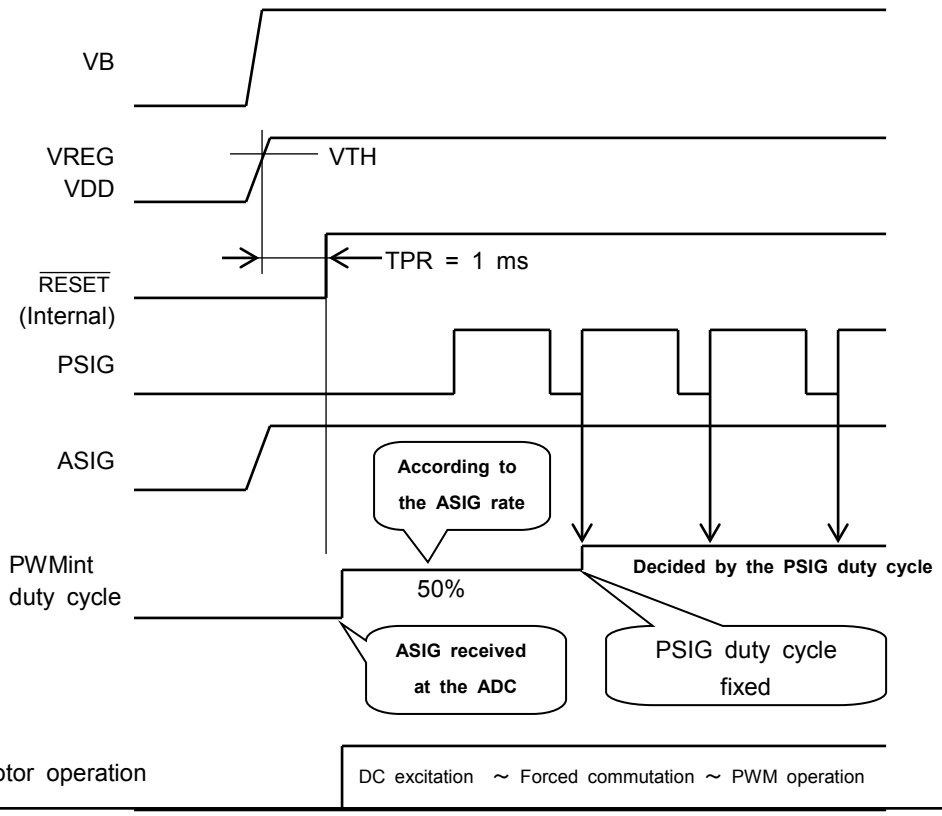
The figure below shows the relation between the PMW duty cycles of input and output signals when some voltage is applied to ASIG. The timing chart shows the start-up operation under such condition.

The ASIG voltage is received at the point when the internal logic starts the operation (TPR = 1 ms). At this time, the PWM Duty Counter value is equal to the initial value, 0%. So the ASIG value takes priority. In the application example shown in the figure below, the output PWM is 50%. If the ASIG voltage is 0%, the output PWM is also 0%; if the ASIG voltage is 100%, the duty cycle of the PWM output is also 100%.

If the PWM Duty Counter value is within the range between 6% and 94%, the output PWM duty cycle is proportional to the counter value. If PSIG is open, the PSIG voltage is set Low by a pull-down resistor and the PWMint duty cycle becomes 0%.







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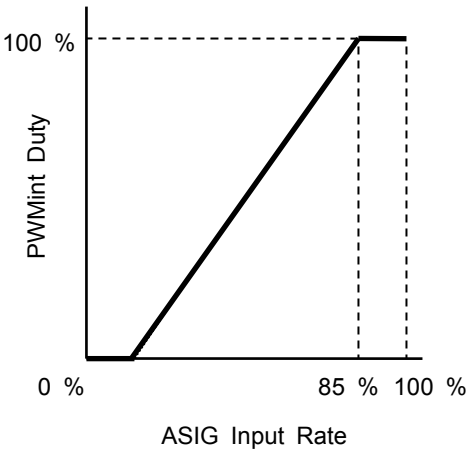
Functional Description

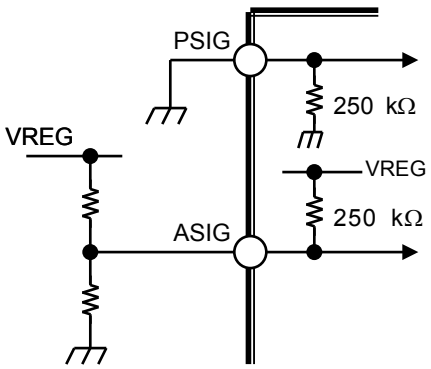
5. Start-up operation (continued)

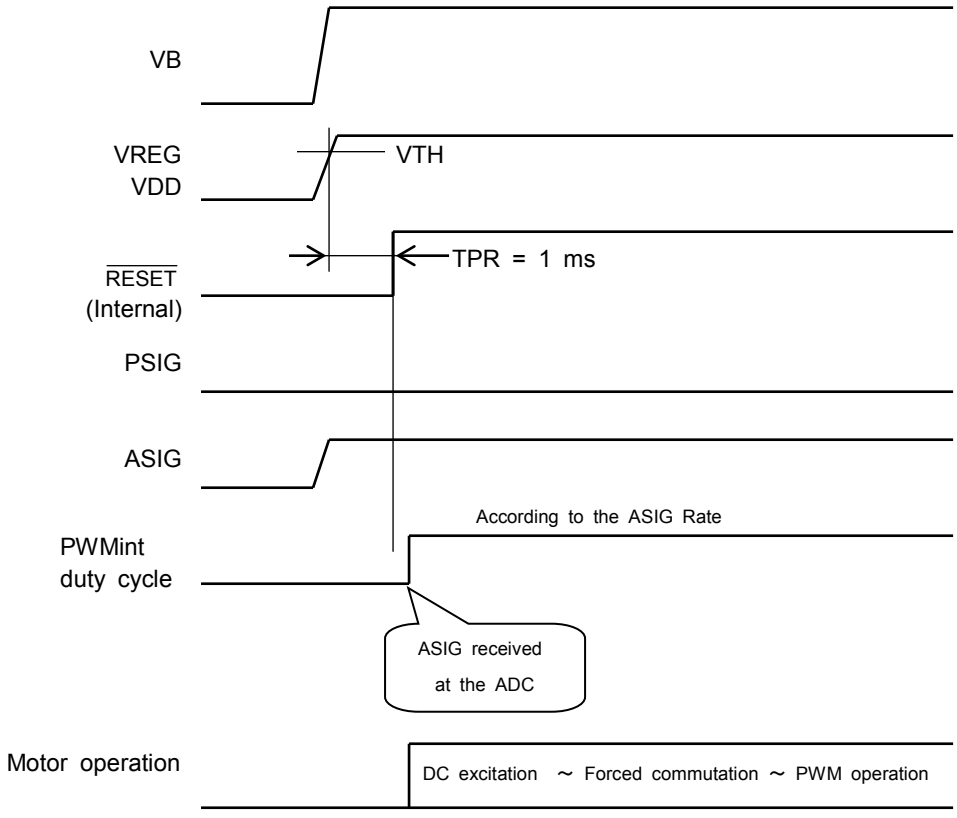
5-3. Analog voltage input control

Analog voltage input to ASIG controls the PWMint duty cycle when PSIG is shorted to GND. The input-to-output conversion characteristics, the connection circuit example and a timing chart are shown below.

When ASIG = VREG, the ASIG input rate is 100%. When ASIG = 0 V, the ASIG input rate is 0%. If ASIG is open, the ASIG voltage is set High by a pull-up resistor and the PWMint duty cycle becomes 100%.







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Functional Description

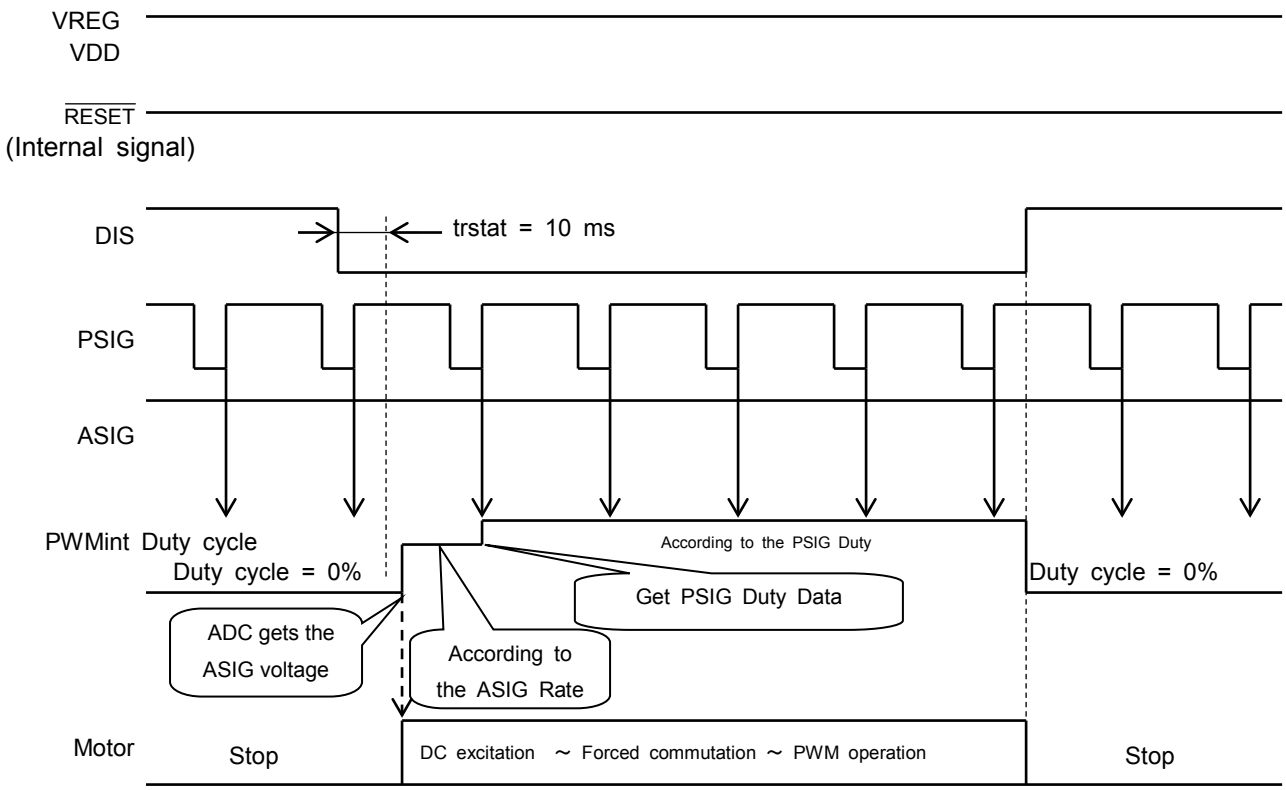
5. Start-up operation (continued)

5-4. Start-up sequence and stop sequence using the DIS pin

The TB9061AFNG can perform start and stop controls of the motor operation with the DIS signal. The start/stop timing is shown below.

- Motor start-up sequence: When DIS is High, the PWMint duty cycle is 0% and the motor driving output is off regardless of the state of PSIG and ASIG.
  From this state, if the DIS signal state is changed to Low, the TB9061AFNG starts to receive the PWM Duty Counter value and the measured ASIG voltage after when trstat = 10 ms. With these data, the TB9061AFNG starts DC excitation and enter the forced commutation and enter the normal commutation mode.

- Motor stop sequence: When DIS becomes High, the PWM Duty Counter value and the measured ASIG voltage value are cleared. The PWMint duty cycle becomes 0% and the motor stops.



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Functional Description

6. Detection of irregular operation

6-1. Overcurrent Detection (ISD)

The TB9061AFNG can detect an overcurrent by monitoring the voltage at a current-detection resistor (Rs) which is connected to external power MOSFETs. There are two detection voltages, 100 mV and 200 mV.

Refer to the block diagram and the timing chart below for the overall operation.

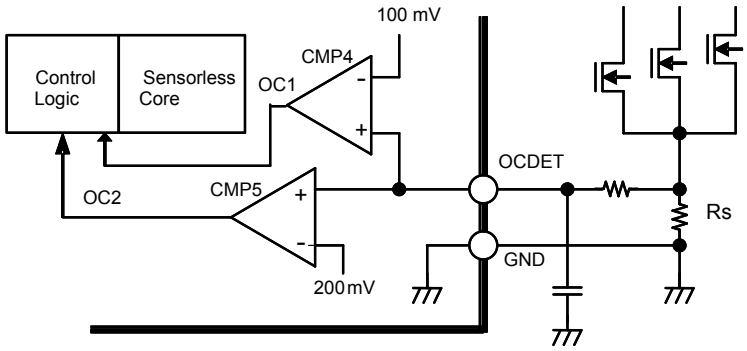
-When the motor is started from the stop state, ISD1 is masked for 100 ms and 1phase excitation fixed .

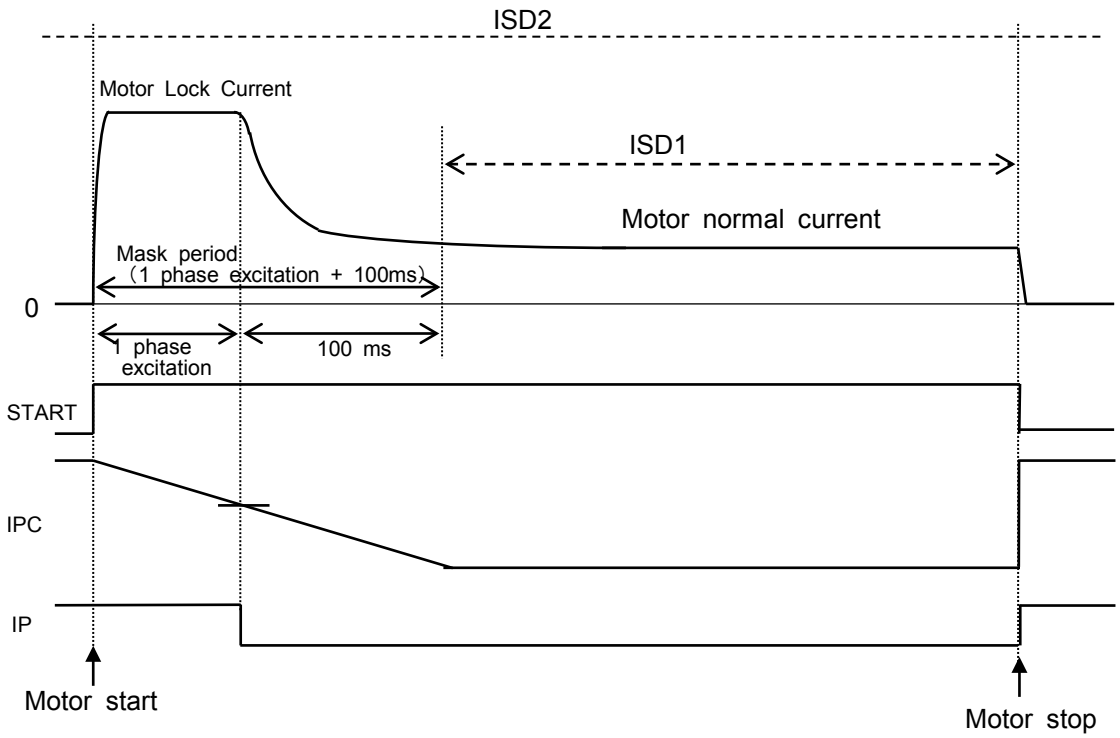
The TB9061AFNG doesn't detect an overcurrent during the masked period. ISD1 doesn't detect the motor 1 phase excitation current but it can detect irregular condition such as a motor lock-up and limit the current in normal PWM operation.

-ISD2 detects a large current due to fault conditions such as motor load shorts, and turns off the output for a certain period. This function is effective to improve the tolerance of MOSFETs to permanent damage. The ISD2 detection is always enabled.

-The following pages explain more specific functions of ISD1 and ISD2.

Note1: ISD1 doesn't detect during 1 phase excitation.





Note2: In the case the motor current might rush to the FET during the DC excitation. Please decide to the DC excitation time setting for un-break-ness or not deterioration by the heat of external FET.

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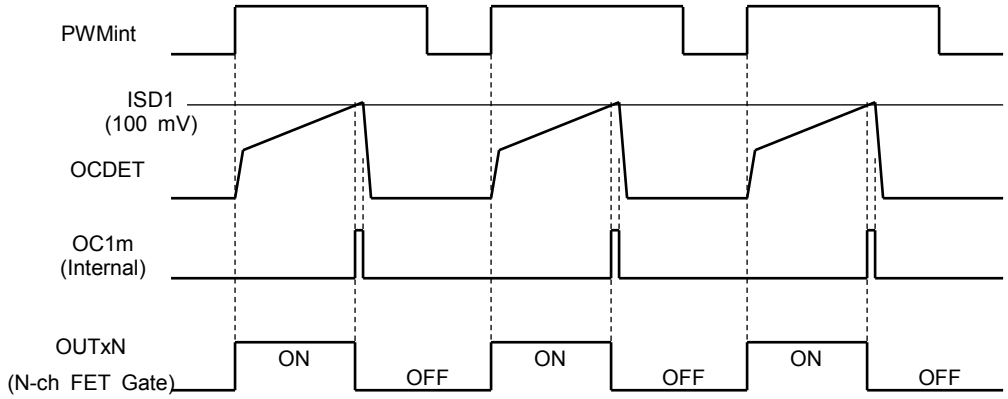
Functional Description

6-1-1. Current limiting operation (ISD1)

The TB9061AFNG detects a voltage of 100 mV at OCDET and limits the motor current by controlling the PWM duty cycle.

（1）When the internal signal PWMint becomes High, OUTxN turns on and a current runs through a motor. If the current exceeds ISD1, the TB9061AFNG changes the OC1m voltage to High and latches OUTxN off. When the current falls below the threshold while OUTxN is off, OC1m goes Low. The latch is then released at the next falling edge of PWMint and OUTxN is turned on again.

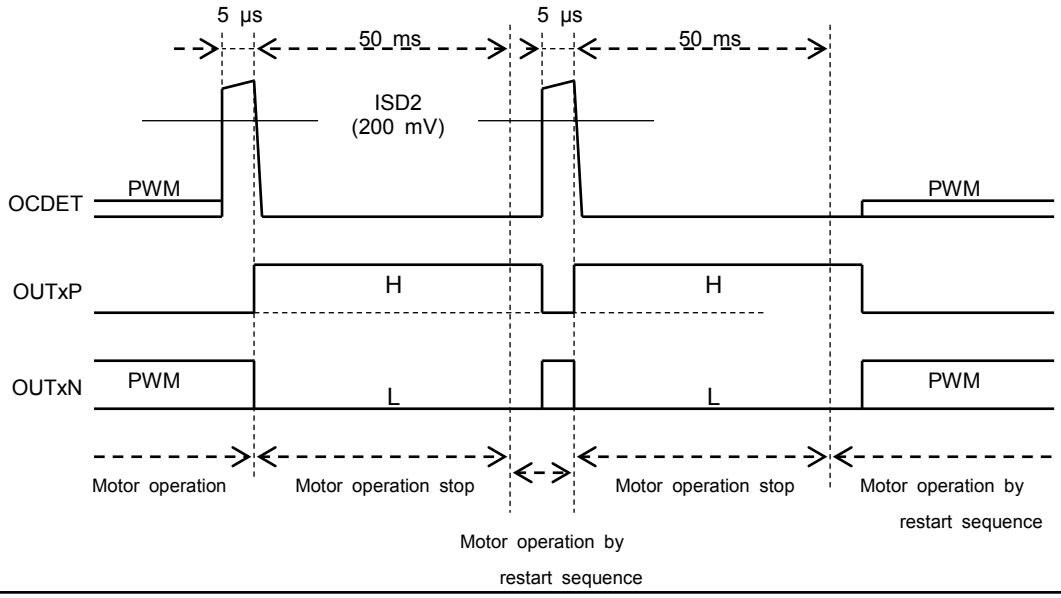
（2）When the load is so heavy that the motor current exceeds ISD1, the TB9061AFNG limits the motor current by reducing the duty cycle of the PWM output until it becomes lower than that of PWMint.



Notes: The current limit operation (ISD1) cannot be used when the PWM input duty is 85% or more (PWMint = 100%) or the ASIG input voltage is VREG*0.85V or more (PWMint = 100%). If the current limit operation occurs when the PWM input is 85% or more or the ASIG input voltage is VREG*0.85V or more, the motor may be loss-of-synchronism. When you use current limit operation, please set the PWM input duty to less than 85% and ASIG input voltage to less than VREG*0.85V.

6-1-2. Overcurrent Detection (ISD2)

If the TB9061AFNG detects a voltage of 200 mV or higher at OCDET for more than 5 μs, it stops motor rotation. It starts motor driving again 50 ms after the OCDET voltage becomes less than 200 mV. However, if the TB9061AFNG detects a current with a voltage higher than ISD2 for more than 5 μs after restart, it stops motor rotation again for 50 ms. This cycle is repeated until the overcurrent is eliminated. When the TB9061AFNG detects a current with a voltage higher than ISD2 for more than 5μs, the data measured and calculated from the values of PSIG and ASIG are cleared and the PWMint duty cycle is reset to 0%. The TB9061AFNG resumes from re-measurement after 50 ms.



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Functional Description

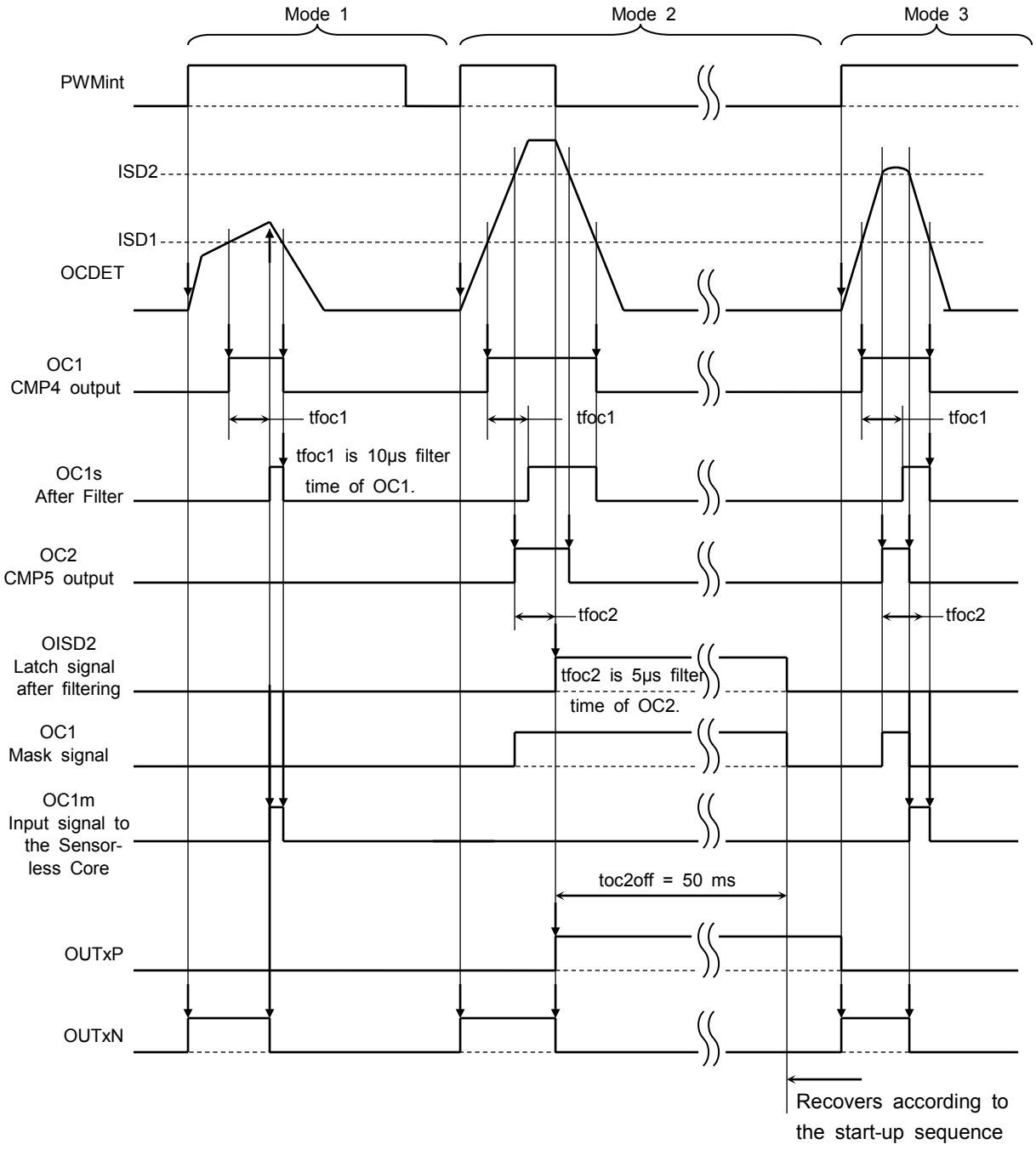
6-1-3. Relations between the overcurrent detection values, ISD1 and ISD2

Both ISD1 and ISD2 are active in normal operation. The relation between ISD1 and ISD2 in the operation is described as follows.

-Mode 1: In the case that the output load current is ≥ ISD1 or ≤ ISD2, the CMP4 asserts the OC1s and OC1m signals after the filtering time (tfoc1 = 10 μs) and the signals are sent to the Sensorless Core Logic. Refer to Section 6-1-1 for the function of the Sensorless Core Logic when the OC1m signal is generated.

-Mode 2: If a voltage higher than ISD2 is detected within the ISD1 filtering time (tfoc1 = 10 μs), the ISD1 detection signal is masked. If OC2 remains High for more than tfoc2 = 5 μs, the TB9061AFNG outputs OISD2 and turns off the motor output. After toc2off = 50 ms, OISD2 is deserted.

-Mode 3: If OC2 remains High for no longer than tfoc2 = 5 μs, the TB9061AFNG doesn't generate OISD2. Thus, the OC1 mask signal is disabled and OC1m is generated.



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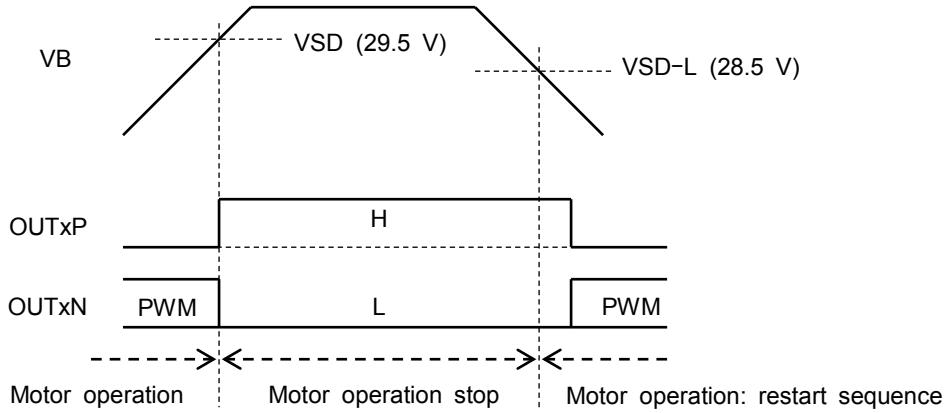
Functional Description

6. Detection of irregular operation (continued)

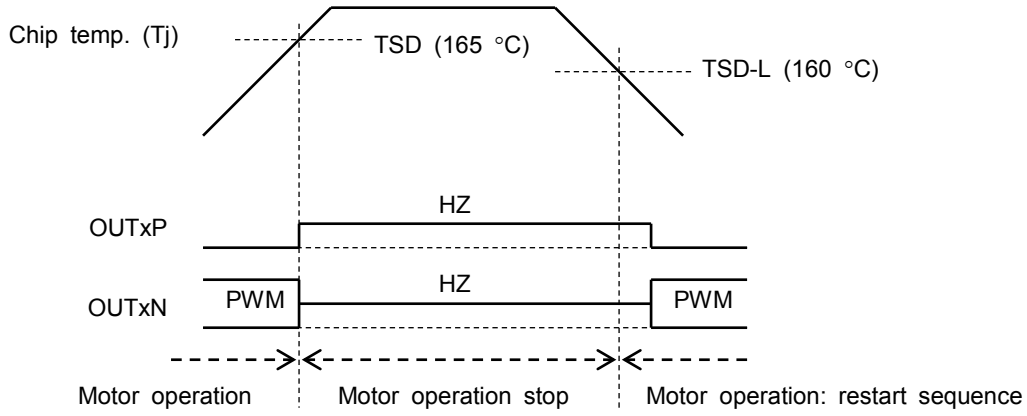
6-2. Overvoltage Detection (VSD)

If an overvoltage is applied to the VB pin, the TB9061AFNG stops the motor operation.
When the motor operation is stopped, the OUTxP pins become High and the OUTxN pins become Low.
When the TB9061AFNG detects an overvoltage, the data measured and calculated from the values of PSIG and ASIG are cleared and the PWMint duty cycle is reset to 0%. The TB9061AFNG resumes from re-measurement after the overvoltage condition is eliminated.



6-3. Over-temperature Detection

If the chip temperature exceeds the detection threshold temperature (TSD), the TB9061AFNG turns the outputs off (high-impedance state) and the motor operation stops. When the over-temperature condition is eliminated, the TB9061AFNG reverts to its normal operation following the start-up sequence.
When the TB9061AFNG detects an over-temperature, the data measured and calculated from the values of PSIG and ASIG are cleared and the PWMint duty cycle is reset to 0%. The TB9061AFNG resumes from re-measurement after the over-temperature condition is eliminated.



HZ: High-Impedance

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Functional Description

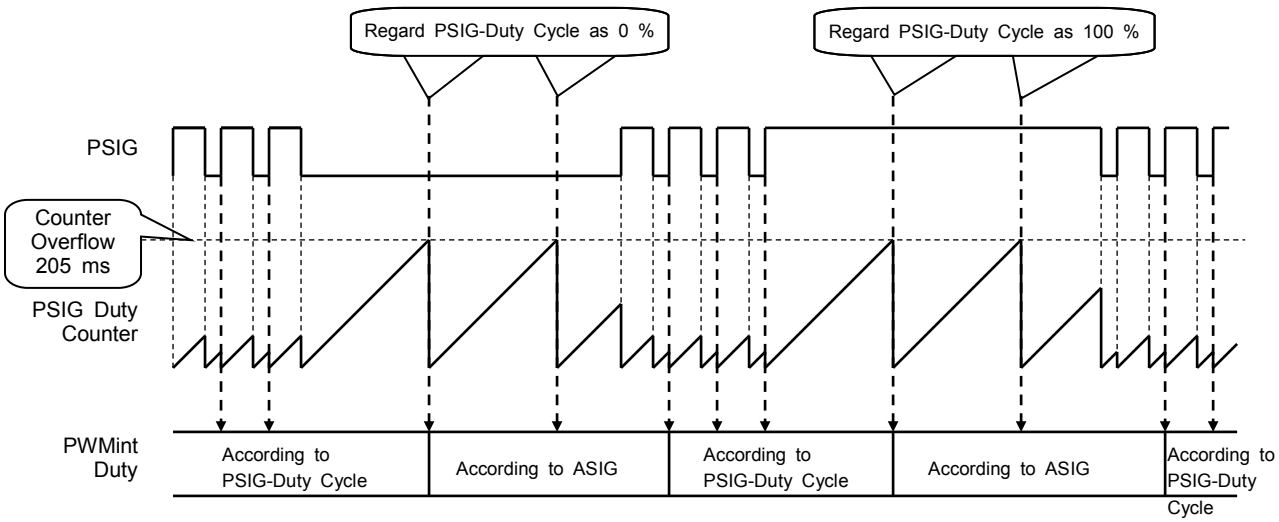
6. Detection of irregular operation (continued)

6-4. Detection of irregular PWM input

The PWM frequency range that can be applied to the PSIG pin is from 10 Hz to 1 KHz. If the TB9061AFNG separates from this range and a cycle abnormality detection value is reached , failure detection operation will be performed.

6-4-1. When the PWM cycle is too long

If the Low or High state of the PWM signal at PSIG continues for 205 ms or longer, the TB9061AFNG regards the PWM Duty cycle as 0 % or 100 % respectively. Thus, the PWMint duty cycle is determined according to the ASIG rate.



6-4-2. When the PWM cycle is too short

If the PSIG PWM cycle is less than 0.8 ms (more than 1.25 kHz), the TB9061AFNG regards it as an irregular cycle period and doesn't revise the data. Therefore, the PWM duty cycle is not changed from the one determined before the detection of irregular operation.

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Functional Description

7. Motor position detection timing

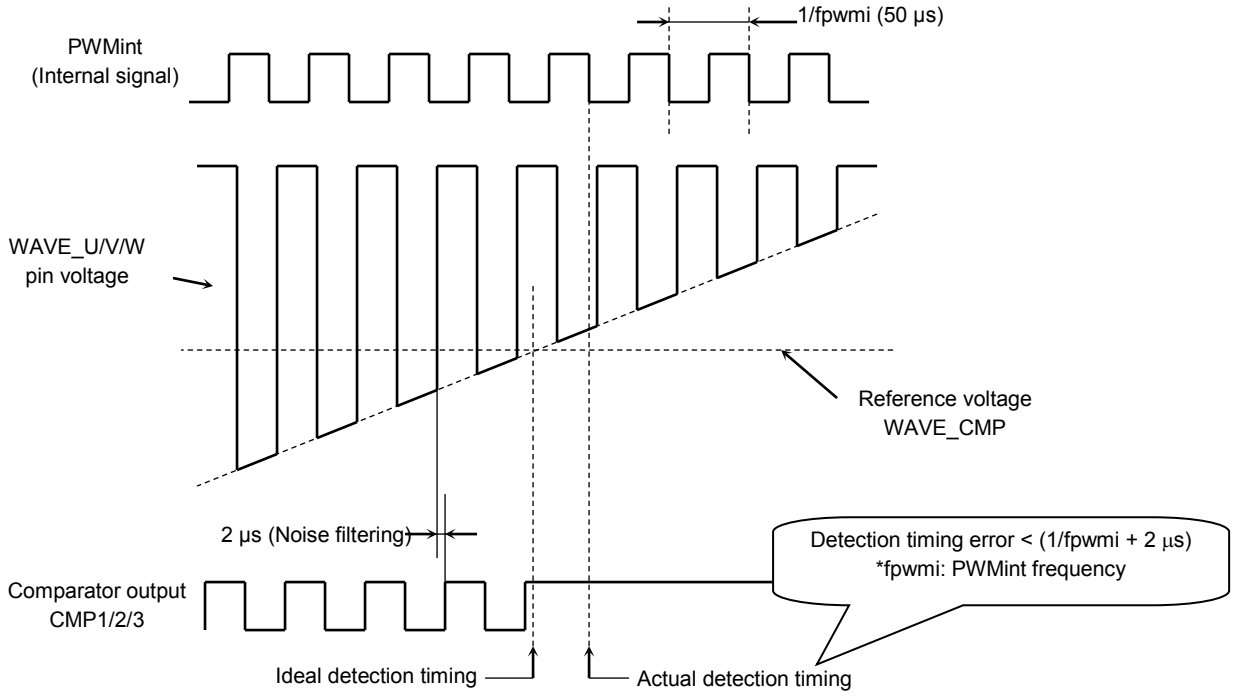
The TB9061AFNG detects the induced voltage from the WAVE_U/V/W pins at the internal comparators and receives it as position signals. When the PWMint duty cycle is less than 100 %, the TB9061AFNG determines the state of the WAVE_U/V/W voltage synchronizing with the PWMint signal. When the PWMint duty cycle is equal to 100 %, the TB9061AFNG determines the state of the WAVE_U/V/W voltage after the noise filtering period of 2 μs.

7-1. When the PWMint duty cycle is less than 100 %

The TB9061AFNG determines the output state (High or Low) of detection comparators synchronizing with the falling edge of the PWMint signal. The timing when the output state is determined as High is regarded as position detection timing and Sensorless Core Logic receives it.

Therefore a position detection timing error of (one clock period + 2 μs), at maximum, may occur. If PWMint is 20 kHz, the position detection timing error is 52 μs.

Caution is required when driving a motor of high-speed rotation.



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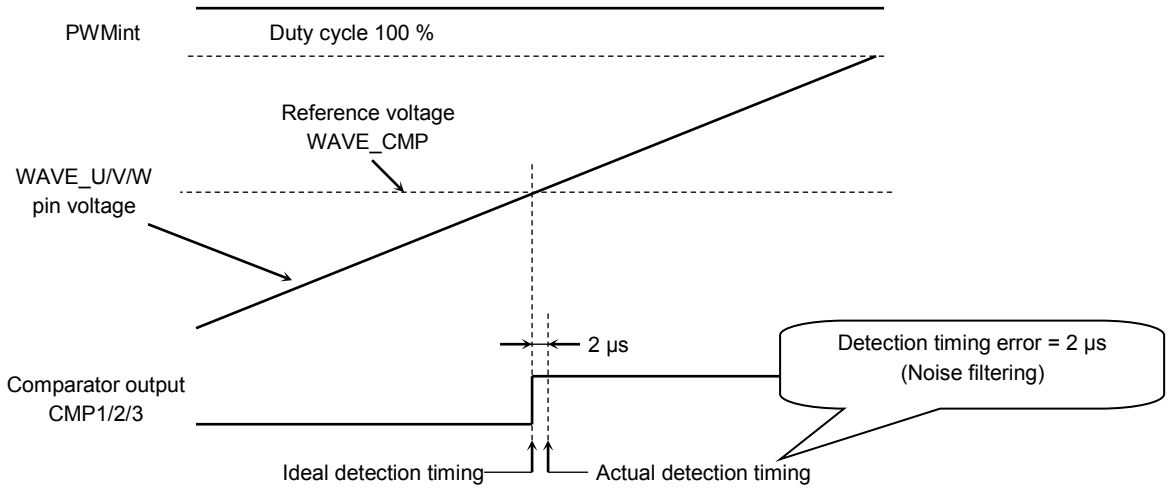
Functional Description

7-2. When the PWMint duty cycle is 100%

The Sensorless Core Logic receives the comparator output signals and determines them as position signals after the noise filtering period of 2μs.



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Functional Description

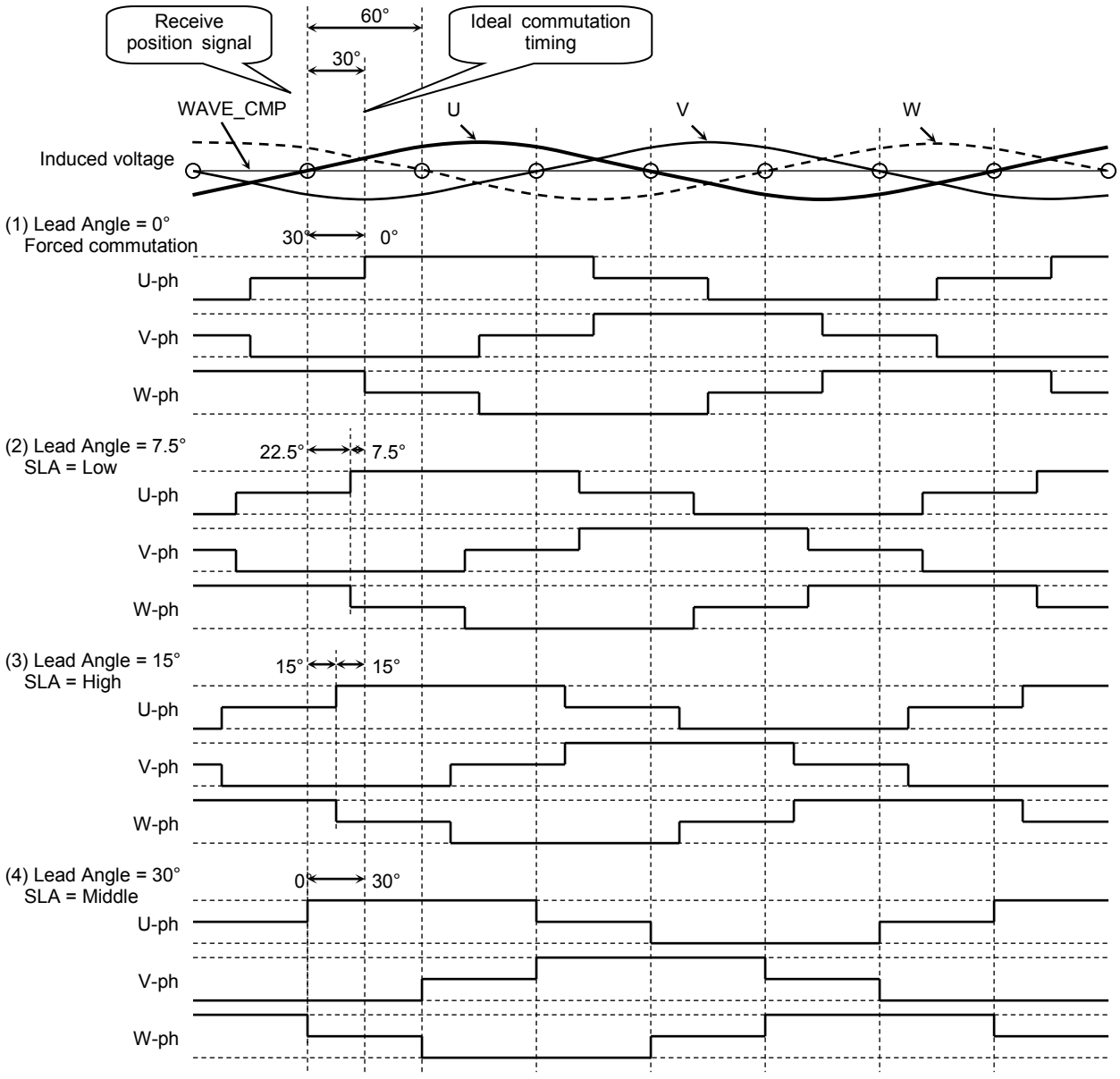
8. Lead angle control

The user can set a lead angle value at 7.5, 15 or 30 ° according to the setting of the SLA pin.

The SLA pin recognizes 3 types of input. When SLA is Low, lead angle is set to 7.5 °. When SLA is High, lead angle is 15 ° set. When SLA is Middle or open, lead angle is set to 30 °.

If 7.5 or 15 ° is selected, the lead angle is set to 0 ° during the forced commutation. When the normal commutation is started, it is then changed to the value set by the SLA pin automatically.

If 30 ° is selected, the lead angle is set to 30 ° even during the forced commutation.



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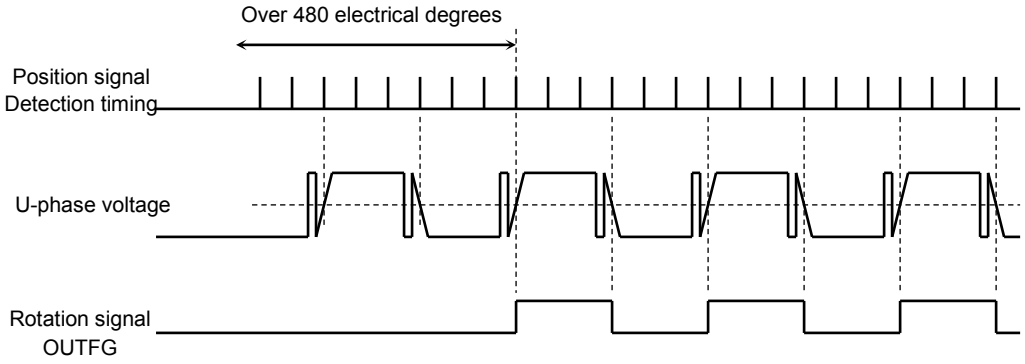
Functional Description

9. Rotational signal monitoring

The OUTFG pin outputs the signal to detect rotation speed and irregular operations, such as a motor lock-up. It is driven Low when a motor is stopped or during the forced commutation period at start-up. When the normal commutation state (under which the position signal detection is performed) continues for a period of more than 480 ° of motor electric angle, the OUTFG pin outputs the signal synchronized with the detected position signal of the U-phase.

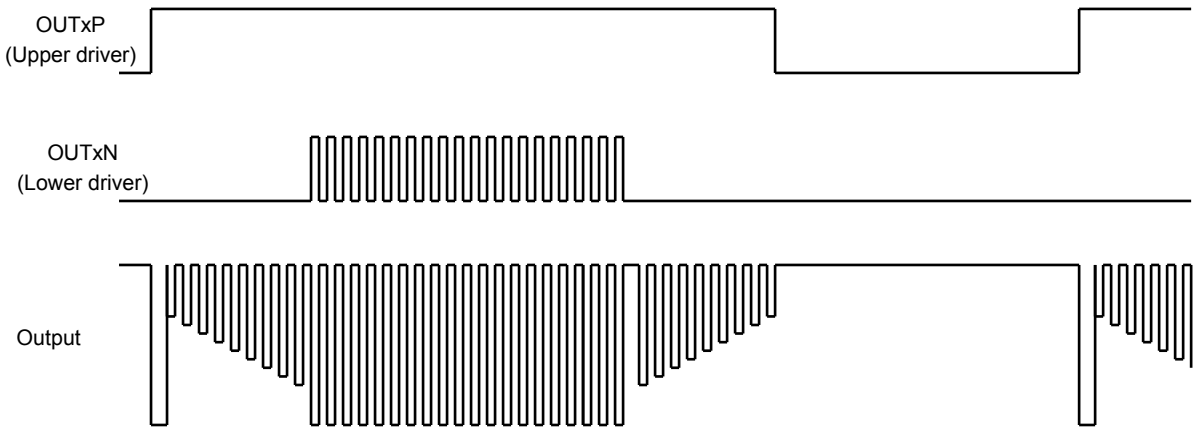
If the motor is locked during the rotation due to overload or other reasons, the TB9061AFNG performs start-up operation with the forced commutation and the OUTFG generates a Low-level voltage.

The irregular operation condition can be determined from the relations between the duty cycle of PWM signal and the rotation frequency.



10. PWM output

PWM control is applied only to the lower driver outputs (OUTUN, OUTVN, OUTWN), not to the upper driver outputs (OUTUP, OUTVP, OUTWP).



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Functional Description

11. Automatic restart control(Function that operates only for analog voltage input)

The sensorless system uses the induced voltage generated by the motor rotation as a position signal. Therefore, when the motor is started from the stop state where no induced voltage is generated, a loss of synchronism may occur for not being able to detect correct position signals.

There are two types of the loss of synchronism: a loss of synchronism for high-speed rotation, which occurs when a position signal is applied continuously resulting in the high-speed commutation; and a loss of synchronism for low-speed rotation, which occurs when a position signal can only be detected irregularly.

To avoid these faults, it is recommended to monitor the motor rotational signal, OUTFG, and restart the operation upon detecting improper frequency. The OUTFG signal can be monitored if the upstream component that generates a PWM signal exists. However, for the applications that perform fixed PWM control using the analog input without monitoring the OUTFG signal, the TB9061AFG incorporates the OUTFG monitoring function internally as well as the automatic restart control function.

The automatic restart control function only operates when an analog voltage is applied.

11-1 Automatic restart control upon detecting a loss of synchronism for high-speed rotation

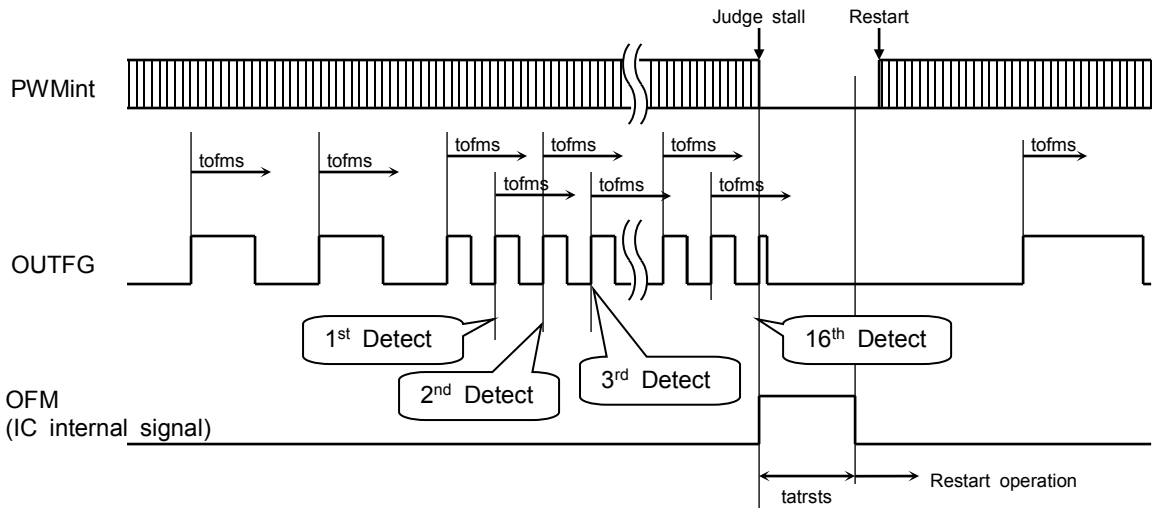
(1) When PWMint duty cycle = 100%

If the TB9061AFNG detects the OUTFG signal period of 800 μs (tofms1) or shorter for 16 times in a row, the TB9061AFNG judges that a loss of synchronism occurred and restarts the rotation. The TB9061AFNG performs a restart operation when the time tatrsts = 50 ms has elapsed after the detection of the loss of synchronism.

(2) When PWMint duty cycle < 100%

If the TB9061AFNG detects the OUTFG signal period of 3.2 ms (tofms2) or shorter for 16 times in a row, the TB9061AFNG judges that a loss of synchronism occurred and restarts the rotation. The TB9061AFNG performs a restart operation when the time tatrsts = 50 ms has elapsed after the detection of the loss of synchronism.

Automatic restart control upon detecting a loss of synchronism for high-speed rotation



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Functional Description

11. Automatic **restart control (continued) (Function that operates only for analog voltage input)**

11-2. Automatic restarting control upon detecting a loss of synchronism for low-speed rotation

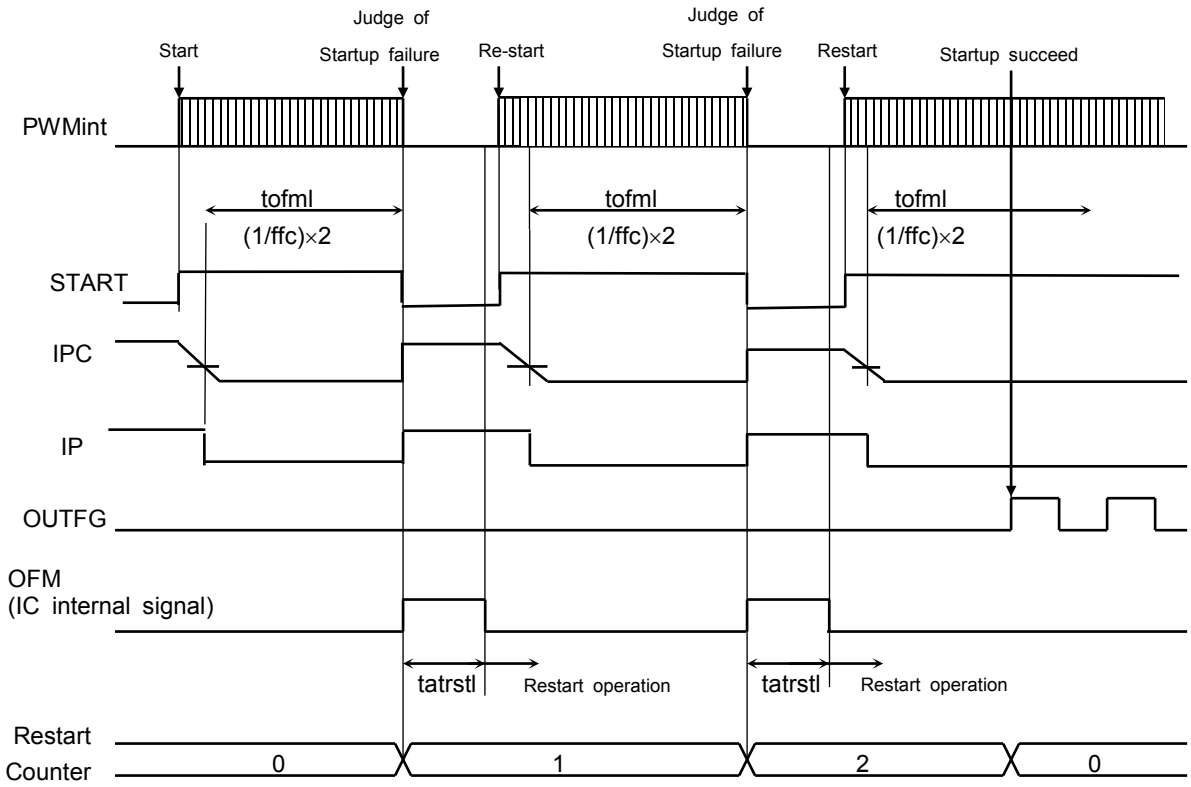
Both when PWMint = 100% and when PWMint < 100%

If the TB9061AFNG cannot detect any OUTFG signal for two cycle periods of forced commutation signal after 1 phase excitation, the TB9061AFNG judges that a startup operation has failed and performs automatic restart control operation. The TB9061AFNG performs restart operation when the time tatrstl = 50 ms has elapsed after the detection of the startup failure.

If the TB9061AFNG detects the same failure pattern 8 times in a row, the motor control function is latched so that the motor remains in the halt state.

For releasing the latch, the user has to set the DIS pin high or turn the VB power supply back on after turning it off.

Automatic restart control upon detecting a loss of synchronism for low-speed rotation



Note: The motor current might rush to the FET during the DC excitation.
Please decide the DC excitation time setting for un-break-ness or not deterioration by the repeating 1 phase excitation.

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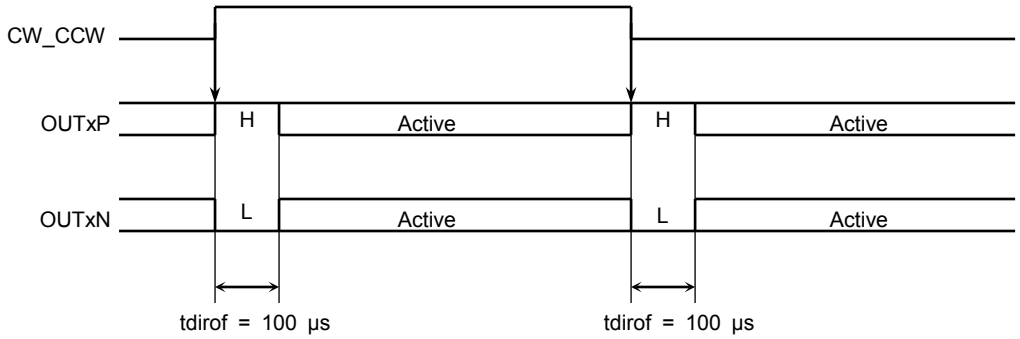
12. CW/CCW switching control

The TB9061AFNG provides a 100 µs OFF-time for preventing shoot-through current in the external MOSFETs upon changing the rotation direction between CW and CCW. The external P-ch/N-ch MOSFETs are turned off for 100 µs.



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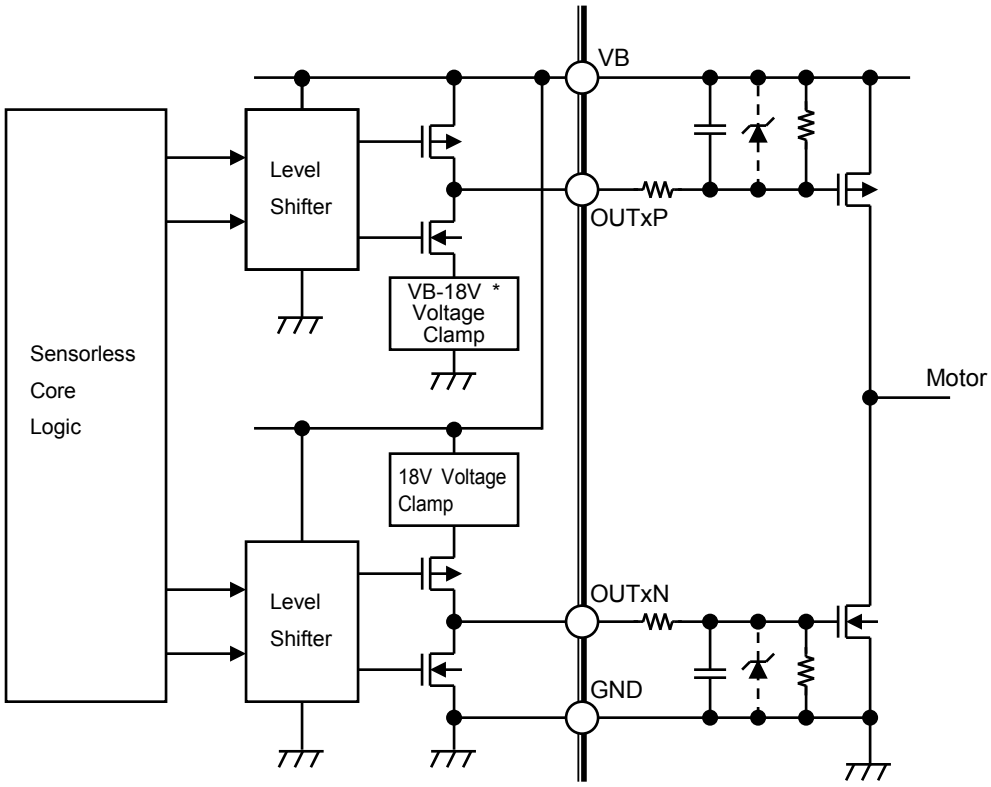
Functional Description

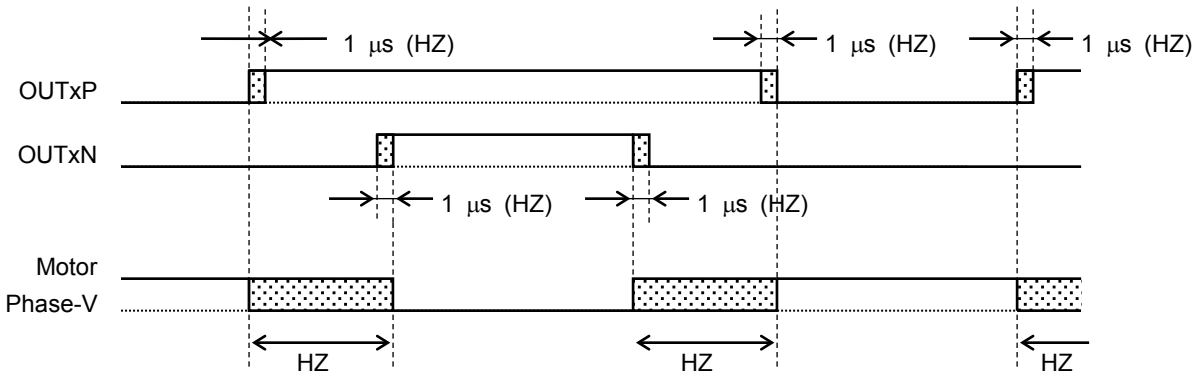
13.Pre-driver output

Pre-drivers have a half-bridge output to drive external MOSFETs by using the output signal from the Sensorless Core Logic. The TB9061AFNG provides a 1 μs OFF-time for preventing shoot-through current upon output switching between High and Low.

In addition, the TB9061AFNG incorporates an 18 V voltage clamp circuit for the protection of the external MOSFET gates. So the gate-to-source voltage of a MOSFET can be limited to 20 V or lower even when the high-voltage power supply is used. When Zener diodes are required to deal with sudden changes in the power supply or to conform to the application requirements, the user can use small-power Zener diodes.



Pre-driver's OFF-time upon output switching



HZ: High-Impedance

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Absolute Maximum Ratings (Ta = 25°C)(Note 1)

Characteristics	Symbol	Adaptable Pins	Rating	Unit
Power supply voltage	VB	VB	-0.3~40	V
	VREG	VREG	-0.3 to 6	
	VDD	VDD	-0.3 to 6	
Input voltage	VIN1	PSIG	-0.3 to 40(0.2s)	V
			-0.3 to 30	
	VIN2	WAVE_CMP, WAVE_U, WAVE_V, WAVE_W	-0.3 to 40(0.2s)	
			-0.3 to 30	
	VIN3	ASIG, SFCF, SLA, IPC, DIS, OCDET	-0.3 to VREG	
	VIN4	CW_CCW, TEST	-0.3 to VDD	
Output current	IOUT1	OUTUP, OUTVP, OUTWP, OUTUN, OUTVN, OUTWN	±20	mA
	IOUT2		±200 (5 μs)	
	IOUT3	OUTFG	±1	
	ILOAD	VREG	-10	
Output voltage	VOUT1	OUTUP, OUTVP, OUTWP, OUTUN, OUTVN, OUTWN	-0.3 to VB	V
	VOUT2	OUTFG	-0.3 to VDD	
Storage temperature	Tstg		-55 to +150	°C
Power dissipation	PD		0.89 (Note 2)	W

Note 1: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded during operation, even for an instant. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may damage any other equipment. Applications using the device should be designed such that the absolute maximum ratings will never be exceeded in any operating conditions. The device must be used within the specified operating range.

Note 2: Mounted on a board (50 × 50 × 1.6 mm, Cu: 40%) when Ta = 25°C.

Electrical Characteristics

Operating Range

Characteristics	Symbol	Operating Range	Unit	Remarks
Power supply voltage	VB	18 to 27	V	Keep controlling motor Outside of Electrical Characteristics assurance
		5.5 to 18	V	Recommended operating voltage range with all spec parameters warranted
		5.0 to 5.5	V	Keep controlling motor Outside of Electrical Characteristics assurance
	VDD	4 to 5.5	V	
Operating temperature	Topr	-40 to 125	°C	Ta (Ambient temperature)
		-40 to 150	°C	Tj (Junction temperature)
Input PWM frequency	PWM	10 to 1 k	Hz	
Input PWM duty cycle	PWMD	0 to 100	%	

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Electrical Characteristics (VB = 5.5 to 18 V, VDD = VREG, Ta = -40 to 125°C, unless otherwise specified.)

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
DC characteristics							
Current consumption	IB	VB	VB = 5.5 to 16 V	—	—	5	mA
Signal input							
Threshold voltage	VIH	PSIG		—	VREG × 0.62	—	V
	VIL			—	VREG × 0.58	—	
Input hysteresis voltage	dVTH	PSIG		—	0.2	—	V
Noise filter	tfpsig	PSIG		—	10	—	μs
Input current	IIH	PSIG	VIN = 16 V	—	64	—	μA
	IIL		VIN = 0 V	-5	—	5	
Input current	IIH	ASIG	VIN = VREG	-5	—	5	μA
	IIL		VIN = 0 V	-40	-20	-10	
Input current	IIH	SFCF	VIN = VREG	28	57	112	μA
	IIL		VIN = 0 V	-90	-45	-23	
Input voltage	VIN			—	VREG × 0.44	—	V
Threshold voltage	VIH	SLA		VREG× 0.75	—	VREG	V
	VIM			VREG× 0.35	—	VREG× 0.65	
	VIL			0	—	VREG× 0.25	
Input current	IIH	SLA	VIN = VREG	25	50	100	μA
	IIL		VIN = 0 V	-100	-50	-25	
Threshold voltage	VIH	DIS		—	VREG× 0.52	—	V
	VIL			—	VREG× 0.48	—	
Input hysteresis voltage	dVTH	DIS		0.15	0.2	0.25	V
Input current	IIH	DIS	VIN = VREG	10	20	40	μA
	IIL		VIN = 0 V	-5	—	5	
Input voltage	VIH	CW_CCW		VDD x 0.8	—	VDD	V
	VIL			0	—	VDD x 0.2	
Input current	IIH	CW_CCW	VIN = VDD	10	20	40	μA
	IIL		VIN = 0 V	-5	—	5	
Output voltage	VOH	OUTFG	IOH = -1 mA	VDD x 0.8	—	VDD	V
	VOL		IOL = 1 mA	0	—	VDD x 0.2	
Regulator/Reset							
5-V output voltage	VREG	VREG	ILOAD = 1 to 10 mA	4.85	5.0	5.15	V
Current limiter	Ilimit	VREG		25	50	—	mA
Reset detect voltage	VRST	VREG		4.0	4.2	4.4	V
Reset release voltage	VRST_R	VREG		—	4.4	—	V
Hysteresis of detect voltage	dVRST	VREG		—	0.2	—	V
Power-on reset	TPR	VREG		0.8	1	1.2	ms

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Electrical characteristics (VB = 5.5 to 18 V, VDD = VREG, Ta = -40 to 125°C, unless otherwise specified.)

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Pre-driver							
Output voltage	VOH	OUTUP OUTVP OUTWP	IOH = -1 mA	VB-0.2V	–	–	V
			IOH = -20 mA	VB-0.5V	–	–	
	VOL		VB = 5.5 to 16 V, IOL = 1 mA	–	–	0.2	V
			VB = 5.5 to 16 V, IOL = 20 mA	–	–	0.5	
	VOH	OUTUN OUTVN OUTWN	VB = 5.5 to 16 V, IOH = -1 mA	VB-0.2V	–	–	V
			VB = 5.5 to 16 V, IOH = -20 mA	VB-0.5V	–	–	
	VOL		IOL = 1 mA	–	–	0.2	V
			IOL = 20 mA	–	–	0.5	
Output leakage current	ILEAK	OUTUP,OUTVP, OUTWP	VOUT = VB	-10	–	10	µA
			VB = 5.5 to 16 V, VOUT = 0 V	-10	–	10	
		OUTUN,OUTVN, OUTWN	VB = 5.5 to 16 V, VOUT = VB	-10	–	10	µA
			VOUT = 0 V	-10	–	10	
Propagation delay time	tpLH	OUTUP, OUTVP, OUTWP, OUTUN, OUTVN, OUTWN	Sensorless Core Logic output to OUTxx	–	–	4	µs
	tpHL			–	–	4	
Comparator							
Input offset voltage	VIO	WAVE_CMP WAVE_U WAVE_V WAVE_W		-10	–	10	mV
Common input voltage range	CMVIN			2	–	VB - 2	V
Input current	IIN		VIN = 0 to VB	-1	–	1	µA
Input filter	Tfilc			–	2	–	µs
Clock, PWM							
Oscillating frequency	fosc			4.10	5.12	6.14	MHz
PWM frequency	fpint			16	20	24	kHz
Detection function							
Overvoltage detection	VSD	VB	Detect	28	29.5	31	V
	VSD-L		Release	27	28.5	30	
Overvoltage hysteresis	dVSD			–	1.0	–	
Overcurrent detection 1	ISD1	OCDET		80	100	120	mV
Overcurrent detection 2	ISD2	OCDET		180	200	220	mV
Overtemperature detection	TSD		Detect	–	165	–	°C
	TSD-L		Release	–	160	–	
Overtemperature hysteresis	dTSD			–	5	–	
PSIG cycle period detection	TPLO	PSIG	Low-level period	–	205	–	ms
	TPHO		High-level period	–	205	–	
	TPCU		Cycle period	–	0.8	–	
IP Control							
Threshold voltage	VTH	IPC		–	VREG × 0.6	–	V
Charge current	Ichg		VIN = VREG to VTH	–	10	–	µA
DC excitation time	TIP	–		–	200 × CIP	–	ms

*The unit of CIP is µF.

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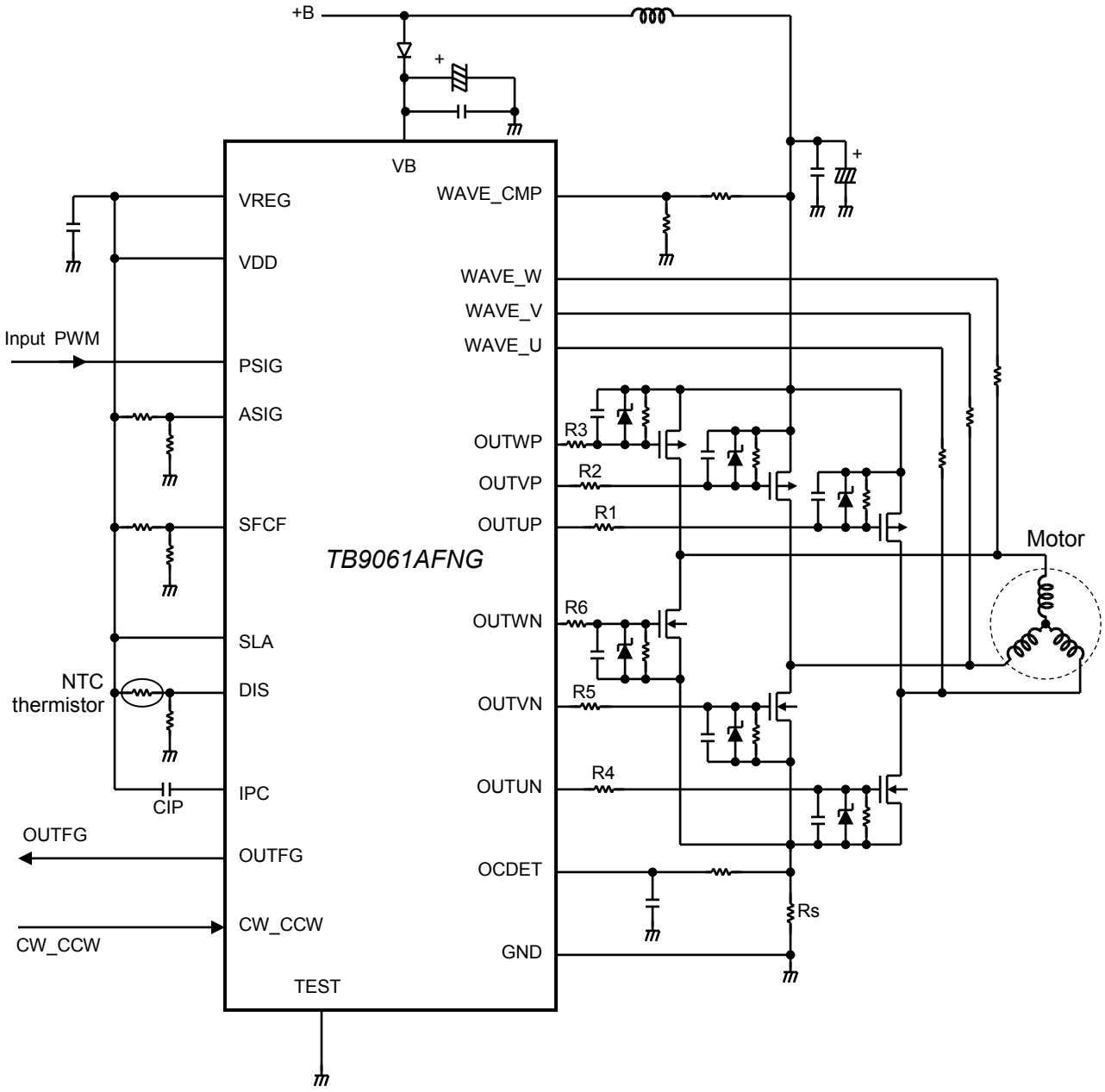
Application Examples

Example of the entire PWM input control circuit

- Output PWM duty cycle: Determined by the PSIG PWM duty cycle
- Lead angle: 15°
- With DC excitation control



Note1:The capacitor connected to the Source pin of the Pch FET is for absorbing disturbance noise, voltage fluctuation by load change, etc. Connect it as close to the Source pin of the Pch FET as possible.
Note2: We recommend more than 100 Ω from R1 to R6 as the external resistance of pre-driver output pin.

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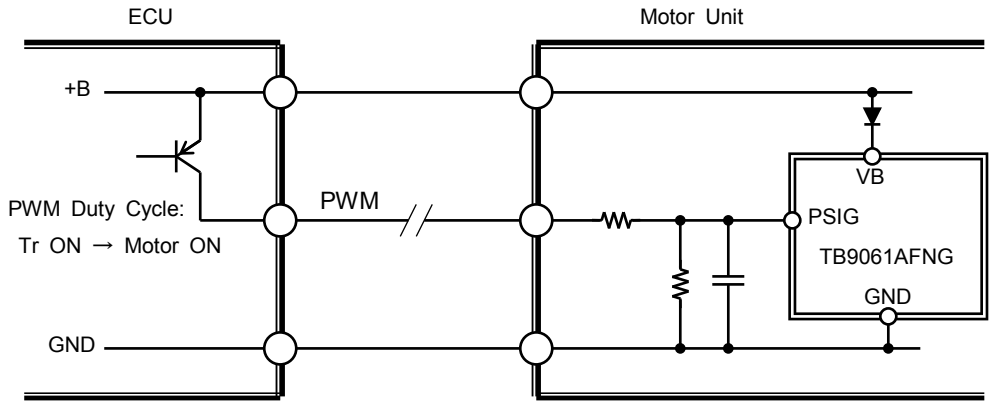
Application examples

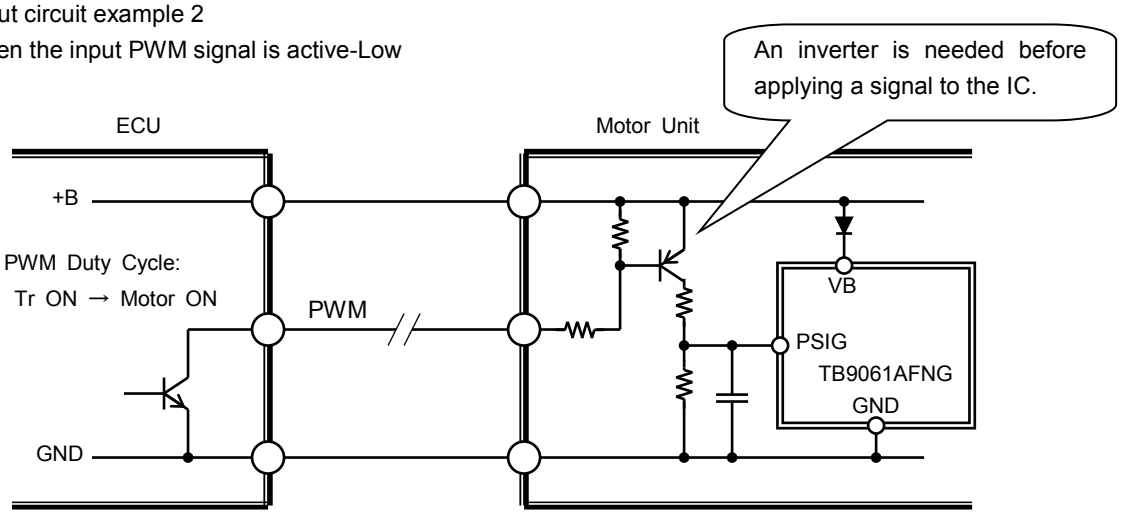
PWM input circuit example 1

When the input PWM signal is active-High



PWM input circuit example 2

When the input PWM signal is active-Low



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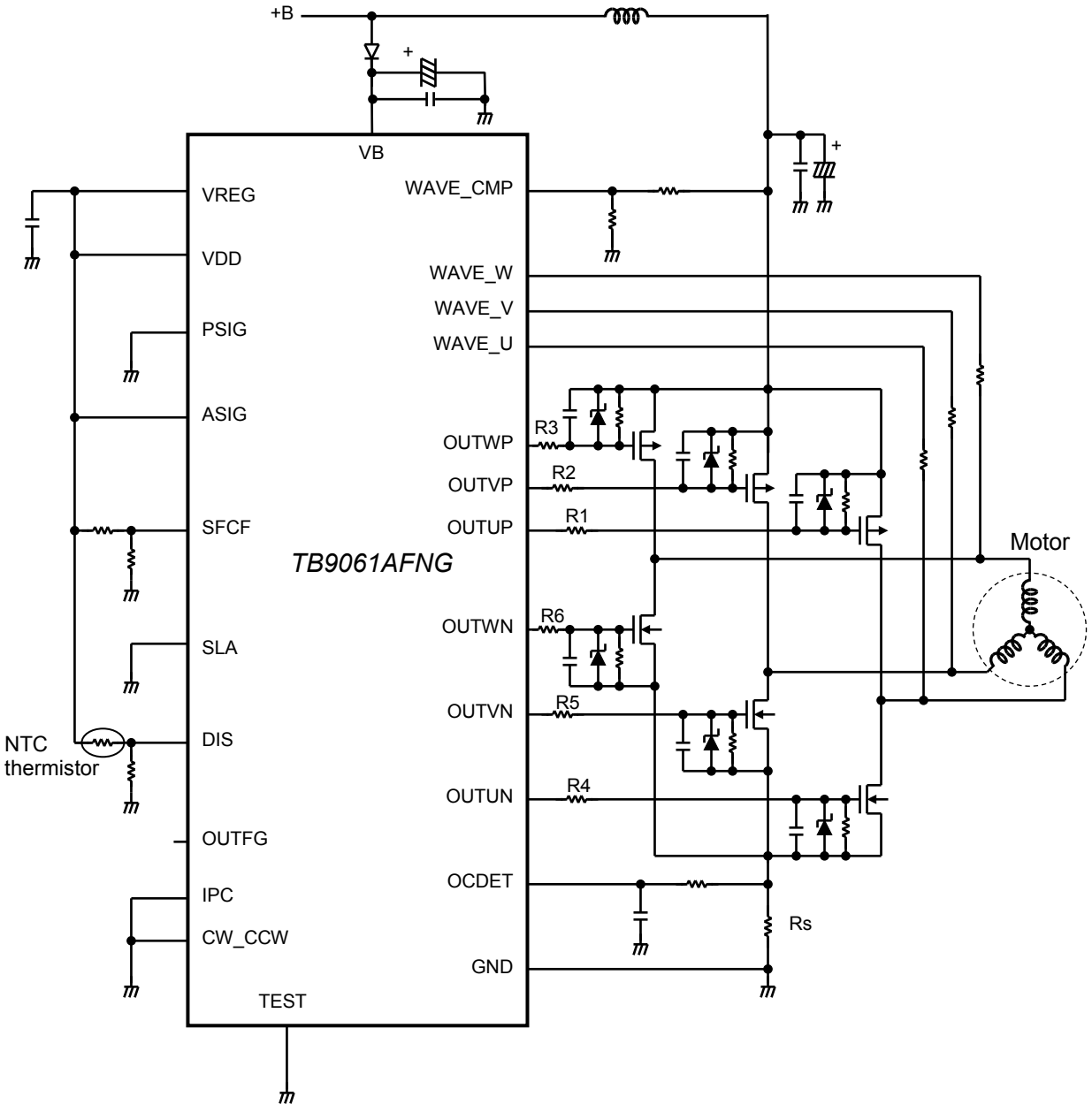
Application Examples

Circuit example with fixed PWM duty cycle (for high-speed rotation)

- Output PWM duty cycle: Determined by the ASIG rate (100%)
- Lead angle: 7.5°
- Without DC excitation control
- Fixed to CW mode



Note1: The capacitor connected to the Source pin of the Pch FET is for absorbing disturbance noise, voltage fluctuation by load change, etc. Connect it as close to the Source pin of the Pch FET as possible.

Note2: We recommend more than 100 Ω from R1 to R6 as the external resistance of pre-driver output pin.

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Notes

Note 1: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Note 2: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Note 3: Timing charts may be simplified for explanatory purposes.

Note 4: Ensure that the IC is mounted correctly as specified. Failing to observe the correct mounting procedure or requirements may damage the IC or target equipment.

Note 5: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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Note 6: Utmost care is necessary in the design of the output OUTXX, VB ,VDD and GND lines since the IC may be destroyed in case of a short-circuit across outputs, a short-circuit to power supply, or a short-circuit to ground.

Note 7: Please use to make a short both VREG and VDD always.
Possibly make a malfunction to potential difference occurs between VREG and VDD.

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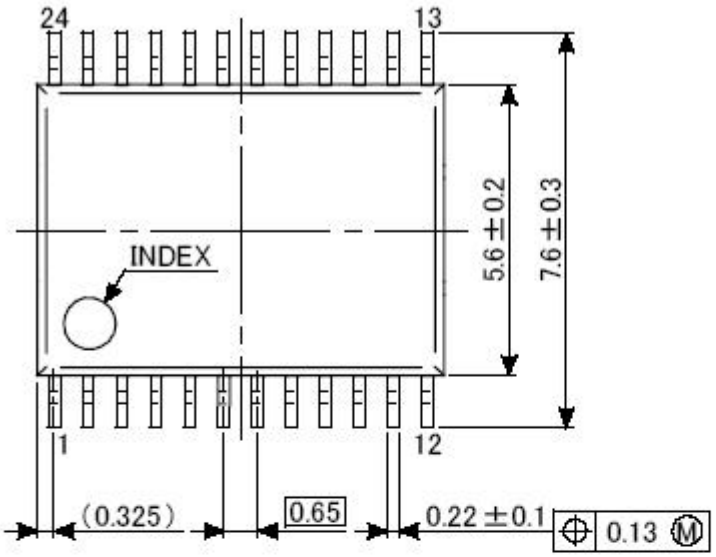
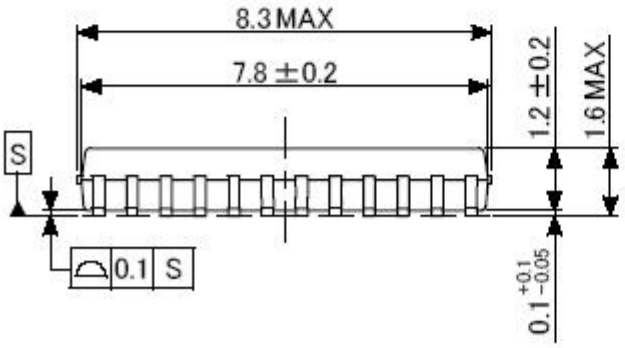
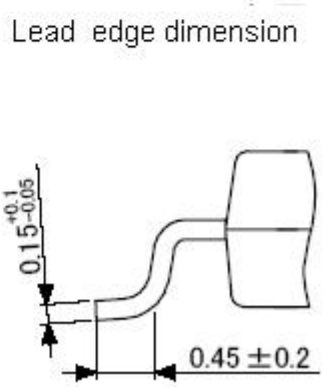
Package Dimensions

Unit:mm







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