# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 40 | V |
| $V_{GS}$ | Gate- source voltage | ±20 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25°C | 120 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$=100°C | 120 | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 480 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25°C | 300 | W |
| dv/dt(3) | Peak diode recovery voltage slope | 6 | V/ns |
| $E_{AS}$ (4) | Single pulse avalanche energy | 1.2 | J |
| $T_j$ | Operating junction temperature range | - 55 to 175 | °C |
| $T_{stg}$ | Storage temperature range | | |

**Notes:**

(1)Current limited by package

(2)Pulse width limited by safe operating area.

(3)$I_{SD}$ ≤120 A, di/dt ≤300A/µs, $V_{DD}$ =$V_{(BR)DSS}$, Tj ≤ $T_{JMAX}$

(4)Starting Tj = 25 °C, $I_D$ = 60 A, $V_{DD}$ = 30 V.

**Table 3: Thermal data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | D²PAK | TO-220 | |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.5 | | °C/W |
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 35 | | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | | 62.5 | °C/W |

**Notes:**

(1)When mounted on a 1-inch² FR-4 board, 2oz Cu.

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4: On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 V | 40 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V $T_C$ = 125°C(1) | | | 10 | µA |
| $I_{GSS}$ | Gate body leakage current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS}$ = 10 V, $I_D$= 50 A | | 4.3 | 4.6 | mΩ |

**Notes:**

(1)Defined by design,not subject to production test

**Table 5: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 5100 | | pF |
| $C_{oss}$ | Output capacitance | | - | 1300 | | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 160 | | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 32 V, $I_D$ = 120 A , $V_{GS}$ = 10 V (see *Figure 21: "Test circuit for gate charge behavior"*) | - | 110 | 150 | nC |
| $Q_{gs}$ | Gate-source charge | | - | 35 | | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 70 | | nC |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 20 V, $I_D$ = 60 A , $R_G$ = 4.7 Ω ,$V_{GS}$ = 10 V (see *Figure 20: "Test circuit for resistive load switching times"* and *Figure 25: "Switching time waveform"*) | - | 35 | | ns |
| $t_r$ | Rise time | | - | 220 | | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 80 | | ns |
| $t_f$ | Fall time | | - | 50 | | ns |

**Table 6: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 120 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 480 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 120 A, $V_{GS}$ = 0 V | - | | 1.3 | V |
| $t_r$ | Reverse recovery time | $I_{SD}$ = 120 A, $V_{DD}$ = 20 V, di/dt = 100 A/µs V, $T_j$ = 150 °C (see *Figure 22: "Test circuit for inductive load switching and diode recovery times"*) | - | 75 | - | ns |
| $t_{d(off)}$ | Reverse recovery charge | | - | 185 | - | nC |
| $t_f$ | Reverse recovery current | | - | 5 | - | A |

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2: Power dissipation vs. temperature

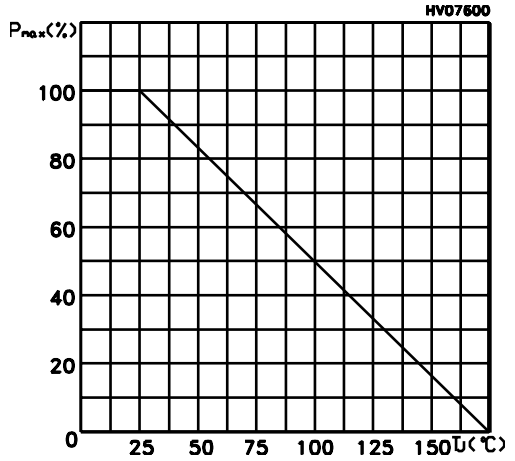



Figure 3: Max Id current vs. temperature

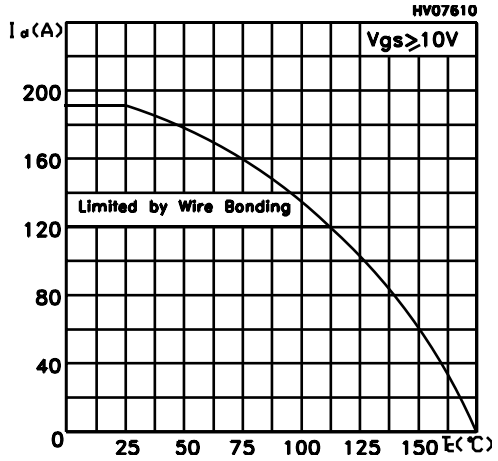



Figure 4: Output characteristics

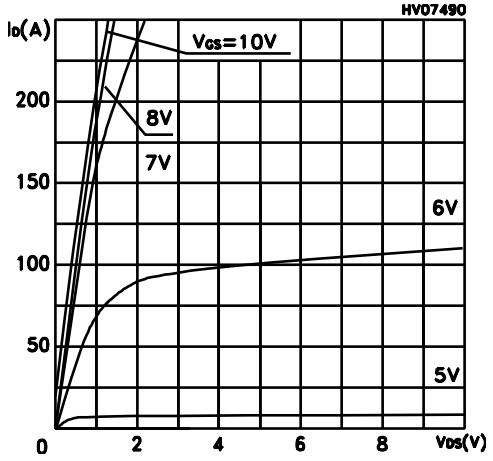



Figure 5: Transfer characteristics

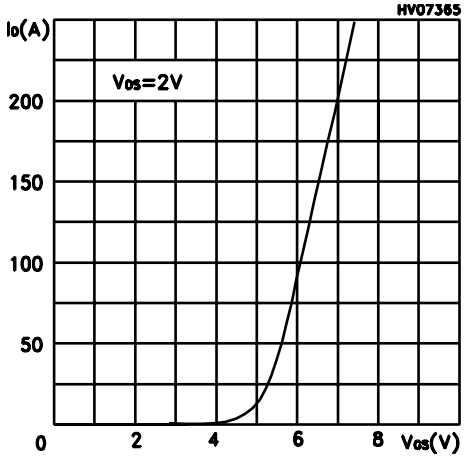



Figure 6: Transconductance

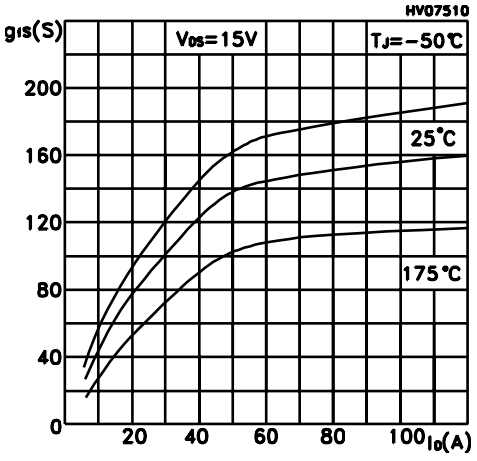



Figure 7: Static drain-source on-resistance

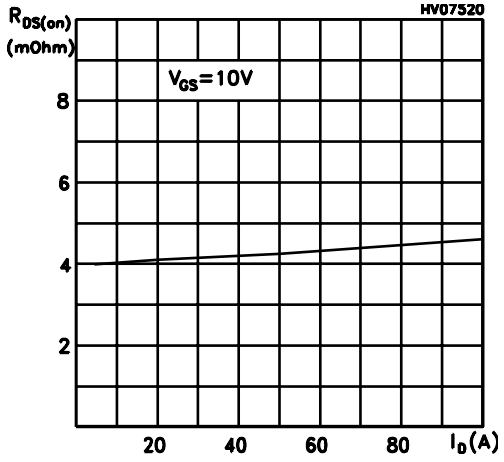


Figure 8: Gate charge vs. gate-source voltage

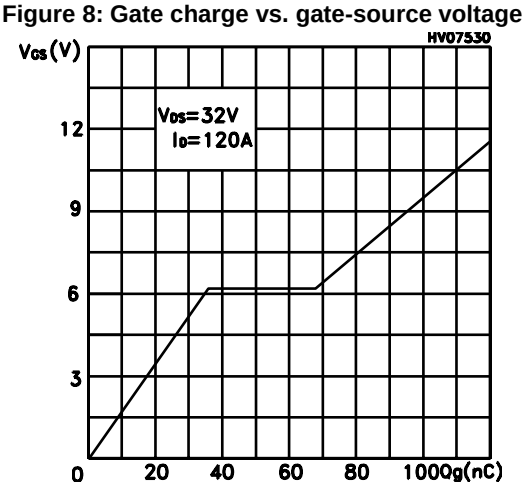



Figure 9: Capacitance variations

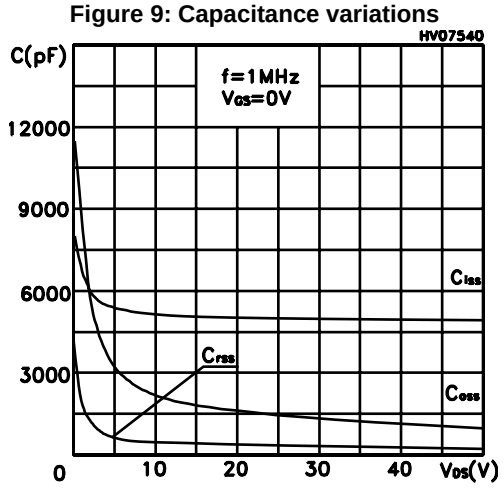



Figure 10: Normalized gate threshold voltage vs. temperature

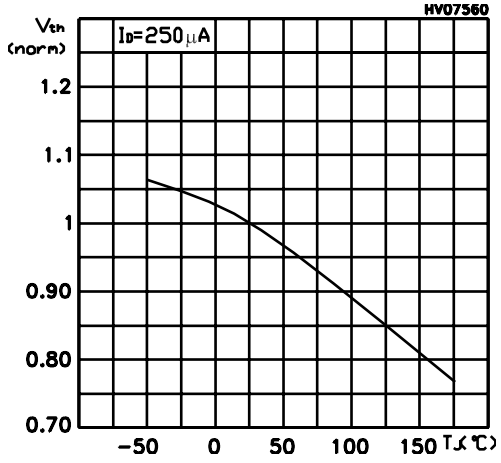



Figure 11: Normalized on-resistance vs. temperature

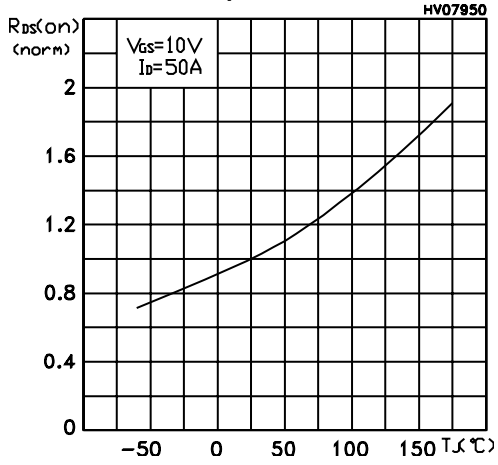



Figure 12: Source-drain diode forward characteristics

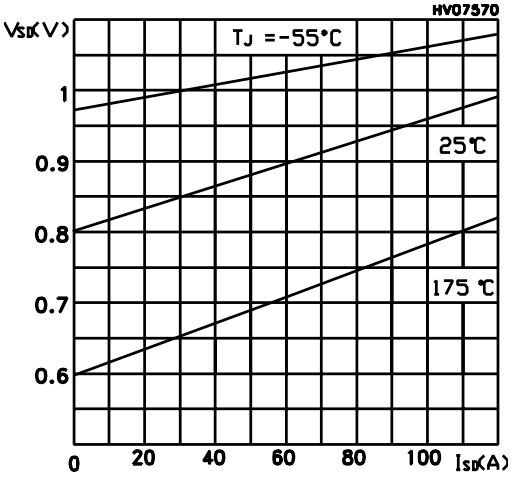



Figure 13: Normalized BVDSS vs. temperature

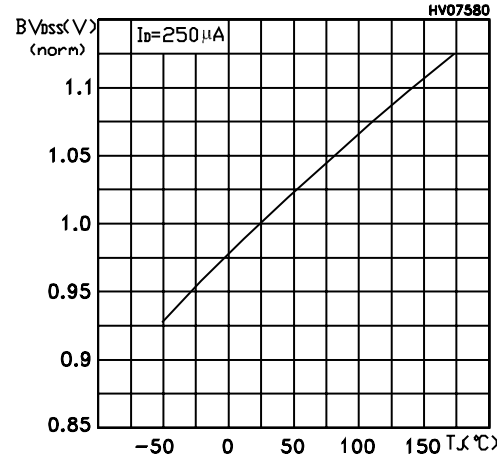


**Figure 14: Thermal resistance Rthj-pcb vs. PCB copper area**

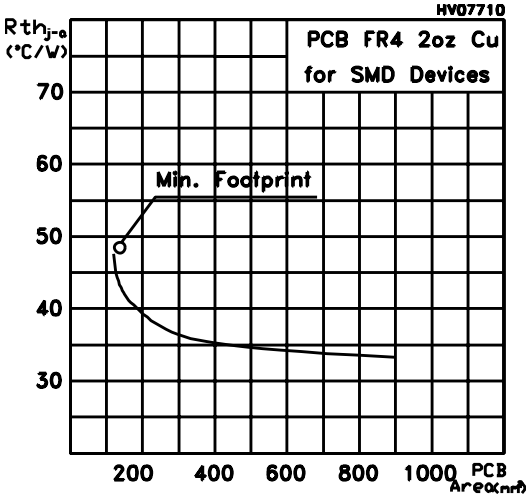



**Figure 15: Thermal impedance**

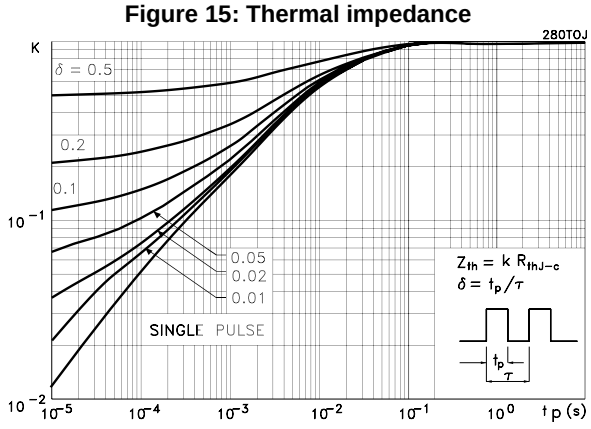



**Figure 16: Max power dissipation vs. PCB copper area**

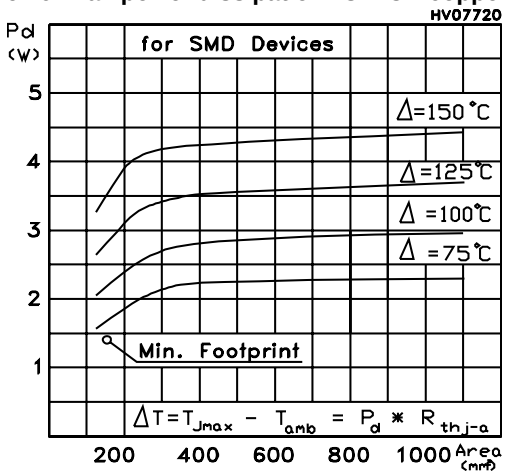



**Figure 17: Safe operating area**

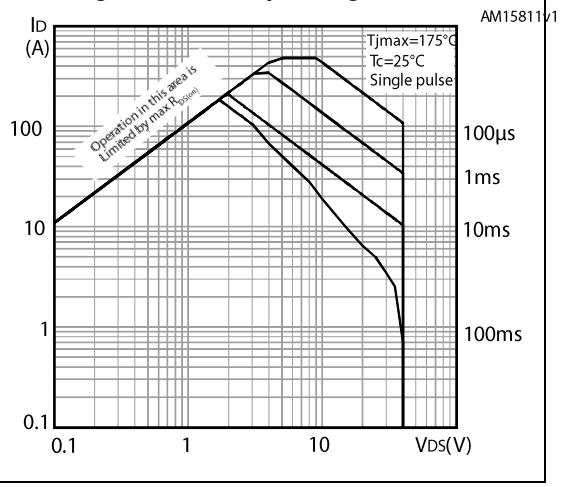
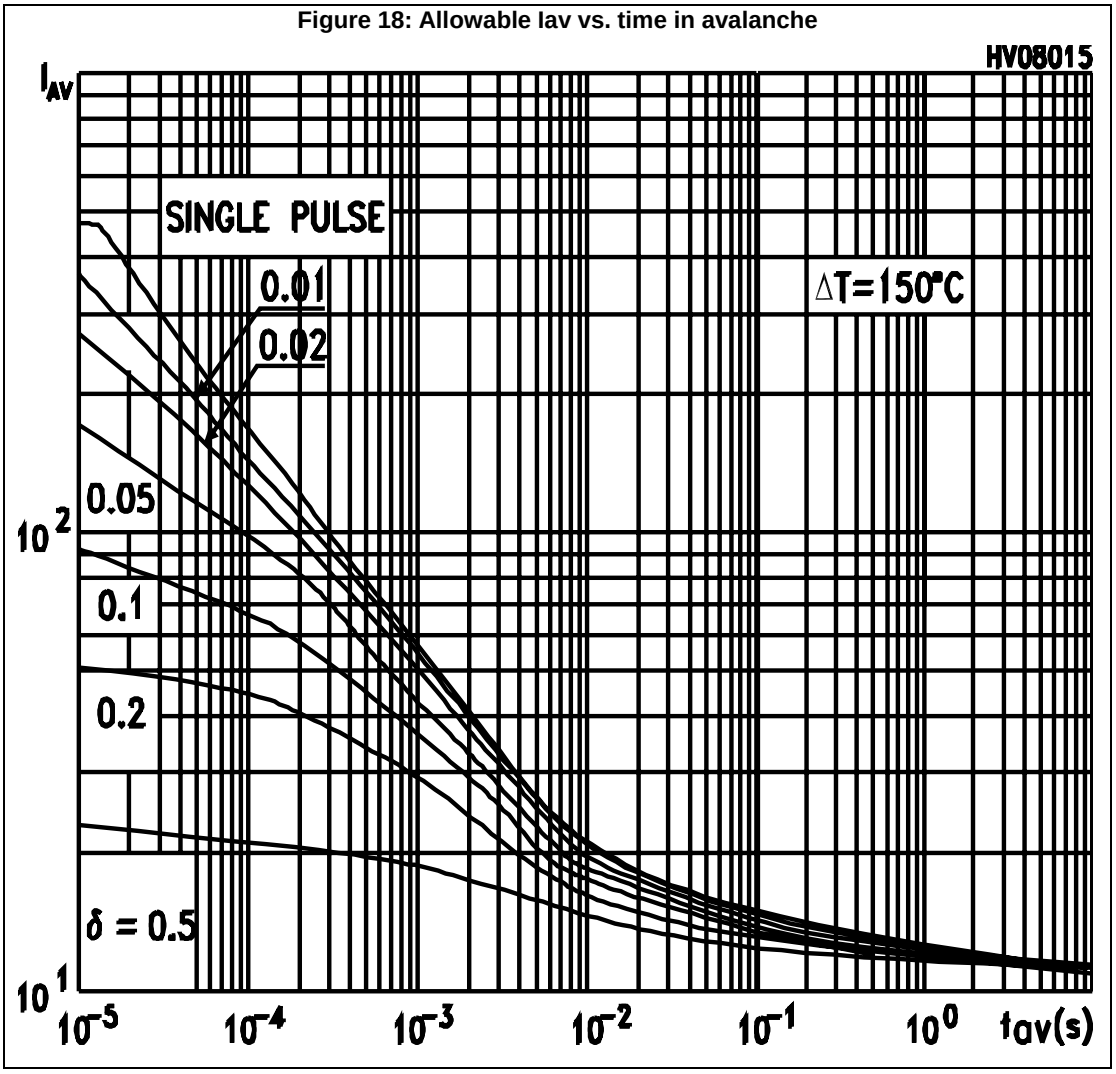


Figure 18: Allowable Iav vs. time in avalanche




The previous curve give the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5*(1.3*BV_{DSS}*I_{AV})$

$E_{AS(AR)} = P_{D(AVE)}*T_{AV}$

Where:

$I_{AV}$ is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalnche(single pulse)

$t_{AV}$ is the time in avalanche

To de rate above 25°C, at fixed IAV, the following equation must be applied:

$IAV = 2*(Tjmax-T_{CASE})/(1.3*B_{VDSS}*Zth)$

Where:

Zth= K*Rth is the value coming from normalized thermal response at fixed pulse width equal to $T_{AV}$

# 3 Spice thermal model

**Figure 19: Spice model schematic**

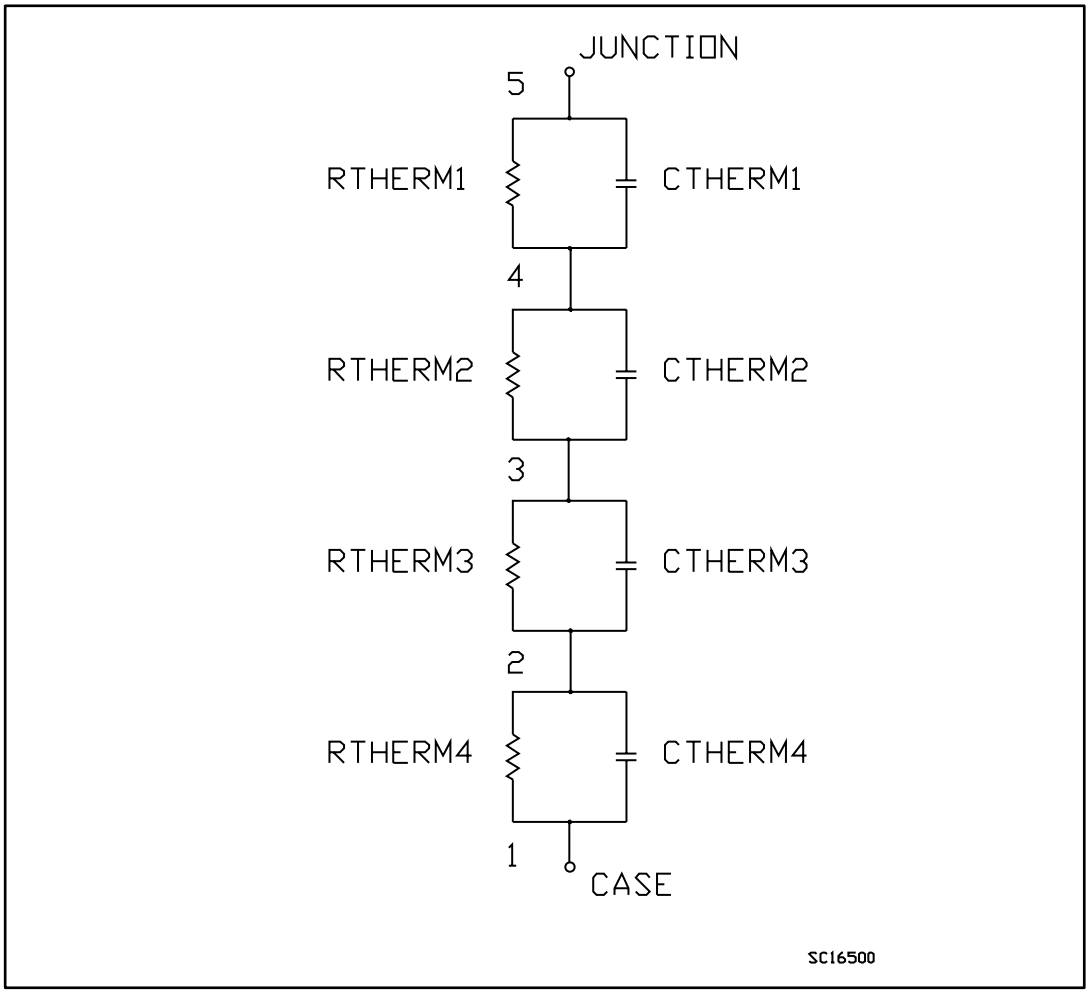



**Table 7: Spice parameter**

| Parameter | Node | Value |
|---|---|---|
| CTHERM1 | 5 - 4 | 0.011 |
| CTHERM1 | 4 - 3 | 0.0012 |
| CTHERM3 | 3 - 2 | 0.05 |
| CTHERM4 | 2 - 1 | 0.1 |
| RTHERM1 | 5 - 4 | 0.09 |
| RTHERM2 | 4 - 3 | 0.02 |
| RTHERM3 | 3 - 2 | 0.11 |
| RTHERM4 | 2 - 1 | 0.17 |

# 4 Test circuits

**Figure 20: Test circuit for resistive load switching times**

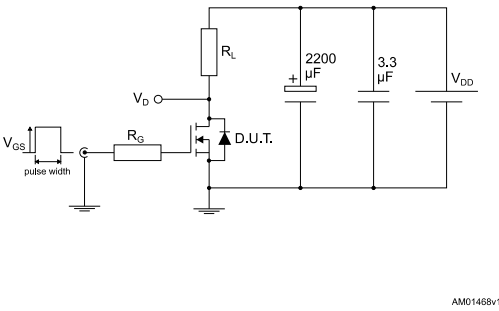



**Figure 21: Test circuit for gate charge behavior**

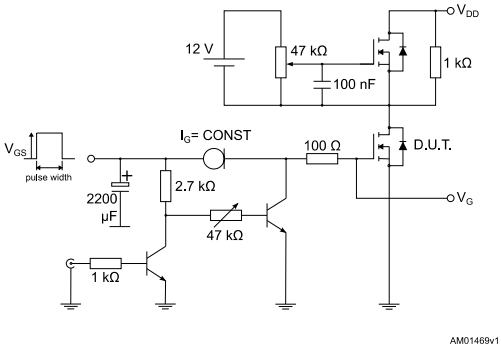



**Figure 22: Test circuit for inductive load switching and diode recovery times**

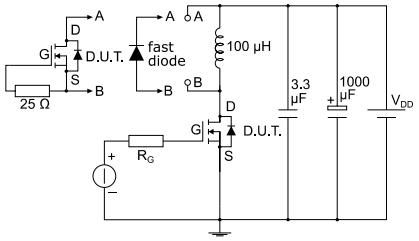



**Figure 23: Unclamped inductive load test circuit**

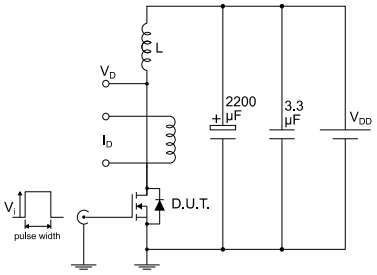



**Figure 24: Unclamped inductive waveform**

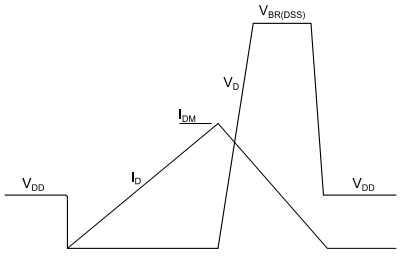
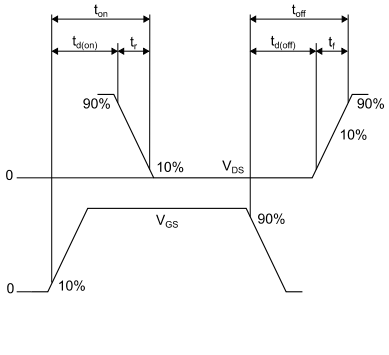



**Figure 25: Switching time waveform**



# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 5.1 D²PAK packing information

**Figure 26: D²PAK (TO-263) type A package outline**

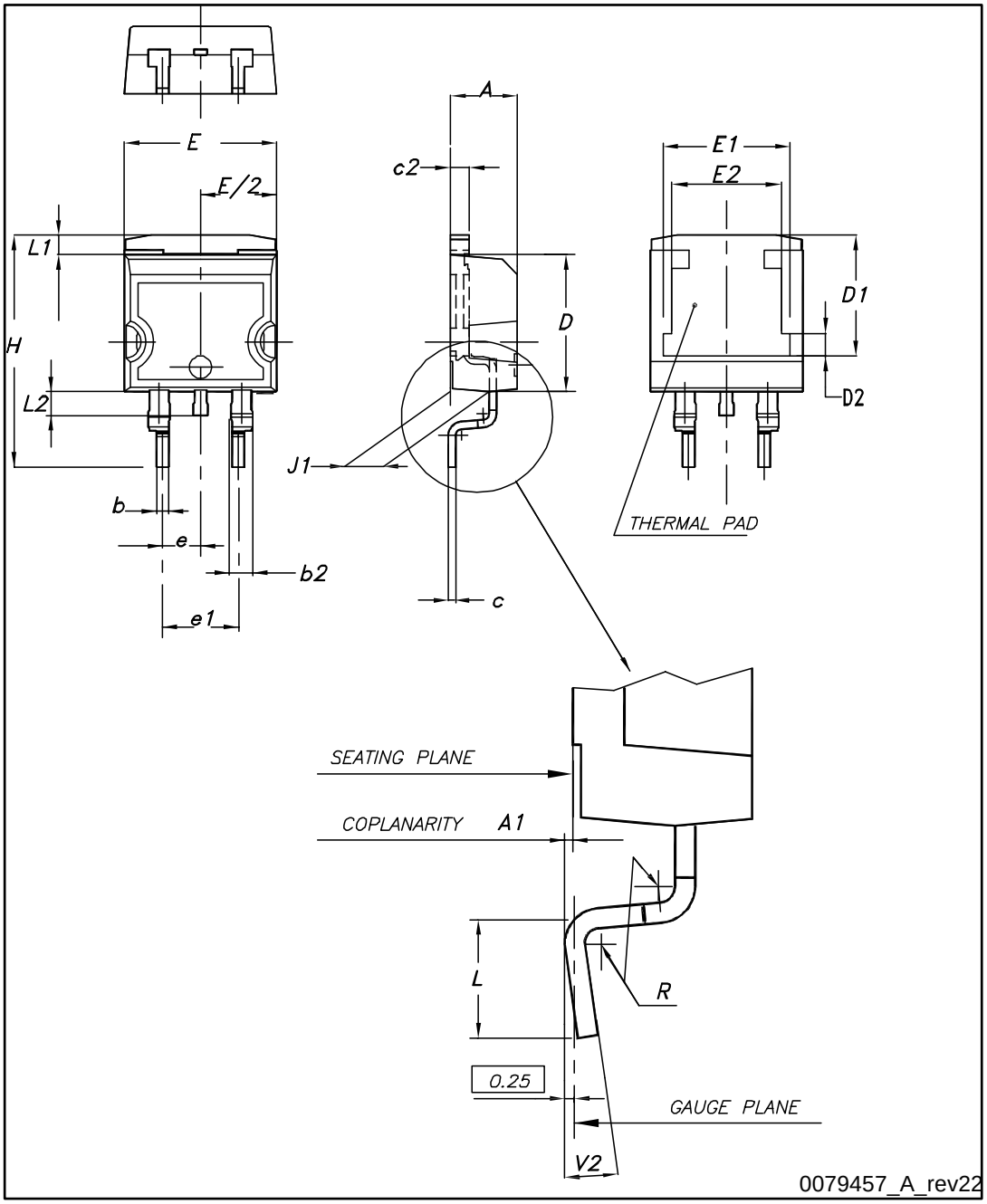
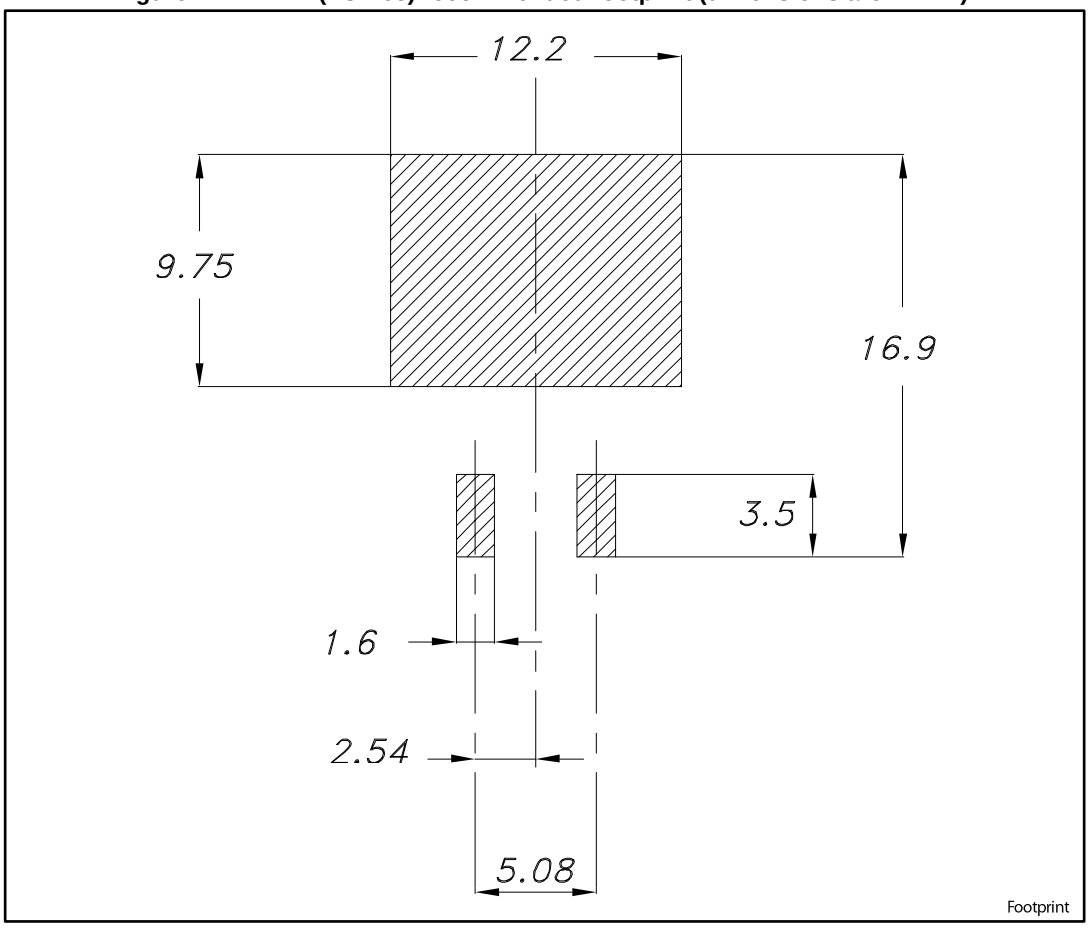


Table 8: D²PAK (TO-263) type A package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10 | | 10.40 |
| E1 | 8.50 | 8.70 | 8.90 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

Figure 27: D²PAK (TO-263) recommended footprint (dimensions are in mm)



## 5.2 D²PAK packing information

**Figure 28: Tape outline**

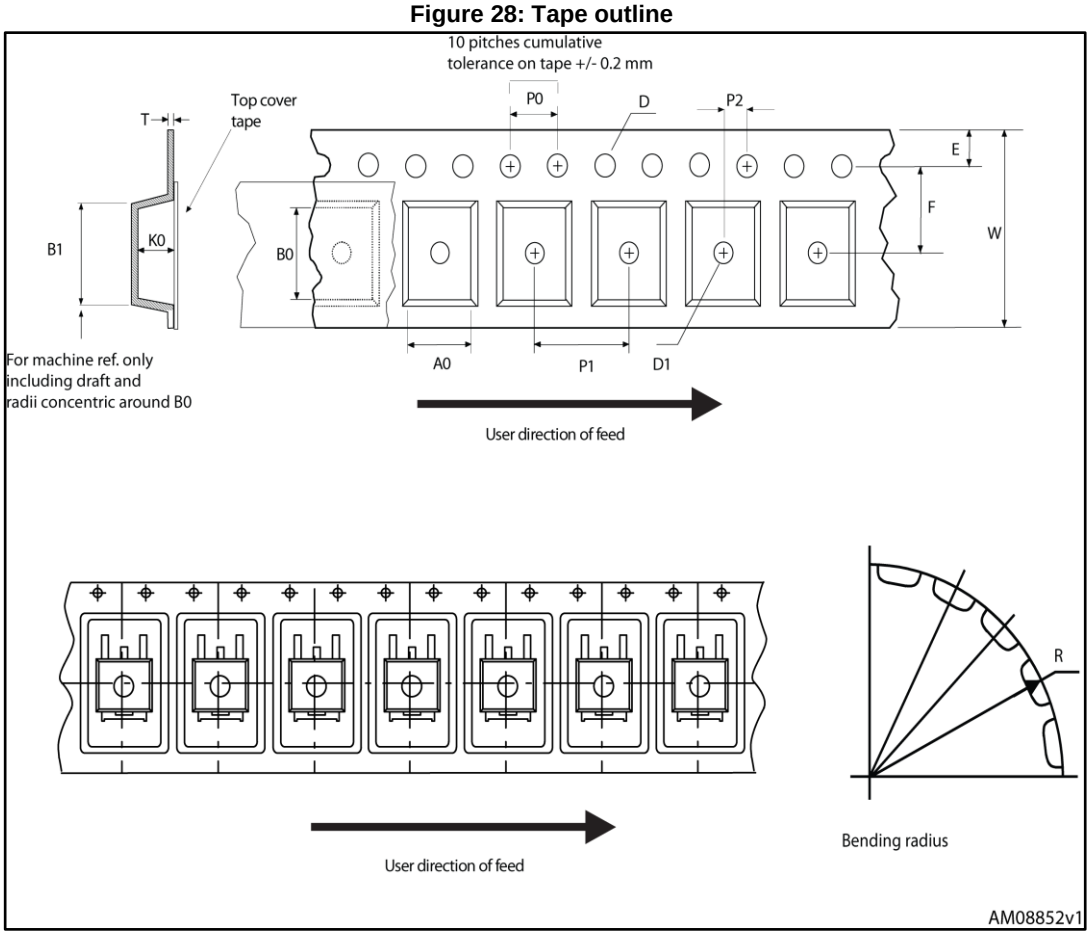


Figure 29: Reel outline

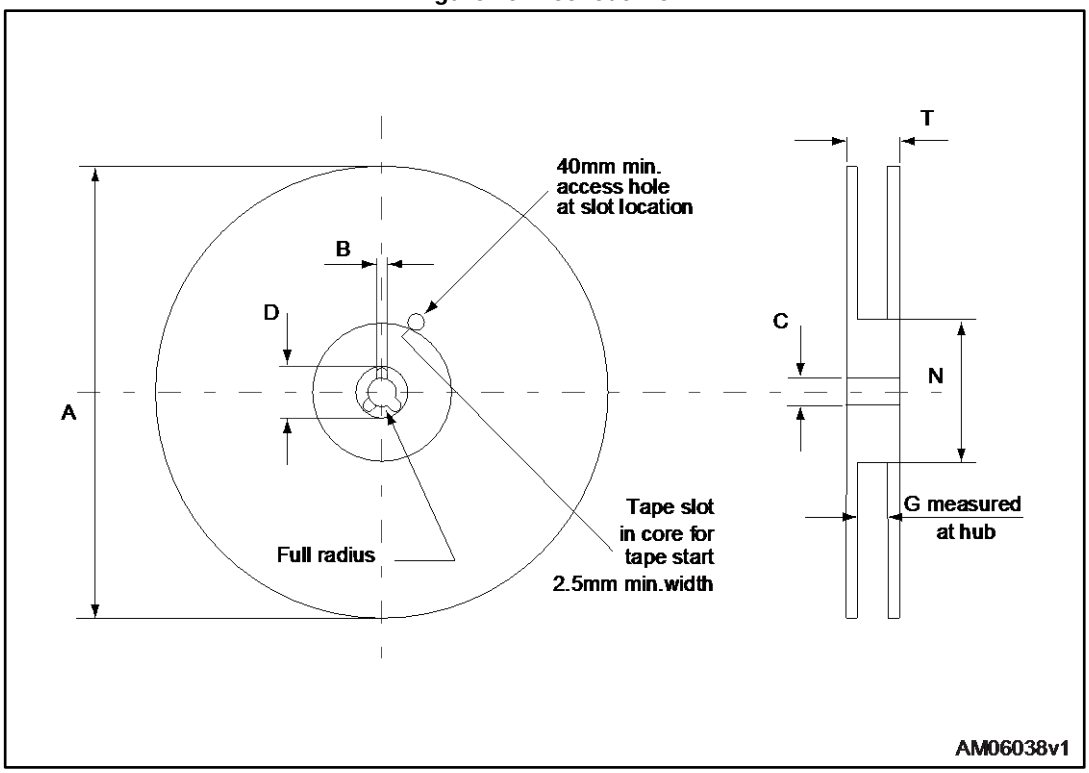



Table 9: D²PAK tape and reel mechanical data

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base quantity | | 1000 |
| P2 | 1.9 | 2.1 | Bulk quantity | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

## 5.3 TO-220 package information

Figure 30: TO-220 type A package outline

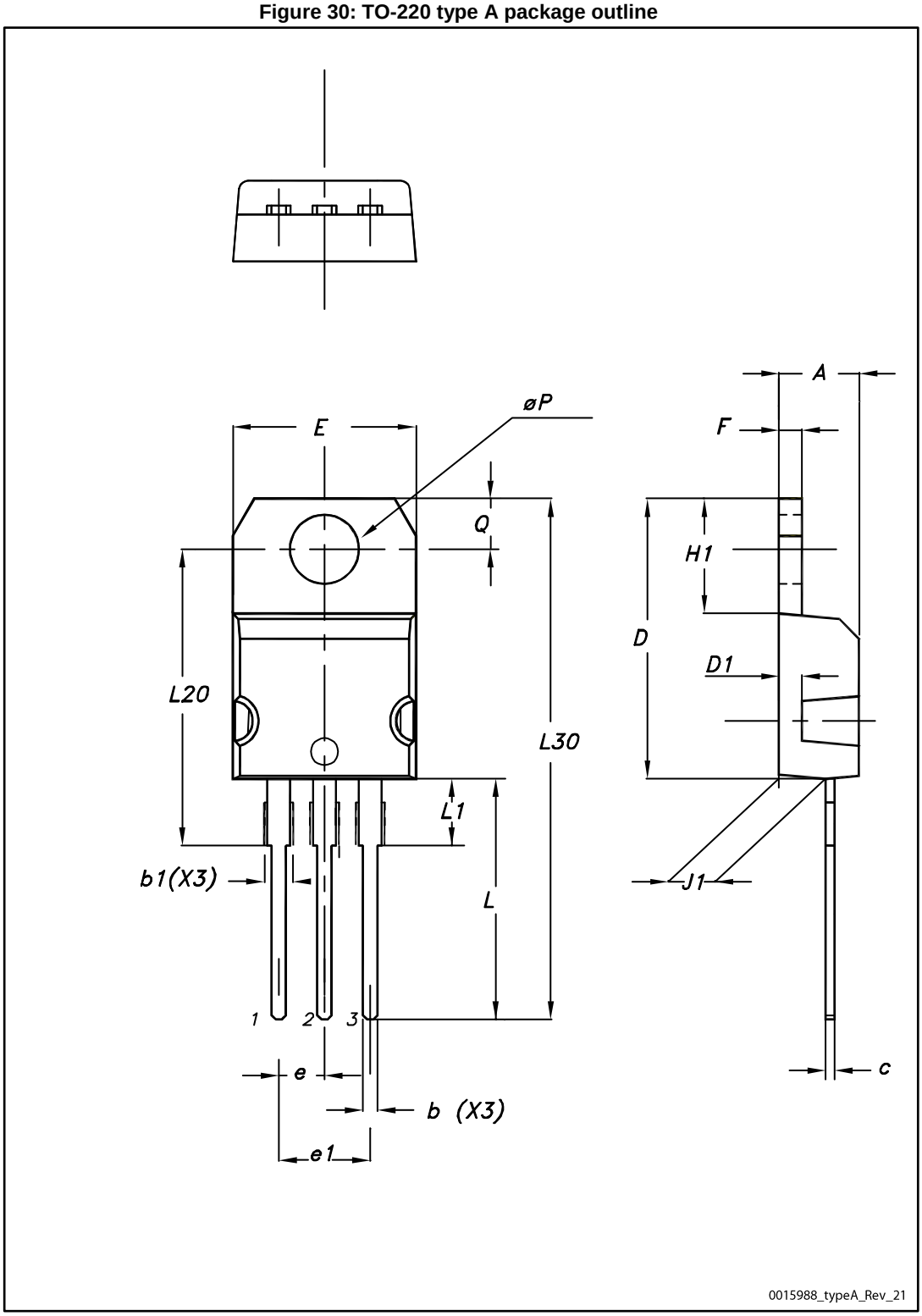


Table 11: TO-220 type A mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| b | 0.61 | | 0.88 |
| b1 | 1.14 | | 1.55 |
| c | 0.48 | | 0.70 |
| D | 15.25 | | 15.75 |
| D1 | | 1.27 | |
| E | 10.00 | | 10.40 |
| e | 2.40 | | 2.70 |
| e1 | 4.95 | | 5.15 |
| F | 1.23 | | 1.32 |
| H1 | 6.20 | | 6.60 |
| J1 | 2.40 | | 2.72 |
| L | 13.00 | | 14.00 |
| L1 | 3.50 | | 3.93 |
| L20 | | 16.40 | |
| L30 | | 28.90 | |
| øP | 3.75 | | 3.85 |
| Q | 2.65 | | 2.95 |

# 6 Revision history

**Table 12: Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 23-Mar-2005 | 2 | New template |
| 01-Mar-2006 | 3 | Removed I²PAK and inserted D²PAK. |
| 04-Sep-2006 | 4 | New template,no content change |
| 20-Feb-2007 | 5 | Typo mistake on page 1 |
| 16-Mar-2013 | 6 | Minor text changes – Modified: *Figure 17* – Updated: Section 4: *Package mechanical data* and Section 5: *Packaging mechanical data* |
| 21-Nov-2016 | 7 | Updated title in cover page.<br>Updated *Section 2: "Electrical characteristics"*.<br>Minor text changes. |

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