TABLE OF CONTENTS

REVISION HISTORY

9/11—Rev. A to Rev. B

Changes to Table 3, Endnote 1, and Figure 2 ... 5

5/11—Rev. 0 to Rev. A

Changes to Table 6, LRSEL Pin Description ... 7

10/10—Revision 0: Initial Version

SPECIFICATIONS

PVDD = 5.0 V, VDD = 1.8 V, f_S = 128×, T_A = 25°C, R_L = 8 Ω + 33 µH, unless otherwise noted. When f_S = 128×, PDM clock = 6.144 MHz; when f_S = 64×, PDM clock = 3.072 MHz.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	f = 1 kHz, BW = 20 kHz				
		R_L = 4 Ω, THD = 1%, PVDD = 5.0 V		2.4		W
		R_L = 8 Ω, THD = 1%, PVDD = 5.0 V		1.38		W
		R_L = 4 Ω, THD = 1%, PVDD = 3.6 V		1.2		W
		R_L = 8 Ω, THD = 1%, PVDD = 3.6 V		0.7		W
		R_L = 4 Ω, THD = 10%, PVDD = 3.6 V		1.5		W
		R_L = 8 Ω, THD = 10%, PVDD = 3.6 V		0.9		W
Total Harmonic Distortion Plus Noise	THD + N	f = 1 kHz, BW = 20 kHz				
		P_O = 100 mW into 8 Ω, PVDD = 3.6 V		0.035		%
		P_O = 500 mW into 8 Ω, PVDD = 3.6 V		0.1		%
		P_O = 1 W into 8 Ω, PVDD = 5.0 V		0.12		%
		R_L = 4 Ω, −6 dBFS input, PVDD = 5.0 V		3.6		%
		R_L = 8 Ω, −6 dBFS input, PVDD = 5.0 V		1.0		%
		R_L = 4 Ω, −6 dBFS input, PVDD = 3.6 V		5.2		%
		R_L = 8 Ω, −6 dBFS input, PVDD = 3.6 V		2.3		%
Efficiency	η	P_O = 2.4 W into 4 Ω, PVDD = 5.0 V		86		%
		P_O = 1.38 W into 8 Ω, PVDD = 5.0 V		92		%
Average Switching Frequency	f_{SW}	No input		290		kHz
Closed-Loop Gain	Gain	−6 dBFS PDM input, BTL output, f = 1 kHz				
		PVDD = 3.6 V		3.5		V_P
		PVDD = 5.0 V		4.78		V_P
Differential Output Offset Voltage	V_{OOS}	Gain = 6 dB		0.5		mV
Low Power Mode Wake Time	t_{WAKE}				0.5	ms
Input Sampling Frequency	f_S	f_S = 64×	1.84	3.072	3.23	MHz
		f_S = 128×	3.68	6.144	6.46	MHz
POWER SUPPLY						
Supply Voltage Range						
Amplifier Power Supply	PVDD		2.5	3.6	5.5	V
Digital Power Supply	VDD		1.62	1.8	3.6	V
Power Supply Rejection Ratio	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz		85		dB
Supply Current, H-Bridge	I_{PVDD}	Dither input, 8 Ω + 33 µH load				
		PVDD = 5.0 V, f_S = 64×		3.1		mA
		PVDD = 5.0 V, f_S = 128×		3.2		mA
		PVDD = 3.6 V, f_S = 64×		2.6		mA
		PVDD = 3.6 V, f_S = 128×		2.7		mA
		PVDD = 2.5 V, f_S = 64×		2.2		mA
		PVDD = 2.5 V, f_S = 128×		2.3		mA
Standby Current		PVDD = 5.0 V		0.0		mA
Power-Down Current				100		nA
Supply Current, Modulator	I_{VDD}	Dither input, 8 Ω + 33 µH load				
		VDD = 3.3 V, f_S = 64×		1.3		mA
		VDD = 3.3 V, f_S = 128×		2.4		mA
		VDD = 1.8 V, f_S = 64×		0.6		mA
		VDD = 1.8 V, f_S = 128×		1.2		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Standby Current		VDD = 1.8 V, f_S = 64×		57		µA
		VDD = 1.8 V, f_S = 128×		114		µA
Shutdown Current		VDD = 3.3 V		3.0		µA
		VDD = 1.8 V		0.9		µA
NOISE PERFORMANCE						
Output Voltage Noise	e_n	Dithered input, A-weighted				
		PVDD = 3.6 V, f_S = 64×		43		µV
		PVDD = 3.6 V, f_S = 128×		52		µV
		PVDD = 5.0 V, f_S = 64×		52		µV
		PVDD = 5.0 V, f_S = 128×		60		µV
Signal-to-Noise Ratio	SNR	P_O = 1.38 W, PVDD = 5.0 V, R_L = 8 Ω, A-weighted				
		f_S = 64×		96		dB
		f_S = 128×		95		dB

DIGITAL INPUT SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
INPUT SPECIFICATIONS					
Input Voltage High	V_{IH}				
PCLK, PDAT, LRSEL Pins		0.7 × VDD		3.6	V
GAIN_FS Pin		1.35		5.5	V
Input Voltage Low	V_{IL}				V
PCLK, PDAT, LRSEL Pins		−0.3		0.3 × VDD	V
GAIN_FS Pin		−0.3		+0.35	V
Input Leakage High	I_{IH}				
PDAT, LRSEL, GAIN_FS Pins				1	µA
PCLK Pin				3	µA
Input Leakage Low	I_{IL}				
PDAT, LRSEL, GAIN_FS Pins				1	µA
PCLK Pin				3	µA
Input Capacitance				5	pF

PDM INTERFACE DIGITAL TIMING SPECIFICATIONS

Table 3.

Parameter	Limit t_{MIN}	Limit t_{MAX}	Unit	Description
t_{DS}	44		ns	Valid data start time[1]
t_{DE}		7	ns	Valid data end time[1]

[1] The SSM2517 was designed so that the data line can transition coincident with or close to a clock edge. It is not necessary to delay the data line transition until after the clock edge because the SSM2517 does this internally to ensure good timing margins. The data line should remain constant during the valid sample period illustrated in Figure 2; it may transition at any other time. Timing is measured from 70% of VDD on the rising edge or 30% VDD on the falling edge.

Timing Diagram

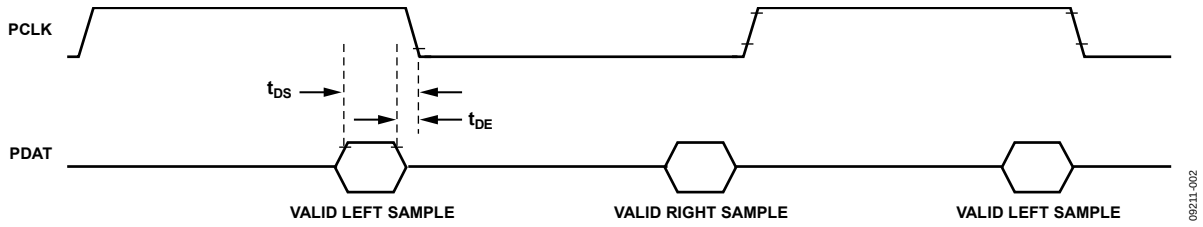

Figure 2. PDM Interface Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
PVDD Supply Voltage	−0.3 V to +6 V
VDD Supply Voltage	−0.3 V to +3.6 V
Input Voltage (Signal Source)	−0.3 V to +3.6 V
ESD Susceptibility	4 kV
OUT− and OUT+ Pins	8 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Junction-to-air thermal resistance (θ_{JA}) is specified for the worst-case conditions, that is, a device soldered in a printed circuit board (PCB) for surface-mount packages. θ_{JA} and θ_{JB} (junction-to-board thermal resistance) are determined according to JEDEC JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 5. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-Ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

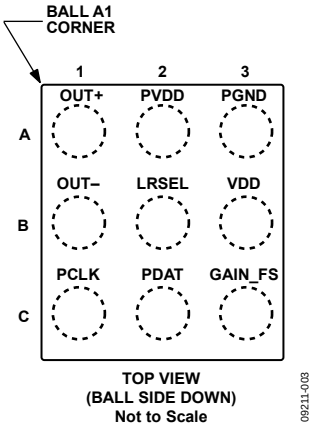

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function	Description
A1	OUT+	Output	Noninverting Output.
A2	PVDD	Supply	Amplifier Power, 2.5 V to 5.5 V.
A3	PGND	Ground	Amplifier Ground.
B1	OUT–	Output	Inverting Output.
B2	LRSEL	Input	Left/Right Channel Select. Pull up to VDD for right channel; tie to ground for left channel.
B3	VDD	Supply	Digital Power, 1.62 V to 3.6 V.
C1	PCLK	Input	PDM Interface Master Clock.
C2	PDAT	Input	PDM Data Signal.
C3	GAIN_FS	Input	Gain and Sample Rate Selection Pin.

TYPICAL PERFORMANCE CHARACTERISTICS

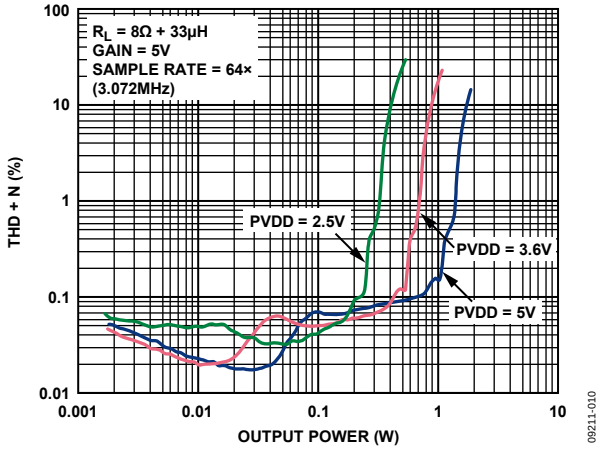

Figure 4. THD + N vs. Output Power into 8 Ω, Gain = 5 V, f_S = 64×

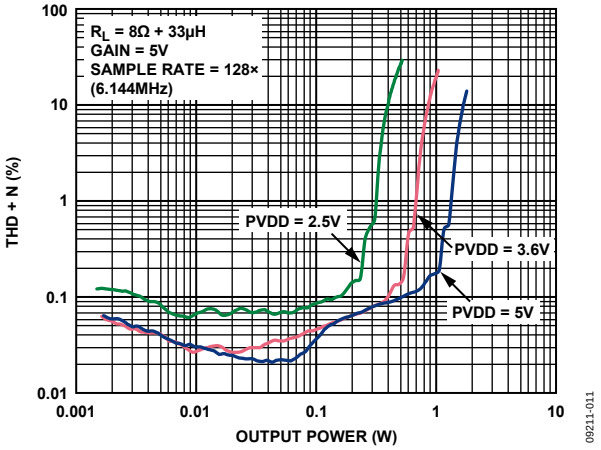

Figure 7. THD + N vs. Output Power into 8 Ω, Gain = 5 V, f_S = 128×

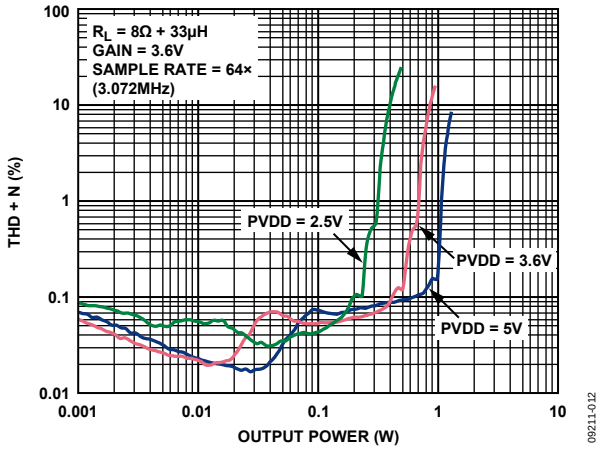

Figure 5. THD + N vs. Output Power into 8 Ω, Gain = 3.6 V, f_S = 64×

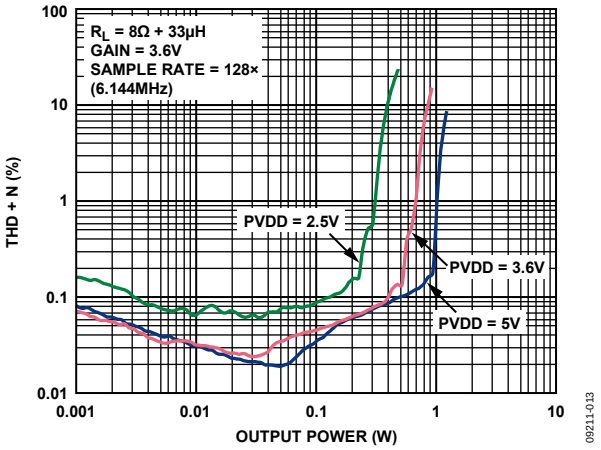

Figure 8. THD + N vs. Output Power into 8 Ω, Gain = 3.6 V, f_S = 128×

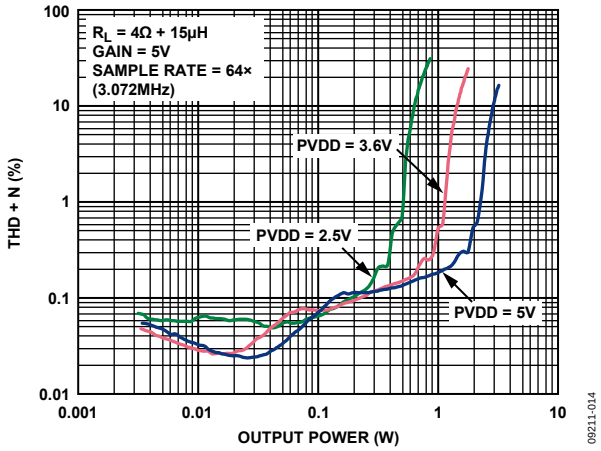

Figure 6. THD + N vs. Output Power into 4 Ω, Gain = 5 V, f_S = 64×

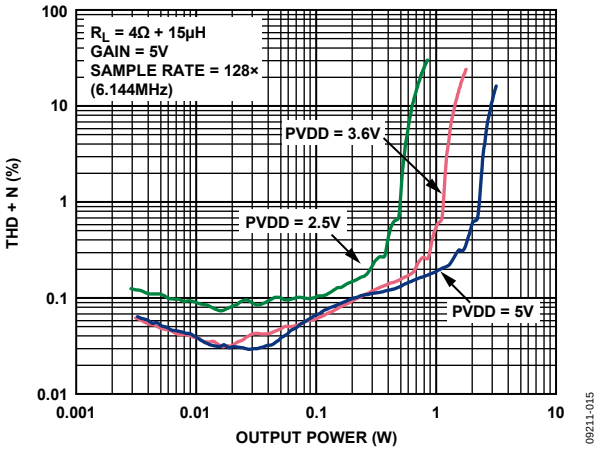

Figure 9. THD + N vs. Output Power into 4 Ω, Gain = 5 V, f_S = 128×

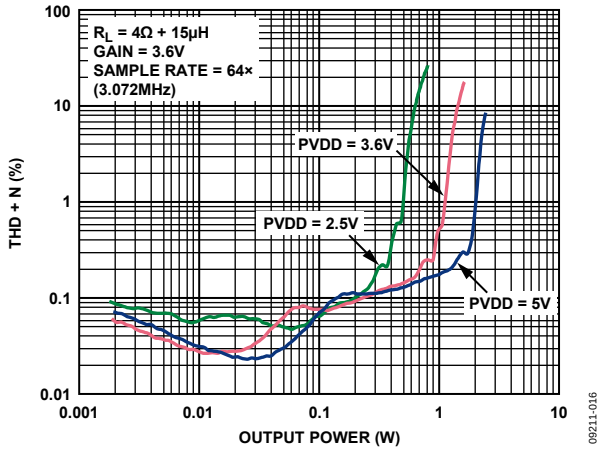

Figure 10. THD + N vs. Output Power into 4 Ω, Gain = 3.6 V, f_S = 64×

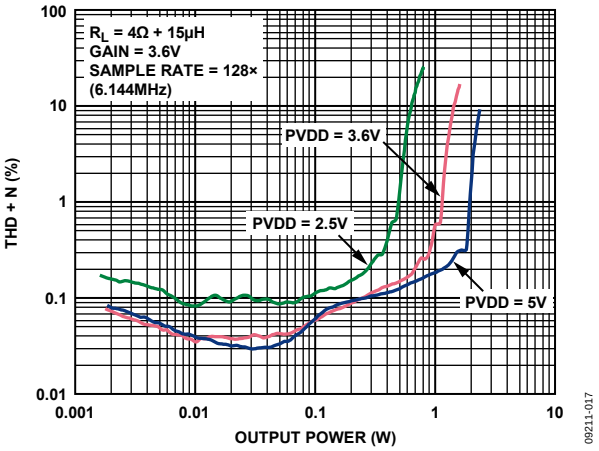

Figure 13. THD + N vs. Output Power into 4 Ω, Gain = 3.6 V, f_S = 128×

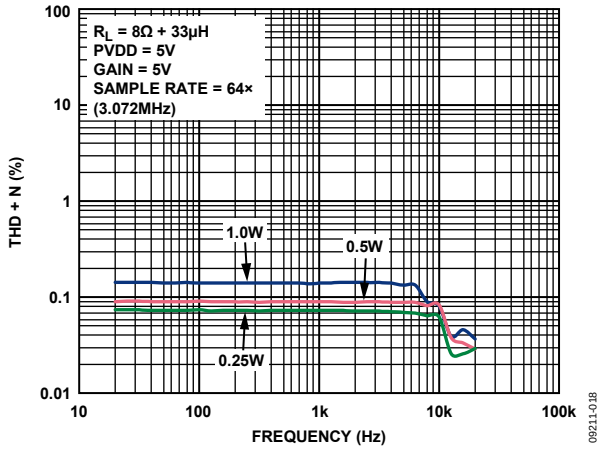

Figure 11. THD + N vs. Frequency, PVDD = 5 V, Gain = 5 V, R_L = 8 Ω, f_S = 64×

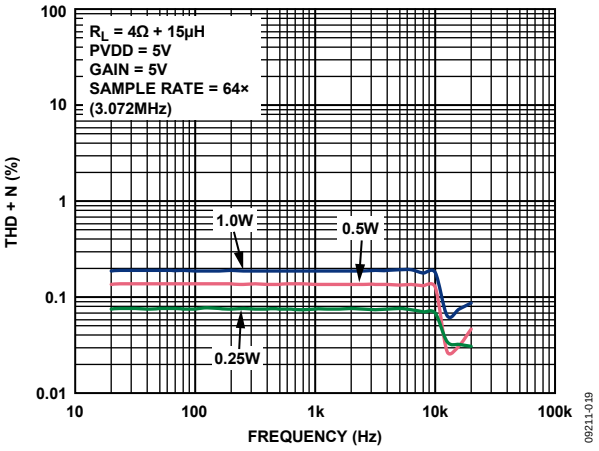

Figure 14. THD + N vs. Frequency, PVDD = 5 V, Gain = 5 V, R_L = 4 Ω, f_S = 64×

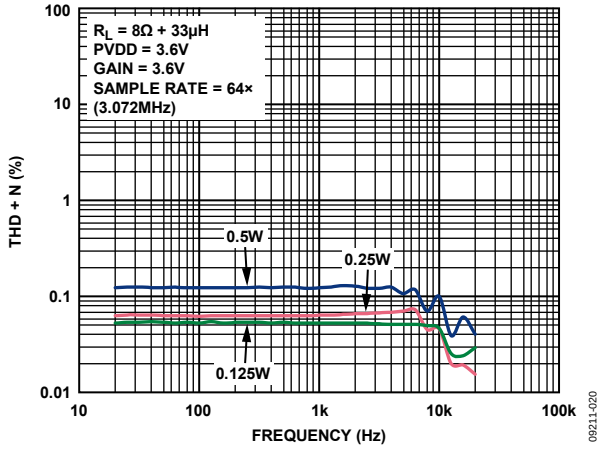

Figure 12. THD + N vs. Frequency, PVDD = 3.6 V, Gain = 3.6 V, R_L = 8 Ω, f_S = 64×

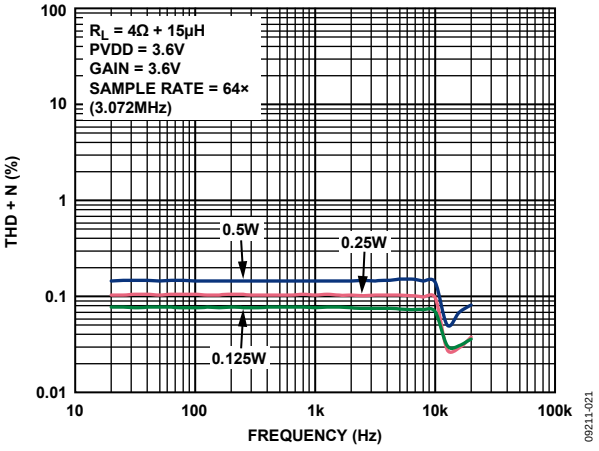

Figure 15. THD + N vs. Frequency, PVDD = 3.6 V, Gain = 3.6 V, R_L = 4 Ω, f_S = 64×

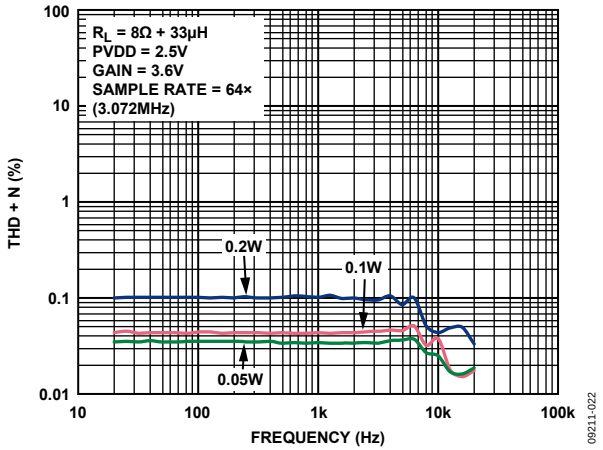

Figure 16. THD + N vs. Frequency, PVDD = 2.5 V, Gain = 3.6 V, R_L = 8 Ω, f_S = 64×

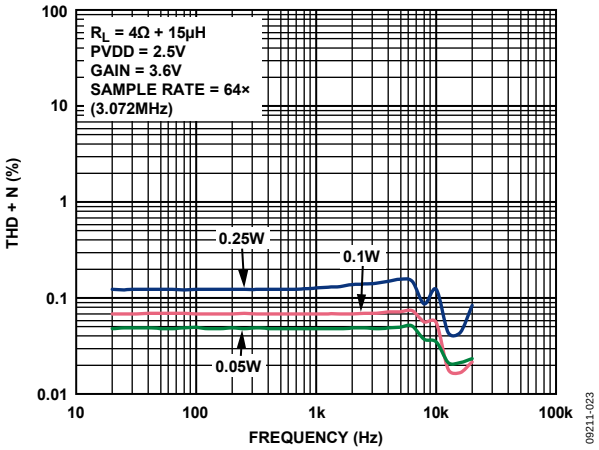

Figure 19. THD + N vs. Frequency, PVDD = 2.5 V, Gain = 3.6 V, R_L = 4 Ω, f_S = 64×

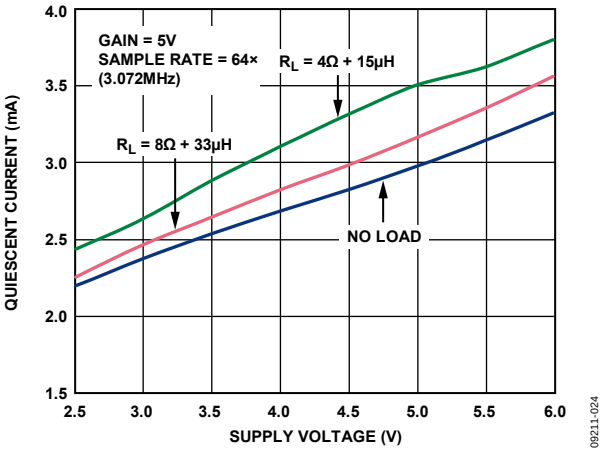

Figure 17. Quiescent Current (H-Bridge) vs. Supply Voltage, Gain = 5 V, f_S = 64×

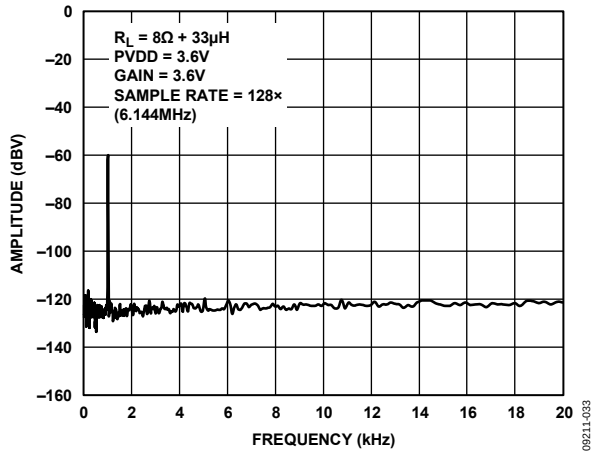

Figure 20. Output Spectrum vs. Frequency, PVDD = 3.6 V, Gain = 3.6 V, R_L = 8 Ω, f_S = 128×

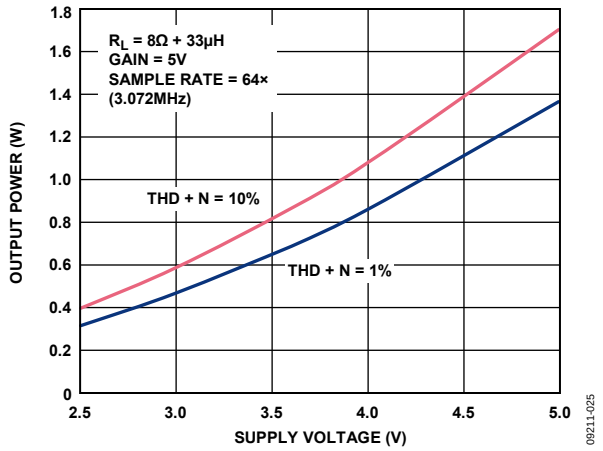

Figure 18. Maximum Output Power vs. Supply Voltage, Gain = 5 V, R_L = 8 Ω, f_S = 64×

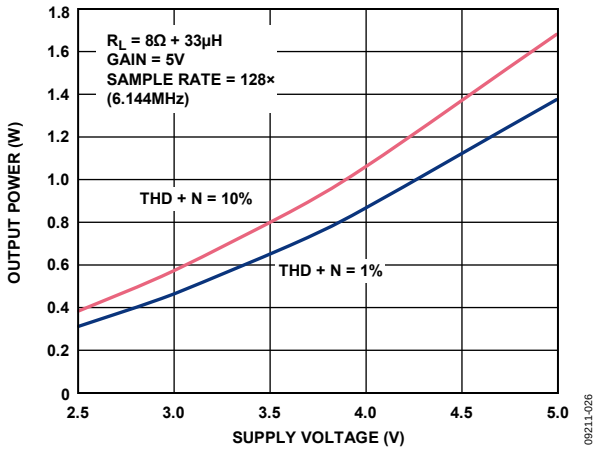

Figure 21. Maximum Output Power vs. Supply Voltage, Gain = 5 V, R_L = 8 Ω, f_S = 128×

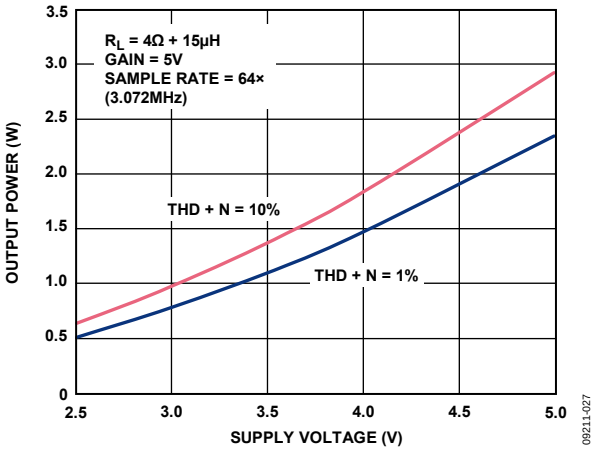

Figure 22. Maximum Output Power vs. Supply Voltage, Gain = 5 V, R_L = 4 Ω, f_S = 64×

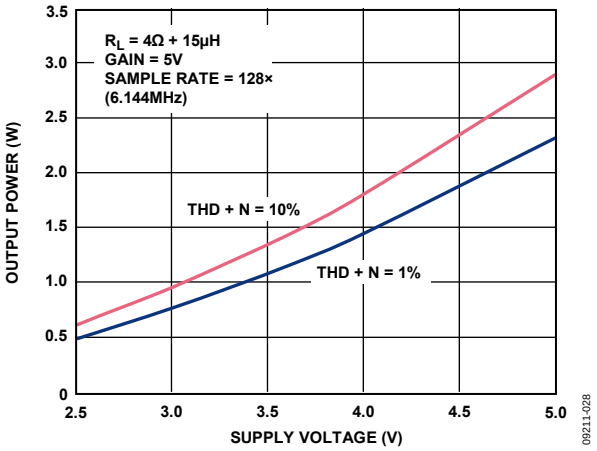

Figure 25. Maximum Output Power vs. Supply Voltage, Gain = 5 V, R_L = 4 Ω, f_S = 128×

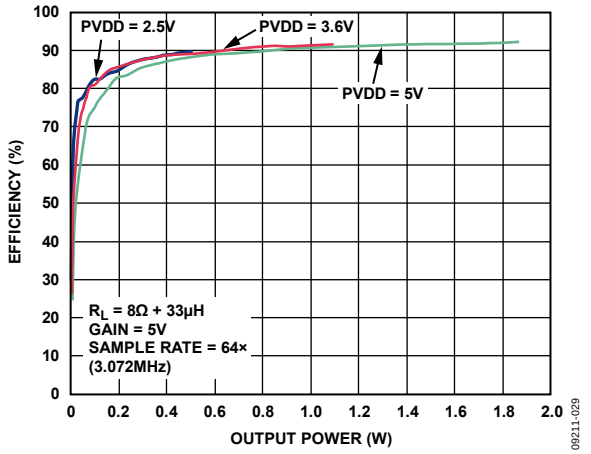

Figure 23. Efficiency vs. Output Power into 8 Ω, Gain = 5 V, f_S = 64×

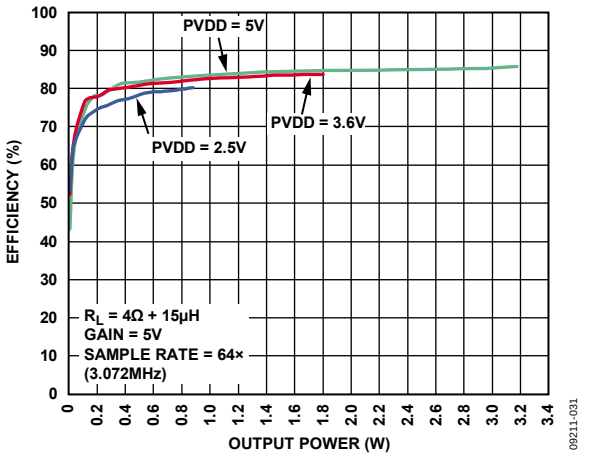

Figure 26. Efficiency vs. Output Power into 4 Ω, Gain = 5 V, f_S = 64×

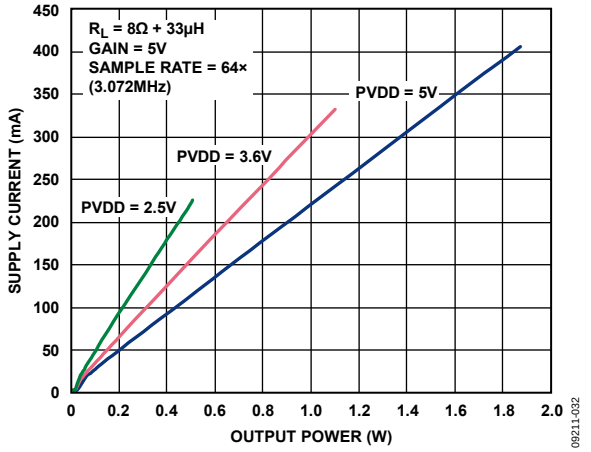

Figure 24. Supply Current (H-Bridge) vs. Output Power into 8 Ω, Gain = 5 V, f_S = 64×

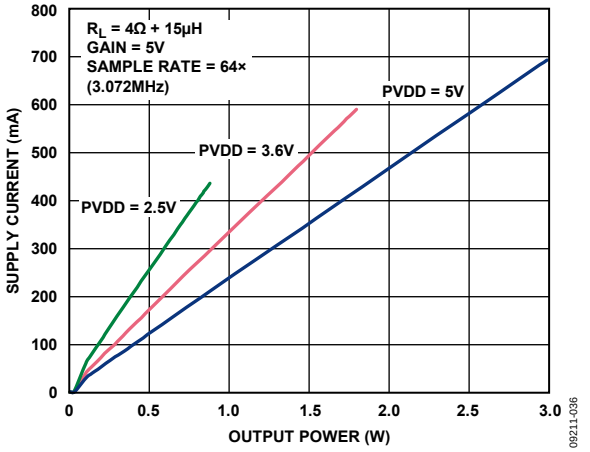

Figure 27. Supply Current (H-Bridge) vs. Output Power into 4 Ω, Gain = 5 V, f_S = 64×

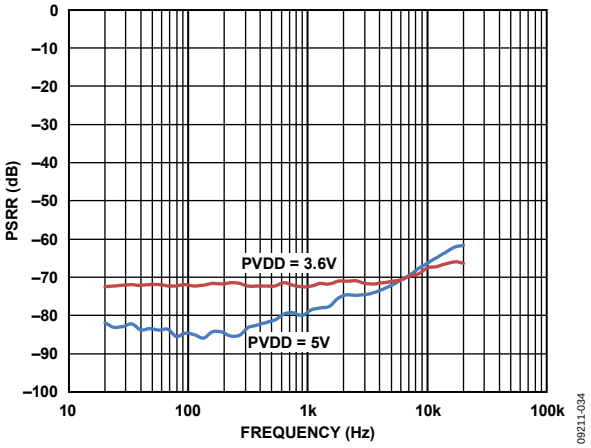

Figure 28. Power Supply Rejection Ratio (PSRR) vs. Frequency

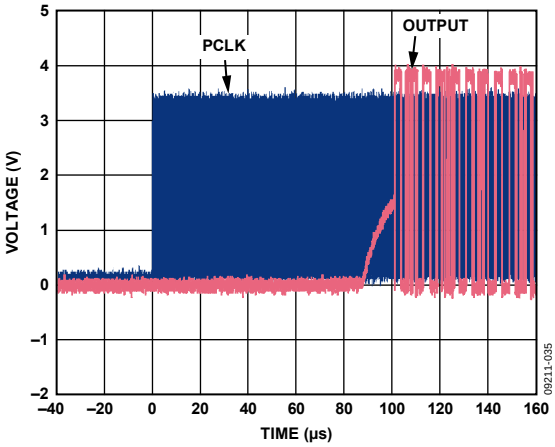

Figure 29. Turn-On Response

THEORY OF OPERATION

MASTER CLOCK

The SSM2517 requires a clock present at the PCLK input pin. This clock must be fully synchronous with the incoming digital audio on the serial interface. The clock frequencies must fall into one of these ranges: 1.84 MHz to 3.23 MHz or 3.68 MHz to 6.46 MHz.

POWER SUPPLIES

The SSM2517 requires two power supplies: PVDD and VDD.

PVDD

The PVDD pin supplies power to the full-bridge power stage of a MOSFET and its associated drive, control, and protection circuitry. It also supplies power to the digital-to-analog converter (DAC) and to the Class-D PDM modulator. PVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the supply voltage of PVDD results in lower maximum output power and, therefore, lower power consumption.

VDD

The VDD pin provides power to the digital logic circuitry. VDD can operate from 1.62 V to 3.6 V and must be present to obtain audio output. Lowering the supply voltage of VDD results in lower power consumption but does not affect audio performance.

POWER CONTROL

On device power-up, PVDD must first be applied to the device, which latches in the designated GAIN_FS pin functionality.

The SSM2517 contains a smart power-down feature. When enabled, the smart power-down feature looks at the incoming digital audio and, if it receives the PDM stop condition of at least 128 repeated 0xAC bytes (1024 clock cycles), it places the SSM2517 in the standby state. In the standby state, the PCLK can be removed, resulting in a full power-down state. This state is the lowest power condition possible. When the PCLK is turned on again and a single non-stop condition input is received, the SSM2517 leaves the full power-down state and resumes normal operation.

POWER-ON RESET/VOLTAGE SUPERVISOR

The SSM2517 includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to all circuitry whenever PVDD or VDD is substantially below the nominal operating threshold. This circuit simplifies supply sequencing during initial power-on.

The circuit also monitors the power supplies to the SSM2517. If the supply voltages fall below the nominal operating threshold, this circuit stops the output and issues a reset. This ensures that no damage occurs due to low voltage operation and that no pops can occur under nearly any power removal condition.

SYSTEM GAIN/INPUT FREQUENCY

The GAIN_FS pin is used to set the internal gain and filtering configuration for different sample rates of the SSM2517. This pin can be set to one of four states by connecting the pin to PVDD or PGND (see Table 7). The internal gain and filtering can also be set via PDM pattern control, allowing these settings to be modified during operation (see the PDM Pattern Control section).

Table 7. GAIN_FS Function Descriptions

Device Setting	GAIN Pin Configuration
f_S = 64 × PCLK, Gain = 5 V	Pull up to PVDD with a 47 kΩ resistor
f_S = 128 × PCLK, Gain = 5 V	Pull down to PGND with a 47 kΩ resistor
f_S = 64 × PCLK, Gain = 3.6 V	Pull up to PVDD
f_S = 128 × PCLK, Gain = 3.6 V	Pull down to PGND

The SSM2517 has an internal analog gain control such that when GAIN_FS is tied to PGND or PVDD via a 47 kΩ resistor (5 V gain setting), a −6.02 dBFS PDM input signal results in an amplifier output voltage of 5 V peak. This setting should produce optimal noise performance when PVDD = 5 V.

When the GAIN_FS pin is tied directly to PGND or PVDD, the gain is adjusted so that a −6.02 dBFS PDM input signal results in an amplifier output voltage of 3.6 V peak. This setting should produce optimal noise performance when PVDD = 3.6 V.

The SSM2517 can handle input sample rates of 64 × f_S (~3 MHz) and 128 × f_S (~6 MHz). Different internal digital filtering is used in each of these cases. Selection of the sample rate is also set via the GAIN_FS pin (see Table 7).

Because the 64 × f_S mode provides better performance with lower power consumption, its use is recommended. The 128 × f_S mode should be used only when overall system noise performance is limited by the source modulator.

PDM PATTERN CONTROL

The SSM2517 has a simple control mechanism that can set the part for low power states and control functionality. This is accomplished by sending a repeating 8-bit pattern to the device. Different patterns set different functionality (see Table 8).

Any pattern must be repeated a minimum of 128 times. The part is automatically muted when a pattern is detected so that a pattern can be set while the part is operational without a pop/click due to pattern transition.

All functionality set via patterns returns to its default value after a clock-loss power-down.

Table 8. PDM Watermarking Pattern Control Descriptions

Pattern	Control Description
0xAC	Power-down. All blocks off except for PDM interface. Normal start-up time.
0xD8	Gain optimized for PVDD = 5 V operation. Overrides GAIN_FS pin setting.
0xD4	Gain optimized for PVDD = 3.6 V operation. Overrides GAIN_FS pin setting.
0xD2	Gain optimized for PVDD = 2.5 V operation. Overrides GAIN_FS pin setting.
0xD1	f_S set to opposite value determined by GAIN_FS pin.
0xE1	Ultralow EMI mode.
0xE2	Half clock cycle pulse mode for power savings.
0xE4	Special 32 kHz/128 × f_S operation mode.

EMI NOISE

The SSM2517 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications that have difficulty passing FCC Class-B emission tests, the SSM2517 includes a modulation select mode (ultralow EMI emissions mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. This mode is enabled by activating PDM Watermarking Pattern 0xE1 (see Table 8).

OUTPUT MODULATION DESCRIPTION

The SSM2517 uses three-level, Σ-Δ output modulation. Each output can swing from PGND to PVDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT−) is generated to follow the input voltage. The differential pulse density (VOUT) is increased by raising the input signal level. Figure 30 depicts three-level, Σ-Δ output modulation with and without input stimulus.

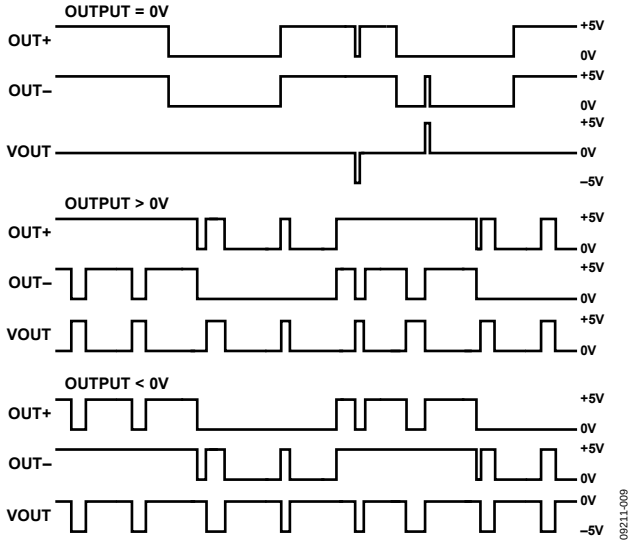

Figure 30. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

APPLICATIONS INFORMATION

LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. The PCB layout engineer must avoid ground loops where possible to minimize common-mode current associated with separate paths to ground. Ensure that track widths are at least 200 mil per inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz.

The power supply inputs must be decoupled with a good quality, low ESL, low ESR capacitor, with a minimum value of 4.7 µF for the PVDD pin and 0.1 µF for the VDD pin. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 µF capacitor as close as possible to the PVDD and VDD pins of the device. Placing the decoupling capacitors as close as possible to the SSM2517 helps to maintain efficient performance.

OUTLINE DIMENSIONS

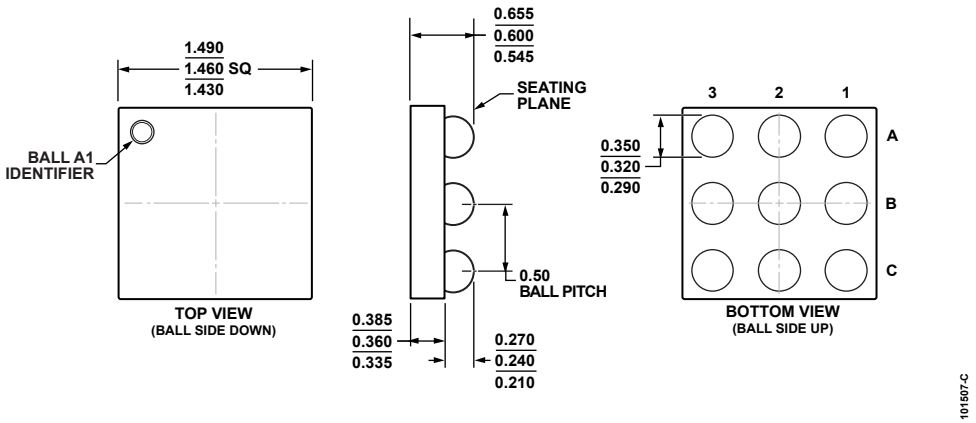

Figure 31. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2517CBZ-R7	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
SSM2517CBZ-RL	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2
EVAL-SSM2517Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

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