Vishay Siliconix



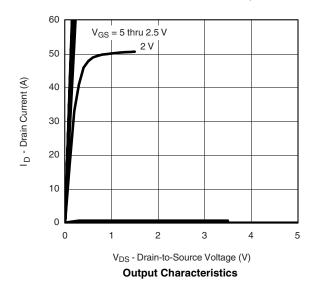
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					<u> </u>	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6		1.5	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 ^{\circ}\text{C}$			1 5	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30		3	Α
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 29 \text{ A}$		0.0023	0.003	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 25 \text{ A}$		0.0032	0.0042	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 \text{ V}, I_{D} = 29 \text{ A}$		70		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.70	1.2	V
Dynamic ^b	<u>'</u>		•	<u>'</u>		
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		5330		pF
Output Capacitance	C _{oss}			1240		
Reverse Transfer Capacitance	C _{rss}			680		
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 29 \text{ A}$		57	85	nC
Gate-Source Charge	Q_{gs}			8.5		
Gate-Drain Charge	Q_{gd}			17		
Gate Resistance	R_g		0.5	1.3	2	Ω
Turn-On Delay Time	t _{d(on)}			40	60	ns
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$	DD . L	44	65	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		150	240	
Fall Time	t _f			72	110	
Source-Drain Reverse Recovery Time	t _{rr}	$I_F = 2.9 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		57	80	

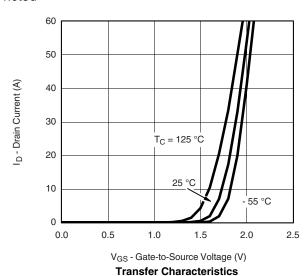
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



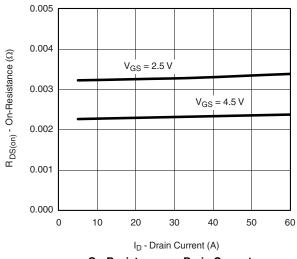


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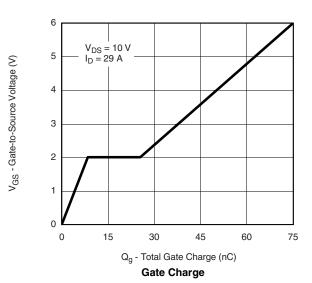


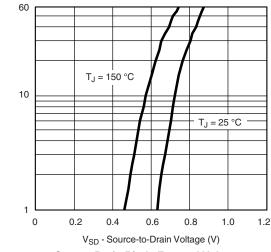


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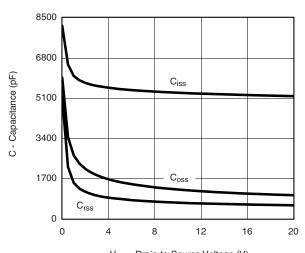


On-Resistance vs. Drain Current



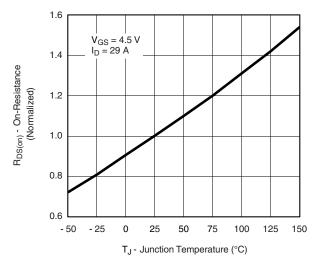


Source-Drain Diode Forward Voltage

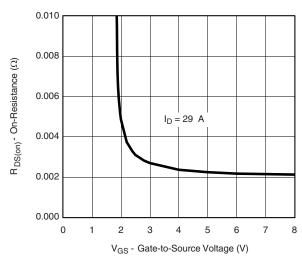


V_{DS} - Drain-to-Source Voltage (V)

Capacitance



On-Resistance vs. Junction Temperature



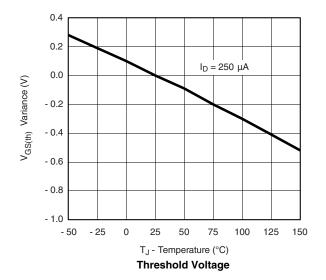
On-Resistance vs. Gate-to-Source Voltage

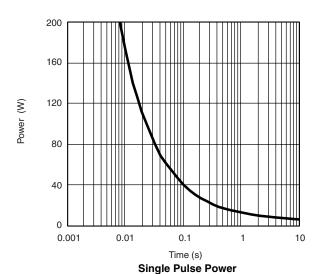
Is - Source Current (A)

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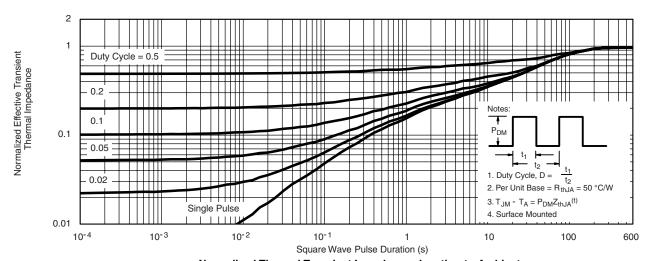
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





100 Limited by R_{DS(or} 1 ms 10 10 ms I_D - Drain Current (A) 100 ms 1 s 10 s 0.1 DC # T_C = 25 °C Single Pulse 0.01 0.01 10 100 V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

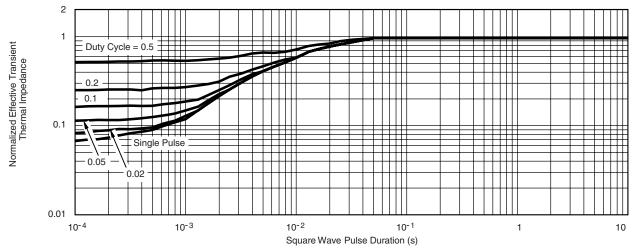
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73166.

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