

Pin Out Diagram

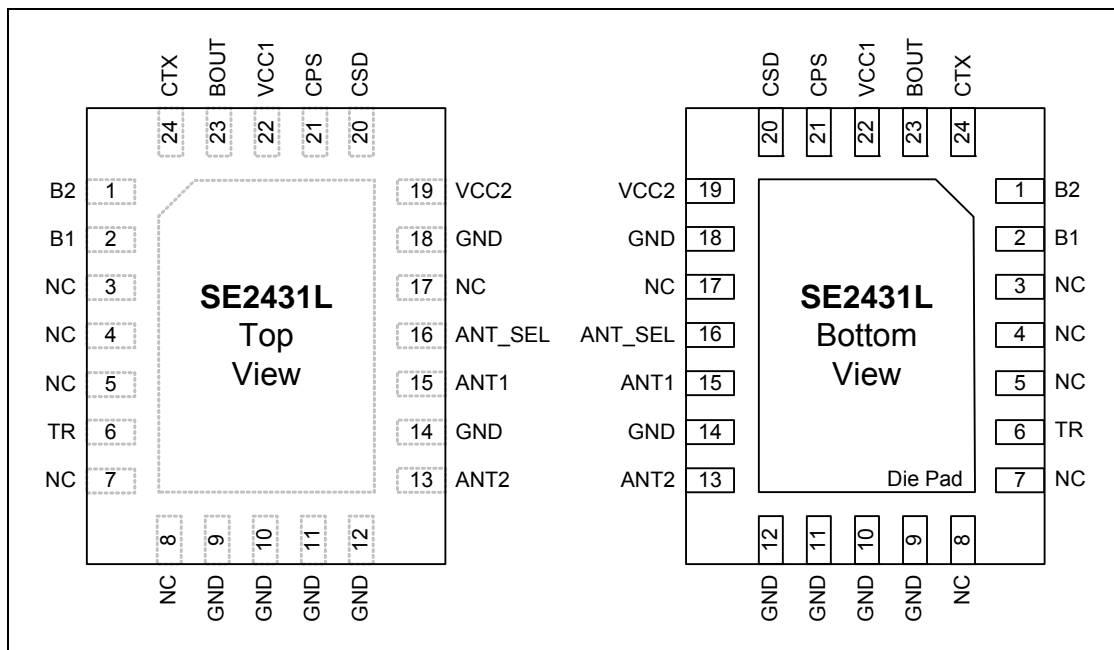


Figure 2: SE2431L Pinout

Pin Out Description

Pin No.	Name	Description
1	B2	Connect through bias resistor to Pin 23
2	B1	Connect through bias resistor to Pin 23
3	NC	Not connected internally to the device
4	NC	Not connected internally to the device
5	NC	Not connected internally to the device
6	T/R	Transmit/Receive port from/to transceiver, single ended 50 Ω
7	NC	Not connected internally to the device
8	NC	Not connected internally to the device
9	GND	Connect to PCB ground
10	GND	Connect to PCB ground
11	GND	Connect to PCB ground
12	GND	Connect to PCB ground
13	ANT2	Connect to 50 Ω antenna
14	GND	Connect to PCB ground
15	ANT1	Connect to 50 Ω antenna
16	ANT_SEL	Connect to GPIO signal to control antenna switch (see "Logic controls" table)
17	NC	Not connected internally to the device

Pin No.	Name	Description
18	GND	Connect to PCB ground
19	VCC2	Connect to positive supply
20	CSD	Connect to GPIO signal to control SE2431L modes (see "Logic controls" table)
21	CPS	Connect to GPIO signal to control SE2431L modes (see "Logic controls" table)
22	VCC1	Connect to positive supply
23	BOU	Connect to Pin 1 and Pin 2 through bias resistors
24	CTX	Connect to GPIO signal to control SE2431L modes (see "Logic controls" table)
Paddle	GND	Exposed die paddle; electrical and thermal ground; Connect to PCB ground

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This device is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

Symbol	Definition	Min.	Max.	Unit
VCC1	Supply Voltage	-0.3	3.6	V
VCC2	Supply Voltage	-0.3	3.8	V
	Control pin voltages	-0.3	3.6	V
T _{OP}	Operating temperature	-40	85	°C
T _{STORAGE}	Storage temperature	-40	125	°C
	ESD Voltage ALL pins (HBM)	-	1000	V
P _{out_Tx_max}	Tx output power at ANT1 or ANT2 port into 50 Ω load	-	24	dBm
P _{in_Tx_max}	Tx input power at TR port	-	+6	dBm
P _{in_Rx_max}	Rx input power at ANT1 or ANT2 ports	-	+5	dBm

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T _A	Ambient temperature	-40	25	85	°C
VCC1	Supply voltage on VCC pins	2.0	3.0	3.6	V
VCC2	Supply voltage on VCC pins	2.0	3.0	3.6	V

DC Electrical Characteristics

Conditions: VCC = 3.0 V, T_A = 25 °C, as measured on SiGe Semiconductor's SE2431L-EK1 evaluation board (de-embedded to device), unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _{CC-Tx20}	Total Supply Current	Tx mode P _{OUT} = 20 dBm CPS = CSD = CTX = 3.0 V	-	115	-	mA
I _{CC-Tx17}	Total Supply Current	Tx mode P _{OUT} = 17 dBm CPS = CSD = CTX = 3.0 V	-	90	-	mA
I _{CC-Tx10}	Total Supply Current	Tx mode P _{OUT} = 10 dBm CPS = CSD = CTX = 3.0 V	-	50	-	mA
I _{CQ-Tx}	Quiescent Current	No RF CPS = CSD = CTX = 3.0 V	-	30	-	mA
I _{CC-Rx}	Total Supply Current	Rx mode CPS = CSD = 3.0 V, CTX = 0 V	-	5	7	mA
I _{CC-RxBypass}	Total Supply Current	Rx bypass mode CSD = 3.0 V, CPS = CTX = 0 V	-	-	300	uA
I _{CC-OFF}	Sleep Supply Current	No RF, CTX=CPS=CSD = 0 V	-	0.05	1	μA

Logic Characteristics

Conditions: $V_{CC} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, as measured on SiGe Semiconductor's SE2431L-EK1 evaluation board (de-embedded to device), unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Logic input high		$V_{CC} - 0.3$	-	3.6	V
V_{IL}	Logic input low		0	-	0.3	V
I_{IH}	Logic input high		-	-	1	μA
I_{IL}	Logic input low		-	-	1	μA

Logic Controls

Conditions: $V_{CC} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$

Mode	Mode description	Note	CPS	CSD	CTX
0	All off (sleep mode)	1, 3	0	0	0
1	Rx bypass mode	1, 2	0	1	0
2	Rx LNA mode	1, 2	1	1	0
3	Tx mode	1, 2	X	1	1

Note: (1) Logic '0' level compliant to V_{IL} as specified in the "Logic Characteristics" table
(2) Logic '1' level compliant to V_{IH} as specified in the "Logic Characteristics" table
(3) All controls must be at logic '0' in order to achieve the specified sleep current

Conditions: $V_{CC} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$

Mode description	Note	CPS	CSD	CTX	ANT_SEL
ANT1 port enabled	1	X	X	X	0
ANT2 port enabled	2	X	X	X	1

Note: (1) Logic '0' level compliant to V_{IL} as specified in the "Logic Characteristics" table
(2) Logic '1' level compliant to V_{IH} as specified in the "Logic Characteristics" table

AC Electrical Characteristics, Transmit

Conditions: $V_{CC} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, as measured on SiGe Semiconductor's SE2431L-EK1 evaluation board (de-embedded to device), all unused ports terminated with $50\text{ }\Omega$, unless otherwise noted.

Symbol	Parameter	Condition	Note	Min.	Typ.	Max.	Unit
F_{IN}	Frequency Range			2400	-	2483	MHz
P_{out}	Output power at ANT1 or ANT2 ports	$V_{CC} = 3.6\text{ V}$ $V_{CC} = 3.3\text{ V}$ $V_{CC} = 3.0\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 2.0\text{ V}$	1, 6	-	24.0 22.5 21.0 20.5 17.0	-	dBm
S_{21}	Small Signal Gain	2400 – 2483 MHz		21	23	25	dB
ΔS_{21}	Small Signal Gain Variation	Gain variation across all ZigBee channels	1	-	-	1	dBp-p
HD2, HD3	Harmonics	$P_{OUT} = 20\text{ dBm}$	1, 2	-	-	-42	dBm/MHz
S_{22_ANT}	Output return loss	At ANT1 or ANT2 ports	1	-	-10	-5	dB
S_{11}	Input return loss	At TR Port, Tx mode	1	-	-10	-5	dB
ACP	Spectral Mask		1, 3	-	-	-30	dBm
Trise	Turn on time		4	-	-	800	ns
Tfall	Turn off time		5	-	-	800	ns
STAB	Stability	CW, $P_{IN} = 0\text{ dBm}$ 0.1 GHz – 20 GHz Load VSWR = 6:1		All non-harmonically related outputs less than -42 dBm/MHz			
RU	Ruggedness	CW, $P_{IN} = +6\text{ dBm}$, Load VSWR = 10:1		No permanent damage			

- Note:**
- (1) 2400 – 2483 MHz
 - (2) IEEE 802.15.4 source
 - (3) Integrated power from band edges to $F_c \pm 3.5\text{ MHz}$
 - (4) From 50% of CTX edge to 90% of final RF output power
 - (5) From 50% of CTX edge to 10% of final RF output power
 - (6) oEVM = 1% typ

AC Electrical Characteristics, Receive

Conditions: $V_{CC} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, as measured on SiGe Semiconductor's SE2431L-EK1 evaluation board (de-embedded to device), all unused ports terminated with $50\text{ }\Omega$, unless otherwise noted.

Symbol	Parameter	Condition	Note	Min.	Typ.	Max.	Unit
F_{IN}	Frequency Range			2400	-	2483	MHz
Rx_gain	Receive gain	CPS = CSD = logic '1', CTX = logic '0'	1	10	12.5	15	dB
NF	Receive noise figure	CPS = CSD = logic '1', CTX = logic '0'	1	-	2	2.5	dB
IIP3	Input 3 rd order intercept	CPS = CSD = logic '1', CTX = logic '0'	1	-3	2	-	dBm
IP1dB	Input 1-dB compression point	CPS = CSD = logic '1', CTX = logic '0'	1	-13	-8	-	dBm
S_{11_ANT}	Antenna port return loss		1	-	-10	-5	dB
S_{22}	Output return loss	At TR Port, Rx mode	1	-	-10	-5	dB
Trise	Turn on time		2	-	-	800	ns
Tfall	Turn off time		3	-	-	800	ns
G_bp	Gain in bypass mode	CPS = CTX = logic '0', CSD = logic '1'		-3	-2	-	dB
IP1dB	Input 1-dB compression point in bypass mode	CPS = CTX = logic '0', CSD = logic '1'		10	-	-	dBm

Note: (1) 2400 – 2483 MHz
(2) From 50% of CTX edge to 90% of final RF output power
(3) From 50% of CTX edge to 10% of final RF output power

AC Electrical Characteristics, Diversity Antenna Function

Conditions: $V_{CC1} = V_{CC2} = 3.0\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, as measured on SiGe Semiconductor's SE2432L-EK1 evaluation board (de-embedded to device), all unused ports terminated with $50\text{ }\Omega$, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
ISOL _{ANTSW}	Isolation Between ANT1 and ANT2 Ports	-	-20	-	dB
$T_{ANT1-ANT2}$	Antenna 1 to Antenna 2 switching time	-	400	-	nsec

Package Information

This package is Pb free, RoHS compliant and halogen free. The product is also rated MSL1.

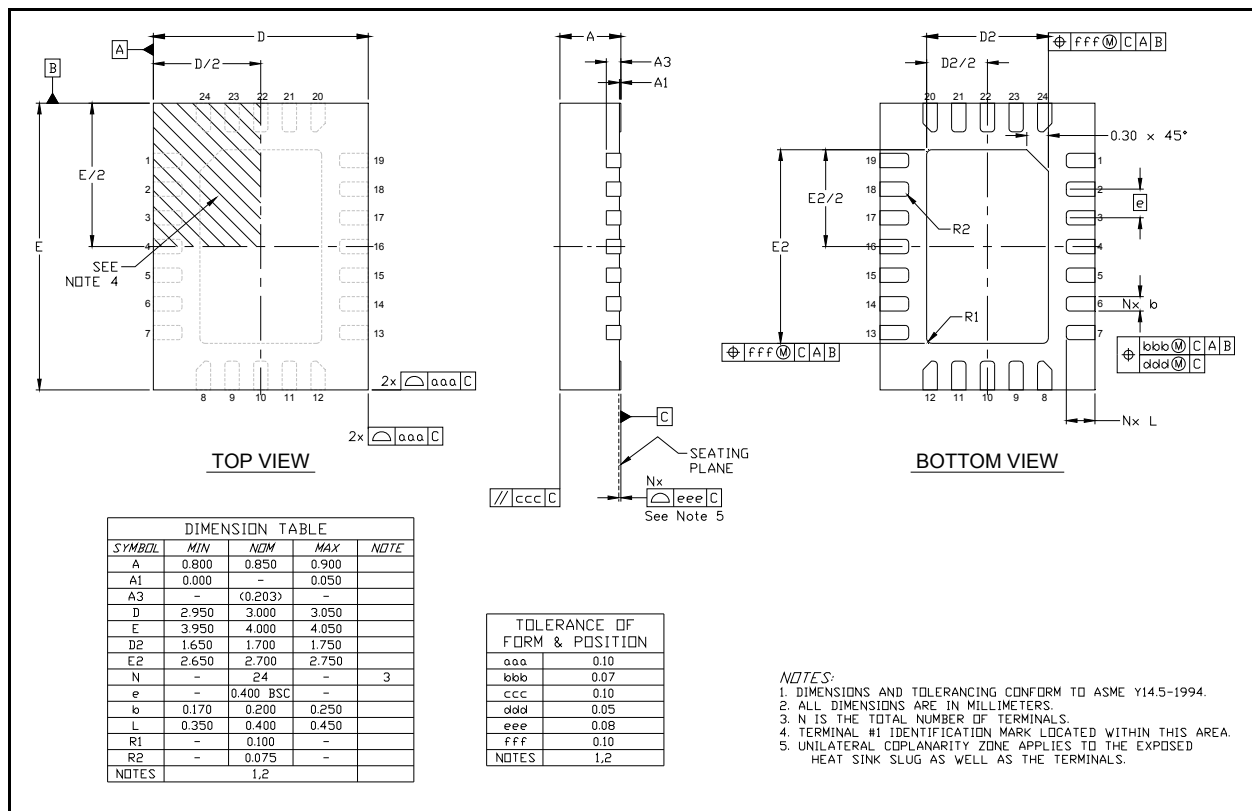


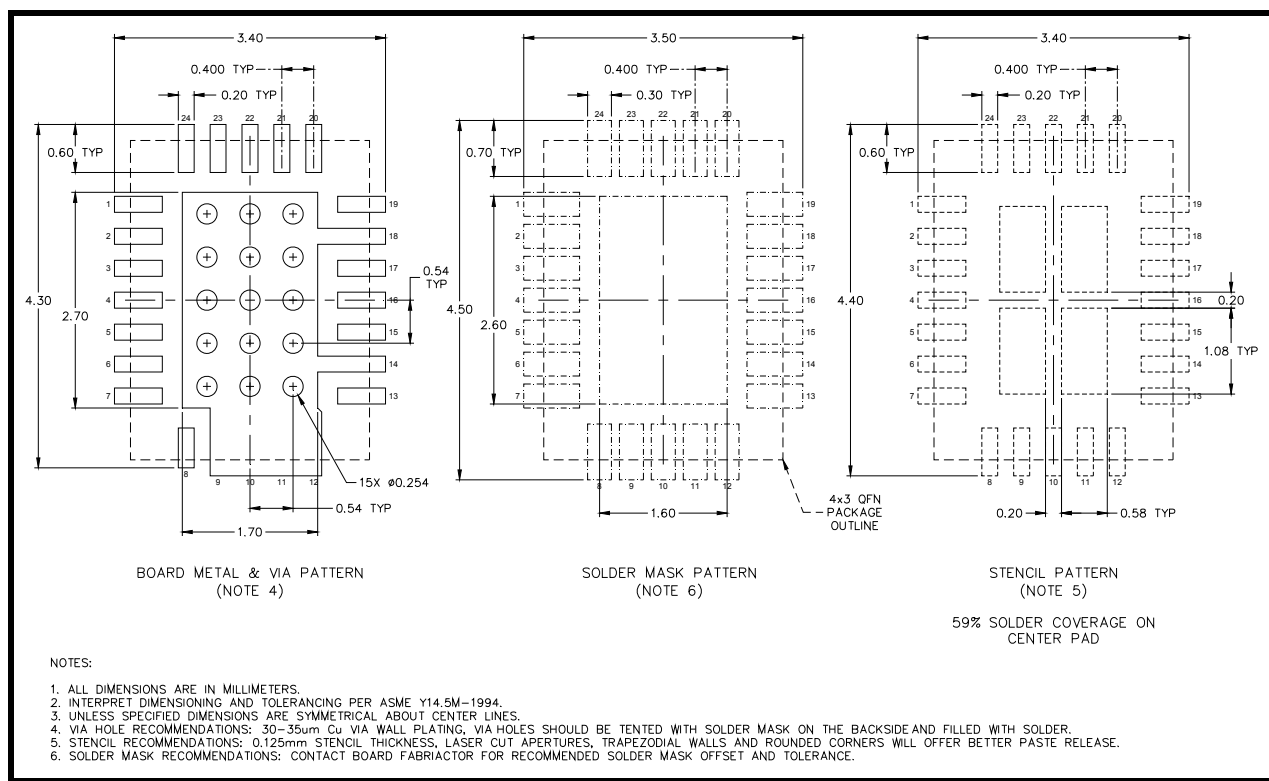
Figure 3: SE2431L Package Diagram

Recommended PCB Footprint

The PCB footprint below is only for reference.

The user should modify the design layout in order to meet their specific solder fillet requirements & solder joint reliability requirements.

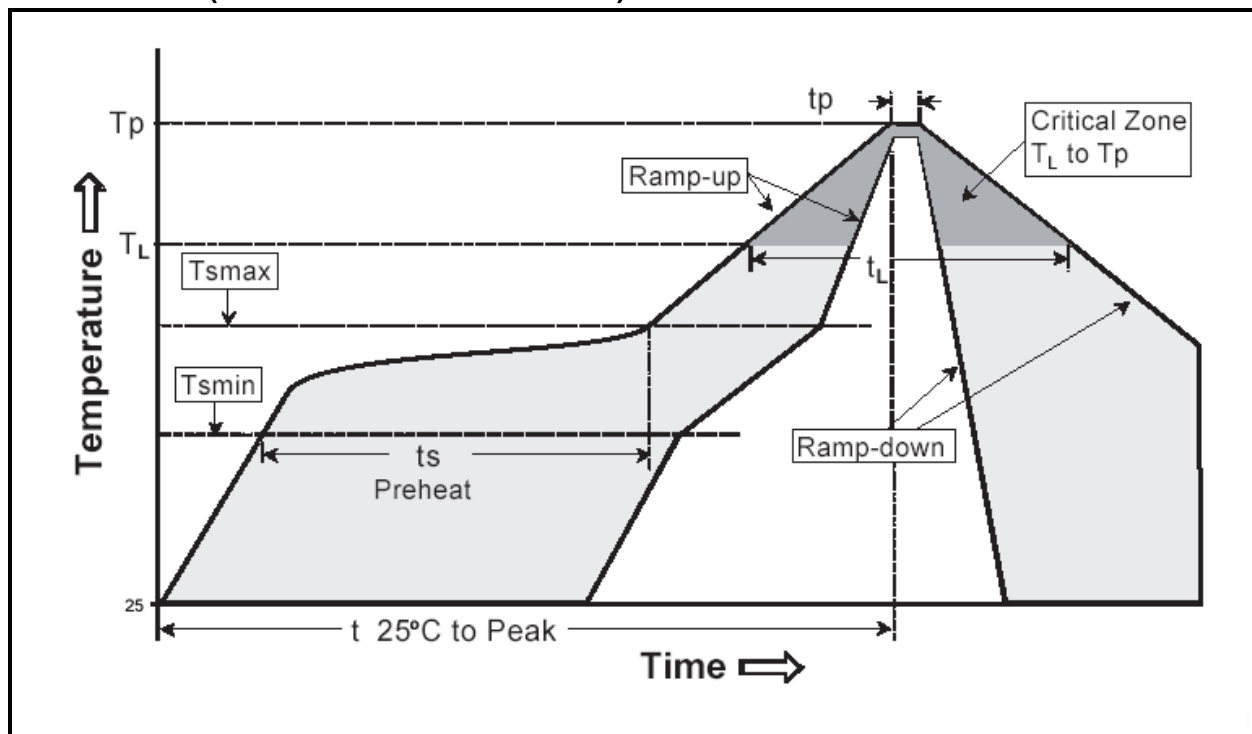
All dimensions in the figure below are in mm.



Recommended Reflow Temperature Profile

Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average Ramp-up Rate (T_L to T_P)	3°C/s (max)	3°C/s (max)
Preheat		
Temperature Min. (T_{smin})	100°C	150°C
Temperature Max. (T_{smax})	150°C	200°C
Time (Min. to Max) (t_s)	60 - 120s	60 - 80s
Ramp Up		
T_{smax} to t_L	-	3°C/s (max)
Time 25°C to Peak Temperature	6 mins. (max)	8 mins. (max)
Reflow		
Temperature (t_L)	183°C	217°C
Time maintained above t_L	60 - 150s	60 - 150s
Peak Temperature (t_p)	240 ±5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (t_p)	10 - 30s	20 - 40s
Ramp-Down		
Ramp-Down Rate	6°C/s (max)	6°C/s (max)

Reflow Profile (Reference JEDEC J-STD-020)



Branding Information

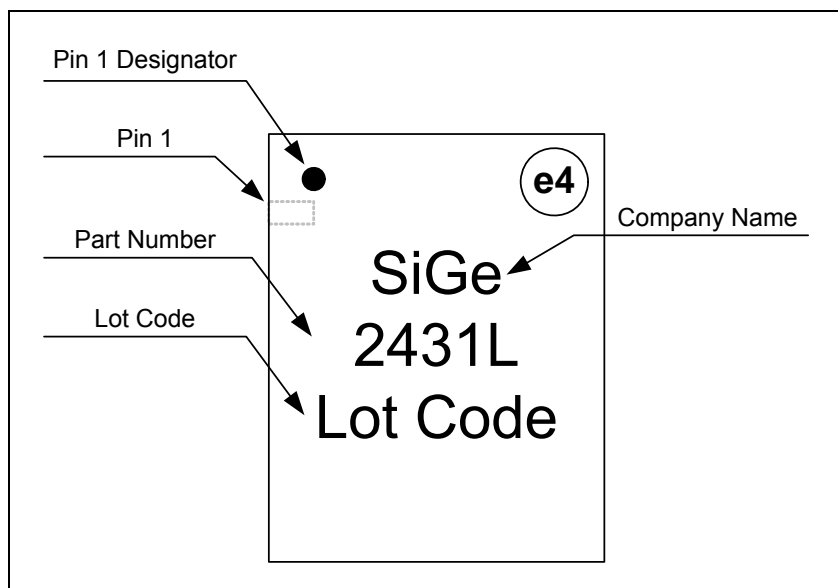


Figure 4: SE2431L Branding

Tape and Reel Information

Parameter	Value
Devices Per Reel	3000
Reel Diameter	13 inches
Tape Width	12 millimeters

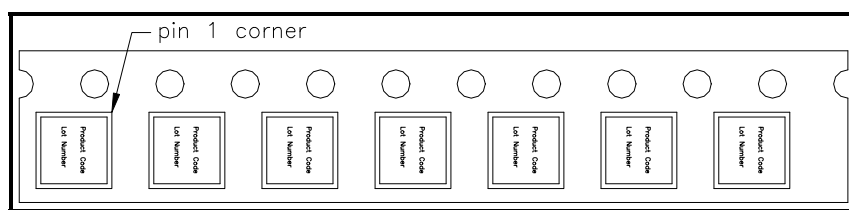


Figure 5: SE2431L-R Tape and Reel Information

<http://www.sige.com>

Email: sales@sige.com

Customer Service Locations:

North America:
1050 Morrison Drive, Suite 100
Ottawa ON K2H 8K7 Canada

Phone: +1 613 820 9244
Fax: +1 613 820 4933

Hong Kong
Phone: +852 3428 7222
Fax: +852 3579 5450

San Diego
Phone: +1 858 668 3541 (ext. 226)
Fax: +1 858 668 3546

United Kingdom
Phone: +44 1279 464217
Fax: +44 1279 464201

Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor, Inc. reserves the right to change information at any time without notification.

Production testing may not include testing of all parameters.

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