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PIC12F635/PIC16F636/639

8/14-Pin Flash-Based, 8-Bit CMOS Microcontrollers With nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%
  - Software selectable frequency range of 8 MHz to 31 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
- Clock mode switching for low power operation
- Power-saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended Temperature range
- Power-on Reset (POR)
- Wake-up Reset (WUR)
- Independent weak pull-up/pull-down resistors
- Programmable Low-Voltage Detect (PLVD)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection (program and data independent)
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low Power Features:

- Standby Current:
  - 1 nA @ 2.0V, typical
- Operating Current:
  - 8.5 µA @ 32 kHz, 2.0V, typical
  - 100 µA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 µA @ 2.0V, typical

Peripheral Features:

- 6/12 I/O pins with individual direction control:
  - High-current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups/ pull-downs
  - Ultra Low-Power Wake-up
- Analog comparator module with:
  - Up to two analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and outputs externally accessible
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- KEELOQ® compatible hardware Cryptographic module
- In-Circuit Serial Programming™ (ICSP™) via two pins

Low Frequency Analog Front-End Features (PIC16F639 only):

- Three input pins for 125 kHz LF input signals
- High input detection sensitivity (3 mV_{PP}, typical)
- Demodulated data, Carrier clock or RSSI output selection
- Input carrier frequency: 125 kHz, typical
- Input modulation frequency: 4 kHz, maximum
- 8 internal configuration registers
- Bidirectional transponder communication (LF talk back)
- Programmable antenna tuning capacitance (up to 63 pF, 1 pF/step)
- Low standby current: 5 µA (with 3 channels enabled), typical
- Low operating current: 15 µA (with 3 channels enabled), typical
- Serial Peripheral Interface (SPI™) with internal MCU and external devices
- Supports Battery Back-up mode and batteryless operation with external circuits

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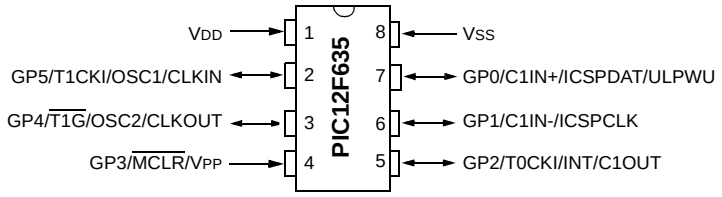
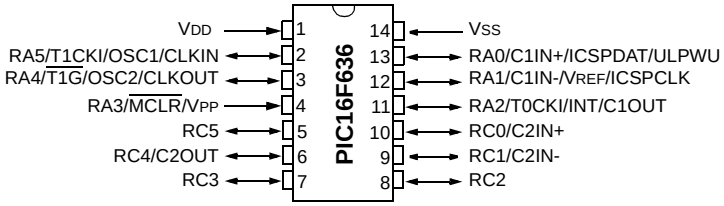
Device	Program Memory	Data Memory		I/O	Comparators	Low Frequency Analog Front-End
	Flash (words)	SRAM (bytes)	EEPROM (bytes)			
PIC12F635	1024	64	128	6	1	N
PIC16F636	2048	128	256	12	2	N
PIC16F639	2048	128	256	12	2	Y

Pin Diagrams

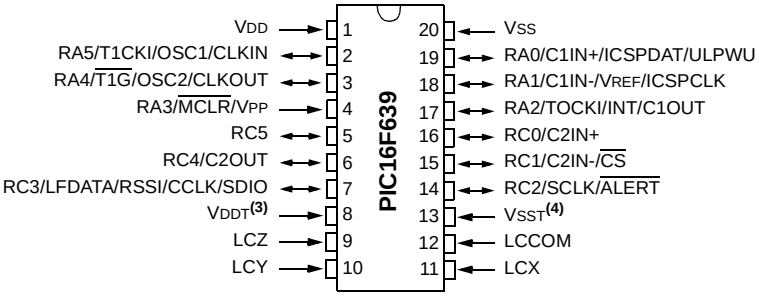
8-Pin PDIP, SOIC, DFN-S



14-Pin PDIP, SOIC, TSSOP



20-Pin SSOP



Note 1: Any references to PORTA, RAn, TRISA and TRISAn refer to GPIO, GPn, TRISIO and TRISIOn, respectively.

2: Additional information on I/O ports may be found in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

3: VDDT is the supply voltage of the Analog Front-End section (PIC16F639 only). VDDT is treated as VDD in this document unless otherwise stated.

4: VSST is the ground reference voltage of the Analog Front-End section (PIC16F639 only). VSST is treated as VSS in this document unless otherwise stated.

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1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F635/PIC16F636/639 devices. Additional information may be found in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The reference manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC12F635/PIC16F636/639 devices are covered by this data sheet. Figure 1-1 shows a block diagram of the PIC12F635/PIC16F636/639 devices. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC12F635 BLOCK DIAGRAM

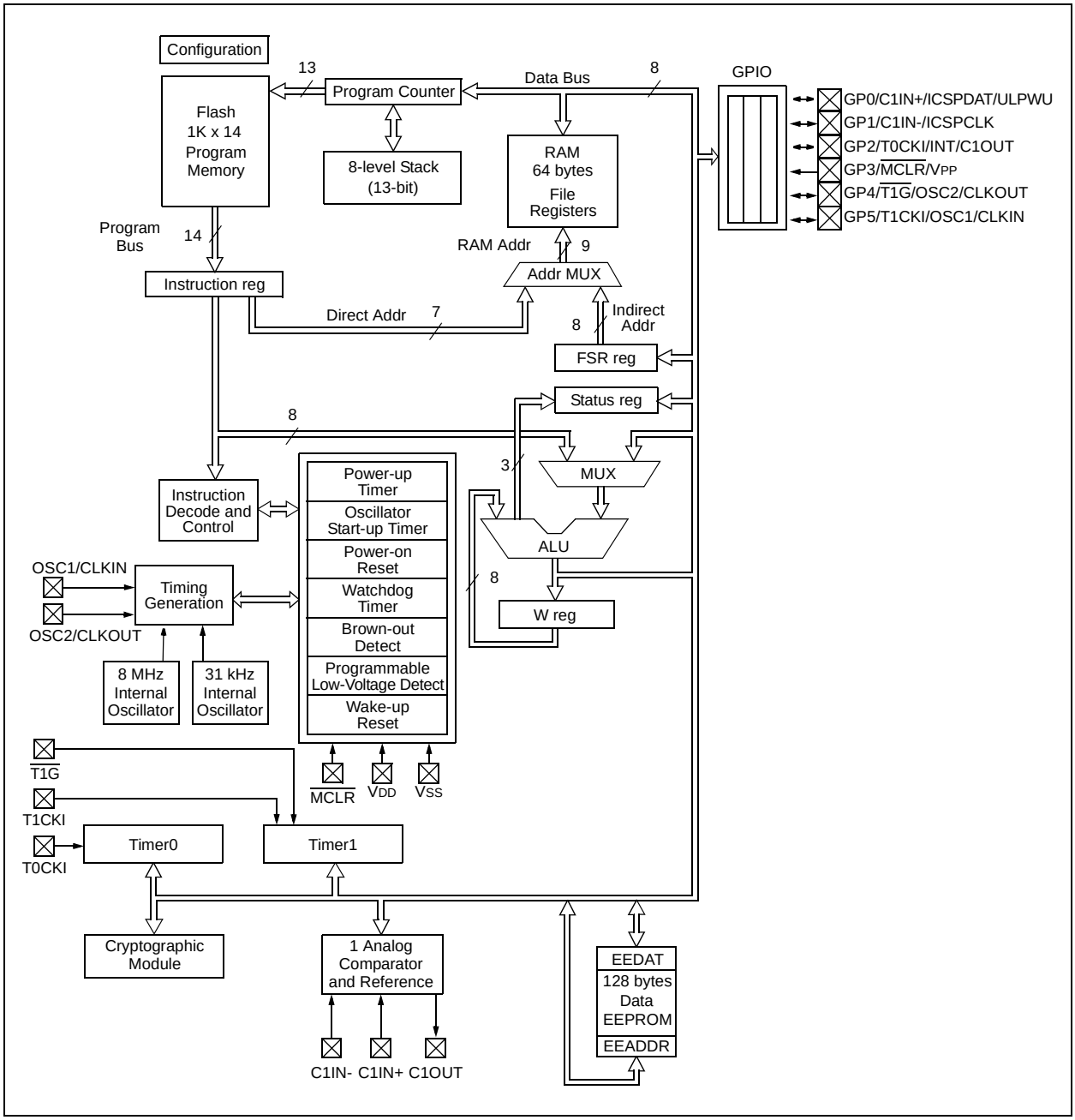

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FIGURE 1-2: PIC16F636 BLOCK DIAGRAM

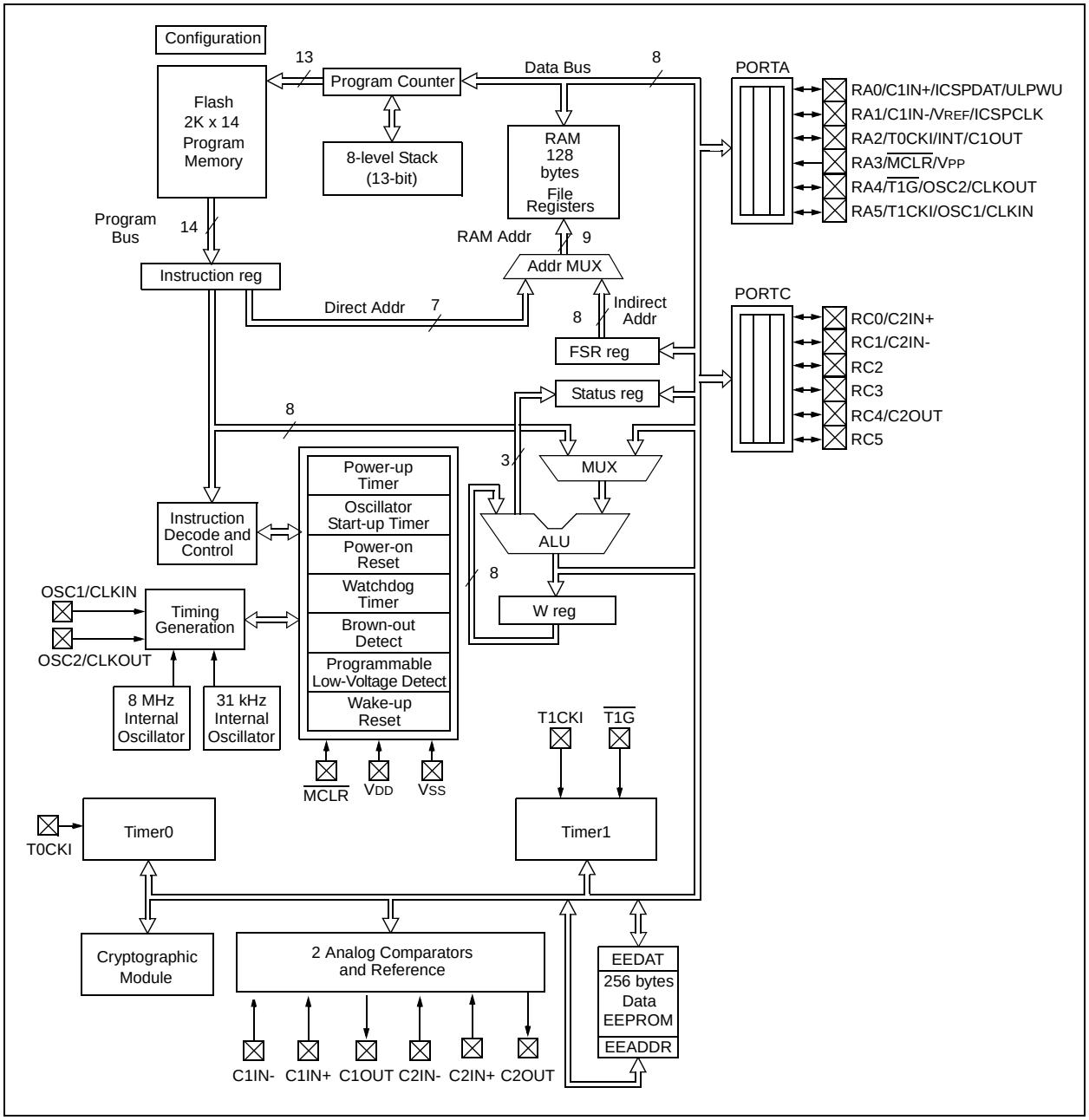

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FIGURE 1-3: PIC16F639 BLOCK DIAGRAM

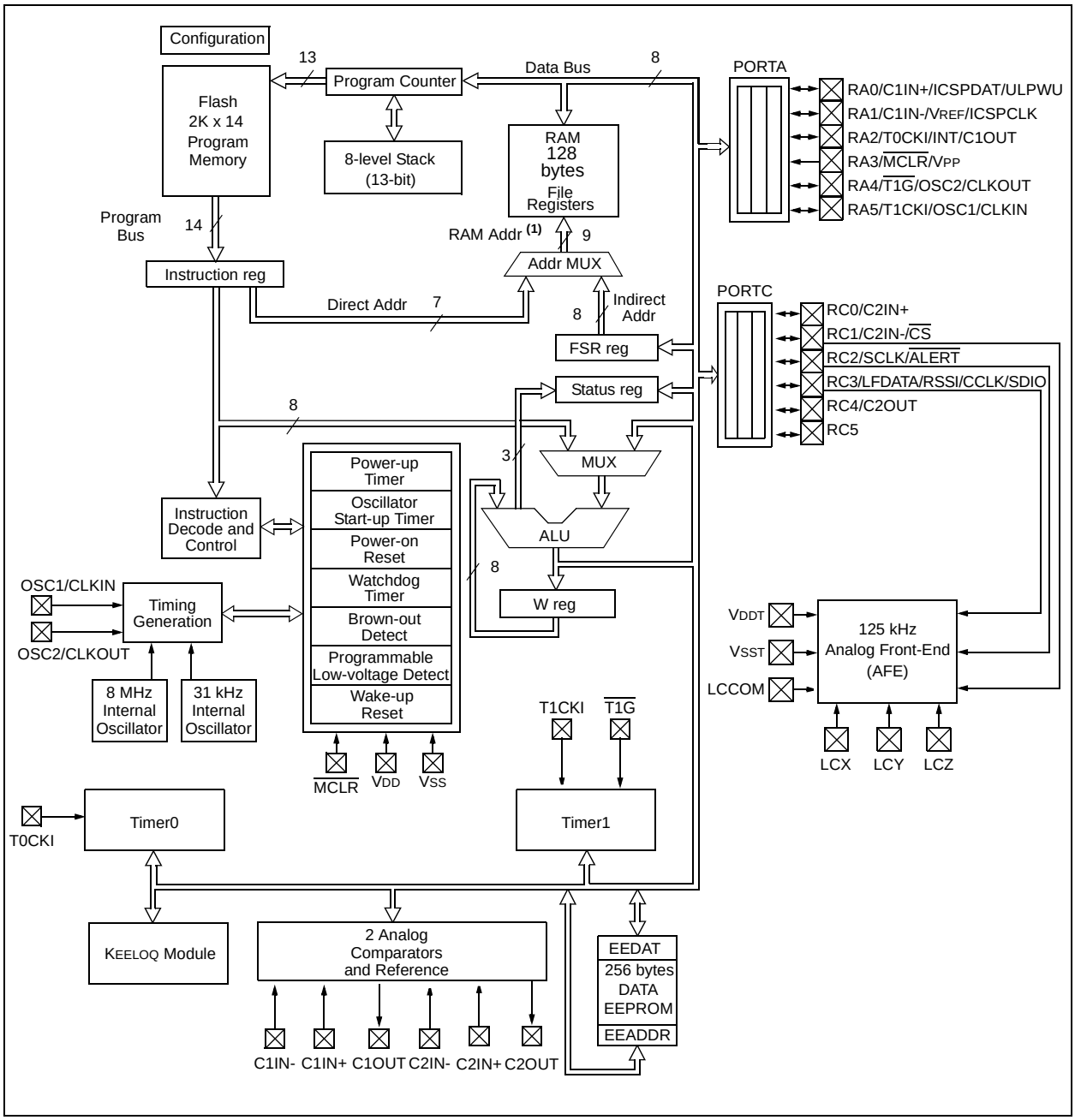

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TABLE 1-1: PIC12F635 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
VDD	VDD	D	—	Power supply for microcontroller.
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC reference clock.
GP4/$\overline{\text{T1G}}$/OSC2/CLKOUT	GP4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
GP3/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
GP2/T0CKI/INT/C1OUT	GP2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
GP1/C1IN-/ICSPCLK	GP1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	ICSPCLK	ST	—	Serial programming clock.
GP0/C1IN+/ICSPDAT/ULPWU	GP0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct; HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL = Crystal

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TABLE 1-2: PIC16F636 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
VDD	VDD	D	—	Power supply for microcontroller.
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock.
	OSC1	XTAL	—	XTAL connection.
	CLKIN	ST	—	TOSC reference clock.
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate.
	OSC2	—	XTAL	XTAL connection.
	CLKOUT	—	CMOS	TOSC/4 reference clock.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage.
RC5	RC5	TTL	CMOS	General purpose I/O.
RC4/C2OUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator 2 output.
RC3	RC3	TTL	CMOS	General purpose I/O.
RC2	RC2	TTL	CMOS	General purpose I/O.
RC1/C2IN-	RC1	TTL	CMOS	General purpose I/O.
	C2IN-	AN	—	Comparator 1 input – negative.
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O.
	C2IN+	AN	—	Comparator 1 input – positive.
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator 1 output.
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator 1 input – negative.
	ICSPCLK	ST	—	Serial programming clock.
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator 1 input – positive.
	ICSPDAT	TTL	CMOS	Serial programming data I/O.
	ULPWU	AN	—	Ultra Low-Power Wake-up input.
VSS	VSS	D	—	Ground reference for microcontroller.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; D = Direct; HV = High Voltage; ST = Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL = Crystal

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TABLE 1-3: PIC16F639 PINOUT DESCRIPTIONS

Name	Function	Input Type	Output Type	Description
VDD	VDD	D	—	Power supply for microcontroller
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	XTAL connection
	CLKIN	ST	—	TOSC/4 reference clock
RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT	RA4	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	$\overline{\text{T1G}}$	ST	—	Timer1 gate
	OSC2	—	XTAL	XTAL connection
	CLKOUT	—	CMOS	TOSC reference clock
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	General purpose input. Individually controlled interrupt-on-change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear Reset. Pull-up enabled when configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Programming voltage
RC5	RC5	TTL	CMOS	General purpose I/O
RC4/C2OUT	RC4	TTL	CMOS	General purpose I/O
	C2OUT	—	CMOS	Comparator2 output
RC3/LFDATA/RSSI/CCLK/SDIO	RC3	TTL	CMOS	General purpose I/O
	LFDATA	—	CMOS	Digital output representation of analog input signal to LC pins.
	RSSI	—	Current	Received signal strength indicator. Analog current that is proportional to input amplitude.
	CCLK	—	—	Carrier clock output
	SDIO	TTL	CMOS	Input/Output for SPI communication
VDDT	VDDT	D	—	Power supply for Analog Front-End. In this document, VDDT is treated the same as VDD, unless otherwise stated.
LCZ	LCZ	AN	—	125 kHz analog Z channel input
LCY	LCY	AN	—	125 kHz analog Y channel input
LCX	LCX	AN	—	125 kHz analog X channel input
LCCOM	LCCOM	AN	—	Common reference for analog inputs
VSST	VSST	D	—	Ground reference for Analog Front-End. In this document, VSST is treated the same as VSS, unless otherwise stated.
RC2/SCLK/$\overline{\text{ALERT}}$	RC2	TTL	CMOS	General purpose I/O
	SCLK	TTL	—	Digital clock input for SPI communication
	$\overline{\text{ALERT}}$	—	OD	Output with internal pull-up resistor for AFE error signal
RC1/C2IN-/$\overline{\text{CS}}$	RC1	TTL	CMOS	General purpose I/O
	C2IN-	AN	—	Comparator1 input - negative
	$\overline{\text{CS}}$	TTL	—	Chip select input for SPI communication with internal pull-up resistor
RC0/C2IN+	RC0	TTL	CMOS	General purpose I/O
	C2IN+	AN	—	Comparator1 input - positive
RA2/T0CKI/INT/C1OUT	RA2	ST	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	T0CKI	ST	—	External clock for Timer0
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator1 output
RA1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down.
	C1IN-	AN	—	Comparator1 input – negative
	ICSPCLK	ST	—	Serial Programming Clock
RA0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	—	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up/pull-down. Selectable Ultra Low-Power Wake-up pin.
	C1IN+	AN	—	Comparator1 input – positive
	ICSPDAT	TTL	CMOS	Serial Programming Data IO
	ULPWU	AN	—	Ultra Low-Power Wake-up input
VSS	VSS	D	—	Ground reference for microcontroller

Legend: AN = Analog input or output; HV = High Voltage; TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; XTAL = Crystal; D = Direct; OD = Direct

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2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F635/PIC16F636/639 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh, for the PIC12F635) and 2K x 14 (0000h-07FFh, for the PIC16F636/639) is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are GPRs, implemented as static RAM for the PIC16F636/639. For the PIC12F635, register locations 40h through 7Fh are GPRs implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

TABLE 2-1: BANK SELECTION

RP0	RP1	Bank
0	0	0
1	0	1
0	1	2
1	1	3

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK OF THE PIC12F635

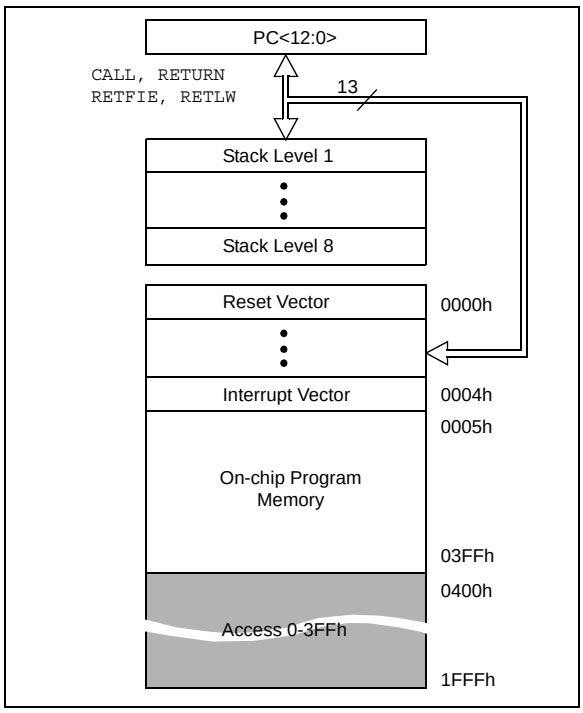
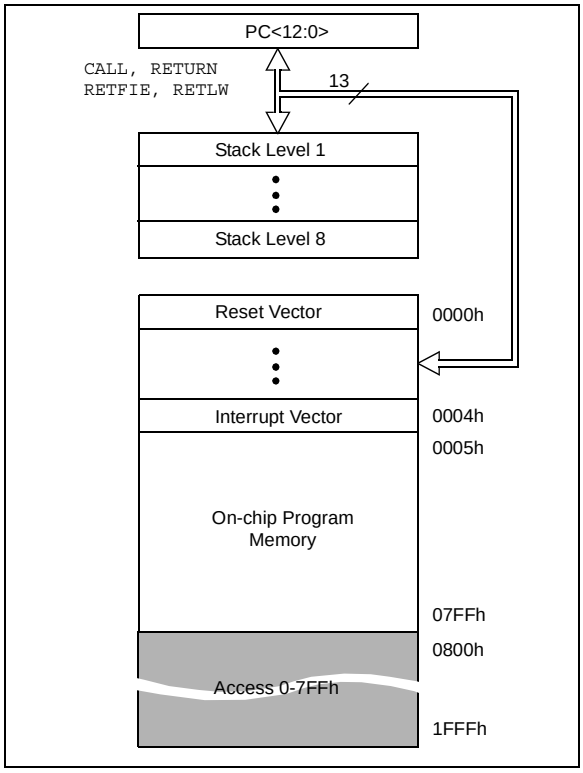


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK OF THE PIC16F636/639



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2.2.1 GENERAL PURPOSE REGISTER

The register file is organized as 64 x 8 for the PIC12F635 and 128 x 8 for the PIC16F636/639. Each register is accessed, either directly or indirectly, through the File Select Register, FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Figure 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

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FIGURE 2-3: PIC12F635 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
GPIO	05h	TRISIO	85h		105h		185h
	06h		86h		106h		186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
	3Fh						
General Purpose Register 64 Bytes	40h						
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> are KEELOQ® hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

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FIGURE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS

	File Address		File Address		File Address		File Address
Indirect addr.(1)	00h	Indirect addr. (1)	80h	Accesses 00h-0Bh	100h	Accesses 80h-8Bh	180h
TMR0	01h	OPTION_REG	81h		101h		181h
PCL	02h	PCL	82h		102h		182h
STATUS	03h	STATUS	83h		103h		183h
FSR	04h	FSR	84h		104h		184h
PORTA	05h	TRISA	85h		105h		185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah		10Ah		18Ah
INTCON	0Bh	INTCON	8Bh		10Bh		18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	CRCON	110h		190h
	11h		91h	CRDAT0(2)	111h		191h
	12h		92h	CRDAT1(2)	112h		192h
	13h		93h	CRDAT2(2)	113h		193h
	14h	LVDCON	94h	CRDAT3(2)	114h		194h
	15h	WPUDA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h	WDA	97h		117h		197h
WDTCON	18h		98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh		11Bh		19Bh
	1Ch	EECON1	9Ch		11Ch		19Ch
	1Dh	EECON2(1)	9Dh		11Dh		19Dh
	1Eh		9Eh		11Eh		19Eh
	1Fh		9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
			EFh		16Fh		1EFh
		Accesses 70h-7Fh	F0h	Accesses 70h-7Fh	170h	Accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: CRDAT<3:0> are KEELOQ hardware peripheral related registers and require the execution of the "KEELOQ® Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

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TABLE 2-2: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD/ WUR	Value on all other Resets(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xx00	--uu uu00
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	—	C1IF	OSFIF	—	TMR1IF	000- 00-0	000- 00-0
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000
19h	CMCON0	—	C1OUT	—	C1INV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

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TABLE 2-3: PIC12F635 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD/ WUR	Value on all other Resets(1)
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 0000	0000 0000
8Ch	PIE1	EEIE	LVDIE	CRIE	—	C1IE	OSFIE	—	TMR1IE	000- 00-0	000- 00-0
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBODEN	$\overline{\text{WUR}}$	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$	--01 q-qq	--0u u-uu
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 x000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: GP3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register.

3: $\overline{\text{MCLR}}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset, but will set again if the mismatch exists.

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TABLE 2-4: PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD/ WUR	Value on all other Resets(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuxx
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xx00	--uu uu00
06h	—	Unimplemented								—	—
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xx00	--uu uu00
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(2)	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	—	Unimplemented								—	—
1Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{MCLR}$ Reset and Watchdog Timer Reset during normal operation.

2: $\overline{MCLR}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

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TABLE 2-5: PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD/ WUR	Value on all other Resets(1)
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
86h	—	Unimplemented								—	—
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	---0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF(3)	0000 0000	0000 0000
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBODEN	$\overline{\text{WUR}}$	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$	--01 q-qq	--0u u-uu
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 x000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
95h	WPUDA(2)	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA(2)	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111
9Bh	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
9Eh	—	Unimplemented								—	—
9Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register.

3: $\overline{\text{MCLR}}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

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TABLE 2-6: PIC12F635/PIC16F636/639 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD/ WUR	Value on all other Resets(1)
Bank 2											
10Ch	—	Unimplemented								—	—
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	CRCON	GO/$\overline{\text{DONE}}$	ENC/$\overline{\text{DEC}}$	—	—	—	—	CRREG1	CRREG0	00-- --00	00-- --00
111h	CRDAT0(2)	Cryptographic Data Register 0								0000 0000	0000 0000
112h	CRDAT1(2)	Cryptographic Data Register 1								0000 0000	0000 0000
113h	CRDAT2(2)	Cryptographic Data Register 2								0000 0000	0000 0000
114h	CRDAT3(2)	Cryptographic Data Register 3								0000 0000	0000 0000
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: CRDAT<3:0> are KEELOQ® hardware peripheral related registers and require the execution of the "KEELOQ Encoder License Agreement" regarding implementation of the module and access to related registers. The "KEELOQ Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ or by contacting your local Microchip Sales Representative.

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2.2.2.1 Status Register

The Status register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (SRAM)

The Status register can be the destination for any instruction, like any other register. If the Status register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the Status register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the Status register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the Status register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 13.0 "Instruction Set Summary"**.

> **Note 1:** The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS – STATUS REGISTER (ADDRESS: 03h OR 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
`1` = Bank 2, 3 (100h-1FFh)
`0` = Bank 0, 1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
`11` = Bank 3 (180h-1FFh)
`10` = Bank 2 (100h-17Fh)
`01` = Bank 1 (80h-FFh)
`00` = Bank 0 (00h-7Fh)
Each bank is 128 bytes.

bit 4 **$\overline{TO}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
For $\overline{\text{Borrow}}$, the polarity is reversed.
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

> **Note:** For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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2.2.2.2 Option Register

The Option register is a readable and writable register which contains various control bits to configure:

- TMR0/WDT prescaler
- External RA2/INT interrupt
- TMR0
- Weak pull-up/pull-downs on PORTA

> **Note:** To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting the PSA bit to '1' (OPTION_REG<3>). See **Section 5.4 "Prescaler"**.

REGISTER 2-2: OPTION_REG – OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up/Pull-down Enable bit
1 = PORTA pull-ups/pull-downs are disabled
0 = PORTA pull-ups/pull-downs are enabled by individual port latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/INT pin
0 = Interrupt on falling edge of RA2/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI pin
0 = Increment on low-to-high transition on RA2/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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2.2.2.3 INTCON Register

The INTCON register is a readable and writable register which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

> **Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON – INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	T0IE	INTE	RAIE(1)	T0IF(2)	INTF	RAIF(3)
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RA2/INT External Interrupt Enable bit
1 = Enables the RA2/INT external interrupt
0 = Disables the RA2/INT external interrupt

bit 3 **RAIE:** PORTA Change Interrupt Enable bit(1)
1 = Enables the PORTA change interrupt
0 = Disables the PORTA change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RA2/INT External Interrupt Flag bit
1 = The RA2/INT external interrupt occurred (must be cleared in software)
0 = The RA2/INT external interrupt did not occur

bit 0 **RAIF:** PORTA Change Interrupt Flag bit(3)
1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software)
0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing the T0IF bit.

3: $\overline{\text{MCLR}}$ and WDT Reset do not affect the previous value data latch. The RAIF bit will be cleared upon Reset but will set again if the mismatch exists.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

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2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1 — PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS: 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE
bit 7							bit 0

bit 7 **EEIE**: EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **LVDIE**: Low-Voltage Detect Interrupt Enable bit
1 = Enables the LVD interrupt
0 = Disables the LVD interrupt

bit 5 **CRIE**: Cryptographic Interrupt Enable bit
1 = Enables the cryptographic interrupt
0 = Disables the cryptographic interrupt

bit 4 **C2IE**: Comparator 2 Interrupt Enable bit(1)
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 3 **C1IE**: Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE**: Oscillator Fail Interrupt Enable bit
1 = Enables the oscillator fail interrupt
0 = Disables the oscillator fail interrupt

bit 1 **Unimplemented**: Read as '0'

bit 0 **TMR1IE**: Timer1 Interrupt Enable bit
1 = Enables the Timer1 interrupt
0 = Disables the Timer1 interrupt

Note 1: PIC16F636/639 only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

> **Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1 – PERIPHERAL INTERRUPT REQUEST REGISTER 1 (ADDRESS: 0Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF
bit 7							bit 0

bit 7 **EEIF**: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **LVDIF**: Low-Voltage Detect Interrupt Flag bit
1 = The supply voltage has crossed selected LVD voltage (must be cleared in software)
0 = The supply voltage has not crossed selected LVD voltage

bit 5 **CRIF**: Cryptographic Interrupt Flag bit
1 = The Cryptographic module has completed an operation (must be cleared in software)
0 = The Cryptographic module has not completed an operation or is Idle

bit 4 **C2IF**: Comparator 2 Interrupt Flag bit(1)
1 = Comparator output (C2OUT bit) has changed (must be cleared in software)
0 = Comparator output (C2OUT bit) has not changed

bit 3 **C1IF**: Comparator 1 Interrupt Flag bit
1 = Comparator output (C1OUT bit) has changed (must be cleared in software)
0 = Comparator output (C1OUT bit) has not changed

bit 2 **OSFIF**: Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed INTOSC (must be cleared in software)
0 = System clock operating

bit 1 **Unimplemented**: Read as '0'

bit 0 **TMR1IF**: Timer1 Interrupt Flag bit
1 = Timer1 rolled over (must be cleared in software)
0 = Timer1 has not rolled over

Note 1: PIC16F636/639 only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-3) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Wake-up Reset ($\overline{\text{WUR}}$)
- Brown-out Detect ($\overline{\text{BOD}}$)
- Watchdog Timer Reset (WDT)
- External $\overline{\text{MCLR}}$ Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the $\overline{\text{BOD}}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON – POWER CONTROL REGISTER (ADDRESS: 8Eh)

U-0	U-0	R/W-0	R/W-1	R/W-x	U-0	R/W-0	R/W-x
—	—	ULPWUE	SBODEN(1)	$\overline{\text{WUR}}$	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **ULPWUE:** Ultra Low-Power Wake-up Enable bit
1 = Ultra Low-Power Wake-up enabled
0 = Ultra Low-Power Wake-up disabled

bit 4 **SBODEN:** Software BOD Enable bit(1)
1 = BOD enabled
0 = BOD disabled

bit 3 **$\overline{\text{WUR}}$**: Wake-up Reset Status bit
1 = No Wake-up Reset occurred
0 = A Wake-up Reset occurred (must be set in software after a Power-on Reset occurs)

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOD}}$:** Brown-out Detect Status bit
1 = No Brown-out Detect occurred
0 = A Brown-out Detect occurred (must be set in software after a Brown-out Detect occurs)

Note 1: BODEN<1:0> = 01 in the Configuration Word register for SBODEN to control the Brown-out Detect module.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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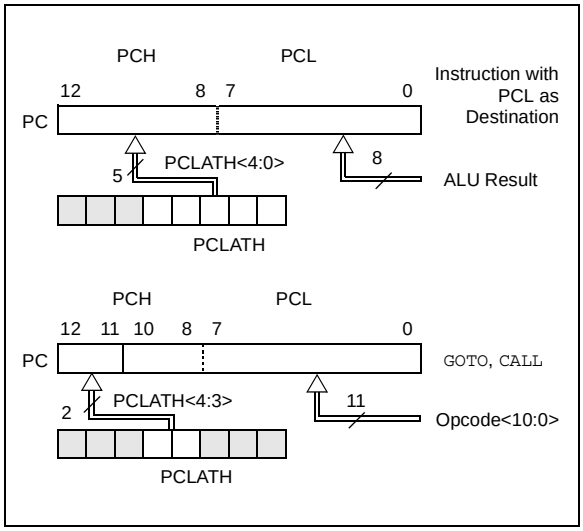
2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-5 shows the two situations for the loading of the PC. The upper example in Figure 2-5 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-5 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-5: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note *AN556, "Implementing a Table Read"* (DS00556).

2.3.2 STACK

The PIC12F635/PIC16F636/639 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

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2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

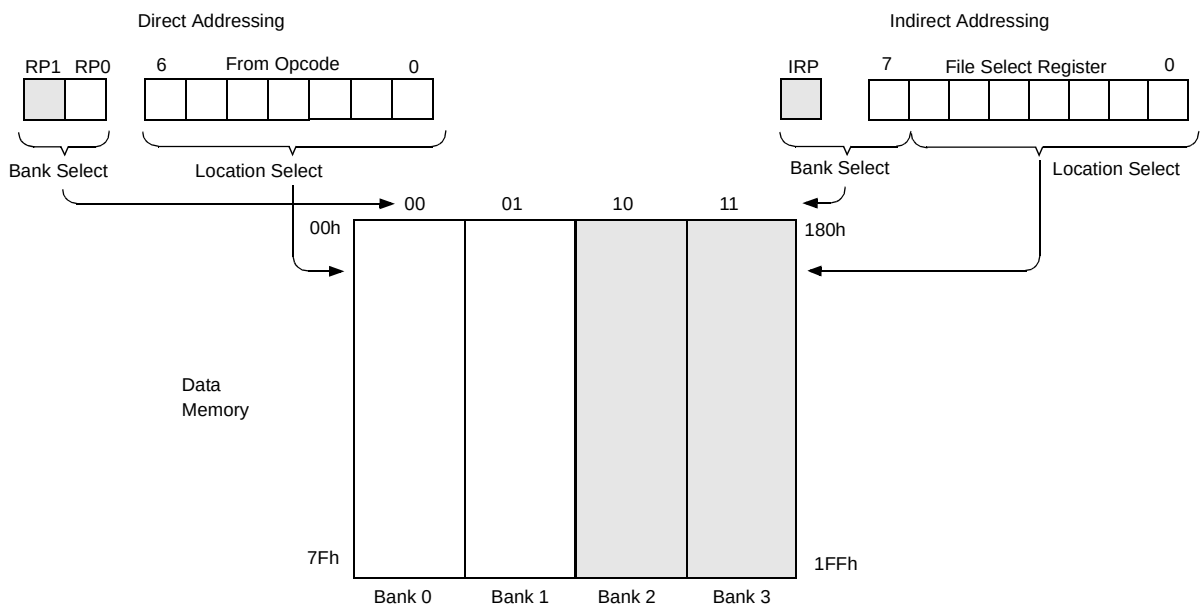
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit (STATUS<7>), as shown in Figure 2-6.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        MOVLW   0x20    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF register
        INCF    FSR     ;INC POINTER
        BTFSS   FSR,4   ;all done?
        GOTO    NEXT    ;no clear next
CONTINUE                ;yes continue
```

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING PIC12F635/PIC16F636/639



Note: For memory map detail, see Figure 2-2.

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NOTES:

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3.0 CLOCK SOURCES

3.1 Overview

The PIC12F635/PIC16F636/639 has a wide variety of clock sources and selection features to allow it to be used in a wide range of applications, while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the PIC12F635/PIC16F636/639 clock sources.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

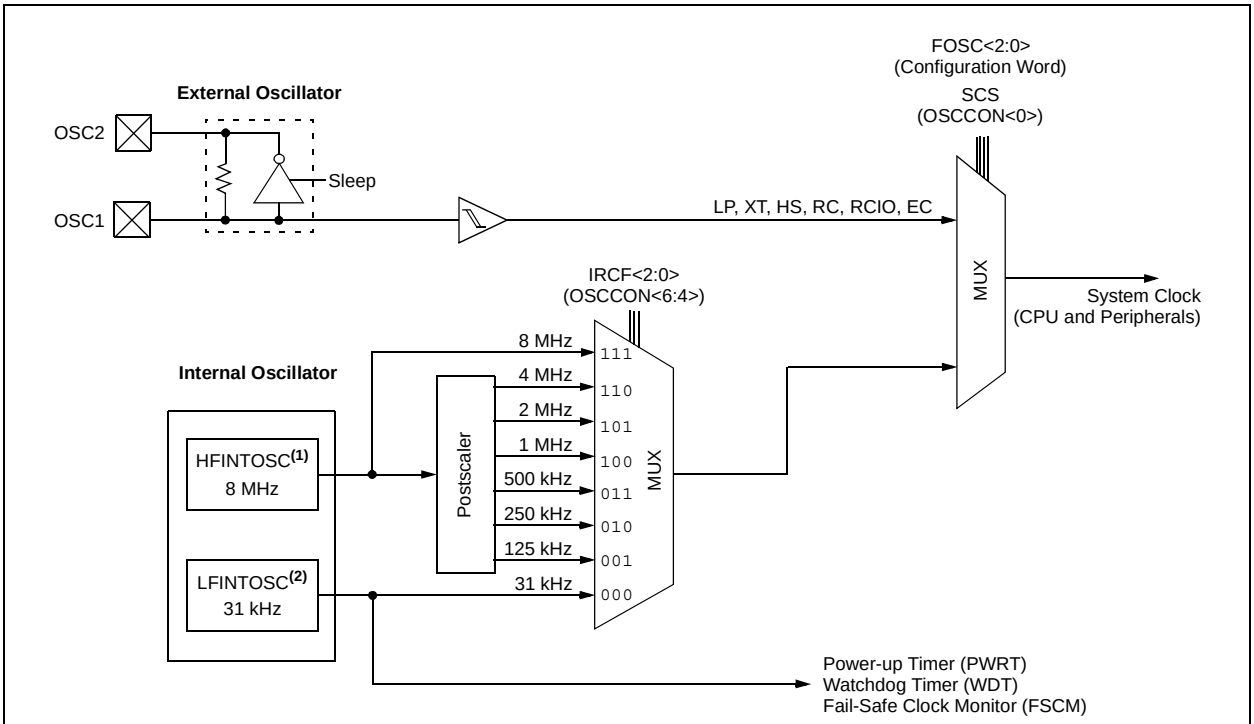
- Selectable system clock source between external or internal via software.
- Two-Speed Clock Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch to the internal oscillator.

The PIC12F635/PIC16F636/639 can be configured in one of eight clock modes.

1. EC – External clock with I/O on RA4.
2. LP – Low gain crystal or Ceramic Resonator Oscillator mode.
3. XT – Medium gain crystal or Ceramic Resonator Oscillator mode.
4. HS – High gain crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with FOSC/4 output on RA4.
6. RCIO – External Resistor-Capacitor (RC) with I/O on RA4.
7. INTOSC – Internal oscillator with FOSC/4 output on RA4 and I/O on RA5.
8. INTOSCIO – Internal oscillator with I/O on RA4 and RA5.

Clock source modes are configured by the FOSC<2:0> bits in the Configuration Word register (see **Section 12.0 "Special Features of the CPU"**). The internal clock can be generated by two oscillators. The HFINTOSC is a high-frequency calibrated oscillator. The LFINTOSC is a low-frequency uncalibrated oscillator.

FIGURE 3-1: PIC12F635/PIC16F636/639 CLOCK SOURCE BLOCK DIAGRAM



Note 1: HFINTOSC = High-Frequency Calibrated Internal Oscillator.
2: LFINTOSC = Low-Frequency Internal Oscillator is not calibrated.

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3.2 Clock Source Modes

Clock source modes can be classified as external or internal.

External clock modes rely on external circuitry for the clock source. Examples are oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC mode) circuits.

Internal clock sources are contained internally within PIC12F635/PIC16F636/639. The device has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 “Clock Switching”**).

3.3 External Clock Modes

3.3.1 OSCILLATOR START-UP TIMER (OST)

If the PIC12F635/PIC16F636/639 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from the OSC1 pin following a Power-on Reset (POR) and the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the PIC12F635/PIC16F636/639.

When switching between clock sources, a delay is required to allow the new clock to stabilize. Table 3-1 shows oscillator delay examples.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 3.6 “Two-Speed Clock Start-up Mode”**).

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz-8 MHz	5 µs-10 µs (approx.) CPU Start-up
Sleep/POR	EC, RC	DC – 20 MHz	
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	
Sleep/POR	LP, XT, HS	31 kHz-20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	125 kHz-8 MHz	1 µs (approx.)

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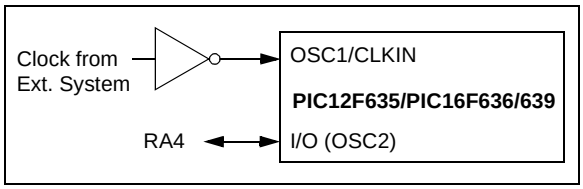
3.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 pin and the RA5 pin is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC12F635/PIC16F636/639 design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



3.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to the OSC1 and OSC2 pins (Figure 3-1). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

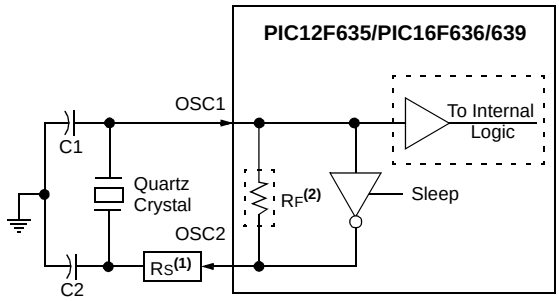
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is better suited to drive resonators with a medium drive level specification, for example, low-frequency AT-cut quartz crystal resonators.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is better suited for resonators that require a high drive setting, for example, high-frequency AT-cut quartz crystal resonators or ceramic resonators.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



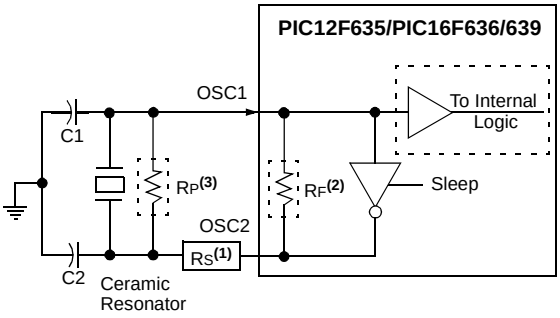
Note 1: A series resistor (R_S) may be required for quartz crystals with low drive level.

2: The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (R_S) may be required for ceramic resonators with low drive level.

2: The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation (typical value 1 MΩ).

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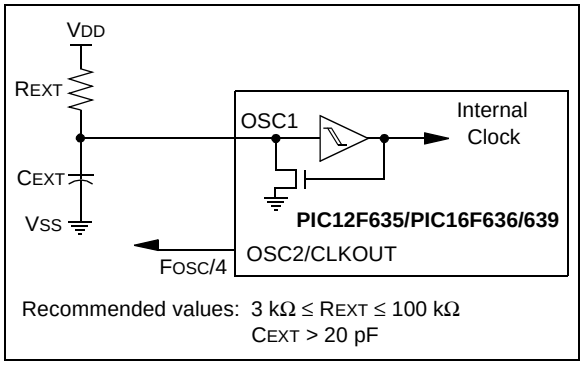
3.3.4 EXTERNAL RC MODES

The External Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes, RC and RCIO.

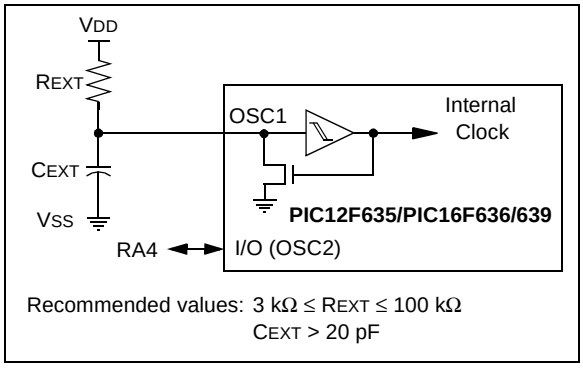
In RC mode, the RC circuit connects to the OSC1 pin. The OSC2/CLKOUT pin outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the RC mode connections.

FIGURE 3-5: RC MODE



In RCIO mode, the RC circuit is connected to the OSC1 pin. The OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 4 of PORTA (RA4). Figure 3-6 shows the RCIO mode connections.

FIGURE 3-6: RCIO MODE



The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal threshold voltage. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency or for low CEXT values. The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The PIC12F635/PIC16F636/639 has two independent, internal oscillators that can be configured or selected as the system clock source.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user adjusted ±12% via software using the OSCTUNE register (Register 3-1).
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at approximately 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select (IRCF) bits.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 “Clock Switching”**).

3.4.1 LFINTOSC AND LFINTOSCIO MODES

The LFINTOSC and LFINTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection (FOSC) bits in the Configuration Word register (Register 12-1).

In **LFINTOSC** mode, the OSC1 pin is available for general purpose I/O. The OSC2/CLKOUT pin outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **LFINTOSCIO** mode, the OSC1 and OSC2 pins are available for general purpose I/O.

3.4.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered approximately ±12% via software using the OSCTUNE register (Register 3-1).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF bits (see **Section 3.4.4 “Frequency Select Bits (IRCF)”**).

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz (IRCF ≠ 000) as the system clock source (SCS = 1), or when Two-Speed Start-up is enabled (IESO = 1 and IRCF ≠ 000).

The HF Internal Oscillator (HTS) bit (OSCCON<2>) indicates whether the HFINTOSC is stable or not.

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3.4.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The OSCTUNE register has a tuning range of approximately ±12%. The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number. Due to process variation, the monotonicity and frequency step cannot be specified.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. The HFINTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-1: OSCTUNE – OSCILLATOR TUNING REGISTER (ADDRESS: 90h)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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3.4.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated (approximate) 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). 31 kHz can be selected via software using the IRCF bits (see **Section 3.4.4 "Frequency Select Bits (IRCF)"**). The LFINTOSC is also the clock source for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF = `000`) as the system clock source (SCS = `1`), or when any of the following are enabled:

- Two-Speed Start-up (IESO = `1` and IRCF = `000`)
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit (OSCCON<1>) indicates whether the LFINTOSC is stable or not.

3.4.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency Select bits, IRCF<2:0> (OSCCON<6:4>), select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz

Note:	Following any Reset, the IRCF bits are set to '`110`' and the frequency selection is set to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.4.5 HFINTOSC AND LFINTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power. If this is the case, there is a 10 µs delay after the IRCF bits are modified before the frequency selection takes place. The LTS/HTS bits will reflect the current active status of the LFINTOSC and the HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. IRCF bits are modified.
2. If the new clock is shut down, a 10 µs clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. HTS/LTS bits are updated as required.
6. Clock switch is complete.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and the new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Note:	Care must be taken to ensure a valid voltage or frequency selection is chosen. See voltage vs. frequency diagrams (Figure 15-2, Figure 15-3 and Figure 15-4) for more detail.

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3.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

3.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit (OSCCON<0>) selects the system clock source that is used for the CPU and peripherals.

When SCS = `0`, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (Register 12-1).

When SCS = `1`, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

3.5.2 OSCILLATOR START-UP TIME-OUT STATUS BIT

The Oscillator Start-up Time-out Status (OSTS) bit (OSCCON<3>) indicates whether the system clock is running from the external clock source, as defined by the FOSC bits, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.6 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note:	Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit (OSCCON<3>) to remain clear.

When the PIC12F635/PIC16F636/639 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.3.1 "Oscillator Start-up Timer (OST)"**). The OST timer will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit (OSCCON<3>) is set, program execution switches to the external oscillator.

3.6.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO = `1` (CONFIG<10>) Internal/External Switchover bit.
- SCS = `0`.
- FOSC configured for LP, XT or HS mode.
- Two-Speed Start-up mode is entered after:
- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.6.2 TWO-SPEED START-UP SEQUENCE

The Two-Speed Start-up sequence is listed below.

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF bits (OSCCON<6:4>).
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

3.6.3 CHECKING EXTERNAL/INTERNAL CLOCK STATUS

Checking the state of the OSTS bit (OSCCON<3>) will confirm if the PIC12F635/PIC16F636/639 is running from the external clock source, as defined by the FOSC bits in the Configuration Word register (Register 12-1) or the internal oscillator.

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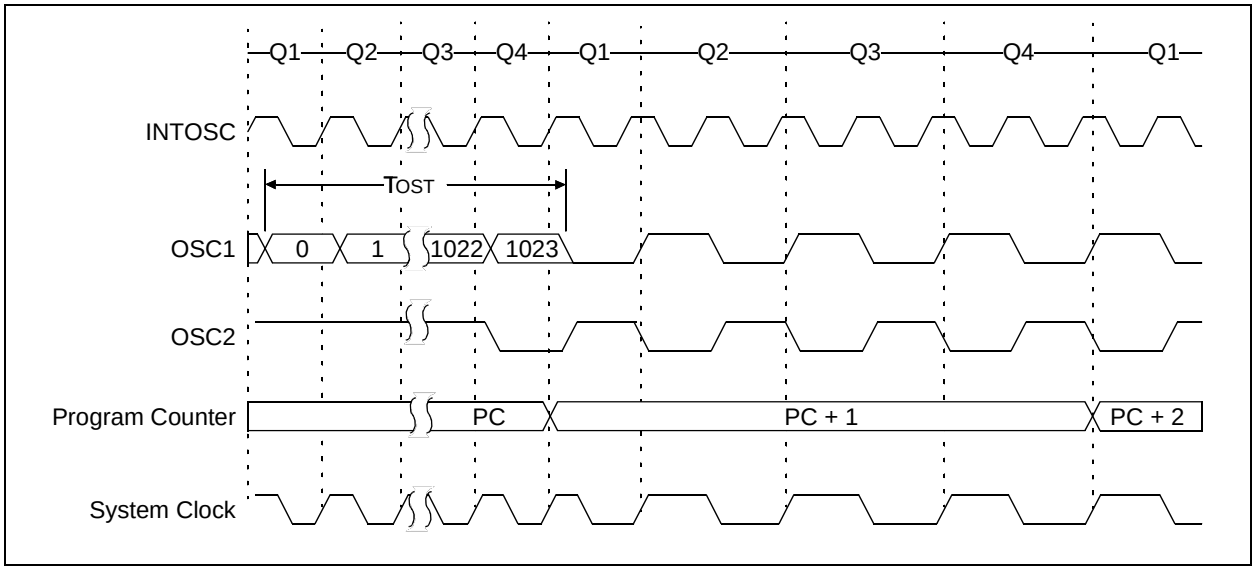
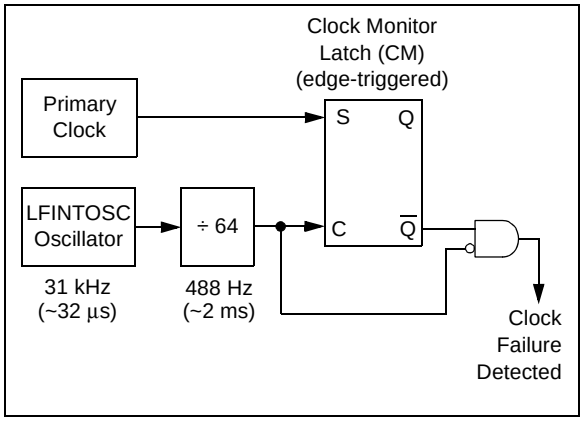
FIGURE 3-7: TWO-SPEED START-UP



3.7 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of an oscillator failure. The FSCM can detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired.

FIGURE 3-8: FSCM BLOCK DIAGRAM



The FSCM function is enabled by setting the FCMEN bit in the Configuration Word register (Register 12-1). It is applicable to all external clock options (LP, XT, HS, EC, RC or I/O modes).

In the event of an external clock failure, the FSCM will set the OSFIF bit (PIR1<2>) and generate an oscillator fail interrupt if the OSFIE bit (PIE1<2>) is set. The device will then switch the system clock to the internal oscillator. The system clock will continue to come from the internal oscillator unless the external clock recovers and the Fail-Safe condition is exited.

The frequency of the internal oscillator will depend upon the value contained in the IRCF bits (OSCCON<6:4>). Upon entering the Fail-Safe condition, the OSTS bit (OSCCON<3>) is automatically cleared to reflect that the internal oscillator is active and the WDT is cleared. The SCS bit (OSCCON<0>) is not updated. Enabling FSCM does not affect the LTS bit.

The FSCM sample clock is generated by dividing the LFINTOSC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur. Figure 3-8 shows the FSCM block diagram.

On the rising edge of the sample clock, the monitoring latch (CM = `0`) will be cleared. On a falling edge of the primary system clock, the monitoring latch will be set (CM = `1`). In the event that a falling edge of the sample clock occurs and the monitoring latch is not set, a clock failure has been detected. The assigned internal oscillator is enabled when FSCM is enabled, as reflected by the IRCF.

Note 1:	Two-Speed Start-up is automatically enabled when the Fail-Safe Clock Monitor mode is enabled.
2:	Primary clocks with a frequency of ≤ ~488 Hz will be considered failed by FSCM. A slow starting oscillator can cause an FCSM interrupt.

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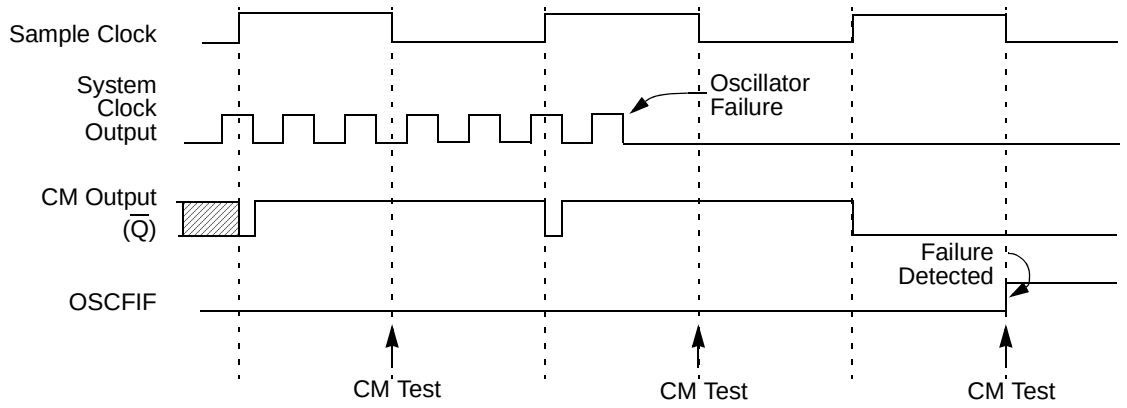
3.7.1 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, the execution of a `SLEEP` instruction, or a modification of the SCS bit. While in Fail-Safe condition, the PIC12F635/PIC16F636/639 uses the internal oscillator as the system clock source. The IRCF bits (OSCCON<6:4>) can be modified to adjust the internal oscillator frequency without exiting the Fail-Safe condition.

The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

FIGURE 3-9: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

3.7.2 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired. If the external clock is EC or RC mode, monitoring will begin immediately following these events.

For LP, XT or HS mode, the external oscillator may require a start-up time considerably longer than the FSCM sample clock time or a false clock failure may be detected (see Figure 3-9). To prevent this, the internal oscillator is automatically configured as the system clock and functions until the external clock is stable (the OST has timed out). This is identical to Two-Speed Start-up mode. Once the external oscillator is stable, the LFINTOSC returns to its role as the FSCM source.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit (OSCCON<3>) to verify the oscillator start-up and system clock switchover has successfully completed.

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REGISTER 3-2: OSCCON – OSCILLATOR CONTROL REGISTER (ADDRESS: 8Fh)

U-0	R/W-1	R/W-1	R/W-0	R-1	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS(1)	HTS	LTS	SCS
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Nominal Internal Oscillator Frequency Select bits
000 = 31 kHz
001 = 125 kHz
010 = 250 kHz
011 = 500 kHz
100 = 1 MHz
101 = 2 MHz
110 = 4 MHz
111 = 8 MHz

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit(1)
1 = Device is running from the external system clock defined by FOSC<2:0>
0 = Device is running from the internal system clock (HFINTOSC or LFINTOSC)

bit 2 **HTS:** HFINTOSC (High Frequency – 8 MHz to 125 kHz) Status bit
1 = HFINTOSC is stable
0 = HFINTOSC is not stable

bit 1 **LTS:** LFINTOSC (Low Frequency – 31 kHz) Stable bit
1 = LFINTOSC is stable
0 = LFINTOSC is not stable

bit 0 **SCS:** System Clock Select bit
1 = Internal oscillator is used for system clock
0 = Clock source defined by FOSC<2:0>

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD, WUR	Value on all other Resets
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
2007h(1)	CONFIG	CPD	CP	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by oscillators.
Note 1: See Register 12-1 for operation of all Configuration Word register bits.

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4.0 I/O PORTS

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-4). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-3) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING PORTA

```
BCF     STATUS,RP0     ;Bank 0
BCF     STATUS,RP1     ;
CLRF    PORTA          ;Init PORTA
MOVLW   07h            ;Set RA<2:0> to
MOVWF   CMCON0         ;digital I/O
BSF     STATUS,RP0     ;Bank 1
BCF     STATUS,RP1     ;
MOVLW   0Ch            ;Set RA<3:2> as inputs
MOVWF   TRISA          ;and set RA<5:4,1:0>
                       ;as outputs
BCF     STATUS,RP0     ;Bank 0
BCF     STATUS,RP1     ;
```

4.2 Additional Pin Functions

Every PORTA pin on the PIC12F635/PIC16F636/639 has an interrupt-on-change option and a weak pull-up/pull-down option. RA0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UP/PULL-DOWN

Each of the PORTA pins, except RA3, has an internal weak pull-up and pull-down. The WDA bits select either a pull-up or pull-down for an individual port bit. Individual control bits can turn on the pull-up or pull-down. These pull-ups/pull-downs are automatically turned off when the port pin is configured as an output, as an alternate function or on a Power-on Reset, setting the $\overline{\text{RAPU}}$ bit (OPTION_REG<7>). A weak pull-up on RA3 is enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word register and disabled when high voltage is detected, to reduce current consumption through RA3, while in Programming mode.

Note:	PORTA = GPIO TRISA = TRISIO

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REGISTER 4-1: WDA – WEAK PULL-UP/PULL-DOWN REGISTER (ADDRESS: 97h)

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **WDA<5:4>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

bit 3 **Unimplemented**: Read as '0'

bit 2-0 **WDA<2:0>**: Pull-up/Pull-down Selection bits
1 = Pull-up selected
0 = Pull-down selected

Note 1: The weak pull-up/pull-down device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WDA bit is enabled (WDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-2: WPUDA – WEAK PULL-UP/PULL-DOWN DIRECTION REGISTER (ADDRESS: 95h)

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUDA5(3)	WPUDA4(3)	—	WPUDA2	WPUDA1	WPUDA0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **WPUDA<5:4>**: Pull-up/Pull-down Direction Selection bits(3)
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

bit 3 **Unimplemented**: Read as '0'

bit 2-0 **WPUDA<2:0>**: Pull-up/Pull-down Direction Selection bits
1 = Pull-up/pull-down enabled
0 = Pull-up/pull-down disabled

Note 1: The weak pull-up/pull-down direction device is enabled only when the global $\overline{\text{RAPU}}$ bit is enabled, the pin is in Input mode (TRIS = 1), the individual WPUDA bit is enabled (WPUDA = 1) and the pin is not configured as an analog input or clock function.

2: RA3 pull-up is enabled when the pin is configured as $\overline{\text{MCLR}}$ in the Configuration Word register and the device is not in Programming mode.

3: WPUDA5 bit can be written if INTOSC is enabled and T1OSC is disabled; otherwise, the bit can not be written and reads as '1'. WPUDA4 bit can be written if not configured as OSC2; otherwise, the bit can not be written and reads as '1'.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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REGISTER 4-3: PORTA – PORTA REGISTER (ADDRESS: 05h)

U-0	U-0	R/W-x	R/W-x	R-x	R/W-x	R/W-0	R/W-0
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5-0: **RA<5:0>**: PORTA I/O pins

1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-4: TRISA – PORTA TRI-STATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5(2)	TRISA4(2)	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-0: **TRISA<5:0>:** PORTA Tri-State Control bits(1,2)

1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.

2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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4.2.2 INTERRUPT-ON-CHANGE

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits, IOCAx, enable or disable the interrupt function for each pin. Refer to Register 4-5. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (RAIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTA. This will end the mismatch condition, then
b) Clear the flag bit RAIF.

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared. The latch holding the last read value is not affected by a $\overline{\text{MCLR}}$ nor BOD Reset. After these Resets, the RAIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

REGISTER 4-5: IOCA – INTERRUPT-ON-CHANGE PORTA REGISTER (ADDRESS: 96h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5(2)	IOCA4(2)	IOCA3(3)	IOCA2	IOCA1	IOCA0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCA<5:0>:** Interrupt-on-change PORTA Control bits(2,3)
1 = Interrupt-on-change enabled(1)
0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOCA<5:4> always reads '0' in XT, HS and LP Oscillator modes.

3: IOCA<3> is ignored when WUR is enabled and the device is in Sleep mode.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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4.2.3 ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on RA0 allows a slow falling voltage to generate an interrupt-on-change on RA0 without excess current consumption. The mode is selected by setting the ULPWUE bit (PCON<5>). This enables a small current sink which can be used to discharge a capacitor on RA0.

To use this feature, the RA0 pin is configured to output '1' to charge the capacitor, interrupt-on-change for RA0 is enabled and RA0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on RA0 drops below V_{IL}, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit (INTCON<7>), the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See **Section 4.2.2 "Interrupt-on-change"** and **Section 12.9.3 "PORTA Interrupt"** for more information.

This feature provides a low power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on RA0. See Example 4-2 for initializing the Ultra Low Power Wake-up module.

The series resistor provides overcurrent protection for the RA0 pin and can allow for software calibration of the time-out (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple Programmable Low-Voltage Detect or temperature sensor.

Note:	For more information, refer to the Application Note *AN879, "Using the Microchip Ultra Low-Power Wake-up Module"* (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
BCF     STATUS,RP0   ;Bank 0
BCF     STATUS,RP1   ;
BSF     PORTA,0      ;Set RA0 data latch
MOVLW   H'7'         ;Turn off
MOVWF   CMCON0       ; comparators
BSF     STATUS,RP0   ;Bank 1
BCF     STATUS,RP1   ;
BCF     TRISA,0      ;Output high to
CALL    CapDelay     ; charge capacitor
BSF     PCON,ULPWUE  ;Enable ULP Wake-up
BSF     IOCA,0       ;Select RA0 IOC
BSF     TRISA,0      ;RA0 to input
MOVLW   B'10001000'  ;Enable interrupt
MOVWF   INTCON       ; and clear flag
SLEEP                ;Wait for IOC
```


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4.2.4 PIN DESCRIPTIONS AND DIAGRAMS

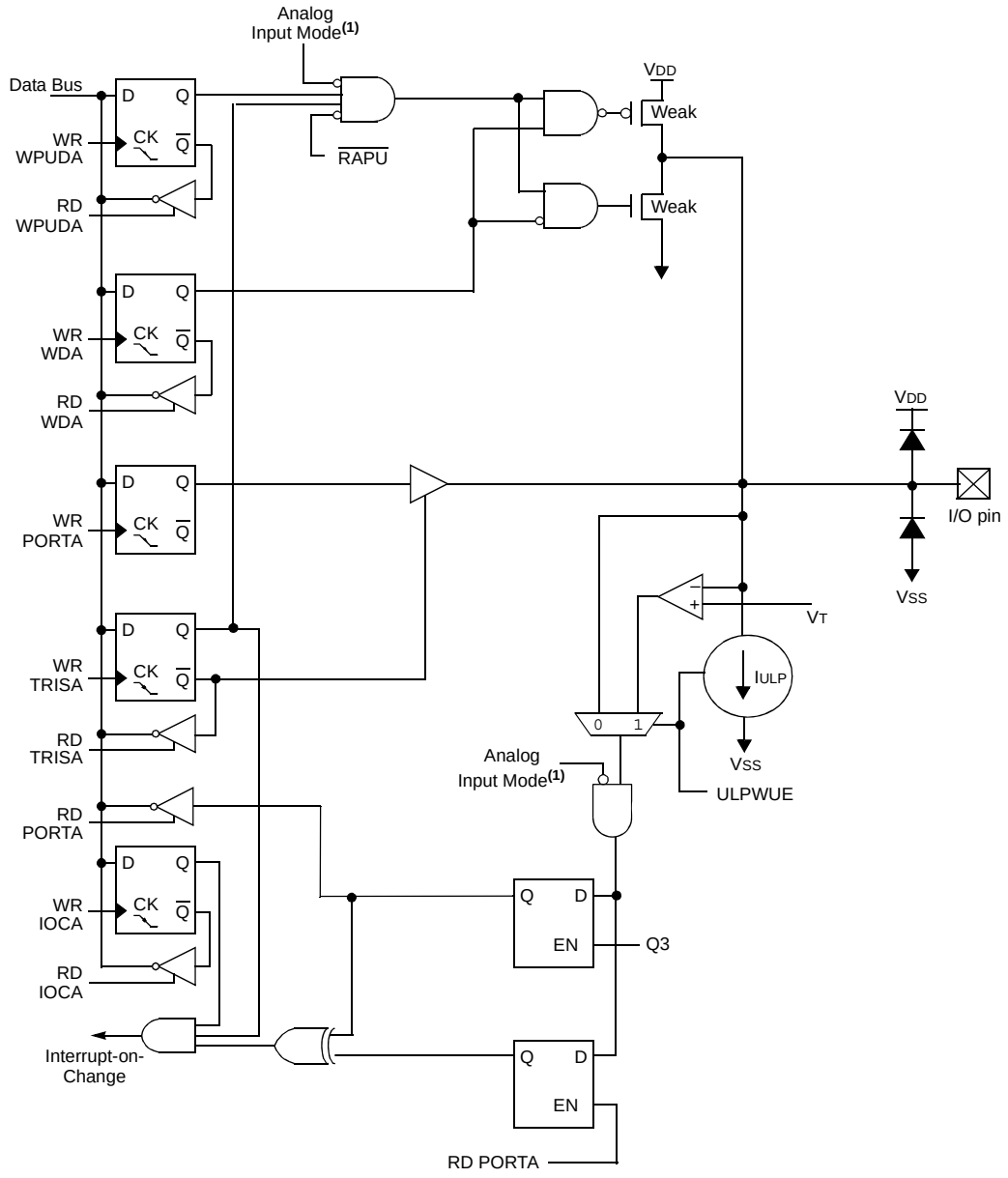
Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions, such as the comparator, refer to the appropriate section in this data sheet.

4.2.4.1 RA0/C1IN+/ICSPDAT/ULPWU

Figure 4-2 shows the diagram for this pin. The RA0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input to the comparator
- In-Circuit Serial Programming™ data
- an analog input for the Ultra Low-Power Wake-up

FIGURE 4-1: BLOCK DIAGRAM OF RA0



Note 1: Comparator mode determines Analog Input mode.

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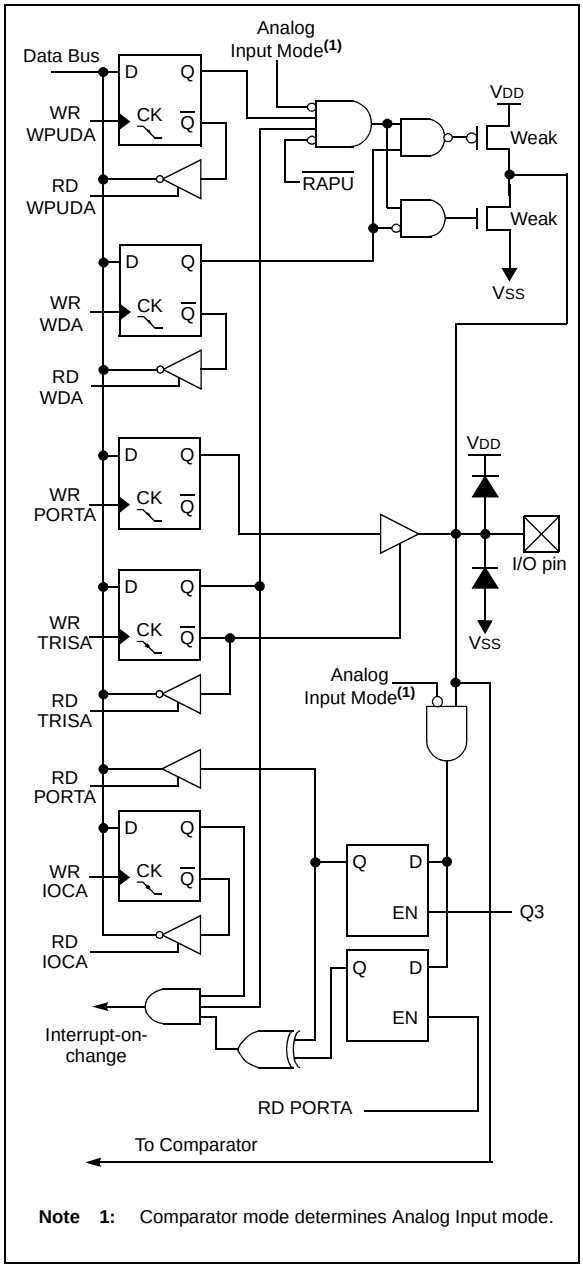
4.2.4.2 RA1/C1IN-/VREF/ICSPCLK

Figure 4-2 shows the diagram for this pin. The RA1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input to the comparator
- In-Circuit Serial Programming clock

FIGURE 4-2: BLOCK DIAGRAM OF RA1



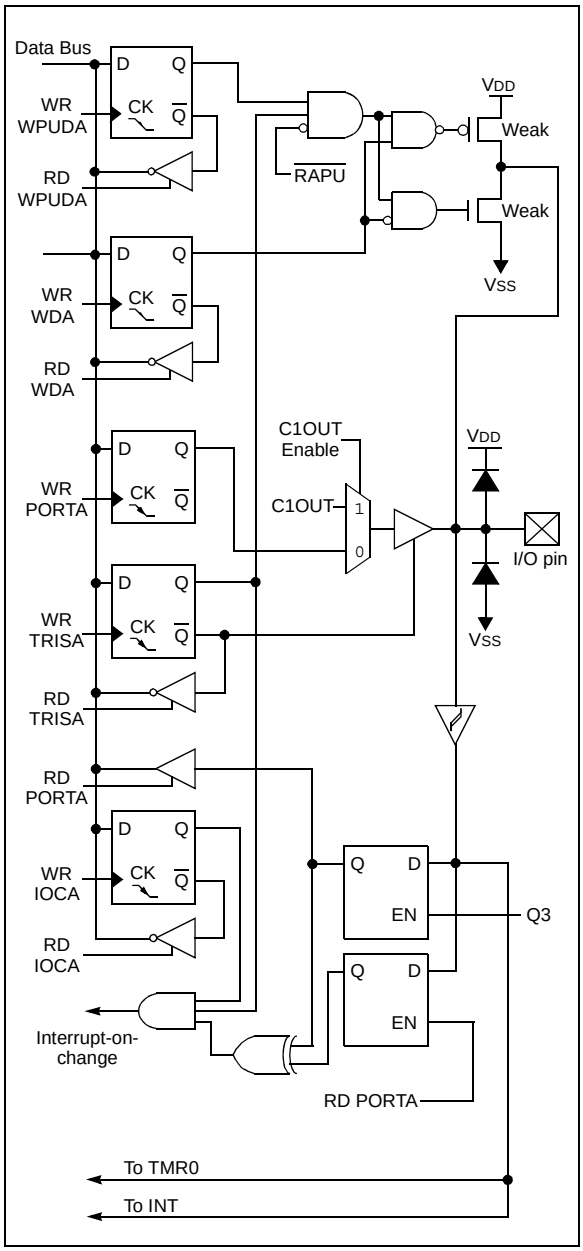
Note 1: Comparator mode determines Analog Input mode.

4.2.4.3 RA2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- the clock input for TMR0
- an external edge-triggered interrupt
- a digital output from the comparator

FIGURE 4-3: BLOCK DIAGRAM OF RA2



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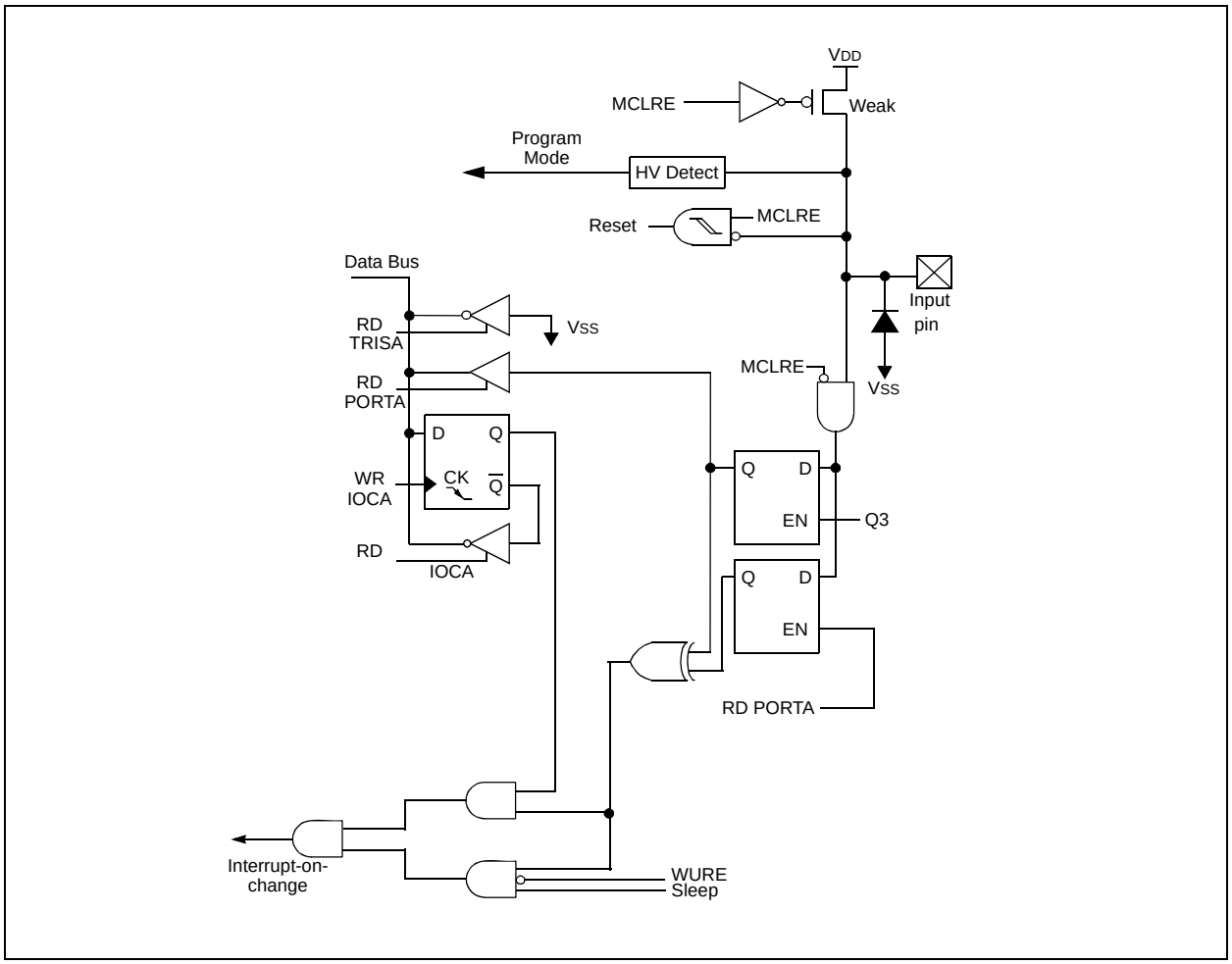
4.2.4.4 RA3/$\overline{\text{MCLR}}$/VPP

Figure 4-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up
- a high-voltage detect for Program mode entry

FIGURE 4-4: BLOCK DIAGRAM OF RA3



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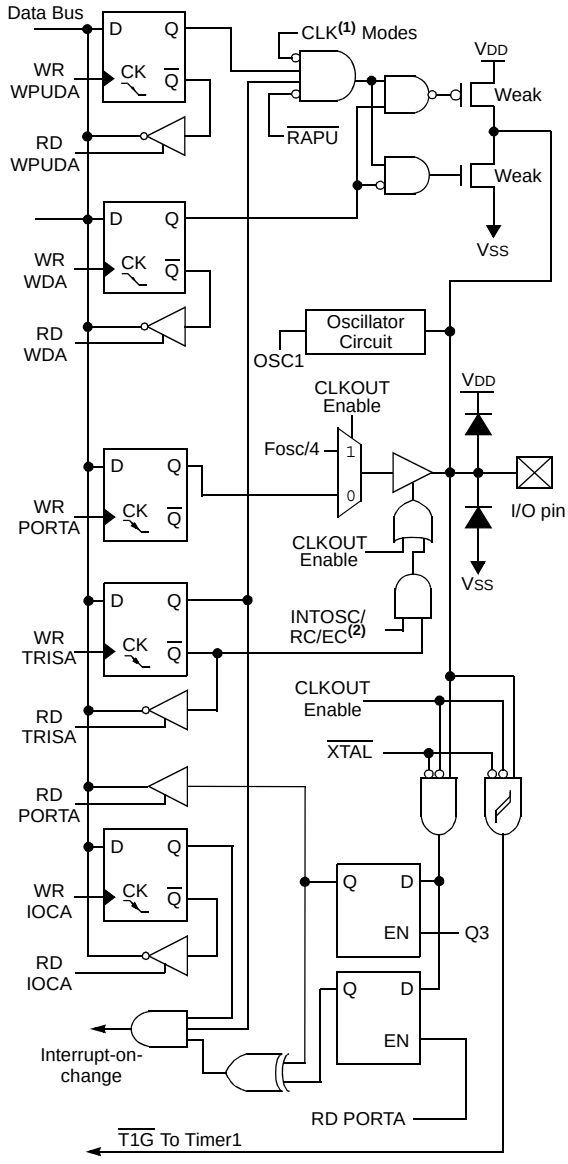
4.2.4.5 RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: Oscillator modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

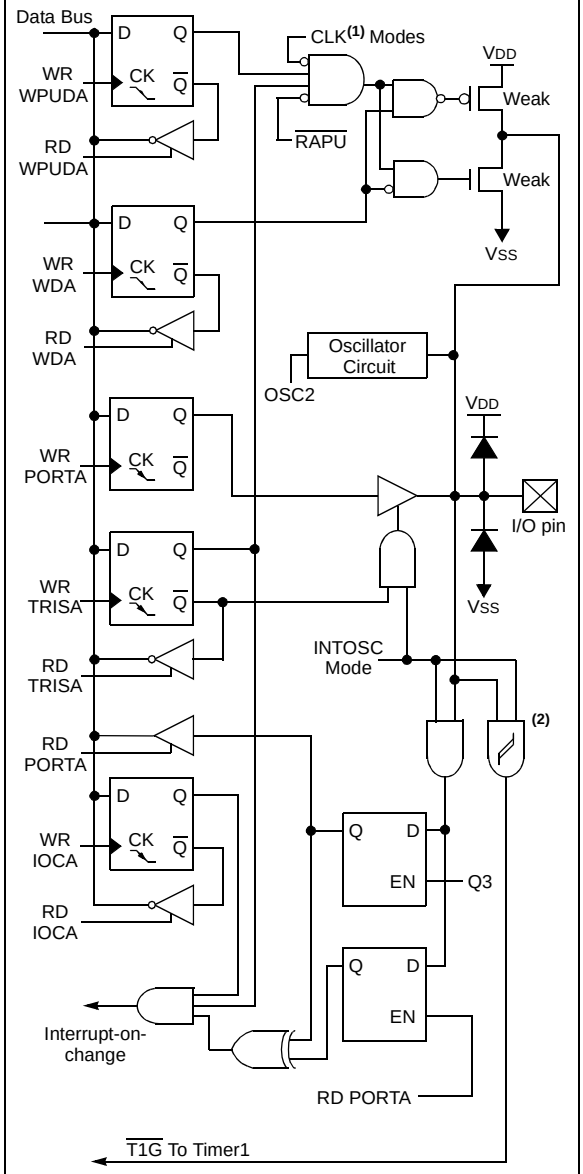
2: With CLKOUT option.

4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



Note 1: Oscillator modes are XT, HS, LP and LPTMR1.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

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TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD, WUR	Value on all other Resets
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xx00	--uu uu00
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
95h	WPUDA	—	—	WPUDA5	WPUDA4	—	WPUDA2	WPUDA1	WPUDA0	--11 -111	--11 -111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
97h	WDA	—	—	WDA5	WDA4	—	WDA2	WDA1	WDA0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

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4.3 PORTC

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to comparator. For specific information about individual functions, refer to the appropriate section in this data sheet.

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-3: INITIALIZING PORTC

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRF    PORTC           ;Init PORTC
MOVLW   07h             ;Set RC<4,1:0> to
MOVWF   CMCON0          ;digital I/O
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1
MOVLW   0Ch             ;Set RC<3:2> as inputs
MOVWF   TRISC           ;and set RC<5:4,1:0>
                        ;as outputs
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
```

4.3.1 RC0/C2IN+

The RC0 pin is configurable to function as one of the following:

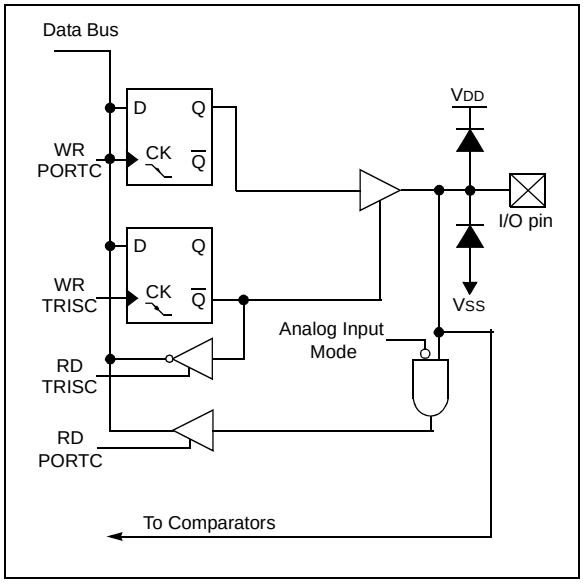
- a general purpose I/O
- an analog input to the comparator

4.3.2 RC1/C2IN-

The RC1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input to the comparator

FIGURE 4-7: BLOCK DIAGRAM OF RC0 AND RC1



4.3.3 RC2

The RC2 pin is configurable to function as a general purpose I/O.

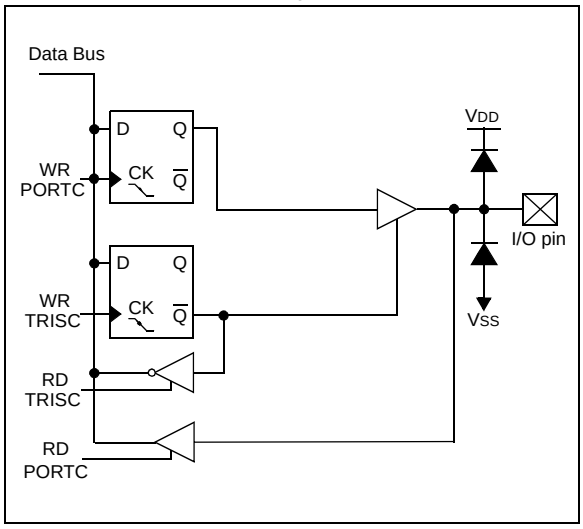
4.3.4 RC3

The RC3 pin is configurable to function as a general purpose I/O.

4.3.5 RC5

The RC5 pin is configurable to function as a general purpose I/O.

FIGURE 4-8: BLOCK DIAGRAM OF RC2, RC3 AND RC5



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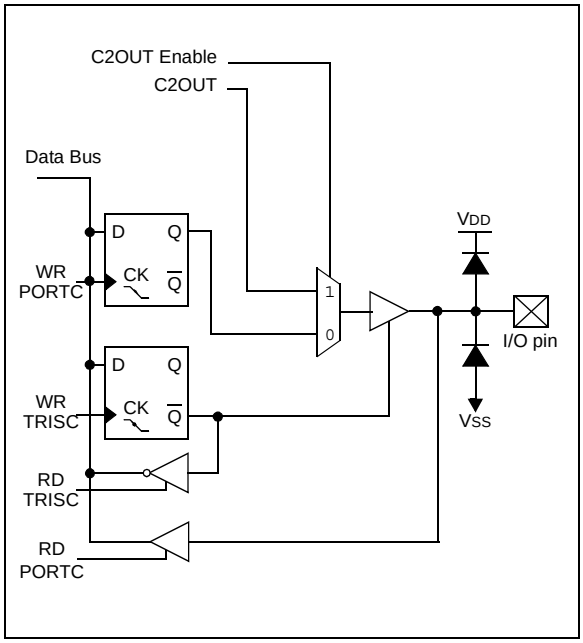
4.3.6 RC4/C2OUT

The RC4 pin is configurable to function as one of the following:

- a general purpose I/O
- a digital output from the comparator

FIGURE 4-9: BLOCK DIAGRAM OF RC4



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REGISTER 4-6: PORTC – PORTC REGISTER (ADDRESS: 07h)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0
—	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-0: **RC<5:0>:** PORTC General Purpose I/O Pin bits

1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-7: TRISC – PORTC TRI-STATE REGISTER (ADDRESS: 87h)

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5-0: **TRISC<5:0>:** PORTC Tri-State Control bit

1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD, WUR	Value on all other Resets
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xx00	--uu uu00
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

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5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 5-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note:	Additional information on the Timer0 module is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

5.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

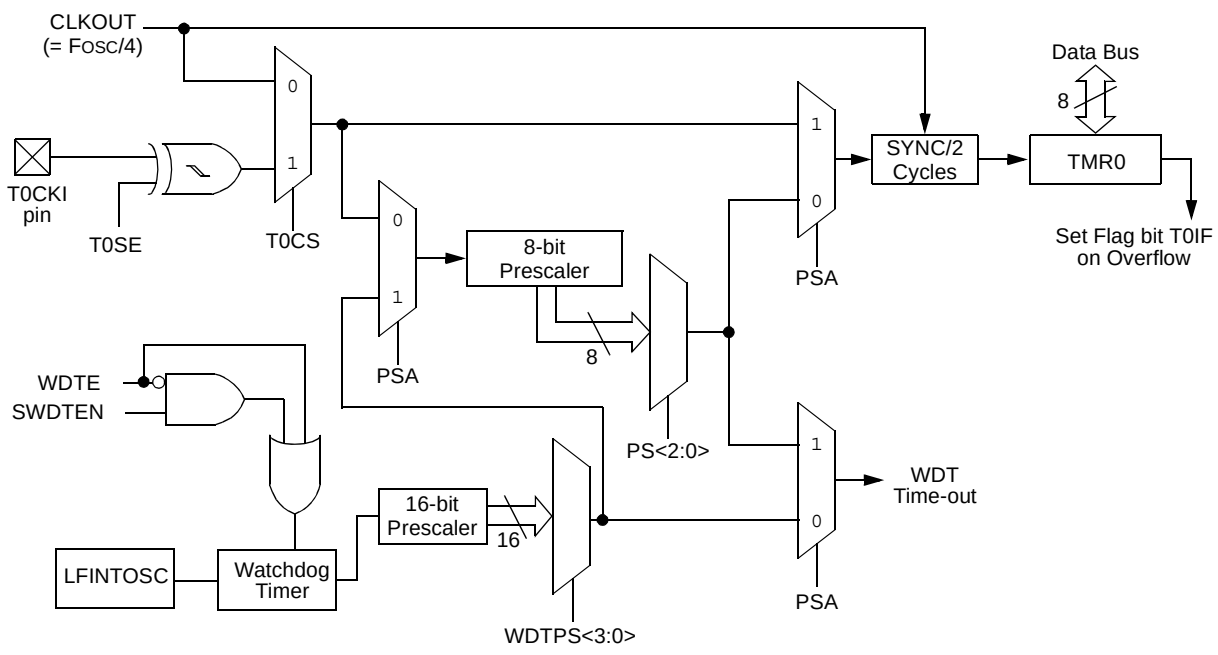
Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note:	Counter mode has specific external clock requirements. Additional information on these requirements is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

5.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit (INTCON<2>). The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep since the timer is shut off during Sleep.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the Option register, WDTPS<3:0> are bits in the WDTCON register.

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5.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 TOSC (and a small RC delay of 20 ns) and low for at least 2 TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

REGISTER 5-1: OPTION_REG – OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual values in the WPUDA register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/T0CKI/INT/C1OUT pin
0 = Interrupt on falling edge of RA2/T0CKI/INT/C1OUT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/T0CKI/INT/C1OUT pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI/INT/C1OUT pin
0 = Increment on low-to-high transition on RA2/T0CKI/INT/C1OUT pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate(1)
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available for the PIC12F635/PIC16F636/639. See **Section 12.11 "Watchdog Timer (WDT)"** for more information.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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5.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this data sheet. The prescaler assignment is controlled in software by the control bit, PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS<2:0> bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1`, `x....`etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

5.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 5-1 and Example 5-2) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 → WDT)

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRWDT                  ;Clear WDT
CLRF    TMR0            ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;
MOVLW   b’00101111’     ;Required if desired
MOVWF   OPTION_REG      ; PS2:PS0 is
CLRWDT                  ; 000 or 001
                        ;
MOVLW   b’00101xxx’     ;Set postscaler to
MOVWF   OPTION_REG      ; desired WDT rate
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 5-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;
MOVLW   b’xxxx0xxx’     ;Select TMR0,
                        ;prescale, and
                        ;clock source
MOVWF   OPTION_REG      ;
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
```

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

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6.0 TIMER1 MODULE WITH GATE CONTROL

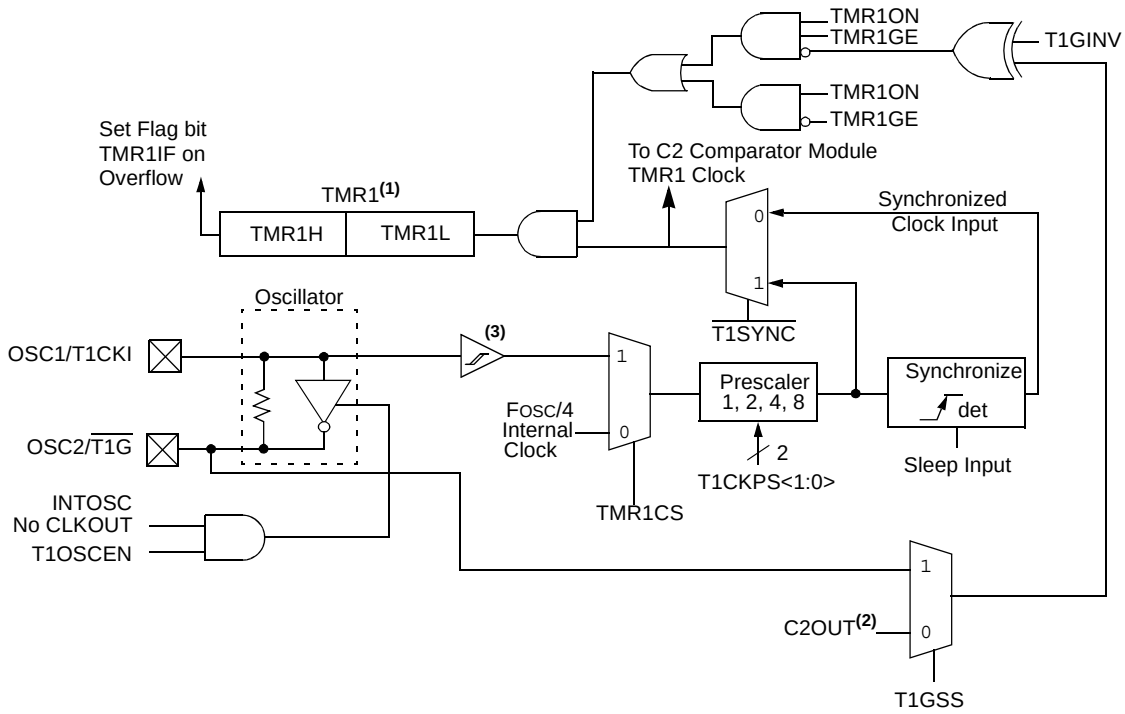
The PIC12F635/PIC16F636/639 has a 16-bit timer. Figure 6-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input:
  - Selectable gate source: $\overline{\text{T1G}}$ or C2 output (T1GSS)
  - Selectable gate polarity (T1GINV)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 6-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note:	Additional information on timer modules is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

FIGURE 6-1: TIMER1 ON THE PIC12F635/PIC16F636/639 BLOCK DIAGRAM



Note 1: Timer1 increments on the rising edge.

2: C2OUT for PIC16F636/639, C1OUT for PIC12F635.

3: ST Buffer is low-power type when using LP oscillator, or high-speed type when using T1CKI.

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6.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:

- 16-bit timer with prescaler
- 16-bit synchronous counter
- 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the Timer1 gate, which can be selected as either the $\overline{T1G}$ pin or the Comparator 2 output.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note:	In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

6.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit (PIE1<0>)
- PEIE bit (INTCON<6>)
- GIE bit (INTCON<7>).

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.3 Timer1 Prescaler

Timer1 has four prescaler options, allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

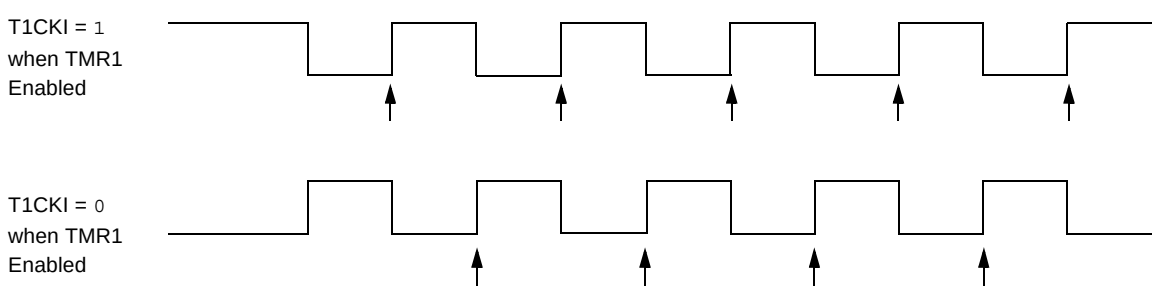
6.4 Timer1 Gate

Timer1 gate source is software configurable to be the $\overline{T1G}$ pin or the output of Comparator 2. This allows the device to directly time external events using $\overline{T1G}$ or analog events using Comparator 2. See CMCON1 (Register 7-2) for selecting the Timer1 gate source. This feature can simplify the software for many other applications.

Note:	TMR1GE bit (T1CON<6>) must be set to use either $\overline{T1G}$ or C2OUT as the Timer1 gate source. See Register 7-2 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the $\overline{T1GINV}$ bit (T1CON<7>), whether it originates from the $\overline{T1G}$ pin or Comparator 2 output. This configures Timer1 to measure either the active-high or active-low time between events.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

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REGISTER 6-1: T1CON – TIMER1 CONTROL REGISTER (ADDRESS: 10h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **T1GINV:** Timer1 Gate Invert bit[(1)]
1 = Timer1 gate is inverted
0 = Timer1 gate is not inverted

bit 6 **TMR1GE:** Timer1 Gate Enable bit[(2)]
If TMR1ON = 0:
This bit is ignored.
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is not active
0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either $\overline{\text{T1G}}$ pin or C2OUT, as selected by the T1GSS bit (CMCON1<1>), as a Timer1 gate source.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

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6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit, T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator rated up to 31 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal. Table 3-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 bits read as '0' and TRISA5 and TRISA4 bits read as '1'.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when set up in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets
0Bh/ 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
1Ah	CMCON 1	—	—	—	—	—	—	T1GSS	C2SYNC	---- --10	---- --10
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

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7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with I/O port pins RA0, RA1, RC0 and RC1, while the outputs are multiplexed to pins RA2 and RC4. An on-chip Comparator Voltage Reference (CVREF) can also be applied to the inputs of the comparators.

The CMCON0 register (Register 7-1) controls the comparator input and output multiplexers. A block diagram of the various comparator configurations is shown in Figure 7-4.

Note:	The PIC12F635 has only 1 comparator. The comparator on the PIC12F635 behaves like comparator 2 of the PIC16F636/639.

REGISTER 7-1: CMCON0 – COMPARATOR CONTROL 0 REGISTER (ADDRESS: 19h)

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT(1)	C1OUT(2)	C2INV(1)	C1INV(2)	CIS	CM2	CM1	CM0
bit 7							bit 0

bit 7 **C2OUT**: Comparator 2 Output bit(1)
When C2INV = 0:
1 = C2 VIN+ > C2 VIN-
0 = C2 VIN+ < C2 VIN-
When C2INV = 1:
1 = C2 VIN+ < C2 VIN-
0 = C2 VIN+ > C2 VIN-

bit 6 **C1OUT**: Comparator 1 Output bit(2)
When C1INV = 0:
1 = C1 VIN+ > C1 VIN-
0 = C1 VIN+ < C1 VIN-
When C1INV = 1:
1 = C1 VIN+ < C1 VIN-
0 = C1 VIN+ > C1 VIN-

bit 5 **C2INV**: Comparator 2 Output Inversion bit(1)
1 = C2 output inverted
0 = C2 output not inverted

bit 4 **C1INV**: Comparator 1 Output Inversion bit(2)
1 = C1 output inverted
0 = C1 output not inverted

bit 3 **CIS**: Comparator Input Switch bit
When CM<2:0> = 010:
1 = C1 VIN- connects to RA0
C2 VIN- connects to RC0
0 = C1 VIN- connects to RA1
C2 VIN- connects to RC1
When CM<2:0> = 001:
1 = C1 VIN- connects to RA0
0 = C1 VIN- connects to RA1

bit 2-0 **CM<2:0>:** Comparator Mode bits
Figure 7-4 shows the Comparator modes and CM<2:0> bit settings.

Note 1: PIC16F636/639 only. Reads as '0' for PIC12F635.
2: PIC12F635 bit names are COUT and CINV.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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7.1 Comparator Operation

A single comparator is shown in Figure 7-1 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-1 represent the uncertainty due to input offsets and response time.

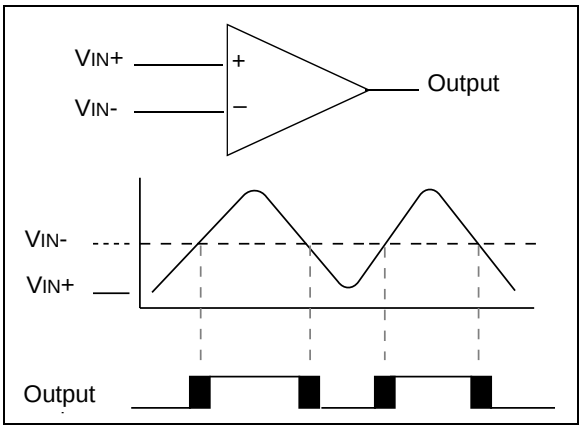
> **Note:** To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be programmed in the CMCON0 (19h) register.

The polarity of the comparator output can be inverted by setting the CxINV bits (CMCON0<5:4>). Clearing CxINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 7-1.

TABLE 7-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	CxOUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

FIGURE 7-1: SINGLE COMPARATOR

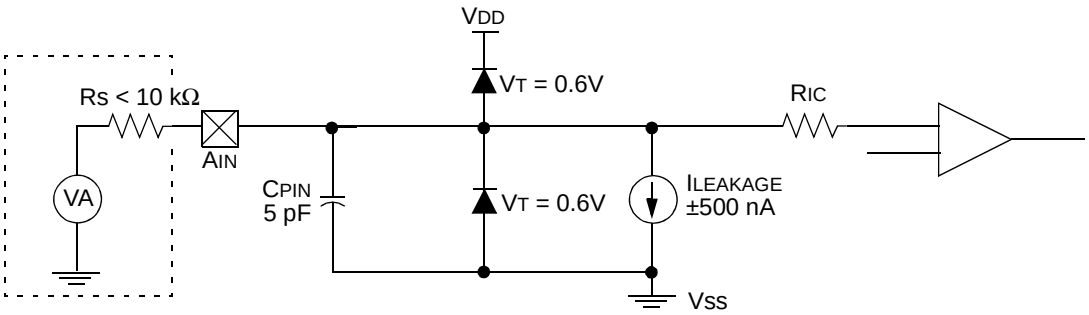


7.2 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-2. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

> **Note 1:** When reading the Port register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as analog inputs according to the input specification.
>
> **2:** Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 7-2: ANALOG INPUT MODEL



Legend:

CPIN	= Input Capacitance
VT	= Threshold Voltage
ILEAKAGE	= Leakage Current at the pin due to various junctions
RIC	= Interconnect Resistance
RS	= Source Impedance
VA	= Analog Voltage

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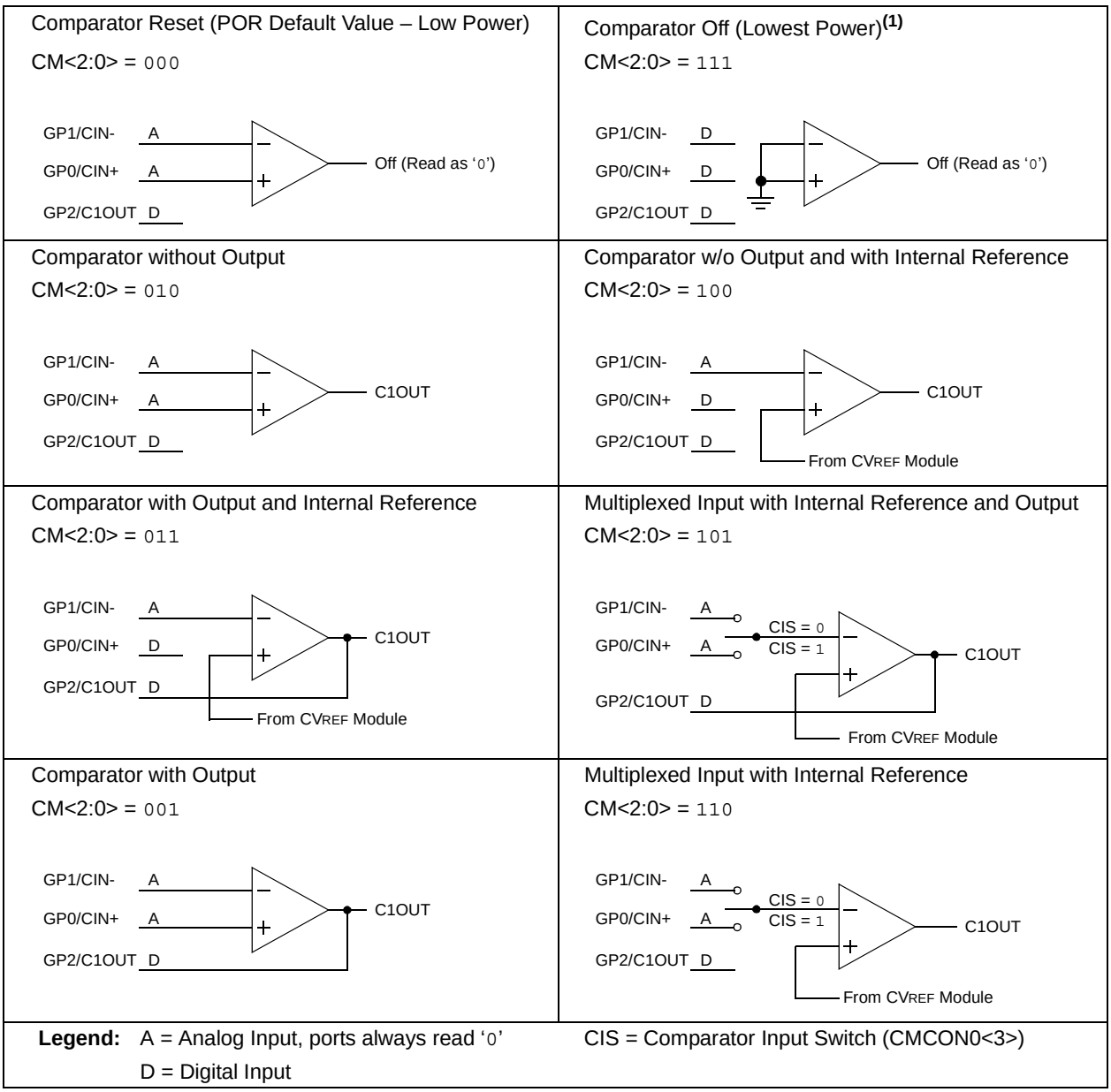
7.3 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON0 register is used to select these modes. Figure 7-3 and Figure 7-4 show the eight possible modes. The TRISA and TRISC registers control the data direction of the comparator output pins for each mode. If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in **Section 15.0 "Electrical Specifications"**.

Note:	Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

FIGURE 7-3: COMPARATOR I/O OPERATING MODES FOR PIC12F635



Note 1: Lowest power statement assures valid digital stats on GPO, GP1 and GP2.

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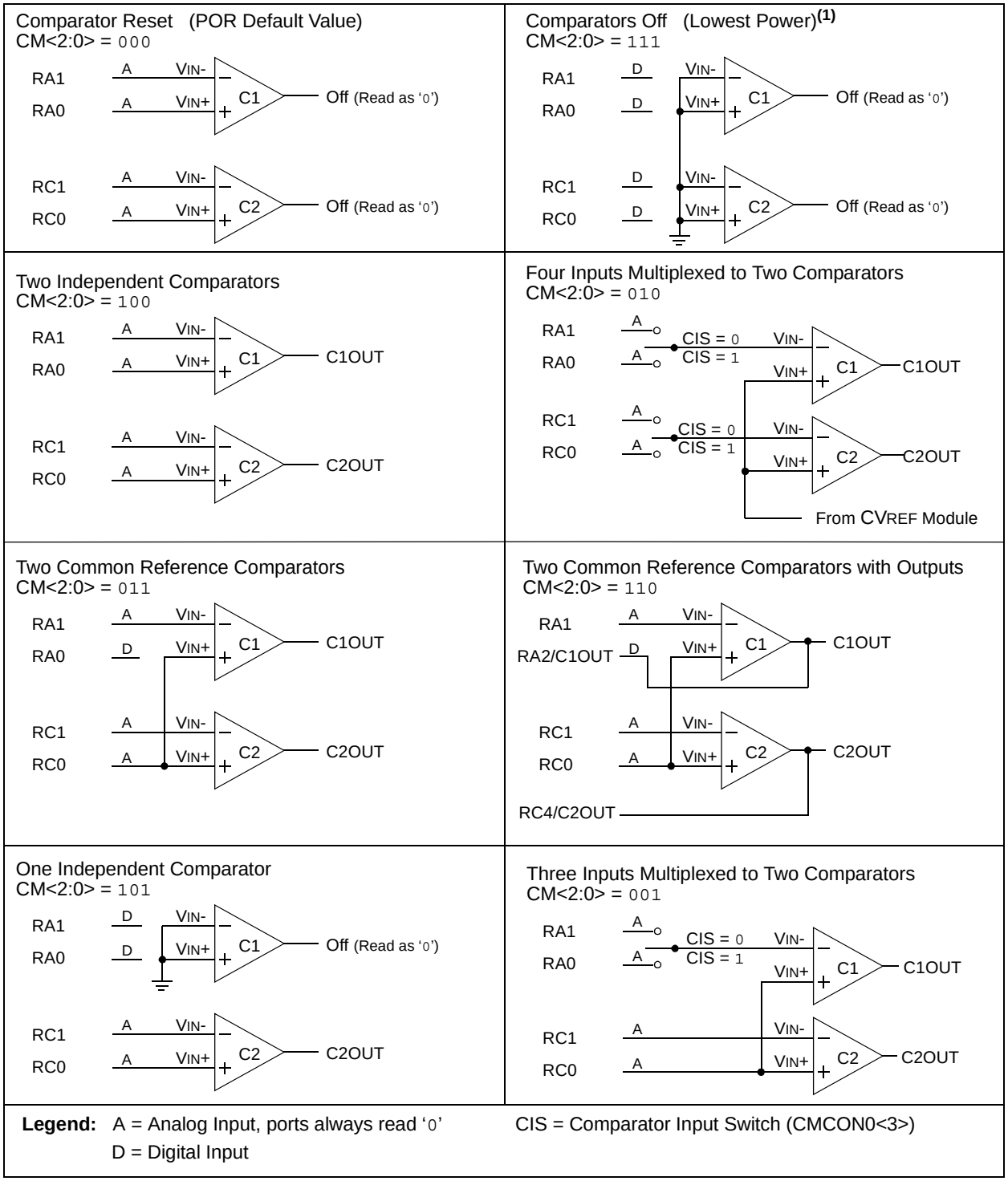
FIGURE 7-4: COMPARATOR I/O OPERATING MODES FOR PIC16F636/639



Legend: A = Analog Input, ports always read '0'
D = Digital Input
CIS = Comparator Input Switch (CMCON0<3>)

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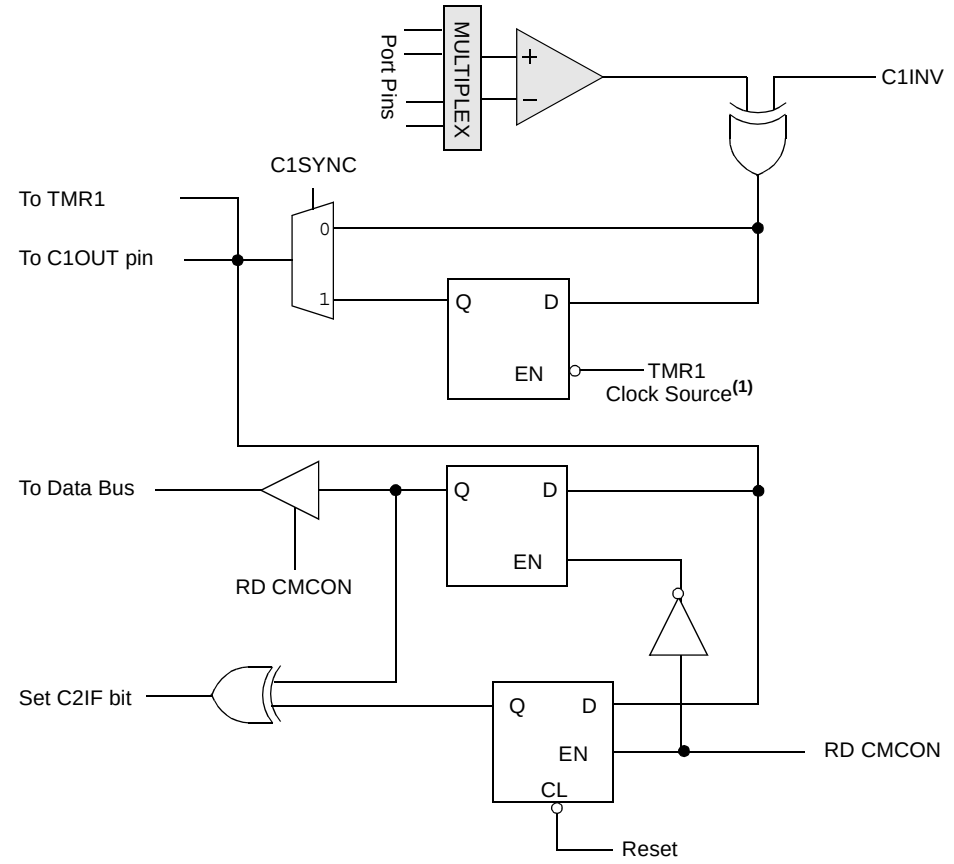
FIGURE 7-5: PIC12F635 COMPARATOR C1 OUTPUT BLOCK DIAGRAM



Note 1: Comparator 1 output is latched on falling edge of T1 clock source.

FIGURE 7-6: PIC16F636/639 COMPARATOR C1 OUTPUT BLOCK DIAGRAM

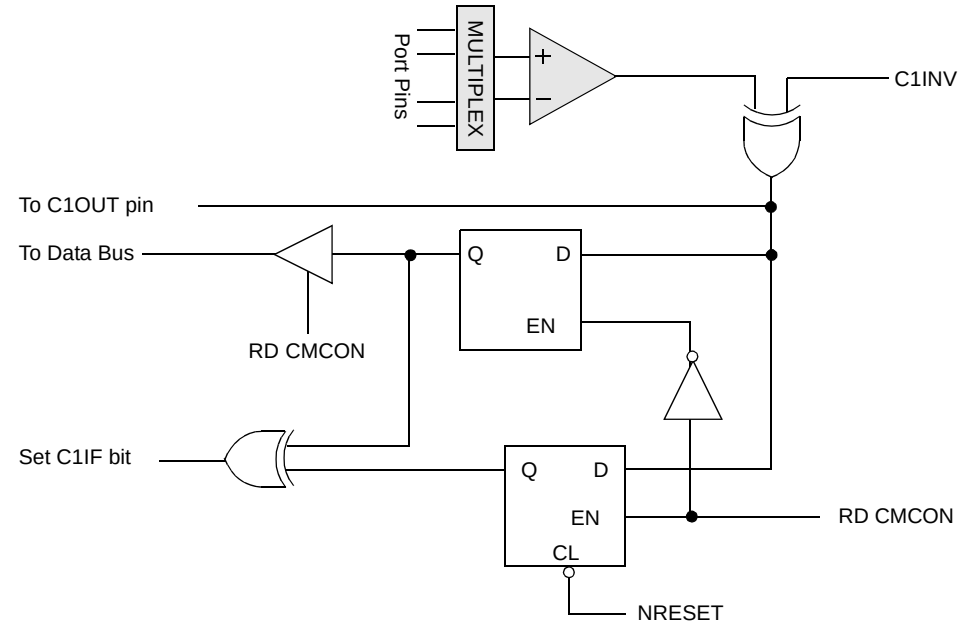


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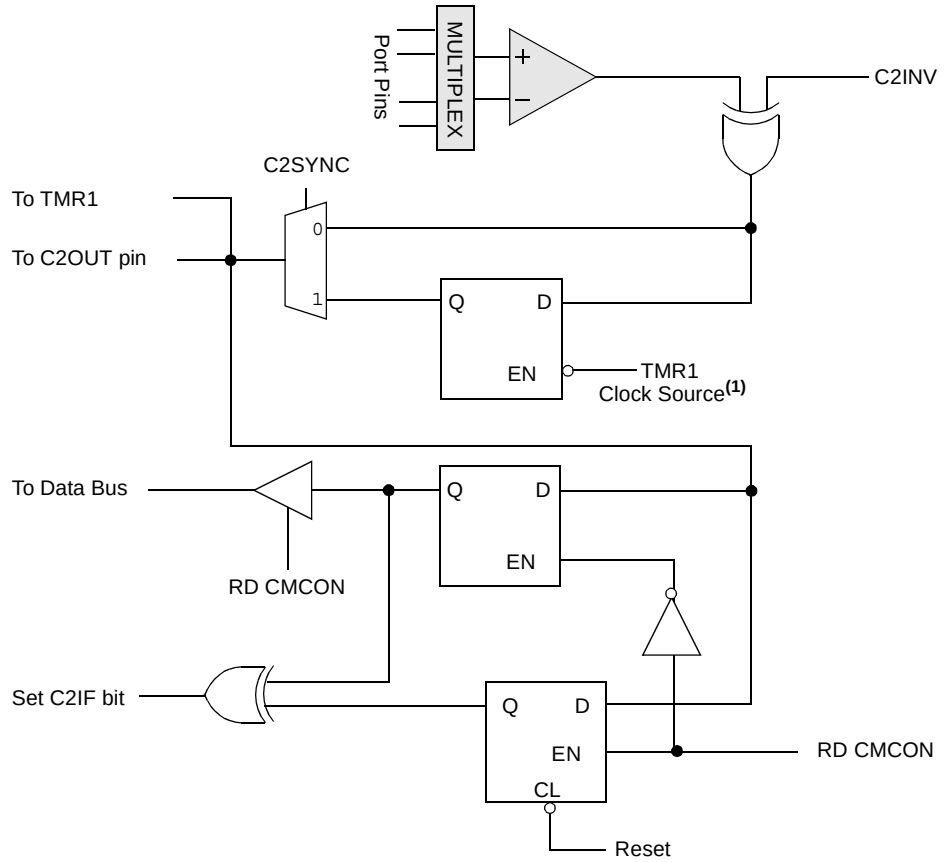
FIGURE 7-7: PIC16F636/639 COMPARATOR C2 OUTPUT BLOCK DIAGRAM



Note 1: Comparator 2 output is latched on falling edge of T1 clock source.

REGISTER 7-2: CMCON1 – COMPARATOR CONTROL 1 REGISTER (ADDRESS: 1Ah)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	C2SYNC(1)
bit 7							bit 0

bit 7-2: **Unimplemented**: Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit
1 = Timer1 gate source is $\overline{\text{T1G}}$ pin (RA4 must be configured as digital input)
0 = Timer1 gate source is Comparator 2 output

bit 0 **C2SYNC:** Comparator 2 Synchronize bit(2)
1 = C2 output synchronized with falling edge of Timer1 clock
0 = C2 output not synchronized with Timer1 clock

Note 1: C2SYNC is C1SYNC in PIC12F635.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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7.4 Comparator Outputs

The comparator outputs are read through the CMCON0 register. These bits are read-only. The comparator outputs may also be directly output to the RA2 and RC4 I/O pins. When enabled, multiplexers in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-5 and Figure 7-6 show the output block diagrams for Comparator 1 and 2.

The TRIS bits will still function as an output enable/disable for the RA2 and RC4 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1INV and C2INV bits (CMCON0<5:4>).

Timer1 gate source can be configured to use the $\overline{\text{T1G}}$ pin or Comparator 2 output as selected by the T1GSS bit (CMCON1<1>). This feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit (CMCON1<0>). When enabled, the output of Comparator 2 is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See Figure 7-6, Comparator C2 Output Block Diagram and Figure 5-1, Timer1 on the PIC12F635/PIC16F636/639 Block Diagram for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

7.5 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CMCON0<7:6>, to determine the actual change that has occurred. The CxIF bits (PIR1<4:3>) are the Comparator Interrupt Flags. These bits must be reset in software by clearing them to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits (PIE1<4:3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition.

b) Clear flag bits CxIF.

A mismatch condition will continue to set flag bits CxIF. Reading CMCON0 will end the mismatch condition and allow flag bits CxIF to be cleared.

Note:	If a change in the CMCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF (PIR1<4:3>) interrupt flags may not get set.

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7.6 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The VRCON register (Register 7-3) controls the voltage reference module shown in Figure 7-8.

7.6.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equation determines the output voltages:

EQUATION 7-1:

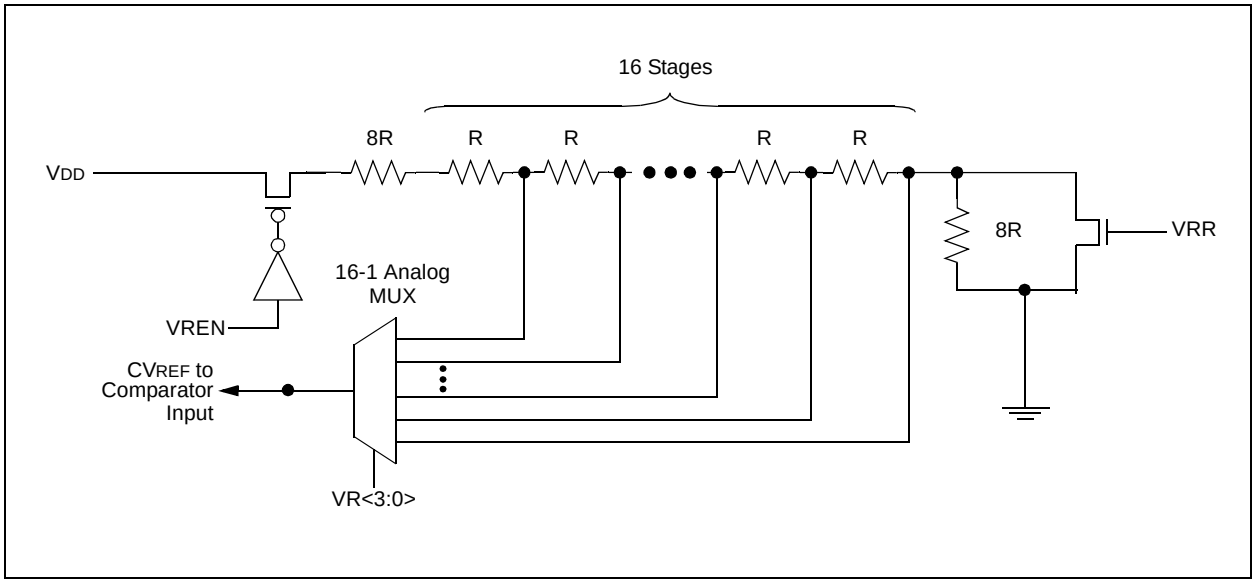
VRR = 1 (low range): CVREF = (VR<3:0>/24) x VDD

VRR = 0 (high range):
CVREF = (VDD/4) + (VR<3:0> x VDD/32)

7.6.2 VOLTAGE REFERENCE ACCURACY/ERROR

The voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 15.0 "Electrical Specifications"**.

FIGURE 7-8: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



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7.7 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 15-7).

7.8 Operation During Sleep

The comparators and voltage reference, if enabled before entering Sleep mode, remain active during Sleep. This results in higher Sleep currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in Sleep mode, turn off the comparator, CM<2:0> = `111` and voltage reference, VRCON<7> = `0`.

While the comparator is enabled during Sleep, an interrupt will wake-up the device. If the GIE bit (INTCON<7>) is set, the device will jump to the interrupt vector (0004h) and if clear, continues execution with the next instruction. If the device wakes up from Sleep, the contents of the CMCON0, CMCON1 and VRCON registers are not affected.

7.9 Effects of a Reset

A device Reset forces the CMCON0, CMCON1 and VRCON registers to their Reset states. This forces the comparator module to be in the Comparator Reset mode, CM<2:0> = `000` and the voltage reference to its OFF state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.

REGISTER 7-3: VRCON – VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 99h)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

bit 7 **VREN:** CV_{REF} Enable bit
`1` = CV_{REF} circuit powered on
`0` = CV_{REF} circuit powered down, no I_{DD} drain and $CV_{REF} = V_{SS}$

bit 6 **Unimplemented:** Read as '`0`'

bit 5 **VRR:** CV_{REF} Range Selection bit
`1` = Low range
`0` = High range

bit 4 **Unimplemented:** Read as '`0`'

bit 3-0 **VR<3:0>:** CV_{REF} Value Selection bits $0 \leq VR<3:0> \leq 15$

When VRR = `1`:
$CV_{REF} = (VR<3:0>/24) * V_{DD}$

When VRR = `0`:
$CV_{REF} = V_{DD}/4 + (VR<3:0>/32) * V_{DD}$

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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NOTES:

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8.0 PROGRAMMABLE LOW-VOLTAGE DETECT (PLVD) MODULE

The Programmable Low-Voltage Detect module is an interrupt driven supply level detection. The voltage detection monitors the internal power supply.

8.1 Voltage Trip Points

The PIC12F635/PIC16F636/639 device supports eight internal PLVD trip points. See Register 8-1 for available PLVD trip point voltages.

REGISTER 8-1: LVDCON – LOW-VOLTAGE DETECT CONTROL REGISTER (ADDRESS: 94h)

U-0	U-0	R-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Status Flag bit
1 = Indicates that the PLVD is stable and PLVD interrupt is reliable
0 = Indicates that the PLVD is not stable and PLVD interrupt should not be enabled

bit 4 **LVDEN:** Low-Voltage Detect Power Enable bit
1 = Enables PLVD, powers up PLVD circuit and supporting reference circuitry
0 = Disables PLVD, powers down PLVD and supporting circuitry

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LVDL<2:0>:** Low-Voltage Detection Limit bits (nominal values)
111 = 4.5V
110 = 4.2V
101 = 4.0V
100 = 2.3V (default)
011 = 2.2V
010 = 2.1V
001 = 2.0V
000 = 1.9V(1)

Note 1: Not tested and below minimum V_{DD}.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 8-1: REGISTERS ASSOCIATED WITH PROGRAMMABLE LOW-VOLTAGE DETECT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets
94h	LVDCON	—	—	IRVST	LVDEN	—	LVDL2	LVDL1	LVDL0	--00 -000	--00 -000
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used by the comparator or comparator voltage reference module.

Note 1: PIC16F636/639 only.

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NOTES:

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9.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. PIC16F636/639 has 256 bytes of data EEPROM and the PIC12F635 has 64 bytes.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip-to-chip. Please refer to A/C specifications in **Section 15.0 "Electrical Specifications"** for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

Additional information on the data EEPROM is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

REGISTER 9-1: EEDAT – EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

bit 7-0 **EEDATn**: Byte Value to Write to or Read From Data EEPROM bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 9-2: EEADR – EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEADR7(1)	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
bit 7							bit 0

bit 7-0 **EEADR**: Specifies 1 of 256 Locations for EEPROM Read/Write Operation bits

Note 1: PIC16F636/639 only. Read as '0' on PIC12F635.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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9.1 EECON1 AND EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit (PIR1<7>), is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 9-3: EECON1 – EEPROM CONTROL 1 REGISTER (ADDRESS: 9Ch)

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
- 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOD detect)
- 0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
- 1 = Allows write cycles
- 0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
- 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
- 0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
- 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
- 0 = Does not initiate an EEPROM read

Legend:			
S = Bit can only be set			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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9.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>), as shown in Example 9-1. The data is available, in the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 9-1: DATA EEPROM READ

```
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;
MOVLW   CONFIG_ADDR     ;
MOVWF   EEADR           ;Address to read
BSF     EECON1,RD       ;EE Read
MOVF    EEDAT,W         ;Move data to W
```

9.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 9-2.

EXAMPLE 9-2: DATA EEPROM WRITE

```
        BSF     STATUS,RP0      ;Bank 1
        BCF     STATUS,RP1      ;
        BSF     EECON1,WREN     ;Enable write
        BCF     INTCON,GIE      ;Disable INTs
Required MOVLW  55h             ;Unlock write
Sequence MOVWF  EECON2          ;
        MOVLW   AAh             ;
        MOVWF   EECON2          ;
        BSF     EECON1,WR       ;Start the write
        BSF     INTCON,GIE      ;Enable INTS
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR1<7>) must be cleared by software.

9.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 9-3) to the desired value to be written.

EXAMPLE 9-3: WRITE VERIFY

```
BSF     STATUS,RP0   ;Bank 1
BCF     STATUS,RP1   ;
MOVF    EEDAT,W      ;EEDAT not changed
                     ;from previous write
BSF     EECON1,RD    ;YES, Read the
                     ;value written
XORWF   EEDAT,W
BTFSS   STATUS,Z     ;Is data the same
GOTO    WRITE_ERR    ;No, handle error
:                    ;Yes, continue
```

9.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). The maximum endurance for any EEPROM cell is specified as D120. D124 specifies a maximum number of writes to any EEPROM location before a refresh is required of infrequently changing memory locations.

9.4.2 EEPROM ENDURANCE

As an example, hypothetically, a data EEPROM is 64 bytes long and has an endurance of 1M writes. It also has a refresh parameter of 10M writes. If every memory location in the cell were written the maximum number of times, the data EEPROM would fail after 64M write cycles. If every memory location, save 1, were written the maximum number of times, the data EEPROM would fail after 63M write cycles, but the one remaining location could fail after 10M cycles. If proper refreshes occurred, then the lone memory location would have to be refreshed 6 times for the data to remain correct.

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9.5 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (nominal 64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- Power glitch
- Software malfunction

9.6 Data EEPROM Operation During Code Protection

Data memory can be code-protected by programming the CPD bit in the Configuration Word (Register 12-1) to '0'.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to '0' will also help prevent data memory code protection from becoming breached.

TABLE 9-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7(1)	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by the data EEPROM module.

Note 1: PIC16F636/639 only.

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10.0 KEELOQ® COMPATIBLE CRYPTOGRAPHIC MODULE

To obtain information regarding the implementation of the KEELOQ module, Microchip Technology requires the execution of the "KEELOQ® Encoder License Agreement".

The "KEELOQ® Encoder License Agreement" may be accessed through the Microchip web site located at www.microchip.com/KEELOQ. Further information may be obtained by contacting your local Microchip Sales Representative.

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11.0 ANALOG FRONT-END (AFE) FUNCTIONAL DESCRIPTION (PIC16F639 ONLY)

The PIC16F639 device consists of the PIC16F636 device and low frequency (LF) Analog Front-End (AFE), with the AFE section containing three analog-input channels for signal detection and LF talk-back. This section describes the Analog Front-End (AFE) in detail.

The PIC16F639 device can detect a 125 kHz input signal as low as 1 mVpp and transmit data by using internal LF talk-back modulation or via an external transmitter. The PIC16F639 can also be used for various bidirectional communication applications. Figure 11-3 and Figure 11-4 show application examples of the device.

Each analog input channel has internal tuning capacitance, sensitivity control circuits, an input signal strength limiter and an LF talk-back modulation transistor. An Automatic Gain Control (AGC) loop is used for all three input channel gains. The output of each channel is OR'd and fed into a demodulator. The digital output is passed to the LFDATA pin. Figure 11-1 shows the block diagram of the AFE and Figure 11-2 shows the LC input path.

There are a total of eight Configuration registers. Six of them are used for AFE operation options, one for column parity bits and one for status indication of AFE operation. Each register has 9 bits including one row parity bit. These registers are readable and writable by SPI (Serial Protocol Interface) commands except for the Status register, which is read-only.

11.1 RF Limiter

The RF Limiter limits LC pin input voltage by de-Q'ing the attached LC resonant circuit. The absolute voltage limit is defined by the silicon process's maximum allowed input voltage (see **Section 15.0 "Electrical Specifications"**). The limiter begins de-Q'ing the external LC antenna when the input voltage exceeds V_{DE_Q}, progressively de-Q'ing harder to reduce the antenna input voltage.

The signal levels from all 3 channels are combined such that the limiter attenuates all 3 channels uniformly, in respect to the channel with the strongest signal.

11.2 Modulation Circuit

The modulation circuit consists of a modulation transistor (FET), internal tuning capacitors and external LC antenna components. The modulation transistor and the internal tuning capacitors are connected between the LC input pin and LCCOM pin. Each LC input has its own modulation transistor.

When the modulation transistor turns on, its low Turn-on Resistance (R_M) clamps the induced LC antenna voltage. The coil voltage is minimized when the modulation transistor turns-on and maximized when the modulation transistor turns-off. The modulation transistor's low Turn-on Resistance (R_M) results in a high modulation depth.

The LF talk-back is achieved by turning on and off the modulation transistor.

The modulation data comes from the microcontroller section via the digital SPI interface as "Clamp On", "Clamp Off" commands. Only those inputs that are enabled will execute the clamp command. A basic block diagram of the modulation circuit is shown in Figure 11-1 and Figure 11-2.

The modulation FET is also shorted momentarily after Soft Reset and Inactivity timer time-out.

11.3 Tuning Capacitor

Each channel has internal tuning capacitors for external antenna tuning. The capacitor values are programmed by the Configuration registers up to 63 pF, 1 pF per step.

Note:	The user can control the tuning capacitor by programming the AFE Configuration registers.

11.4 Variable Attenuator

The variable attenuator is used to attenuate, via AGC control, the input signal voltage to avoid saturating the amplifiers and demodulators.

Note:	The variable attenuator function is accomplished by the device itself. The user cannot control its function.

11.5 Sensitivity Control

The sensitivity of each channel can be reduced by the channel's Configuration register sensitivity setting. This is used to desensitize the channel from optimum.

Note:	The user can desensitize the channel sensitivity by programming the AFE Configuration registers.

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11.6 AGC Control

The AGC controls the variable attenuator to limit the internal signal voltage to avoid saturation of internal amplifiers and demodulators (Refer to **Section 11.4 "Variable Attenuator"**).

The signal levels from all 3 channels are combined such that AGC attenuates all 3 channels uniformly in respect to the channel with the strongest signal.

Note:	The AGC control function is accomplished by the device itself. The user cannot control its function.

11.7 Fixed Gain Amplifiers 1 and 2

FGA1 and FGA2 provides a maximum two-stage gain of 40 dB.

Note:	The user cannot control the gain of these two amplifiers.

11.8 Auto Channel Selection

The Auto Channel Selection feature is enabled if the Auto Channel Select bit AUTOCHSEL<8> in Configuration Register 5 (Register 11-6) is set, and disabled if the bit is cleared. When this feature is active (i.e., AUTOCHSE <8> = 1), the control circuit checks the demodulator output of each input channel immediately after the AGC settling time (T_{STAB}). If the output is high, it allows this channel to pass data, otherwise it is blocked.

The status of this operation is monitored by AFE Status Register 7 bits <8:6> (Register 11-8). These bits indicate the current status of the channel selection activity, and automatically updates for every Soft Reset period. The auto channel selection function resets after each Soft Reset (or after Inactivity timer time-out). Therefore, the blocked channels are reenabled after Soft Reset.

This feature can make the output signal cleaner by blocking any channel that was not high at the end of T_{AGC}. This function works only for demodulated data output, and is not applied for carrier clock or RSSI output.

11.9 Carrier Clock Detector

The Detector senses the input carrier cycles. The output of the Detector switches digitally at the signal carrier frequency. Carrier clock output is available when the output is selected by the DATOUT bit in the AFE Configuration Register 1 (Register 11-2).

11.10 Demodulator

The Demodulator consists of a full-wave rectifier, low pass filter, peak detector and Data Slicer that detects the envelope of the input signal.

11.11 Data Slicer

The Data Slicer consists of a reference generator and comparator. The Data Slicer compares the input with the reference voltage. The reference voltage comes from the minimum modulation depth requirement setting and input peak voltage. The data from all 3 channels are OR'd together and sent to the output enable filter.

11.12 Output Enable Filter

The Output Enable Filter enables the LFDATA output once the incoming signal meets the wake-up sequence requirements (see **Section 11.15 "Configurable Output Enable Filter"**).

11.13 RSSI (Received Signal Strength Indicator)

The RSSI provides a current which is proportional to the input signal amplitude (see **Section 11.31.3 "Received Signal Strength Indicator (RSSI) Output"**).

11.14 Analog Front-End Timers

The AFE has an internal 32 kHz RC oscillator. The oscillator is used in several timers:

- Inactivity timer
- Alarm timer
- Pulse Width timer
- Period timer
- AGC settling timer

11.14.1 RC OSCILLATOR

The RC oscillator is low power, 32 kHz ± 10% over temperature and voltage variations.

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11.14.2 INACTIVITY TIMER

The Inactivity Timer is used to automatically return the AFE to Standby mode, if there is no input signal. The time-out period is approximately 16 ms (TINACT), based on the 32 kHz internal clock.

The purpose of the Inactivity Timer is to minimize AFE current draw by automatically returning the AFE to the lower current Standby mode, if there is no input signal for approximately 16 ms.

The timer is reset when:

- An amplitude change in LF input signal, either high-to-low or low-to-high
- $\overline{CS}$ pin is low (any SPI™ command)
- Timer-related Soft Reset

The timer starts when:

- AFE receives any LF signal

The timer causes an AFE Soft Reset when:

- A previously received LF signal does not change either high-to-low or low-to-high for TINACT

The Soft Reset returns the AFE to Standby mode where most of the analog circuits, such as the AGC, demodulator and RC oscillator, are powered down. This returns the AFE to the lower Standby Current mode.

11.14.3 ALARM TIMER

The Alarm Timer is used to notify the MCU that the AFE is receiving LF signal that does not pass the output enable filter requirement. The time-out period is approximately 32 ms (TALARM) in the presence of continuing noise.

The Alarm Timer time-out occurs if there is an input signal for longer than 32 ms that does not meet the output enable filter requirements. The Alarm Timer time-out causes:

a) The $\overline{ALERT}$ pin to go low.

b) The ALARM bit to set in the AFE Status Configuration 7 register (Register 11-8).

The MCU is informed of the Alarm timer time-out by monitoring the $\overline{ALERT}$ pin. If the Alarm timer time-out occurs, the MCU can take appropriate actions such as lowering channel sensitivity or disabling channels. If the noise source is ignored, the AFE can return to a lower standby current draw state.

The timer is reset when the:

- $\overline{CS}$ pin is low (any SPI command).
- Output enable filter is disabled.
- LFDATA pin is enabled (signal passed output enable filter).

The timer starts when:

- Receiving a LF signal.

The timer causes a low output on the $\overline{ALERT}$ pin when:

- Output enable filter is enabled and modulated input signal is present for TALARM, but does not pass the output enable filter requirement.

Note:	The Alarm timer is disabled if the output enable filter is disabled.

11.14.4 PULSE WIDTH TIMER

The Pulse Width Timer is used to verify that the received output enable sequence meets both the minimum TOEH and minimum TOEL requirements.

11.14.5 PERIOD TIMER

The Period Timer is used to verify that the received output enable sequence meets the maximum TOET requirement.

11.14.6 AGC SETTLING TIMER (TAGC)

This timer is used to keep the output enable filter in Reset while the AGC settles on the input signal. The time-out period is approximately 3.5 ms. At end of this time (TAGC), the input should remain high (TPAGC), otherwise the counting is aborted and a Soft Reset is issued. See Figure 11-6 for details.

Note 1:	The AFE needs continuous and uninterrupted high input signal during AGC settling time (TAGC). Any absence of signal during this time may reset the timer and a new input signal is needed for AGC settling time, or may result in improper AGC gain settings which will produce invalid output.
2:	The rest of the AFE section wakes up if any of these input channels receive the AGC settling time correctly. AFE Status Register 7 bits <4:2> (Register 11-8) indicate which input channels have waken up the AFE first. Valid input signal on multiple input pins can cause more than one channel's indicator bit to be set.

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FIGURE 11-1: FUNCTIONAL BLOCK DIAGRAM – ANALOG FRONT-END

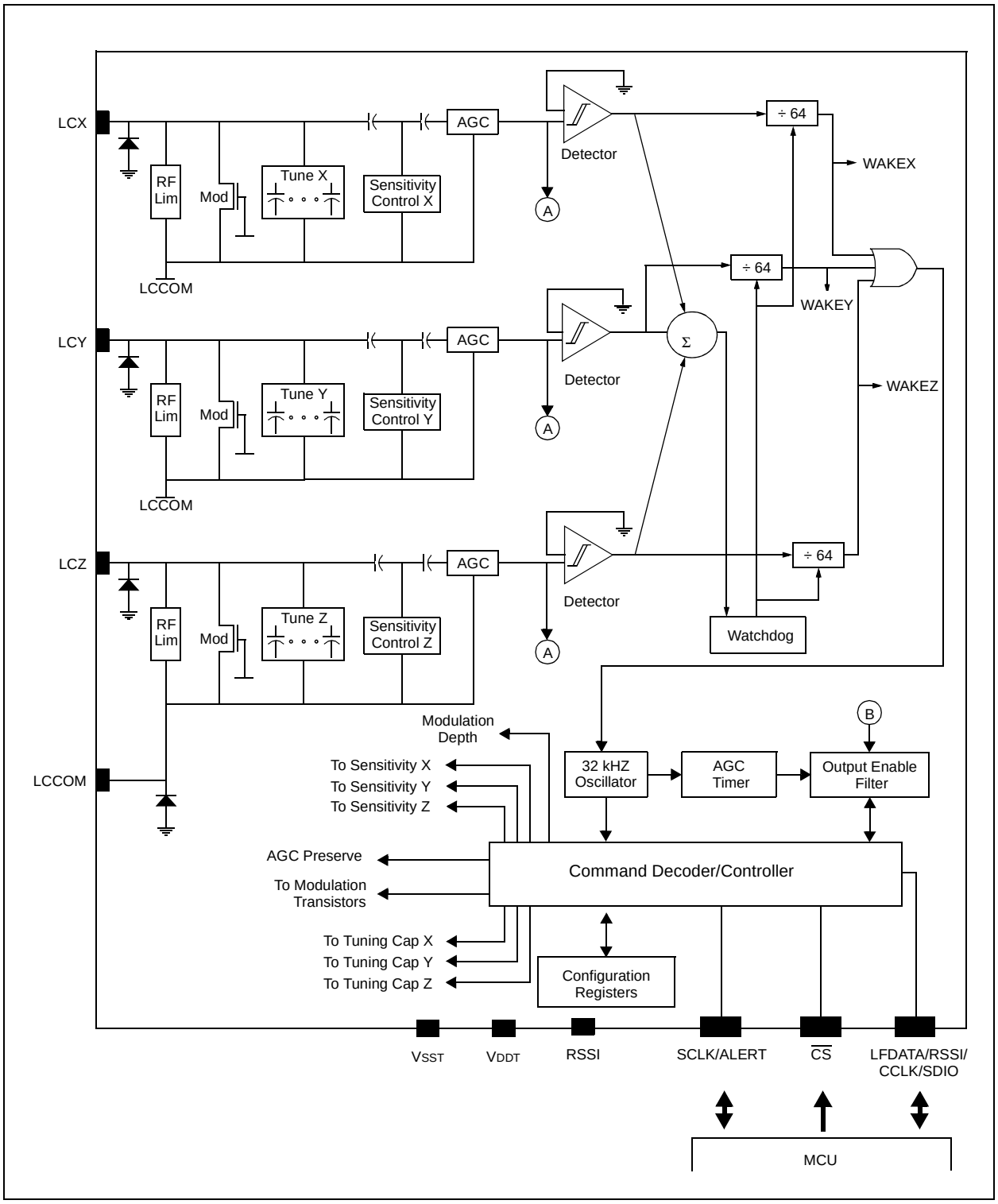

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FIGURE 11-2: LC INPUT PATH

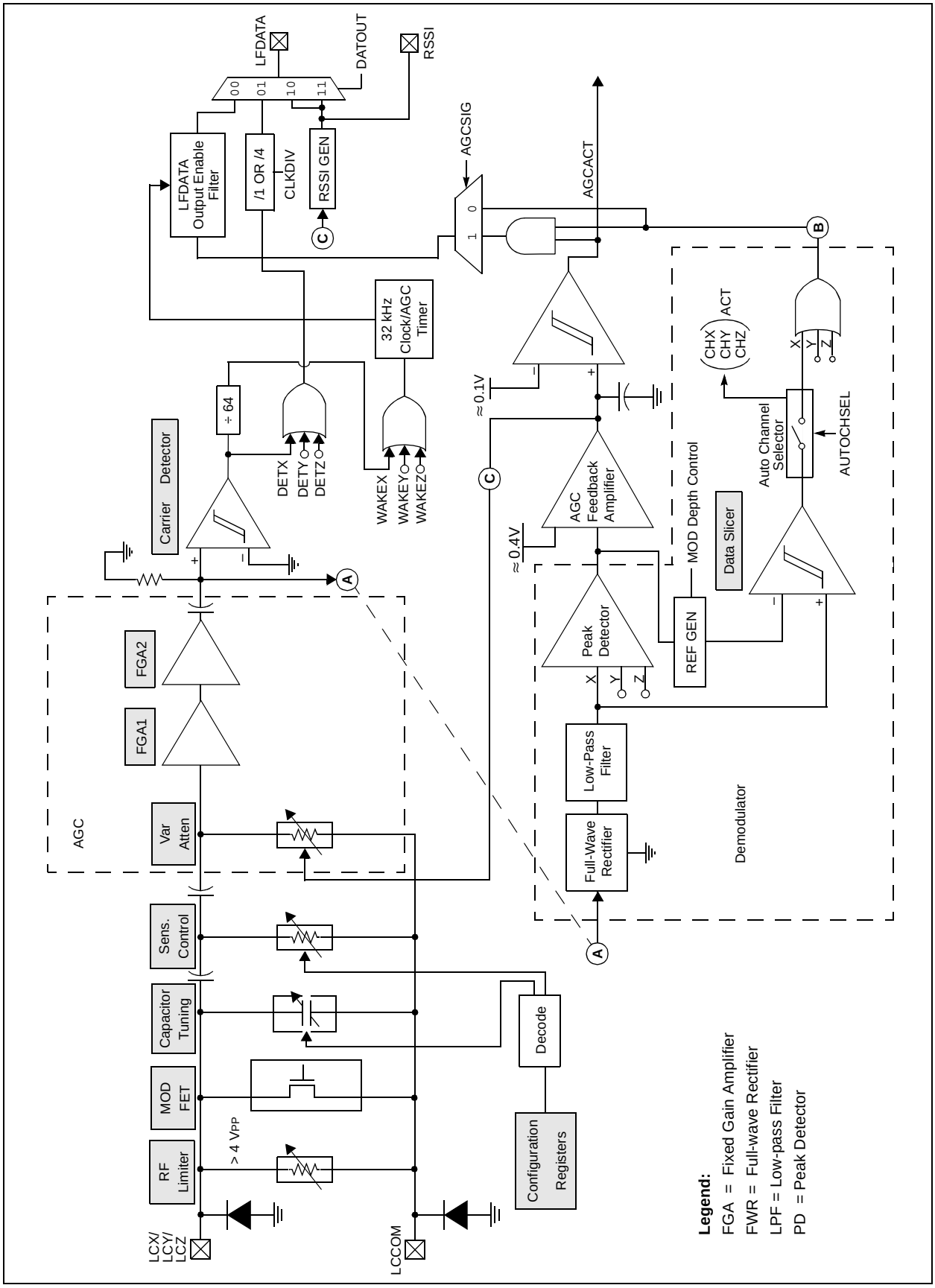

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FIGURE 11-3: BIDIRECTIONAL PASSIVE KEYLESS ENTRY (PKE) SYSTEM APPLICATION EXAMPLE

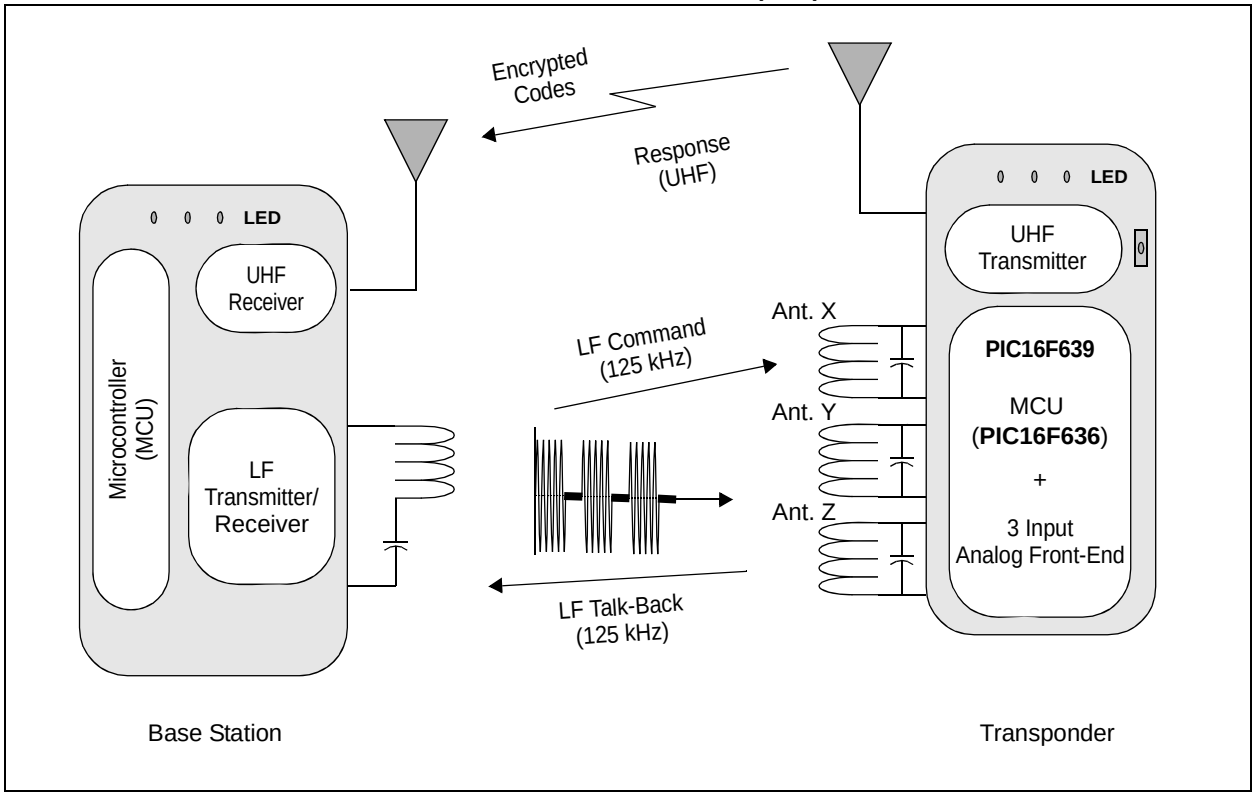
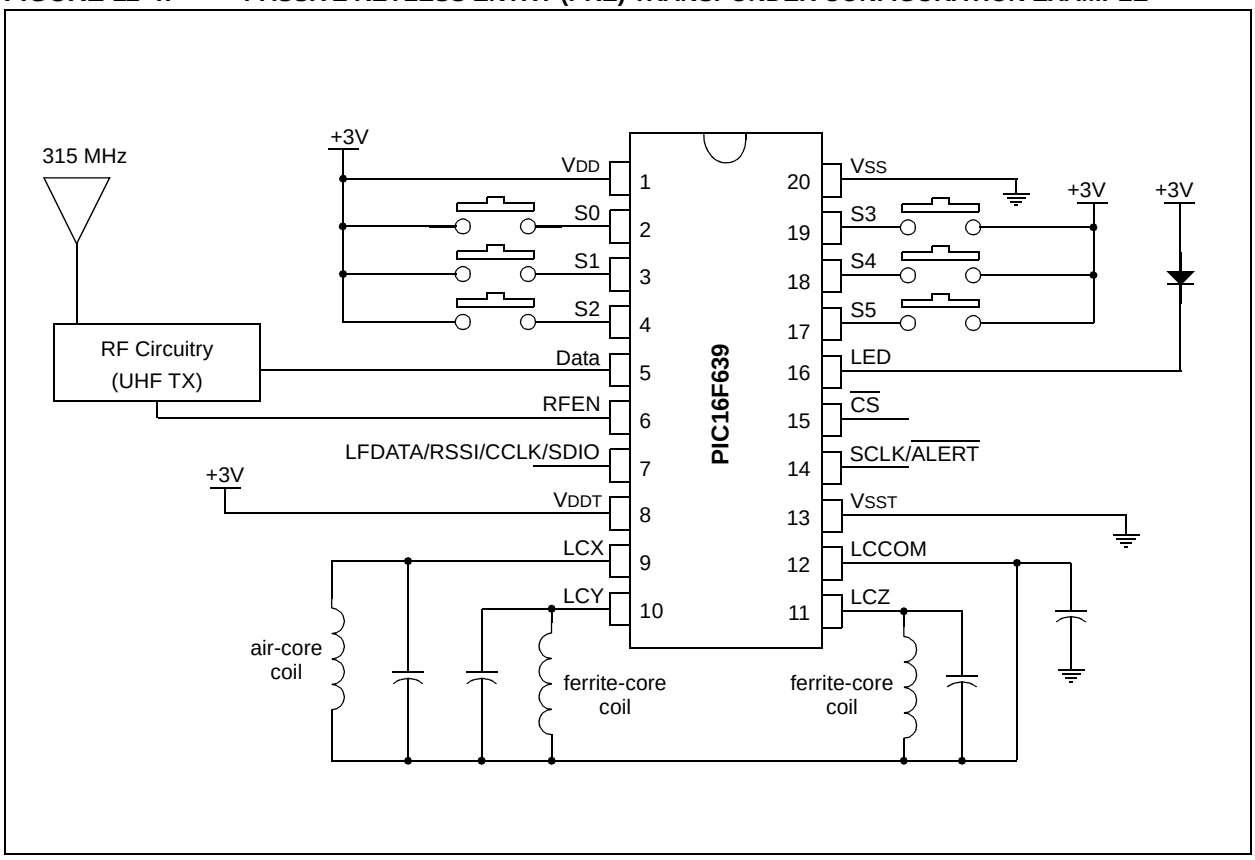


FIGURE 11-4: PASSIVE KEYLESS ENTRY (PKE) TRANSPONDER CONFIGURATION EXAMPLE



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11.15 Configurable Output Enable Filter

The purpose of this filter is to enable the LFDATA output and wake the microcontroller only after receiving a specific sequence of pulses on the LC input pins. Therefore, it prevents the AFE from waking up the microcontroller due to noise or unwanted input signals. The circuit compares the timing of the demodulated header waveform with a pre-defined value, and enables the demodulated LFDATA output when a match occurs.

The output enable filter consists of a high (TOEH) and low duration (TOEL) of a pulse immediately after the AGC settling gap time. The selection of high and low times further implies a max period time. The output enable high and low times are determined by SPI interface programming. Figure 11-5 and Figure 11-6 show the output enable filter waveforms.

There should be no missing cycles during TOEH. Missing cycles may result in failing the output enable condition.

FIGURE 11-5: OUTPUT ENABLE FILTER TIMING

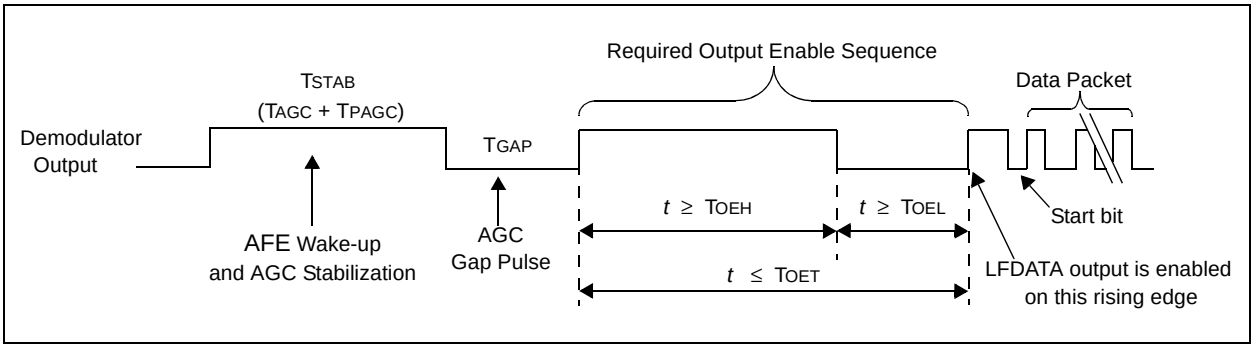

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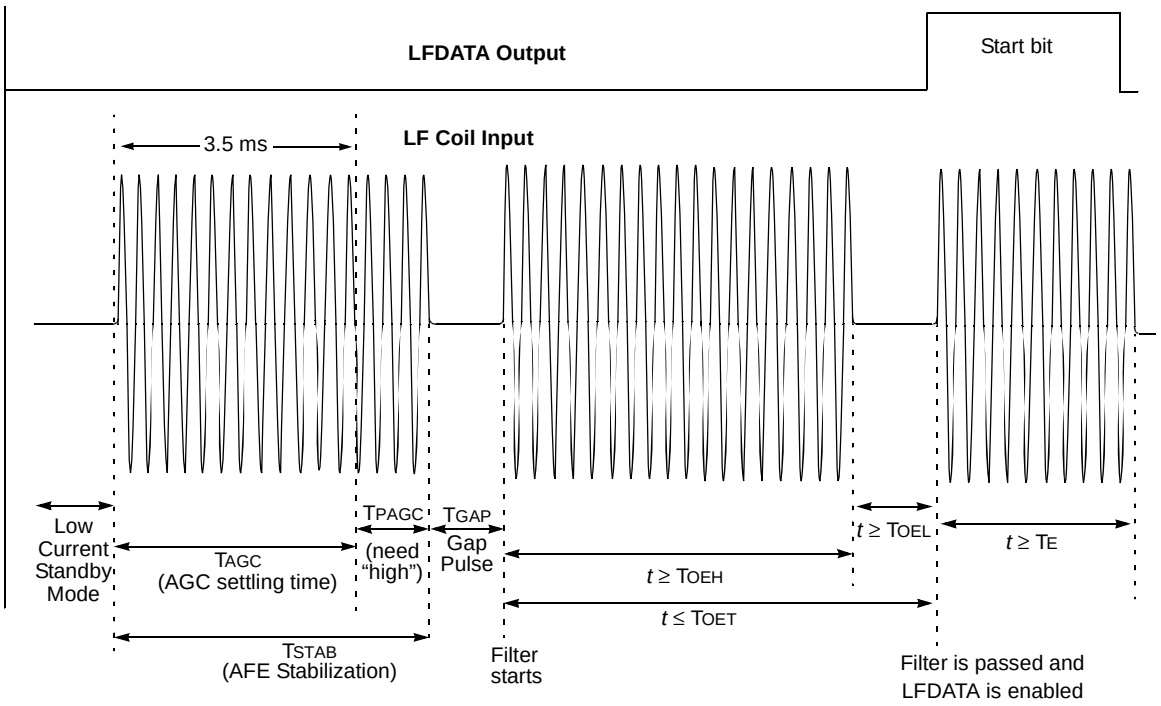
FIGURE 11-6: OUTPUT ENABLE FILTER TIMING EXAMPLE (DETAILED)



Legend:

TAGC	=	AGC stabilization time
TE	=	Time element of pulse
TGAP	=	AGC stabilization gap
TOEH	=	Minimum output enable filter high time
TOEL	=	Minimum output enable filter low time
TOET	=	Maximum output enable filter period
TPAGC	=	High time after TAGC
TSTAB	=	TAGC + TPAGC

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TABLE 11-1: TYPICAL OUTPUT ENABLE FILTER TIMING

OEH <1:0>	OEL <1:0>	TOEH (ms)	TOEL (ms)	TOET (ms)
01	00	1	1	3
01	01	1	1	3
01	10	1	2	4
01	11	1	4	6
10	00	2	1	4
10	01	2	1	4
10	10	2	2	5
10	11	2	4	8
11	00	4	1	6
11	01	4	1	6
11	10	4	2	8
11	11	4	4	10
00	xx	Filter Disabled		

Note 1: Typical at room temperature and VDD = 3.0V, 32 kHz oscillator.

TOEH is measured from the rising edge of the demodulator output to the first falling edge. The pulse width must fall within TOEH ≤ *t* ≤ TOET.

TOEL is measured from the falling edge of the demodulator output to the rising edge of the next pulse. The pulse width must fall within TOEL ≤ *t* ≤ TOET.

TOET is measured from rising edge to the next rising edge (i.e., the sum of TOEH and TOEL). The pulse width must be *t* ≤ TOET. If the Configuration Register 0 (Register 11-1), OEL<8:7> is set to '00', then TOEH must not exceed TOET and TOEL must not exceed TINACT.

The filter will reset, requiring a complete new successive high and low period to enable LFDATA, under the following conditions.

- The received high is not greater than the configured minimum TOEH value.
- During TOEH, a loss of signal > 56 µs. A loss of signal < 56 µs may or may not cause a filter Reset.
- The received low is not greater than the configured minimum TOEL value.
- The received sequence exceeds the maximum TOET value:
  - TOEH + TOEL > TOET
  - or TOEH > TOET
  - or TOEL > TOET
- A Soft Reset SPI command is received.

If the filter resets due to a long high (TOEH > TOET), the high-pulse timer will not begin timing again until after a gap of TE and another low-to-high transition occurs on the demodulator output.

Disabling the output enable filter disables the TOEH and TOEL requirement and the AFE passes all received LF data. See Figure 11-10, Figure 11-11 and Figure 11-12 for examples.

When viewed from an application perspective, from the pin input, the actual output enable filter timing must factor in the analog delays in the input path (such as demodulator charge and discharge times).

- **TOEH** - TDR + TDF
- **TOEL** + TDR - TDF

The output enable filter starts immediately after TGAP, the gap after AGC stabilization period.

11.16 Input Sensitivity Control

The AFE is designed to have typical input sensitivity of 3 mVPP. This means any input signal with amplitude greater than 3 mVPP can be detected. The AFE's internal AGC loop regulates the detecting signal amplitude when the input level is greater than approximately 20 mVPP. This signal amplitude is called "AGC-active level". The AGC loop regulates the input voltage so that the input signal amplitude range will be kept within the linear range of the detection circuits without saturation. The AGC Active Status bit (AGCACT<5>) in the AFE Status Register 7 (Register 11-8) is set if the AGC loop regulates the input voltage.

Table 11-2 shows the input sensitivity comparison when the AGCSIG option is used. When AGCSIG option bit is set, the demodulated output is available only when the AGC loop is active (see Table 11-1). The AFE has also input sensitivity reduction options per each channel. The Configuration Register 3 (Register 11-4), Configuration Register 4 (Register 11-5) and Configuration Register 5 (Register 11-6) have the option to reduce the channel gains from 0 dB to approximately -30 dB.

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TABLE 11-2: INPUT SENSITIVITY VS. MODULATED SIGNAL STRENGTH SETTING (AGCSIG <7>)

AGCSIG<7> (Config. Register 5)	Description	Input Sensitivity (Typical)
0	Disabled – the AFE passes signal of any amplitude level it is capable of detecting (demodulated data and carrier clock).	3.0 mVPP
1	Enabled – No output until AGC Status = 1 (i.e., VPEAK ≈ 20 mVPP) (demodulated data and carrier clock). • Provides the best signal to noise ratio.	20 mVPP

11.17 Input Channels (Enable/Disable)

Each channel can be individually enabled or disabled by programming bits in Configuration Register 0<3:1> (Register 11-1).

The purpose of having an option to disable a particular channel is to minimize current draw by powering down as much circuitry as possible, if the channel is not needed for operation. The exact circuits disabled when an input is disabled are amplifiers, detector, full-wave rectifier, data slicer, and modulation FET. However, the RF input limiter remains active to protect the silicon from excessive antenna input voltages.

11.18 AGC Amplifier

The circuit automatically amplifies input signal voltage levels to an acceptable level for the data slicer. Fast attack and slow release by nature, the AGC tracks the carrier signal level and not the modulated data bits.

The AGC inherently tracks the strongest of the three antenna input signals. The AGC requires an AGC stabilization time (TAGC).

The AGC will attempt to regulate a channel's peak signal voltage into the data slicer to a desired regulated AGC voltage – reducing the input path's gain as the signal level attempts to increase above regulated AGC voltage, and allowing full amplification on signal levels below the regulated AGC voltage.

The AGC has two modes of operation:

1. During the AGC settling time (TAGC), the AGC time constant is fast, allowing a reasonably short acquisition time of the continuous input signal.
2. After TAGC, the AGC switches to a slower time constant for data slicing.

Also, the AGC is frozen when the input signal envelope is low. The AGC tracks only high envelope levels.

11.19 AGC Preserve

The AGC preserve feature allows the AFE to preserve the AGC value during the AGC settling time (TAGC) and apply the value to the data slicing circuit for the following data streams instead of using a new tracking value. This feature is useful to demodulate the input signal correctly when the input has random amplitude variations at a given time period. This feature is enabled when the AFE receives an AGC Preserve On command and disabled if it receives an AGC Preserve Off command. Once the AGC Preserve On command is received, the AFE acquires a new AGC value during each AGC settling time and preserves the value until a Soft Reset or an AGC Preserve Off command is issued. Therefore, it does not need to issue another AGC Preserve On command. An AGC Preserve Off command is needed to disable the AGC preserve feature (see **Section 11.32.2.5 "AGC Preserve On Command"** and **Section 11.32.2.6 "AGC Preserve Off Command"** for AGC Preserve commands).

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11.20 Soft Reset

The AFE issues a Soft Reset in the following events:

a) After Power-on Reset (POR),
b) After Inactivity timer time-out,
c) If an “Abort” occurs,
d) After receiving SPI Soft Reset command.

The “Abort” occurs if there is no positive signal detected at the end of the AGC stabilization period (T_{AGC}). The Soft Reset initializes internal circuits and brings the AFE into a low current Standby mode operation. The internal circuits that are initialized by the Soft Reset include:

- Output Enable Filter
- AGC circuits
- Demodulator
- 32 kHz Internal Oscillator

The Soft Reset has no effect on the Configuration register setup, except for some of the AFE Status Register 7 bits. (Register 11-8).

The circuit initialization takes one internal clock cycle (1/32 kHz = 31.25 µs). During the initialization, the modulation transistors between each input and LCCOM pins are turned-on to discharge any internal/external parasitic charges. The modulation transistors are turned-off immediately after the initialization time.

The Soft Reset is executed in Active mode only. It is not valid in Standby mode.

11.21 Minimum Modulation Depth Requirement for Input Signal

The AFE demodulates the modulated input signal if the modulation depth of the input signal is greater than the minimum requirement that is programmed in the AFE Configuration Register 5 (Register 11-6). Figure 11-7 shows the definition of the modulation depth and examples. MODMIN<6:5> of the Configuration Register 5 offer four options. They are 75%, 50%, 25% and 12%, with a default setting of 50%.

The purpose of this feature is to enhance the demodulation integrity of the input signal. The 12% setting is the best choice for the input signal with weak modulation depth, which is typically observed near the high-voltage base station antenna and also at far-distance from the base station antenna. It gives the best demodulation sensitivity, but is very susceptible to noise spikes that can result in a bit detection error. The 75% setting can reduce the bit errors caused by noise, but gives the least demodulation sensitivity. See Table 11-3 for minimum modulation depth requirement settings.

TABLE 11-3: SETTING FOR MINIMUM MODULATION DEPTH REQUIREMENT

MODMIN Bits (Config. Register 5)		Modulation Depth
Bit 6	Bit 5	
0	0	50% (default)
0	1	75%
1	0	25%
1	1	12%

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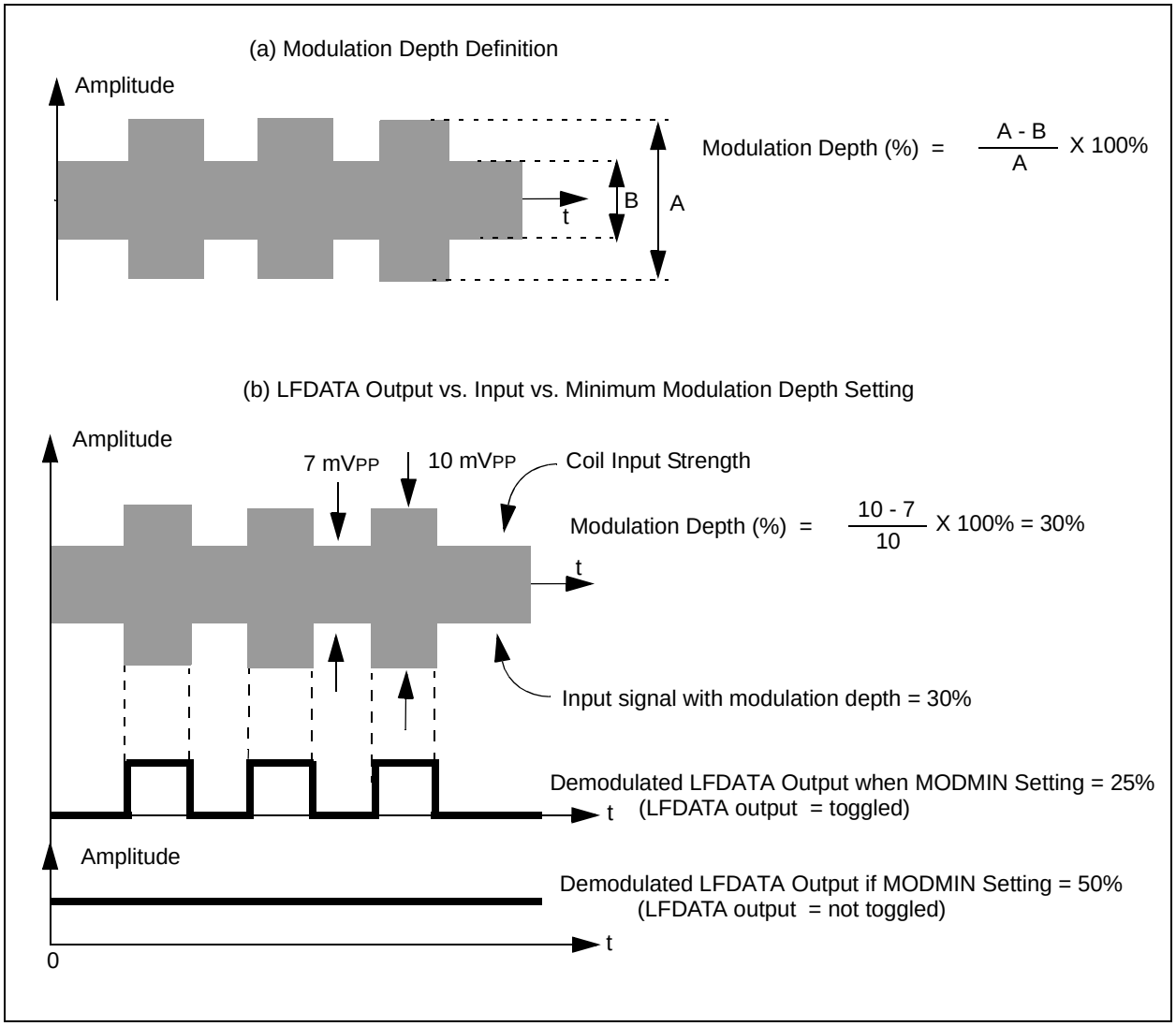
FIGURE 11-7: MODULATION DEPTH EXAMPLES



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11.22 Low Current Sleep Mode

The Sleep command from the microcontroller, via an SPI Interface command, places the AFE into an ultra Low-current mode. All circuits including the RF Limiter, except the minimum circuitry required to retain register memory and SPI capability, will be powered down to minimize the AFE current draw. Power-on Reset or any SPI command, other than Sleep command, is required to wake the AFE from Sleep.

11.23 Low Current Standby Mode

The AFE is in Standby mode when no LF signal is present on the antenna inputs but the AFE is powered and ready to receive any incoming signals.

11.24 Low Current Operating Mode

The AFE is in Low-current Operating mode when a LF signal is present on an LF antenna input and internal circuitry is switching with the received data.

11.25 Error Detection of AFE Configuration Register Data

The AFE's Configuration registers are volatile memory. Therefore, the contents of the registers can be corrupted or cleared by any electrical incidence such as battery disconnect. To ensure the data integrity, the AFE has an error detection mechanism using row and column parity bits of the Configuration register memory map. The bit 0 of each register is a row parity bit which is calculated over the eight configuration bits (from bit 1 to bit 8). The Column Parity Register (Configuration Register 6) holds column parity bits; each bit is calculated over the respective columns (Configuration registers 0 to 5) of the Configuration bits. The Status register is not included for the column parity bit calculation. Parity is to be odd. The parity bit set or cleared makes an odd number of set bits. The user needs to calculate the row and column parity bits using the contents of the registers and program them. During operation, the AFE continuously calculates the row and column parity bits of the configuration memory map. If a parity error occurs, the AFE lowers the SCLK/$\overline{\text{ALERT}}$ pin (interrupting the microcontroller section) indicating the configuration memory has been corrupted or unloaded and needs to be reprogrammed.

At an initial condition after a Power-On-Reset, the values of the registers are all clear (default condition). Therefore, the AFE will issue the parity bit error by lowering the SCLK/$\overline{\text{ALERT}}$ pin. If user reprograms the registers with correct parity bits, the SCLK/$\overline{\text{ALERT}}$ pin will be toggled to logic high level immediately.

The parity bit errors do not change or affect the AFE's functional operation.

Table 11-4 shows an example of the register values and corresponding parity bits.

TABLE 11-4: AFE CONFIGURATION REGISTER PARITY BIT EXAMPLE

Register Name	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (Row Parity)
Configuration Register 0	1	0	1	0	1	0	0	0	**0**
Configuration Register 1	0	0	0	0	0	0	0	0	**1**
Configuration Register 2	0	0	0	0	0	0	0	0	**1**
Configuration Register 3	0	0	0	0	0	0	0	0	**1**
Configuration Register 4	0	0	0	0	0	0	0	0	**1**
Configuration Register 5	1	0	0	0	0	0	0	0	**0**
Configuration Register 6 (Column Parity Register)	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**

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11.26 Factory Calibration

Microchip calibrates the AFE to reduce the device-to-device variation in standby current, internal timing and sensitivity, as well as channel-to-channel sensitivity variation.

11.27 De-Q'ing of Antenna Circuit

When the transponder is close to the base station, the transponder coil may develop coil voltage higher than V_{DE_Q}. This condition is called "near field". The AFE detects the strong near field signal through the AGC control, and de-Q'ing the antenna circuit to reduce the input signal amplitude.

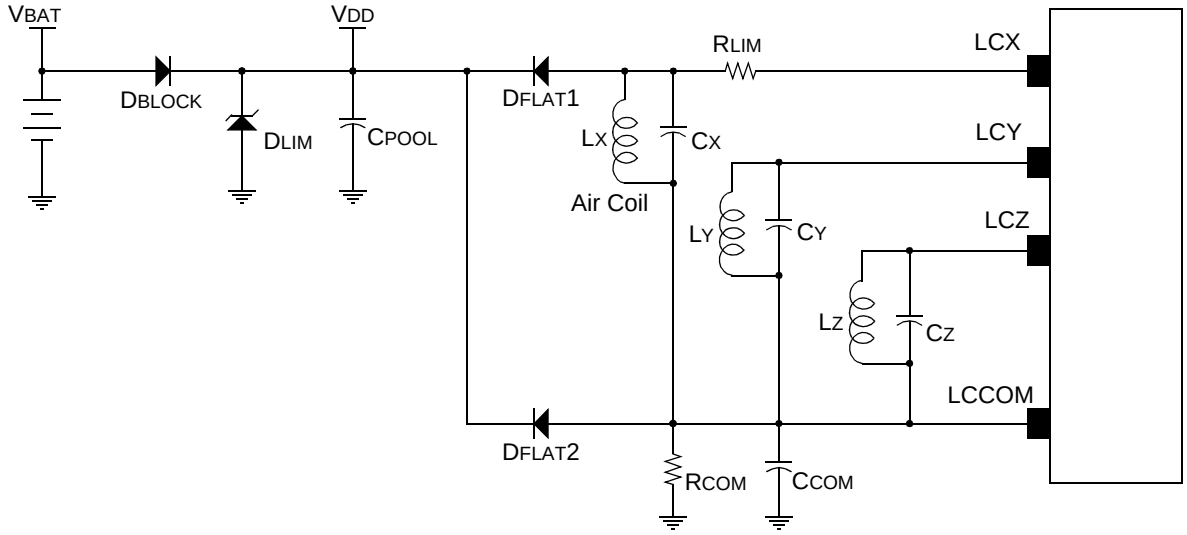
11.28 Battery Back-up and Batteryless Operation

The device supports both battery back-up and batteryless operation by the addition of external components, allowing the device to be partially or completely powered from the field.

Figure 11-8 shows an example of the external circuit for the battery back-up.

Note:	Voltage on LCCOM combined with coil input voltage must not exceed the maximum LC input voltage.

FIGURE 11-8: LF FIELD POWERING AND BATTERY BACK-UP EXAMPLE



Legend:
- CCOM = LCCOM charging capacitor.
- CPOOL = Pool capacitor (or battery back-up capacitor), charges in field and powers device.
- DBLOCK = Battery protection from reverse charge. Schottky for low forward bias drop.
- DFLAT = Field rectifier diodes.
- DLIM = Voltage limiting diode, may be required to limit VDD voltage when in strong fields.
- RCOM = Ccom discharge path.
- RLIM = Current limiting resistor, required for air coil in strong fields.

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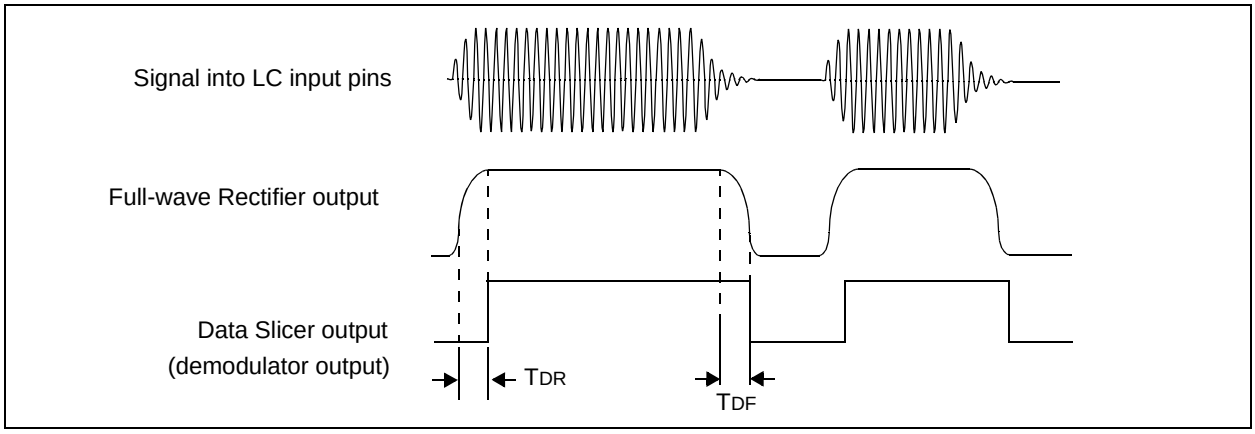
11.29 Demodulator

The demodulator recovers the modulation data from the received signal, containing carrier plus data, by appropriate envelope detection. The demodulator has a fast rise (charge) time (T_{DR}) and a fall time (T_{DF}) appropriate to an envelope of input signal (see **Section 15.0 "Electrical Specifications"** for T_{DR} and T_{DF} specifications). The demodulator contains the full-wave rectifier, low-pass filter, peak detector and data slicer.

FIGURE 11-9: DEMODULATOR CHARGE AND DISCHARGE



11.30 Power-On Reset

This circuit remains in a Reset state until a sufficient supply voltage is applied to the AFE. The Reset releases when the supply is sufficient for correct AFE operation, nominally V_{POR} of AFE.

The Configuration registers are all cleared on a Power-on Reset. As the Configuration registers are protected by odd row and column parity, the $\overline{\text{ALERT}}$ pin will be pulled down – indicating to the microcontroller section that the AFE configuration memory is cleared and requires loading.

11.31 LFDATA Output Selection

The LFDATA output can be configured to pass the Demodulator output, Received Signal Strength Indicator (RSSI) output, or Carrier Clock. See Configuration Register 1 (Register 11-2) for more details.

11.31.1 DEMODULATOR OUTPUT

The demodulator output is the default configuration of the output selection. This is the output of an envelope detection circuit. See Figure 11-9 for the demodulator output.

For a clean data output or to save operating power, the input channels can be individually enabled or disabled. If more than one channel is enabled, the output is the sum of each output of all enabled channels. There will be no valid output if all three channels are disabled. When the demodulated output is selected, the output is available in two different conditions depending on how the options of Configuration Register 0 (Register 11-1) are set: Output Enable Filter is disabled or enabled.

Related Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT <8:7>:
  - bit 8 bit 7
    - 0 0: Demodulator Output
    - 0 1: Carrier Clock Output
    - 1 0: RSSI Output
    - 0 1: RSSI Output
- Configuration Register 0 (Register 11-1): all bits

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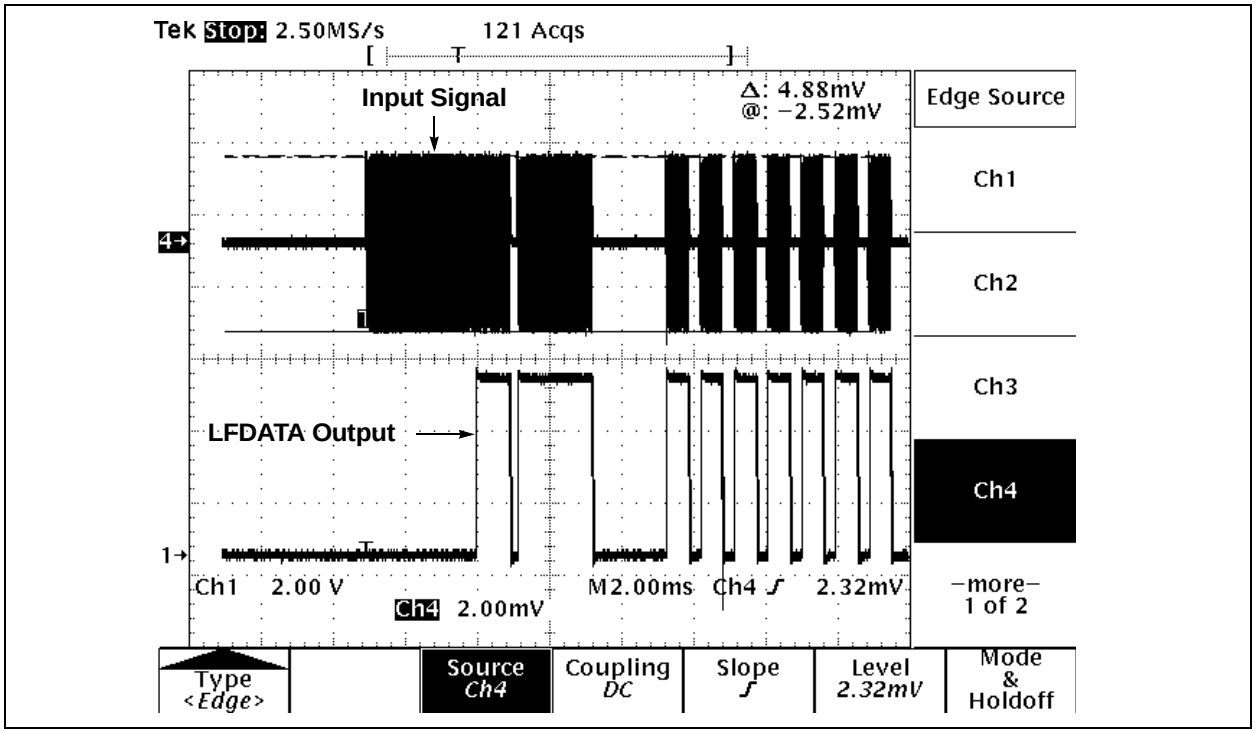
Case I. When Output Enable Filter is disabled: Demodulated output is available immediately after the AGC stabilization time (TAGC). Figure 11-10 shows an example of demodulated output when the Output Enable Filter is disabled.

FIGURE 11-10: INPUT SIGNAL AND DEMODULATOR OUTPUT WHEN THE OUTPUT ENABLE FILTER IS DISABLED



Case II. When Output Enable Filter is enabled: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 11-1). If the criteria is met, the output is available after the low timing (TOEL) of the Enable Filter. Figure 11-11 and Figure 11-12 shows examples of demodulated output when the Output Enable Filter is enabled.

FIGURE 11-11: INPUT SIGNAL AND DEMODULATOR OUTPUT (WHEN OUTPUT ENABLE FILTER IS ENABLED AND INPUT MEETS FILTER TIMING REQUIREMENTS)

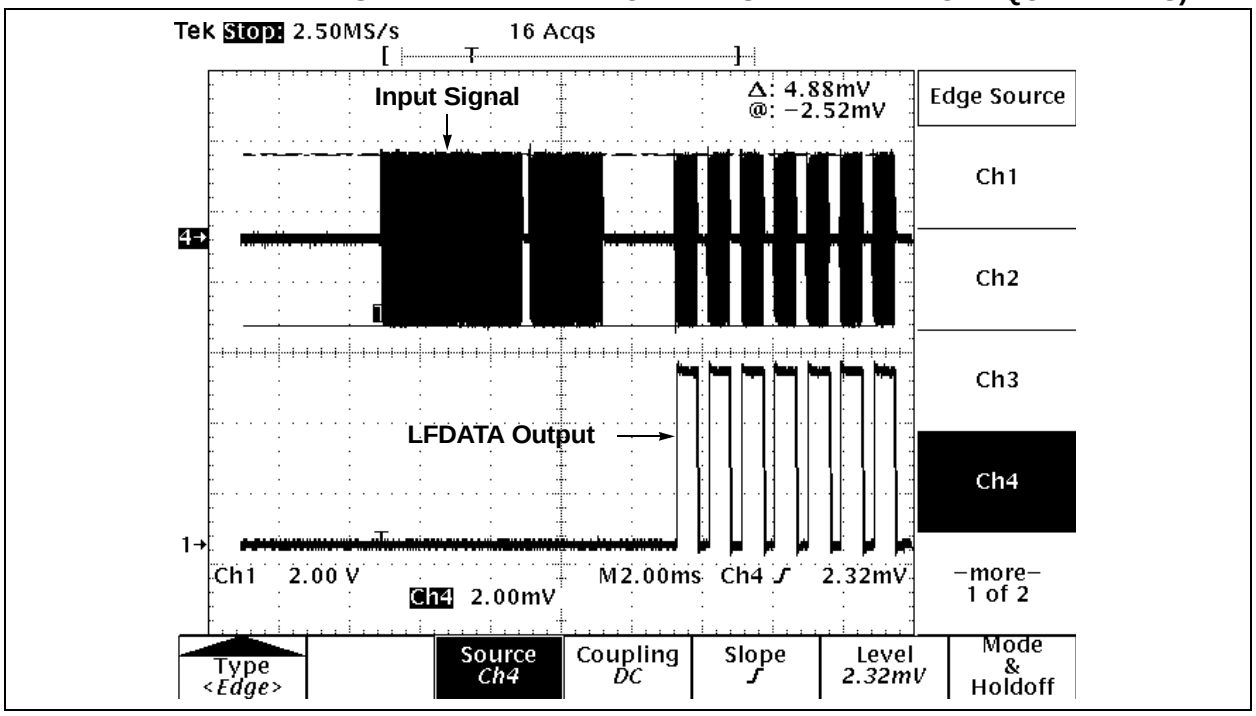


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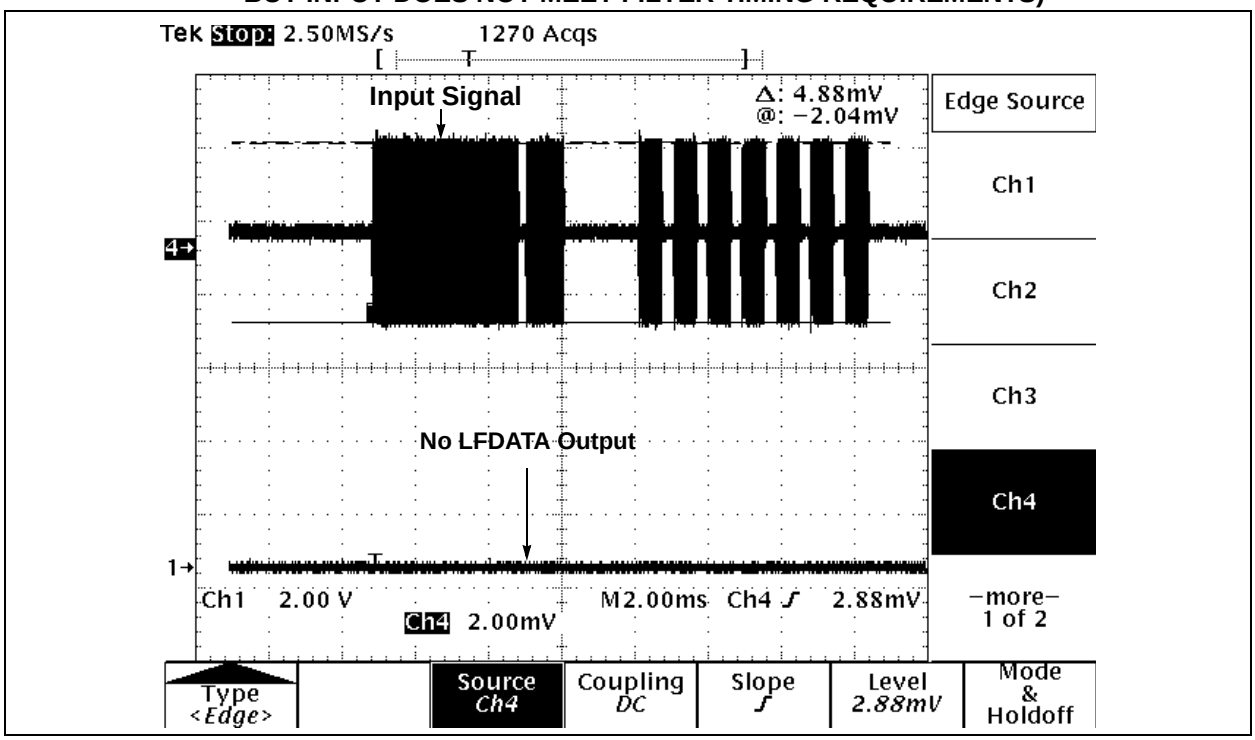
FIGURE 11-12: NO DEMODULATOR OUTPUT (WHEN OUTPUT ENABLE FILTER IS ENABLED BUT INPUT DOES NOT MEET FILTER TIMING REQUIREMENTS)



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11.31.2 CARRIER CLOCK OUTPUT

When the Carrier Clock output is selected, the LFDATA output is a square pulse of the input carrier clock and available as soon as the AGC stabilization time (T_{AGC}) is completed. There are two Configuration register options for the carrier clock output: (a) clock divide-by one or (b) clock divide-by four, depending on bit DATOUT<7> of Configuration Register 2 (Register 11-3). The carrier clock output is available immediately after the AGC settling time. The Output Enable Filter, AGCSIG, and MODMIN options are applicable for the carrier clock output in the same way as the demodulated output. The input channel can be individually enabled or disabled for the output. If more than one channel is enabled, the output is the sum of each output of all enabled channels. Therefore, the carrier clock output waveform is not as precise as when only one channel is enabled. It is recommended to enable one channel only if a precise output waveform is desired.

There will be no valid output if all three channels are disabled. See Figure 11-13 for carrier clock output examples.

Related Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT <8:7>:

bit 8	bit 7	
0	0	Demodulator Output
0	1	Carrier Clock Output
1	0	RSSI Output
1	1	RSSI Output

- Configuration Register 2 (Register 11-3), CLKDIV<7>:

  0: Carrier Clock/1

  1: Carrier Clock/4

- Configuration Register 0 (Register 11-1): all bits are affected
- Configuration Register 5 (Register 11-6)

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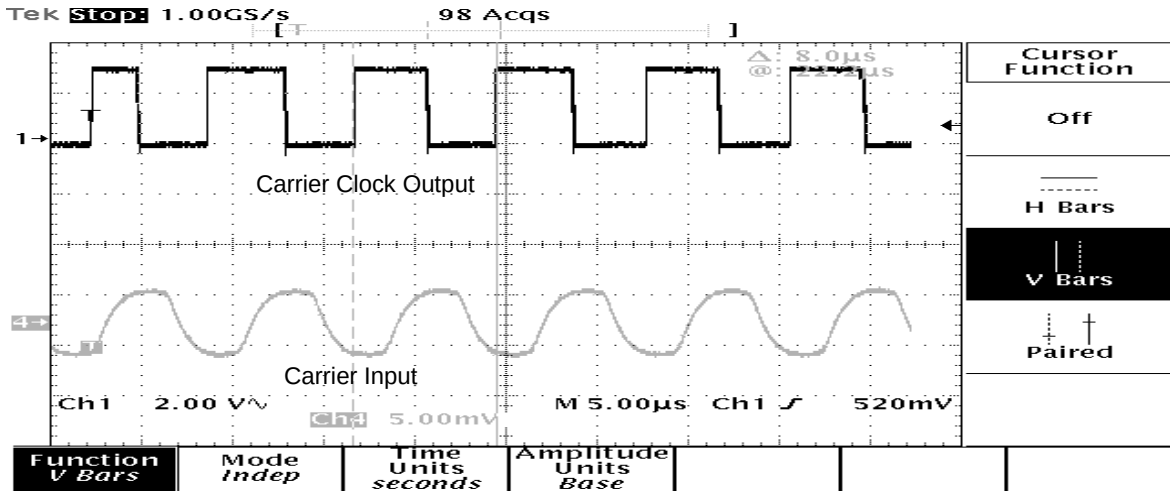
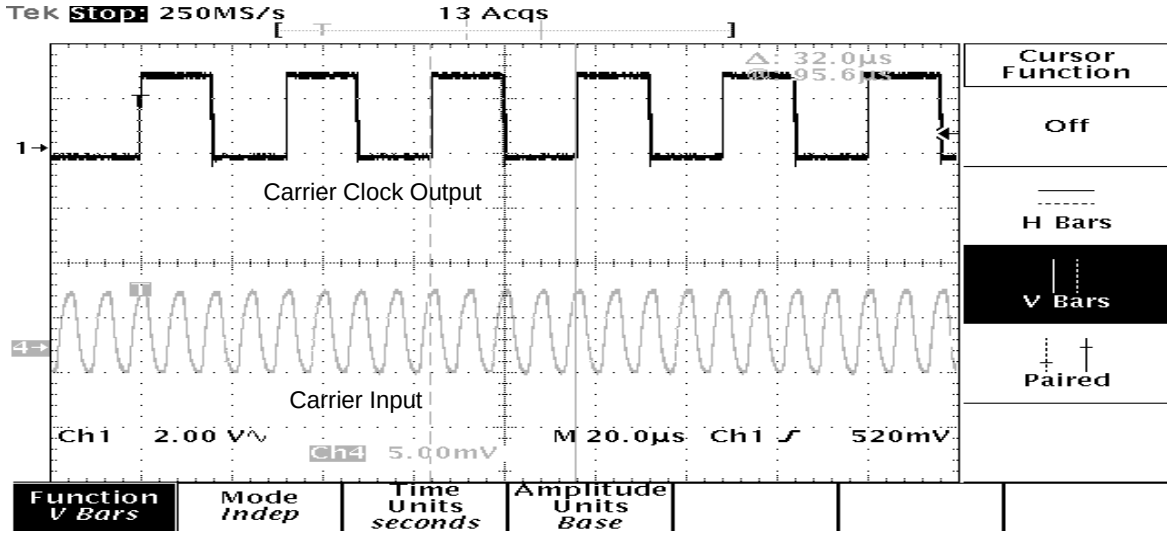
FIGURE 11-13: CARRIER CLOCK OUTPUT EXAMPLES

(A) CARRIER CLOCK OUTPUT WITH CARRIER/1 OPTION



(B) CARRIER CLOCK OUTPUT WITH CARRIER/4 OPTION



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11.31.3 RECEIVED SIGNAL STRENGTH INDICATOR (RSSI) OUTPUT

An analog current is available at the LFDATA pin when the Received Signal Strength Indicator (RSSI) output is selected for the AFE's Configuration register. The analog current is linearly proportional to the input signal strength (see Figure 11-15).

All timers in the circuit, such as inactivity timer, alarm timer, and AGC settling time, are disabled during the RSSI mode. Therefore, the RSSI output is not affected by the AGC settling time, and available immediately when the RSSI option is selected. The AFE enters Active mode immediately when the RSSI output is selected. The MCU I/O pin (RC3) connected to the LFDATA pin, must be set to high-impedance state during the RSSI Output mode.

When the AFE receives an SPI command during the RSSI output, the RSSI mode is temporary disabled until the SPI interface communication is completed. It returns to the RSSI mode again after the SPI interface communication is completed. The AFE holds the RSSI mode until another output type is selected ($\overline{CS}$ low turns off the RSSI signal). To obtain the RSSI output for a particular input channel, or to save operating power, the input channel can be individually enabled or disabled. If more than one channel is enabled, the RSSI output is from the strongest signal channel. There will be no valid output if all three channels are disabled.

Related AFE Configuration register bits:

- Configuration Register 1 (Register 11-2), DATOUT<8:7>:

bit 8	bit 7	
0	0	Demodulated Output
0	1	Carrier Clock Output
1	0	RSSI Output
1	1	RSSI Output

- Configuration Register 2 (Register 11-3), RSSIFET<8>:

  0: Pull-Down MOSFET off

  1: Pull-Down MOSFET on.

> **Note:** The pull-down MOSFET option is valid only when the RSSI output is selected. The MOSFET is not controllable by users when Demodulated or Carrier Clock output option is selected.

- Configuration Register 0 (Register 11-1): all bits are affected.

FIGURE 11-14: RSSI OUTPUT PATH

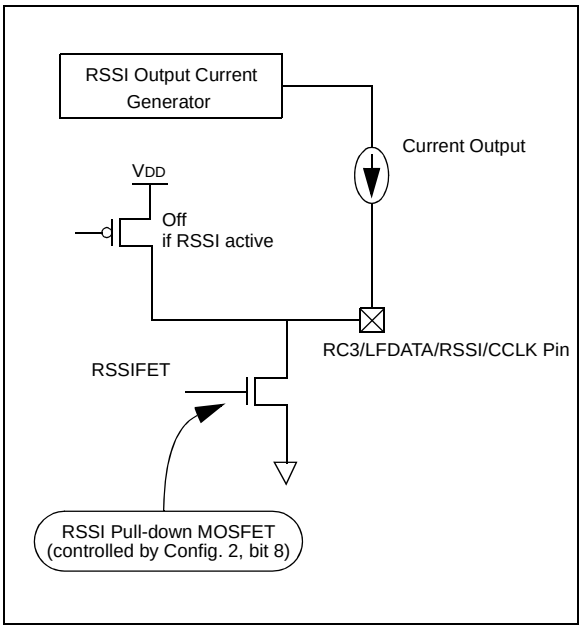

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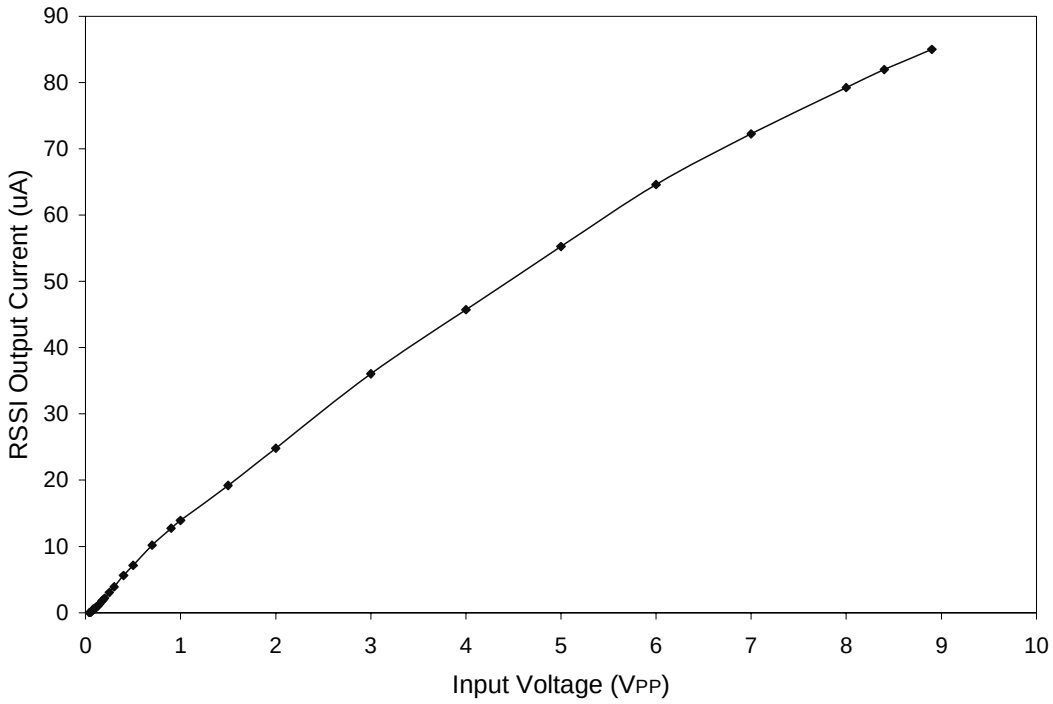
FIGURE 11-15: RSSI OUTPUT CURRENT VS. INPUT SIGNAL LEVEL EXAMPLE



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11.31.3.1 ANALOG-TO-DIGITAL DATA CONVERSION OF RSSI SIGNAL

The AFE's RSSI output is an analog current. It needs an external analog-to-digital (ADC) data conversion device for digitized output. The ADC data conversion can be accomplished by using a stand-alone external ADC device or by firmware utilizing MCU's internal comparator along with a few external resistors and a capacitor. For slope ADC implementations, the external capacitor at the LFDATA pad needs to be discharged before data sampling. For this purpose, the internal pull-down MOSFET on the LFDATA pad can be utilized. The MOSFET can be turned on or off with bit RSSIFET<8> of the Configuration Register 2 (Register 11-3). When it is turned on, the internal MOSFET provides a discharge path for the external capacitor. This MOSFET option is valid only if RSSI output is selected and not controllable by users for demodulated or carrier clock output options.

See separate application notes for various external ADC implementation methods for this device.

11.32 AFE Configuration

11.32.1 SPI COMMUNICATION

The AFE SPI interface communication is used to read or write the AFE's Configuration registers and to send command only messages. For the SPI interface, the device has three pads; $\overline{CS}$, SCLK/$\overline{ALERT}$, and LFDATA/RSSI/CCLK/SDIO. Figure 11-15, Figure 11-14, Figure 11-16 and Figure 11-17 shows examples of the SPI communication sequences.

When the device powers up, these pins will be high-impedance inputs until firmware modifies them appropriately. The AFE pins connected to the MCU pins will be as follows.

$\overline{CS}$

- Pin is permanently an input with an internal pull-up.

SCLK/$\overline{ALERT}$

- Pin is an open collector output when $\overline{CS}$ is high. An internal pull-up resistor exists internal to the AFE to ensure no spurious SPI communication between powering and the MCU configuring its pins. This pin becomes the SPI clock input when $\overline{CS}$ is low.

LFDATA/RSSI/CCLK/SDIO

- Pin is a digital output (LFDATA) so long as $\overline{CS}$ is high. During SPI communication, the pin is the SPI data input (SDI) unless performing a register Read, where it will be the SPI data output (SDO).

FIGURE 11-16: POWER-UP SEQUENCE

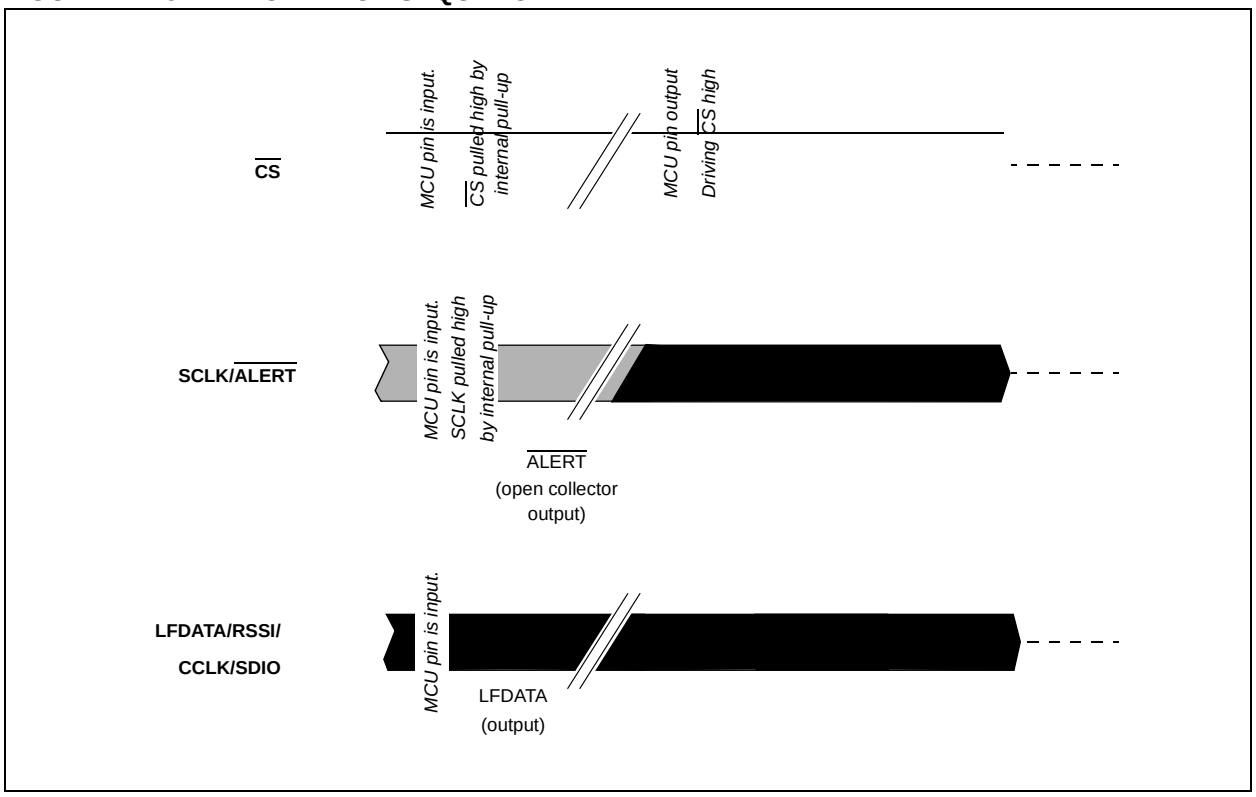

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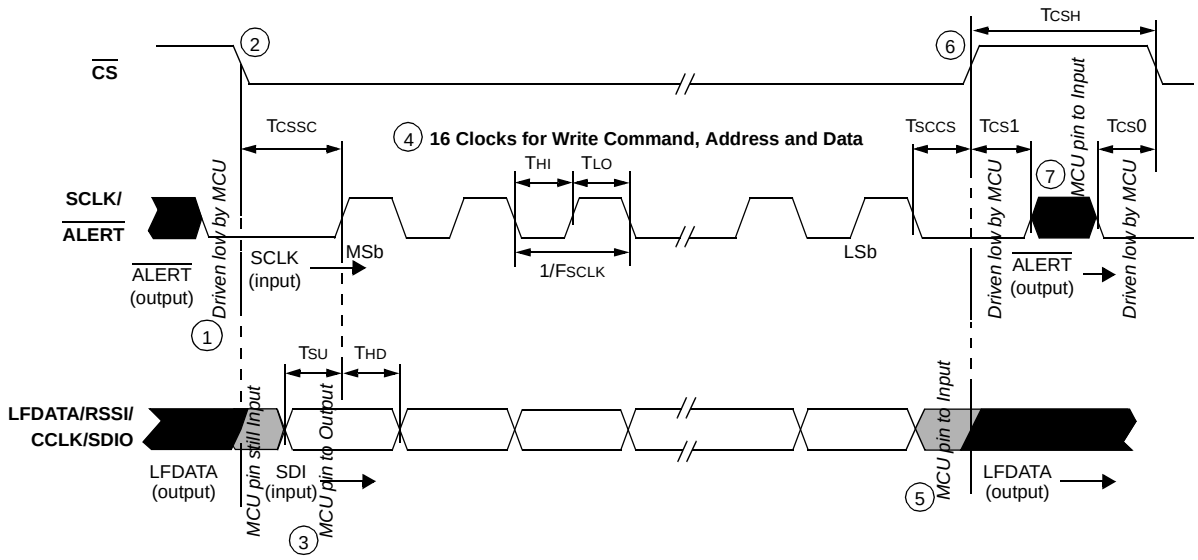
FIGURE 11-17: SPI WRITE SEQUENCE



MCU SPI Write Details:

1. Drive the AFE's open collector $\overline{\text{ALERT}}$ output low.
   - to ensure no false clocks occur when $\overline{\text{CS}}$ drops
2. Drop $\overline{\text{CS}}$.
   - AFE SCLK/$\overline{\text{ALERT}}$ becomes SCLK input
   - LFDATA/RSSI/CCLK/SDIO becomes SDI input
3. Change LFDATA/RSSI/CCLK/SDIO connected pin to output.
   - driving SPI data
4. Clock in 16-bit SPI Write sequence - command, address, data and parity bit.
   - command, address, data and parity bit
5. Change LFDATA/RSSI/CCLK/SDIO connected pin to input.
6. Raise $\overline{\text{CS}}$ to complete the SPI Write.
7. Change SCLK/$\overline{\text{ALERT}}$ back to input.

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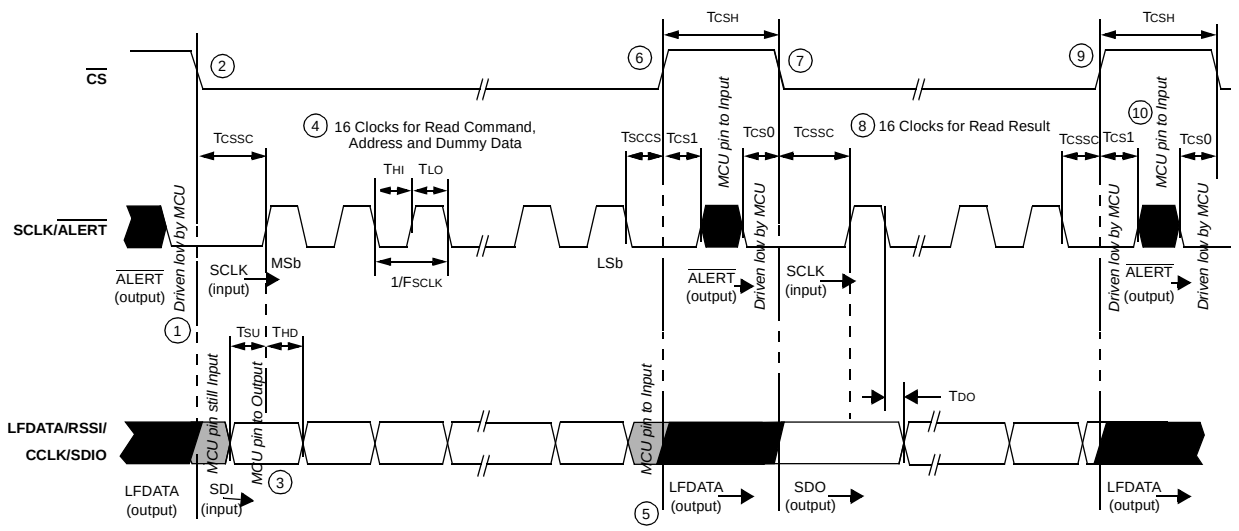
FIGURE 11-18: SPI READ SEQUENCE



MCU SPI Read Details:

1. Drive the AFE's open collector $\overline{\text{ALERT}}$ output low.
   - To ensure no false clocks occur when $\overline{\text{CS}}$ drops.
2. Drop $\overline{\text{CS}}$
   - AFE SCLK/$\overline{\text{ALERT}}$ becomes SCLK input.
   - LFDATA/RSSI/CCLK/SDIO becomes SDI input.
3. Change LFDATA/RSSI/CCLK/SDIO connected pin to output.
   - Driving SPI data.
4. Clock in 16-bit SPI Read sequence.
   - Command, address and dummy data.
5. Change LFDATA/RSSI/CCLK/SDIO connected pin to input.
6. Raise $\overline{\text{CS}}$ to complete the SPI Read entry of command and address.
7. Drop $\overline{\text{CS}}$.
   - AFE SCLK/$\overline{\text{ALERT}}$ becomes SCLK input.
   - LFDATA/RSSI/CCLK/SDIO becomes SDO output.
8. Clock out 16-bit SPI Read result.
   - First seven bits clocked-out are dummy bits.
   - Next eight bits are the Configuration register data.
   - The last bit is the Configuration register row parity bit.
9. Raise $\overline{\text{CS}}$ to complete the SPI Read.
10. Change SCLK/$\overline{\text{ALERT}}$ back to input.

Note: The T_{CSH} is considered as one clock. Therefore, the Configuration register data appears at 6th clock after T_{CSH}.

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11.32.2 COMMAND DECODER/ CONTROLLER

The circuit executes 8 SPI commands from the MCU. The command structure is:

Command (3 bits) + Configuration Address (4 bits) + Data Byte and Row Parity Bit received by the AFE Most Significant bit first. Table 11-5 shows the available SPI commands.

The AFE operates in SPI mode 0,0. In mode 0,0 the clock idles in the low state (Figure 11-19). SDI data is loaded into the AFE on the rising edge of SCLK and SDO data is clocked out on the falling edge of SCLK. There must be multiples of 16 clocks (SCLK) while $\overline{CS}$ is low or commands will abort.

TABLE 11-5: SPI COMMANDS (AFE)

Command	Address	Data	Row Parity	Description
Command only – Address and Data are "Don't Care", but need to be clocked in regardless.				
000	XXXX	XXXX XXXX	X	Clamp on – enable modulation circuit
001	XXXX	XXXX XXXX	X	Clamp off – disable modulation circuit
010	XXXX	XXXX XXXX	X	Enter Sleep mode (any other command wakes the AFE)
011	XXXX	XXXX XXXX	X	AGC Preserve On – to temporarily preserve the current AGC level
100	XXXX	XXXX XXXX	X	AGC Preserve Off – AGC again tracks strongest input signal
101	XXXX	XXXX XXXX	X	Soft Reset – resets various circuit blocks
Read Command – Data will be read from the specified register address.				
110	0000	Config Byte 0	P	General – options that may change during normal operation
	0001	Config Byte 1	P	LCX antenna tuning and LFDATA output format
	0010	Config Byte 2	P	LCY antenna tuning
	0011	Config Byte 3	P	LCZ antenna tuning
	0100	Config Byte 4	P	LCX and LCY sensitivity reduction
	0101	Config Byte 5	P	LCZ sensitivity reduction and modulation depth
	0110	Column Parity	P	Column parity byte for Config Byte 0 -> Config Byte 5
	0111	AFE Status	X	AFE status – parity error, which input is active, etc.
Write Command – Data will be written to the specified register address.				
111	0000	Config Byte 0	P	General – options that may change during normal operation
	0001	Config Byte 1	P	LCX antenna tuning and LFDATA output format
	0010	Config Byte 2	P	LCY antenna tuning
	0011	Config Byte 3	P	LCZ antenna tuning
	0100	Config Byte 4	P	LCX and LCY sensitivity reduction
	0101	Config Byte 5	P	LCZ sensitivity reduction and modulation depth
	0110	Column Parity	P	Column parity byte for Config Byte 0 -> Config Byte 5
	0111	Not Used	X	Register is readable, but not writable
Note: 'P' denotes the row parity bit (odd parity) for the respective data byte.				

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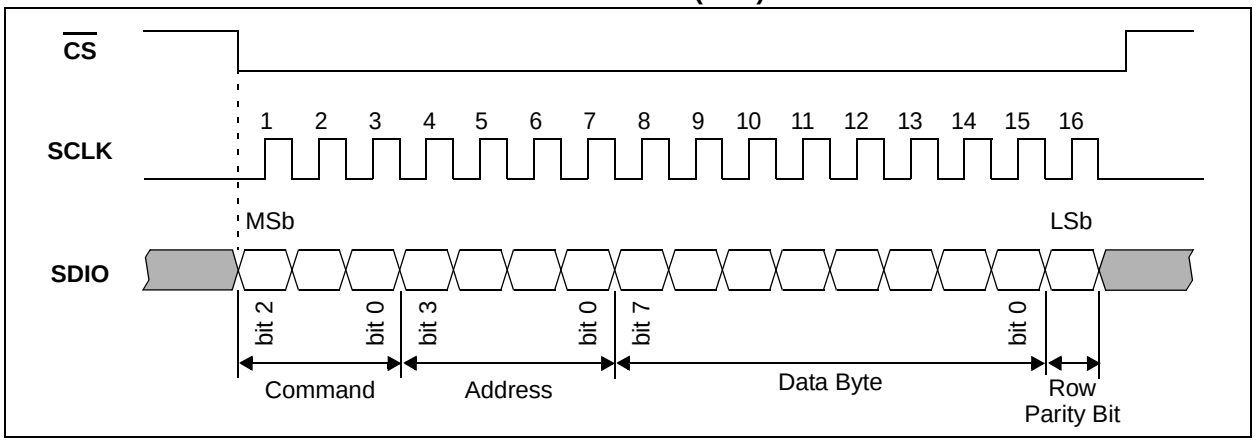
FIGURE 11-19: DETAILED SPI INTERFACE TIMING (AFE)



11.32.2.1 Clamp On Command

This command results in activating (turning on) the modulation transistors of all enabled channels; channels enabled in Configuration Register 0 (Register 11-1).

11.32.2.2 Clamp Off Command

This command results in de-activating (turning off) the modulation transistors of all channels.

11.32.2.3 Sleep Command

This command places the AFE in Sleep mode – minimizing current draw by disabling all but the essential circuitry. Any other command wakes the AFE (example: Clamp Off command).

11.32.2.4 Soft Reset Command

The AFE issues a Soft Reset when it receives an external Soft Reset command. The external Soft Reset command is typically used to end a SPI communication sequence or to initialize the AFE for the next signal detection sequence, etc. See **Section 11.20 "Soft Reset"** for more details on Soft Reset.

If a Soft Reset command is sent during a "Clamp-on" condition, the AFE still keeps the "Clamp-on" condition after the Soft Reset execution. The Soft Reset is executed in Active mode only, not in Standby mode. The SPI Soft Reset command is ignored if the AFE is not in Active mode.

11.32.2.5 AGC Preserve On Command

This command results in preserving the AGC level during each AGC settling time and apply the value to the data slicing circuit for the following data stream. The preserved AGC value is reset by a Soft Reset, and a new AGC value is acquired and preserved when it starts a new AGC settling time. This feature is disabled by an AGC Preserve Off command (see **Section 11.19 "AGC Preserve"**).

11.32.2.6 AGC Preserve Off Command

This command disables the AGC preserve feature and returns the AFE to the normal AGC tracking mode, fast tracking during AGC settling time and slow tracking after that (see **Section 11.19 "AGC Preserve"**).

11.32.3 CONFIGURATION REGISTERS

The AFE includes 8 Configuration registers, including a column parity register and AFE Status register. All registers are readable and writable via SPI, except Status register, which is readable only. Bit 0 of each register is a row parity bit (except for the AFE Status Register 7) that makes the register contents an odd number.

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TABLE 11-6: ANALOG FRONT-END CONFIGURATION REGISTERS SUMMARY

Register Name	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Register 0	OEH		OEL		ALRTIND	LCZEN	LCYEN	LCXEN	R0PAR
Configuration Register 1	DATOUT		Channel X Tuning Capacitor						R1PAR
Configuration Register 2	RSSIFET	CLKDIV	Channel Y Tuning Capacitor						R2PAR
Configuration Register 3	Unimplemented		Channel Z Tuning Capacitor						R3PAR
Configuration Register 4	Channel X Sensitivity Control				Channel Y Sensitivity Control				R4PAR
Configuration Register 5	AUTOCHSEL	AGCSIG	MODMIN	MODMIN	Channel Z Sensitivity Control				R5PAR
Column Parity Register 6	Column Parity Bits								R6PAR
AFE Status Register 7	Active Channel Indicators			AGCACT	Wake-up Channel Indicators			ALARM	PEI

REGISTER 11-1: CONFIGURATION REGISTER 0 (ADDRESS: 0000)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OEH1	OEH0	OEL1	OEL0	ALRTIND	LCZEN	LCYEN	LCXEN	R0PAR
bit 8								bit 0

bit 8-7 **OEH<1:0>**: Output Enable Filter High Time (TOEH) bit
00 = Output Enable Filter disabled (no wake-up sequence required, passes all signal to LFDATA)
01 = 1 ms
10 = 2 ms
11 = 4 ms

bit 6-5 **OEL<1:0>**: Output Enable Filter Low Time (TOEL) bit
00 = 1 ms
01 = 1 ms
10 = 2 ms
11 = 4 ms

bit 4 **ALRTIND**: $\overline{\text{ALERT}}$ bit, output triggered by:
1 = Parity error and/or expired Alarm timer (receiving noise, see **Section 11.14.3 "Alarm Timer"**)
0 = Parity error

bit 3 **LCZEN:** LCZ Enable bit
1 = Disabled
0 = Enabled

bit 2 **LCYEN:** LCY Enable bit
1 = Disabled
0 = Enabled

bit 1 **LCXEN:** LCX Enable bit
1 = Disabled
0 = Enabled

bit 0 **R0PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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REGISTER 11-2: CONFIGURATION REGISTER 1 (ADDRESS: 0001)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATOUT1	DATOUT0	LCXTUN5	LCXTUN4	LCXTUN3	LCXTUN2	LCXTUN1	LCXTUN0	R1PAR
bit 8								bit 0

bit 8-7 **DATOUT<1:0>:** LFDATA Output type bit
`00` = Demodulated output
`01` = Carrier Clock output
`10` = RSSI output
`11` = RSSI output

bit 6-1 **LCXTUN<5:0>:** LCX Tuning Capacitance bit
`000000` =+0 pF (Default)
:
`111111` =+63 pF

bit 0 **R1PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 11-3: CONFIGURATION REGISTER 2 (ADDRESS: 0010)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSSIFET	CLKDIV	LCYTUN5	LCYTUN4	LCYTUN3	LCYTUN2	LCYTUN1	LCYTUN0	R2PAR
bit 8								bit 0

bit 8 **RSSIFET**: Pull-down MOSFET on LFDATA pad bit (controllable by user in the RSSI mode only)
`1` = Pull-down RSSI MOSFET on
`0` = Pull-down RSSI MOSFET off

bit 7 **CLKDIV:** Carrier Clock Divide-by bit
`1` = Carrier Clock/4
`0` = Carrier Clock/1

bit 6-1 **LCYTUN<5:0>:** LCY Tuning Capacitance bit
`000000` =+0 pF (Default)
:
`111111` =+63 pF

bit 0 **R2PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

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REGISTER 11-4: CONFIGURATION REGISTER 3 (ADDRESS: 0011)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	LCZTUN5	LCZTUN4	LCZTUN3	LCZTUN2	LCZTUN1	LCZTUN0	R3PAR
bit 8								bit 0

bit 8-7 **Unimplemented**: Read as '0'

bit 6-1 **LCZTUN<5:0>:** LCZ Tuning Capacitance bit
000000 =+0 pF (Default)
:
111111 =+63 pF

bit 0 **R3PAR**: Register Parity Bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-5: CONFIGURATION REGISTER 4 (ADDRESS: 0100)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LCXSEN3	LCXSEN2	LCXSEN1	LCXSEN0	LCYSEN3	LCYSEN2	LCYSEN1	LCYSEN0	R4PAR
bit 8								bit 0

bit 8-5 **LCXSEN<3:0>(1)**: Typical LCX Sensitivity Reduction bit
0000 = -0 dB (Default)
0001 = -2 dB
0010 = -4 dB
0011 = -6 dB
0100 = -8 dB
0101 = -10 dB
0110 = -12 dB
0111 = -14 dB
1000 = -16 dB
1001 = -18 dB
1010 = -20 dB
1011 = -22 dB
1100 = -24 dB
1101 = -26 dB
1110 = -28 dB
1111 = -30 dB

bit 4-1 **LCYSEN<3:0>(1): Typical** LCY Sensitivity Reduction bit
0000 = -0 dB (Default)
:
1111 = -30 dB

bit 0 **R4PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Note 1: Assured monotonic increment (or decrement) by design.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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REGISTER 11-6: CONFIGURATION REGISTER 5 (ADDRESS: 0101)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUTOCHSEL	AGCSIG	MODMIN1	MODMIN0	LCZSEN3	LCZSEN2	LCZSEN1	LCZSEN0	R5PAR
bit 8								bit 0

bit 8 **AUTOCHSEL**: Auto Channel Select bit
1 = Enabled – AFE selects channel(s) that has demodulator output "high" at the end of T_{STAB}; or otherwise, blocks the channel(s).
0 = Disabled – AFE follows channel enable/disable bits defined in Register 0

bit 7 **AGCSIG**: Demodulator Output Enable bit, after the AGC loop is active
1 = Enabled – No output until AGC is regulating at around 20 mV_{PP} at input pins. The AGC Active Status bit is set when the AGC begins regulating.
0 = Disabled – the AFE passes signal of any level it is capable of detecting

bit 6-5 **MODMIN<1:0>**: Minimum Modulation Depth bit
00 = 50%
01 = 75%
10 = 25%
11 = 12%

bit 4-1 **LCZSEN<3:0>**(1): LCZ Sensitivity Reduction bit
0000 = -0dB (Default)
:
1111 = -30dB

bit 0 **R5PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Note 1: Assured monotonic increment (or decrement) by design.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-7: COLUMN PARITY REGISTER 6 (ADDRESS: 0110)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COLPAR7	COLPAR6	COLPAR5	COLPAR4	COLPAR3	COLPAR2	COLPAR1	COLPAR0	R6PAR
bit 8								bit 0

bit 8 **COLPAR7**: Set/Cleared so that this 8th parity bit + the sum of the config register row parity bits contain an odd number of set bits.

bit 7 **COLPAR6**: Set/Cleared such that this 7th parity bit + the sum of the 7th bits in config registers 0 through 5 contain an odd number of set bits.

bit 6 **COLPAR5**: Set/Cleared such that this 6th parity bit + the sum of the 6th bits in config registers 0 through 5 contain an odd number of set bits.

bit 5 **COLPAR4**: Set/Cleared such that this 5th parity bit + the sum of the 5th bits in config registers 0 through 5 contain an odd number of set bits.

bit 4 **COLPAR3**: Set/Cleared such that this 4th parity bit + the sum of the 4th bits in config registers 0 through 5 contain an odd number of set bits.

bit 3 **COLPAR2**: Set/Cleared such that this 3rd parity bit + the sum of the 3rd bits in config registers 0 through 5 contain an odd number of set bits.

bit 2 **COLPAR1**: Set/Cleared such that this 2nd parity bit + the sum of the 2nd bits in config registers 0 through 5 contain an odd number of set bits.

bit 1 **COLPAR0**: Set/Cleared such that this 1st parity bit + the sum of the 1st bits in config registers 0 through 5 contain an odd number of set bits.

bit 0 **R6PAR**: Register Parity bit – set/cleared so the 9-bit register contains odd parity – an odd number of set bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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REGISTER 11-8: AFE STATUS REGISTER 7 (ADDRESS: 0111)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
bit 8								bit 0

bit 8 **CHZACT**: Channel Z Active[(1)] bit (cleared via Soft Reset)
1 = Channel Z is passing data after TAGC
0 = Channel Z is not passing data after TAGC

bit 7 **CHYACT**: Channel Y Active[(1)] bit (cleared via Soft Reset)
1 = Channel Y is passing data after TAGC
0 = Channel Y is not passing data after TAGC

bit 6 **CHXACT**: Channel X Active[(1)] bit (cleared via Soft Reset)
1 = Channel X is passing data after TAGC
0 = Channel X is not passing data after TAGC

bit 5 **AGCACT**: AGC Active Status bit (real time, cleared via Soft Reset)
1 = AGC is active (Input signal is strong). AGC is active when input signal level is approximately > 20 mVPP range.
0 = AGC is inactive (Input signal is weak)

bit 4 **WAKEZ**: Wake-up Channel Z Indicator Status bit (cleared via Soft Reset)
1 = Channel Z caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Z did not cause a AFE wake-up

bit 3 **WAKEY**: Wake-up Channel Y Indicator Status bit (cleared via Soft Reset)
1 = Channel Y caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel Y did not cause a AFE wake-up

bit 2 **WAKEX**: Wake-up Channel X Indicator Status bit (cleared via Soft Reset)
1 = Channel X caused a AFE wake-up (passed ÷64 clock counter)
0 = Channel X did not cause a AFE wake-up

bit 1 **ALARM**: Indicates whether an Alarm timer time-out has occurred (cleared via read “Status Register command”)
1 = The Alarm timer time-out has occurred. It may cause the $\overline{\text{ALERT}}$ output to go low depending on the state of bit 4 of the Configuration register 0
0 = The Alarm timer is not timed out

bit 0 **PEI**: Parity Error Indicator bit – indicates whether a Configuration register parity error has occurred (real time)
1 = A parity error has occurred and caused the $\overline{\text{ALERT}}$ output to go low
0 = A parity error has not occurred

Note 1: Bit is high whenever channel is passing data. Bit is low in Standby mode.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

See Table 11-7 for the bit conditions of the AFE Status register after various SPI commands and the AFE Power-on Reset.

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TABLE 11-7: AFE STATUS REGISTER BIT CONDITION (AFTER POWER-ON RESET AND VARIOUS SPI COMMANDS)

Condition	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CHZACT	CHYACT	CHXACT	AGCACT	WAKEZ	WAKEY	WAKEX	ALARM	PEI
POR	0	0	0	0	0	0	0	0	1
Read Command (STATUS Register only)	u	u	u	u	u	u	u	0	u
Sleep Command	u	u	u	u	u	u	u	u	u
Soft Reset Executed(1)	0	0	0	0	0	0	0	u	u

Legend: u = unchanged

Note 1: See **Section 11.20 “Soft Reset”** and **Section 11.32.2.4 “Soft Reset Command”** for the condition of Soft Reset execution.

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12.0 SPECIAL FEATURES OF THE CPU

The PIC12F635/PIC16F636/639 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Wake-up Reset (WUR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F635/PIC16F636/639 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a nominal 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An Interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 12-1).

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12.1 Configuration Word Bits

The Configuration Word bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for more information.

REGISTER 12-1: CONFIG – CONFIGURATION WORD (ADDRESS: 2007h)

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	$\overline{\text{WURE}}$	FCMEN	IESO	BODEN1	BODEN0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$(1)	WDTE	FOSC2	F0SC1	F0SC0
bit 13													bit 0

bit 13 **Unimplemented:** Read as '1'

bit 12 **$\overline{\text{WURE}}$:** Wake-up Reset Enable bit
1 = Standard wake-up and continue enabled
0 = Wake-up and Reset enabled

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor enabled
0 = Fail-Safe Clock Monitor disabled

bit 10 **IESO:** Internal-External Switchover bit
1 = Internal External Switchover mode enabled
0 = Internal External Switchover mode disabled

bit 9-8 **BODEN<1:0>:** Brown-out Detect Enable bits
11 = BOD enabled and SBODEN bit disabled
10 = BOD enabled while running and disabled in Sleep. SBODEN bit disabled.
01 = SBODEN in Register 2-6 controls BOD function
00 = BOD and SBODEN disabled

bit 7 **$\overline{\text{CPD}}$**: Code Protection Data bit
1 = Data memory is not protected
0 = Data memory is external read protected

bit 6 **$\overline{\text{CP}}$**: Code Protection bit
1 = Program memory is not code-protected
0 = Program memory is external read and write-protected

bit 5 **MCLRE**: $\overline{\text{MCLR}}$ Pin Function Select bit
1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ function and weak internal pull-up is enabled
0 = $\overline{\text{MCLR}}$ pin is alternate function, $\overline{\text{MCLR}}$ function is internally disabled

bit 4 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled using SWDTEN in Register 12-2

bit 2-0 **FOSC<2:0>**: Oscillator Selection bits
000 = LP oscillator: Low power crystal on RA5/T1CKI/OSC1/CLKIN and RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT
001 = XT oscillator: Crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT
010 = HS oscillator: High-speed crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT
011 = EC: I/O function on RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT, CLKIN on RA5/T1CKI/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
110 = EXTRCIO oscillator: I/O function on RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN
111 = EXTRC oscillator: CLKOUT function on RA4/$\overline{\text{T1G}}$/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN

Note 1: Enabling Brown-out Detect does not automatically enable the Power-up Timer (PWRT).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

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12.2 Reset

The PIC12F635/PIC16F636/639 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) Wake-up Reset (WUR)
c) WDT Reset during normal operation
d) WDT Reset during Sleep
e) $\overline{\text{MCLR}}$ Reset during normal operation
f) $\overline{\text{MCLR}}$ Reset during Sleep
g) Brown-out Detect (BOD)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

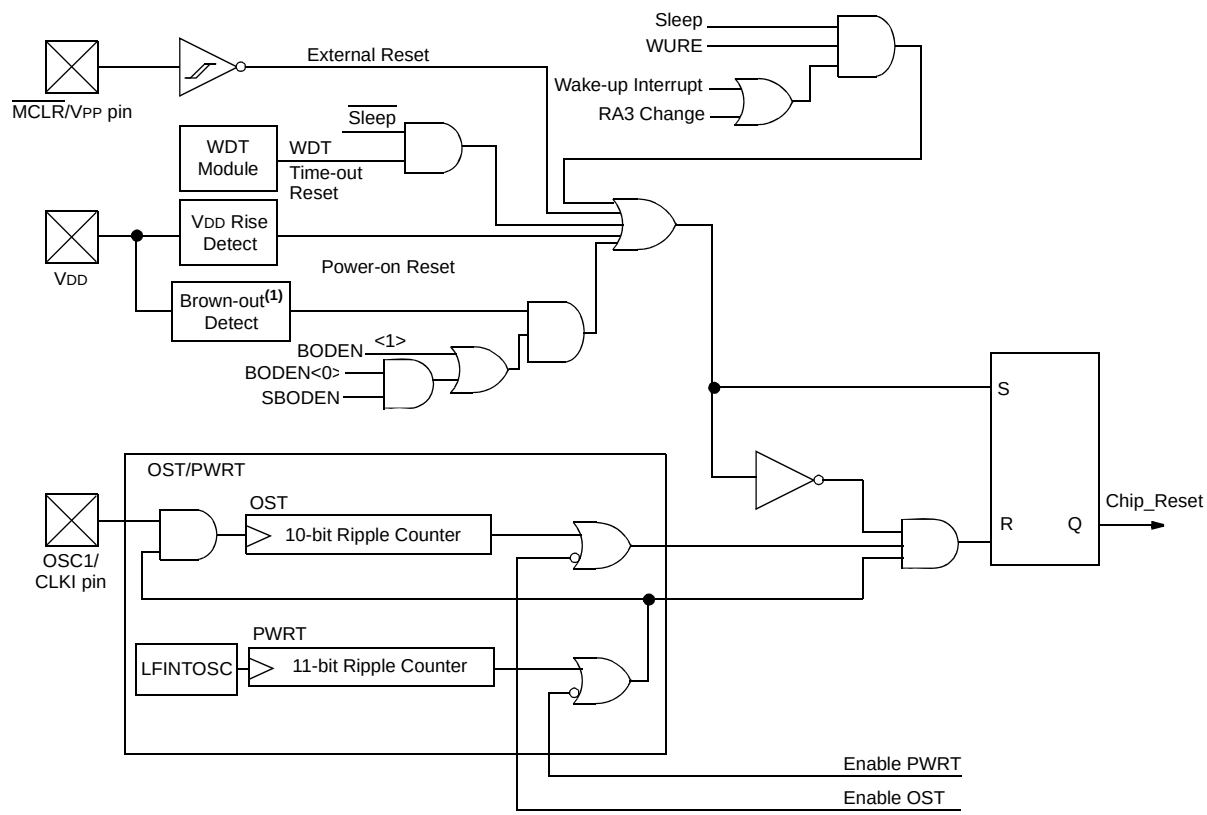
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Detect

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-3. These bits are used in software to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 12-1).

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12.3 Power-on Reset

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 15.0 "Electrical Specifications"** for details. If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in Reset until V_{DD} reaches V_{BOD} (see **Section 12.6 "Brown-out Detect (BOD)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach V_{SS} for a minimum of 100 µs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note *AN607, "Power-up Trouble Shooting"* (DS00607).

12.4 Wake-up Reset (WUR)

The PIC12F635/PIC16F636/639 has a modified wake-up from Sleep mechanism. When waking from Sleep, the WUR function resets the device and releases Reset when V_{DD} reaches an acceptable level.

If the $\overline{WURE}$ bit is enabled ('0') in the Configuration Word register, the device will Wake-up Reset from Sleep through one of the following events:

1. On any event that causes a wake-up event. The peripheral must be enabled to generate an interrupt or wake-up, GIE state is ignored.
2. When WURE is enabled, RA3 will always generate an interrupt-on-change signal during Sleep.

The $\overline{WUR}$, $\overline{POR}$ and $\overline{BOD}$ bits in the PCON register and the $\overline{TO}$ and $\overline{PD}$ bits in the Status register can be used to determine the cause of device Reset.

To allow WUR upon RA3 change:

1. Enable the WUR function, $\overline{WURE}$ Configuration Bit = 0.
2. Enable RA3 as an input, MCLRE Configuration Bit = 0.
3. Read PORTA to establish the current state of RA3.
4. Execute SLEEP instruction.
5. When RA3 changes state, the device will wake-up and then reset. The $\overline{WUR}$ bit in PCON will be cleared to '0'.

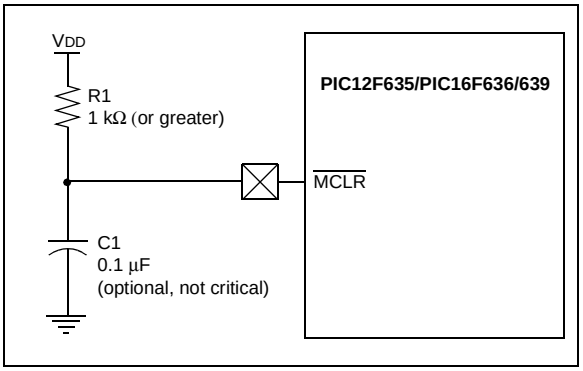
12.5 $\overline{MCLR}$

PIC12F635/PIC16F636/639 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low. See Figure 12-2 for the recommended $\overline{MCLR}$ circuit.

An internal $\overline{MCLR}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When cleared, $\overline{MCLR}$ is internally tied to V_{DD} and an internal weak pull-up is enabled for the $\overline{MCLR}$ pin. In-Circuit Serial Programming is not affected by selecting the internal $\overline{MCLR}$ option.

FIGURE 12-2: RECOMMENDED $\overline{MCLR}$ CIRCUIT



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12.6 Brown-out Detect (BOD)

The BODEN0 and BODEN1 bits in the Configuration Word register select one of four BOD modes. Two modes have been added to allow software or hardware control of the BOD enable. When BODEN<1:0> = 01, the SBODEN bit (PCON<4>) enables/disables the BOD allowing it to be controlled in software. By selecting BODEN<1:0>, the BOD is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBODEN bit is disabled. See Register 12-1 for the Configuration Word definition.

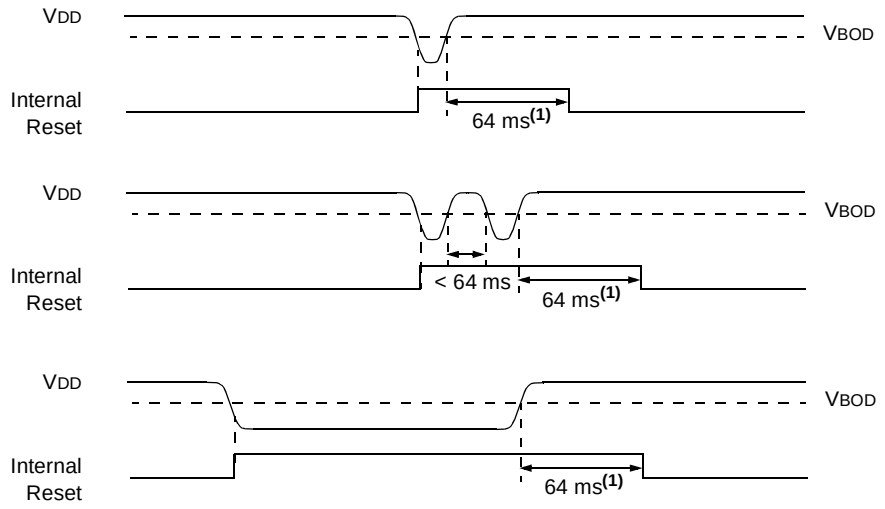
If VDD falls below VBOD for greater than parameter (TBOD) (see **Section 15.0 "Electrical Specifications"**), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not ensured to occur if VDD falls below VBOD for less than parameter (TBOD).

On any Reset (Power-on, Brown-out Detect, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOD (see Figure 12-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional nominal 64 ms.

Note:	The Power-up Timer is enabled by the $\overline{\text{PWRTE}}$ bit in the Configuration Word register.

If VDD drops below VBOD while the Power-up Timer is running, the chip will go back into a Brown-out Detect and the Power-up Timer will be re-initialized. Once VDD rises above VBOD, the Power-up Timer will execute a 64 ms Reset.

FIGURE 12-3: BROWN-OUT DETECT SITUATIONS



Note 1: Nominal 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

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12.7 Time-out Sequence

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences. The device can execute code from the INTOSC, while OST is active, by enabling Two-Speed Start-up or Fail-Safe Clock Monitor (See **Section 3.6.2 "Two-Speed Start-up Sequence"** and **Section 3.7 "Fail-Safe Clock Monitor"**).

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F635/PIC16F636/639 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

12.8 Power Control (PCON) Register

The Power Control register, PCON (address 8Eh), has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOD}}$ (Brown-out). $\overline{\text{BOD}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOD}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOD}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BODEN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., V_{DD} may have gone too low).

For more information, see **Section 4.2.3 "Ultra Low-Power Wake-up"** and **Section 12.6 "Brown-out Detect (BOD)"**.

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Detect		Wake-up from Sleep
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	
XT, HS, LP	T_{PWRT} + 1024 • T_{OSC}	1024 • T_{OSC}	T_{PWRT} + 1024 • T_{OSC}	1024 • T_{OSC}	1024 • T_{OSC}
RC, EC, INTOSC	T_{PWRT}	—	T_{PWRT}	—	—

TABLE 12-2: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT DETECT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets(1)
03h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
8Eh	PCON	—	—	ULPWUE	SBODEN	$\overline{\text{WUR}}$	—	$\overline{\text{POR}}$	$\overline{\text{BOD}}$	--01 q-qq	--0u u-uu

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOD.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

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TABLE 12-3: PCON BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOD}$	$\overline{WUR}$	$\overline{TO}$	$\overline{PD}$	Condition
0	x	x	1	1	Power-on Reset
u	0	u	1	1	Brown-out Detect
u	u	u	0	u	WDT Reset
u	u	u	0	0	WDT Wake-up
u	u	u	u	u	$\overline{MCLR}$ Reset during normal operation
u	u	u	1	0	$\overline{MCLR}$ Reset during Sleep
u	u	0	1	0	Wake-up Reset during Sleep
u	0	u	1	1	Brown-out Detect during Sleep

Legend: u = unchanged, x = unknown

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FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$)

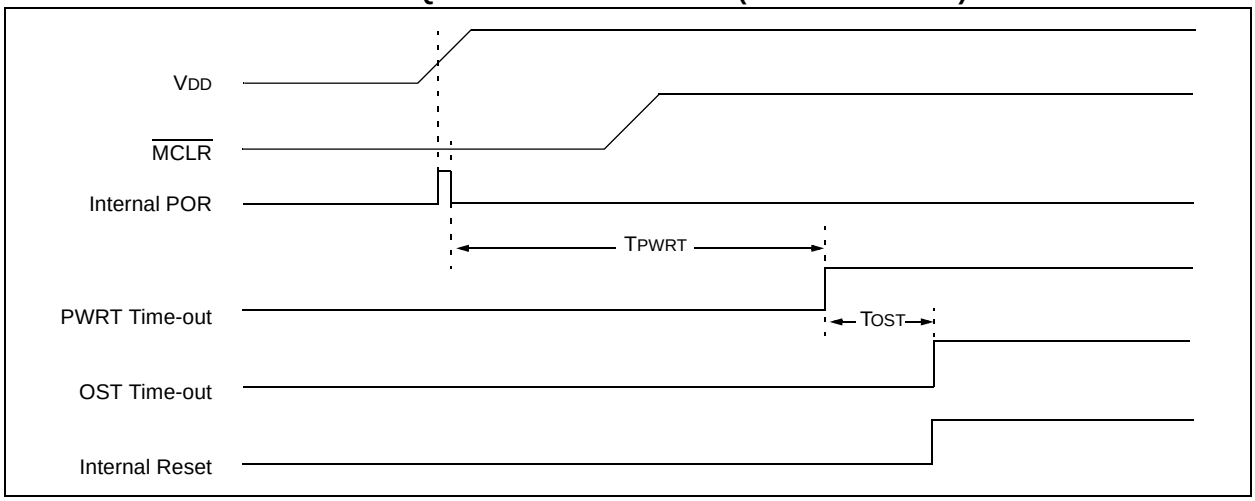

FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$)

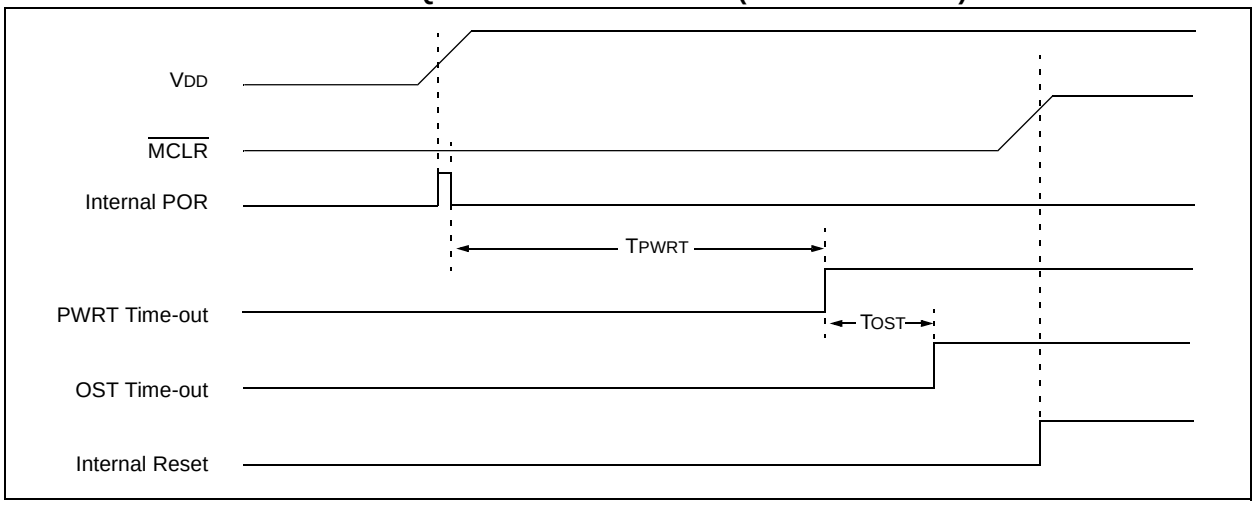

FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)

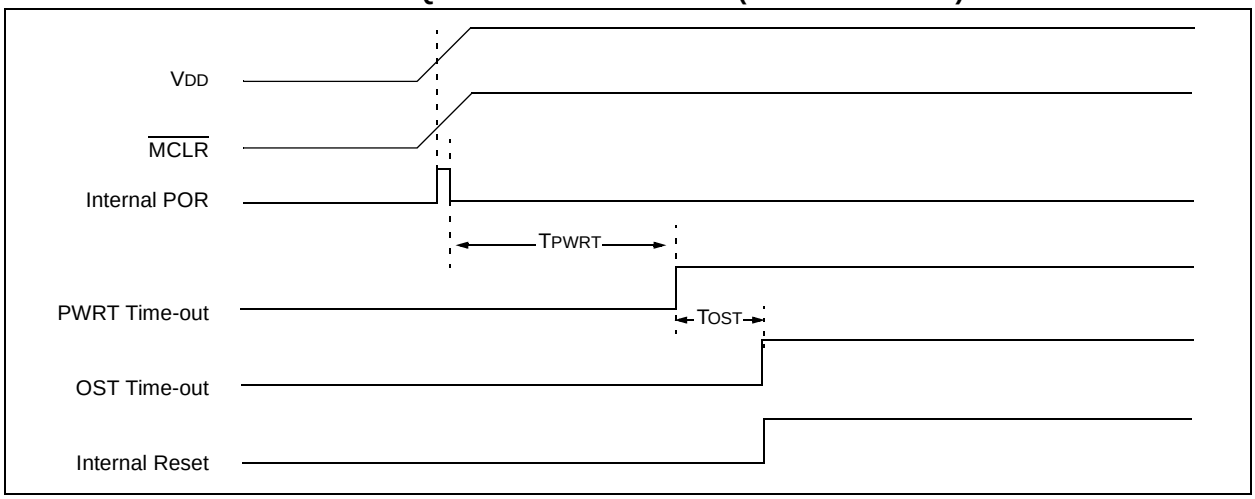

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TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset Wake-up Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Detect(1) Wake-up Reset	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xx00	--00 0000	--uu uu00
PORTC(6)	07h	--xx xx00	--00 0000	--uu uu00
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	0000 00-0	0000 00-0	uuuu uu-u(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
CMCON0	19h	0000 0000	0000 0000	uuuu uuuu
CMCON1	1Ah	---- --10	---- --10	---- --uu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu 1uuu
TRISC(6)	87h	--11 1111	--11 1111	--uu 1uuu
PIE1	8Ch	0000 00-0	0000 00-0	uuuu uu-u
PCON	8Eh	--01 q-qq	--0u u-uu(1,5)	--0u u-uu
OSCCON	8Fh	-110 x000	-110 x000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
WPUDA	95h	--11 -111	--11 -111	uuuu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
WDA	97h	--11 -111	--11 -111	uuuu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu uuuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	---- ----	---- ----	---- ----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000 ----	-000 ----	-uuu ----
LVDCON	94h	--00 -000	--00 -000	--uu -uuu
CRCON	110h	00-- --00	00-- --00	uu-- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: PIC16F636/639 only.

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TABLE 12-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	--01 --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	--0u --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	--0u --uu
WDT Reset	000h	0000 uuuu	--0u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	--uu --uu
Brown-out Detect	000h	0001 1uuu	--01 --10
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	--uu --uu
Wake-up Reset	000h	0001 1xxx	--01 --0x

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and the Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

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12.9 Interrupts

The PIC12F635/PIC16F636/639 has 8 sources of interrupt:

- External Interrupt RA2/INT
- Timer0 Overflow Interrupt
- PORTA Change Interrupts
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Fail-Safe Clock Monitor Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, comparators or data EEPROM modules, refer to the respective peripheral section.

12.9.1 RA2/INT INTERRUPT

External interrupt on RA2/INT pin is edge-triggered; either rising if the INTEDG bit (OPTION<6>) is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See **Section 12.12 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 12-10 for timing of wake-up from Sleep through RA2/INT interrupt.

Note:	The CMCON0 (19h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘`0`’.

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12.9.2 TMR0 INTERRUPT

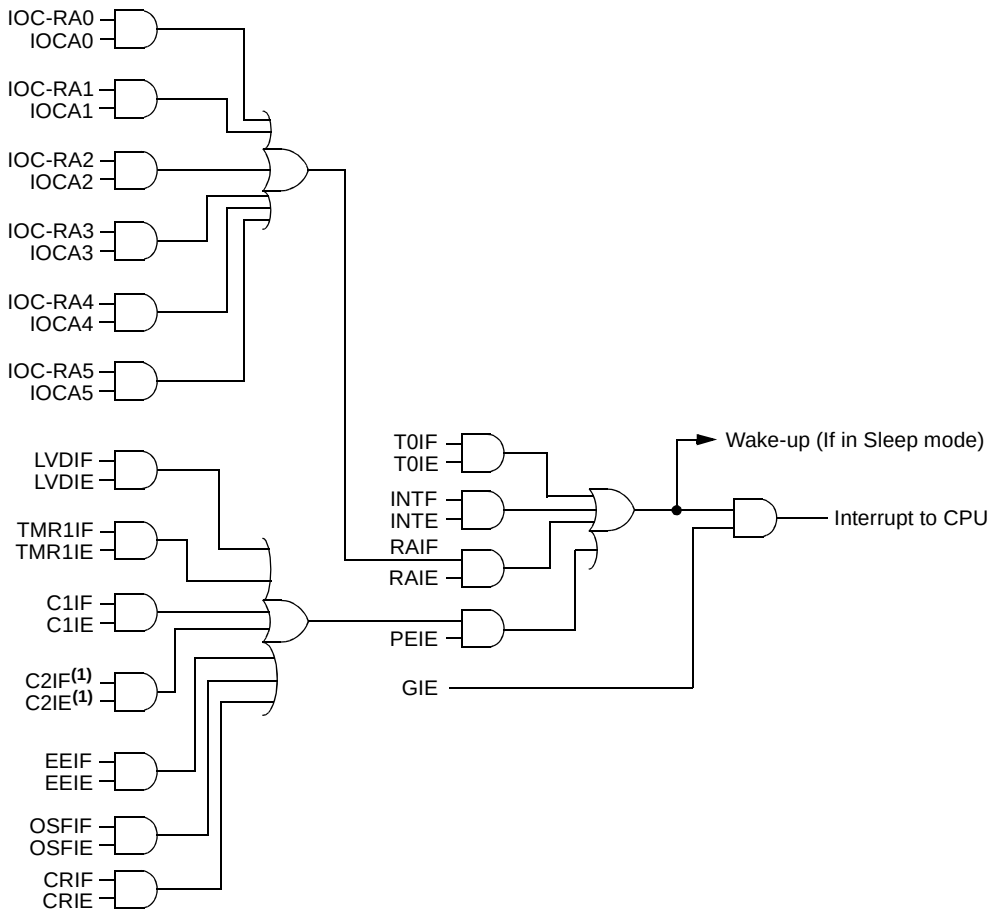
An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. See **Section 5.0 "Timer0 Module"** for operation of the Timer0 module.

12.9.3 PORTA INTERRUPT

An input change on PORTA change sets the RAIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RAIE (INTCON<3>) bit. Plus, individual pins can be configured through the IOCA register.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

FIGURE 12-7: INTERRUPT LOGIC



Note 1: PIC16F636/639 only.

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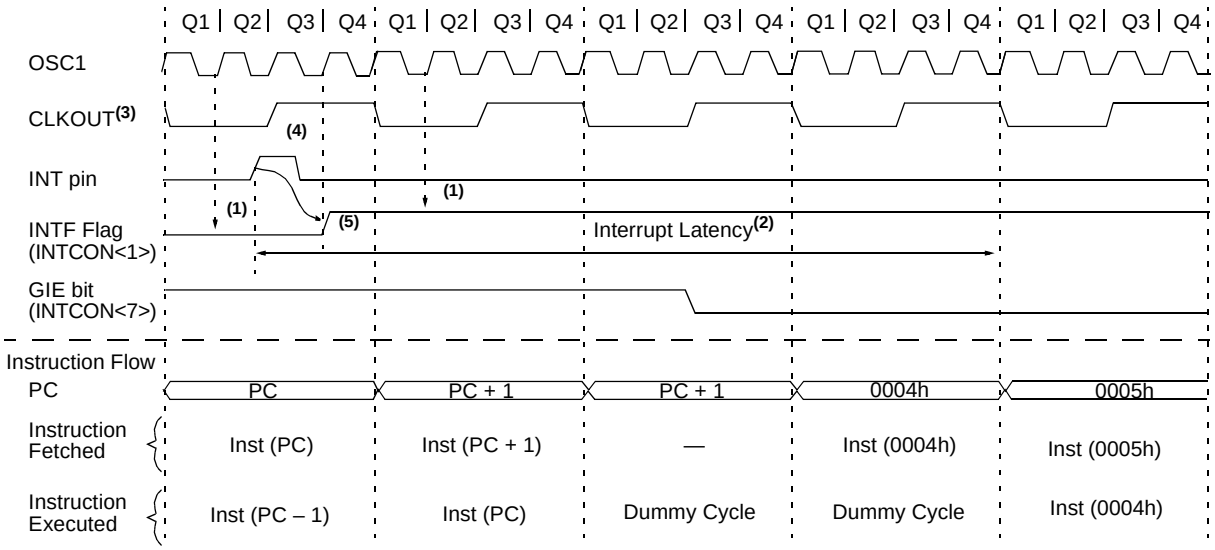
FIGURE 12-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 15.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 12-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD, WUR	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	LVDIF	CRIF	C2IF(1)	C1IF	OSFIF	—	TMR1IF	0000 00-0	0000 00-0
8Ch	PIE1	EEIE	LVDIE	CRIE	C2IE(1)	C1IE	OSFIE	—	TMR1IE	0000 00-0	0000 00-0

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', q = value depends upon condition.
Shaded cells are not used by the interrupt module.

Note 1: PIC16F636/639 only.

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12.10 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and Status registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC12F635/PIC16F636/639 (see Figure 2-2), temporary holding registers, W_TEMP and STATUS_TEMP, should be placed in here. These 16 locations do not require banking and therefore, make it easier to context save and restore. The same code shown in Example 12-1 can be used to:

- Store the W register.
- Store the Status register.
- Execute the ISR code.
- Restore the Status (and Bank Select Bit register).
- Restore the W register.

Note: The PIC12F635/PIC16F636/639 normally does not require saving the PCLATH. However, if computed `GOTO`'s are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
CLRF    STATUS              ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into Status register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

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12.11 Watchdog Timer (WDT)

The PIC12F635/PIC16F636/639 WDT is code and functionally compatible with other PIC16F WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to have a scaler value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 12-7.

12.11.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '`---0 1000`' on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous PIC12F635/PIC16F636/639 microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the INTRC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTRC by 32 to 65536, giving the WDT a nominal range of 1 ms to 268s.

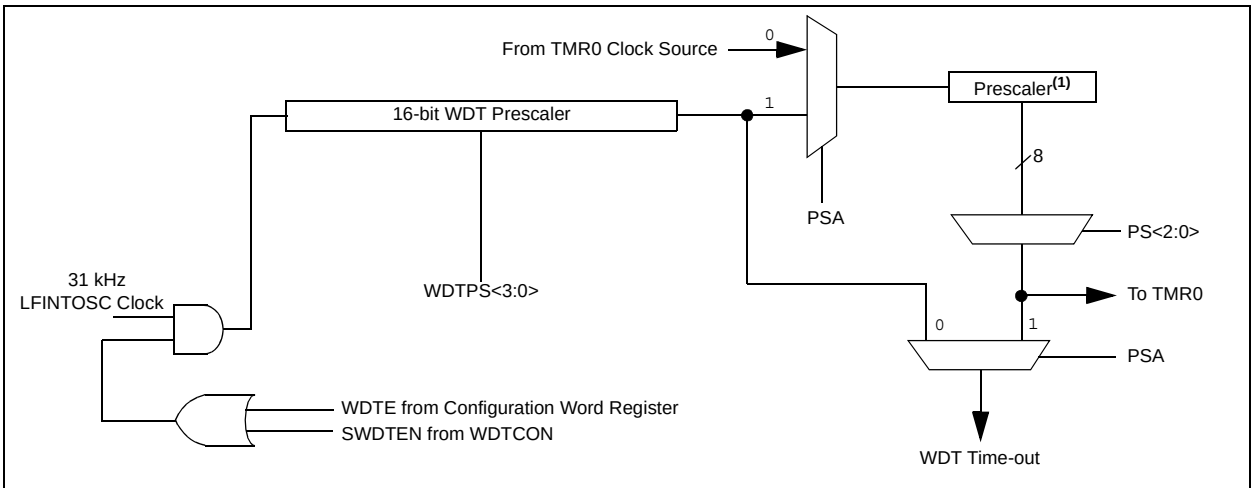
12.11.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit (WDTCON<0>) has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits (OPTION_REG) have the same function as in previous versions of the PIC16F family of microcontrollers. See **Section 5.0 "Timer0 Module"** for more information.

FIGURE 12-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.4 "Prescaler"** for more information.

TABLE 12-7: WDT STATUS

Conditions	WDT
WDTE = `0`	Cleared
`CLRWDT` Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, HFINTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

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REGISTER 12-2: WDTCON – WATCHDOG TIMER CONTROL REGISTER (ADDRESS: 18h)

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN(1)
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32
0001 = 1:64
0010 = 1:128
0011 = 1:256
0100 = 1:512
0101 = 1:1024
0110 = 1:2048
0111 = 1:4096
1000 = 1:8192
1001 = 1:16394
1010 = 1:32768
1011 = 1:65536
1100 = reserved
1101 = reserved
1110 = reserved
1111 = reserved

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit(1)

1 = WDT is turned on
0 = WDT is turned off

Note 1: If WDTE configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 12-8: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
2007h(1)	CONFIG	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of all Configuration Word register bits.

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12.12 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- $\overline{PD}$ bit in the Status register is cleared.
- $\overline{TO}$ bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The $\overline{MCLR}$ pin must be at a logic high level.

Note 1:	It should be noted that a Reset generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.
2:	The Analog Front-End (AFE) section in the PIC16F639 device is independent of the microcontroller's power-down mode (Sleep). See **Section 11.32.2.3 "Sleep Command"** for AFE's Sleep mode.

12.12.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on $\overline{MCLR}$ pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from RA2/INT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the Status register can be used to determine the cause of device Reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when Sleep is invoked. $\overline{TO}$ bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. Special event trigger (Timer1 in Asynchronous mode using an external clock).
3. EEPROM write operation completion.
4. Comparator output changes state.
5. Interrupt-on-change.
6. External Interrupt from INT pin.

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note:	If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

Note:	If WUR is enabled (WURE = 0 in Configuration Word), then the Wake-up Reset module will force a device Reset.

12.12.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the $\overline{TO}$ bit will not be set and the $\overline{PD}$ bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

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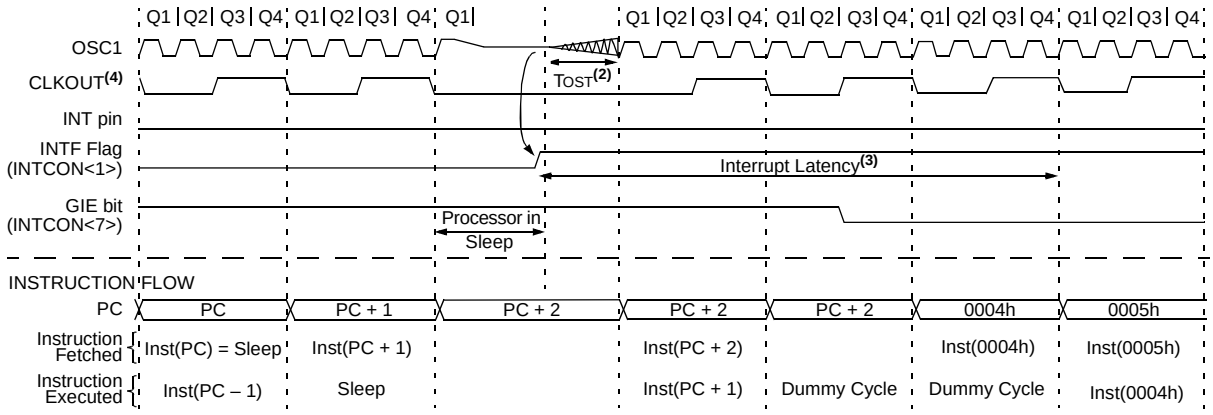
FIGURE 12-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC and RC Oscillator modes.

3: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

12.13 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for more information.

12.14 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

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12.15 In-Circuit Serial Programming

The PIC12F635/PIC16F636/639 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- Power
- Ground
- Programming Voltage

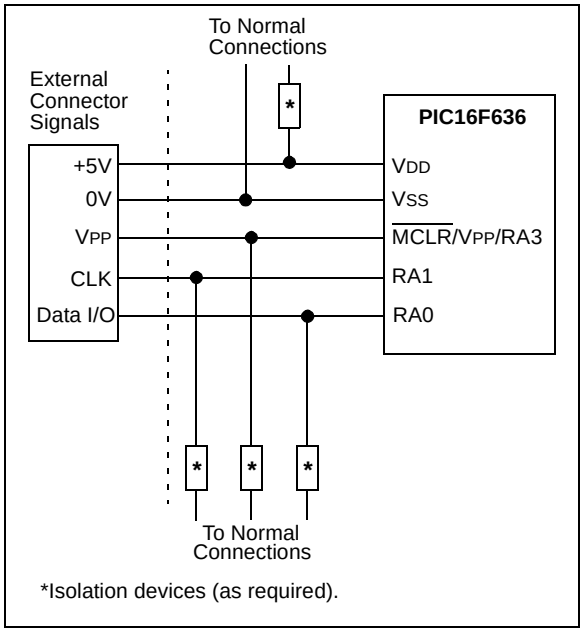
This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the $\overline{\text{MCLR}}$ (V_{PP}) pin from V_{IL} to V_{IHH}. See the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204).

A typical In-Circuit Serial Programming connection is shown in Figure 12-11.

FIGURE 12-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



12.16 In-Circuit Debugger

Since in-circuit debugging requires the loss of clock, data and $\overline{\text{MCLR}}$ pins, MPLAB® ICD 2 development with a 14-pin device is not practical. A special 20-pin PIC16F636 ICD device is used with MPLAB ICD 2 to provide separate clock, data and $\overline{\text{MCLR}}$ pins and frees all normally available pins to the user.

Use of the ICD device requires the purchase of a special header. On the top of the header is an MPLAB ICD 2 connector. On the bottom of the header is a 14-pin socket that plugs into the user's target via the 14-pin stand-off connector.

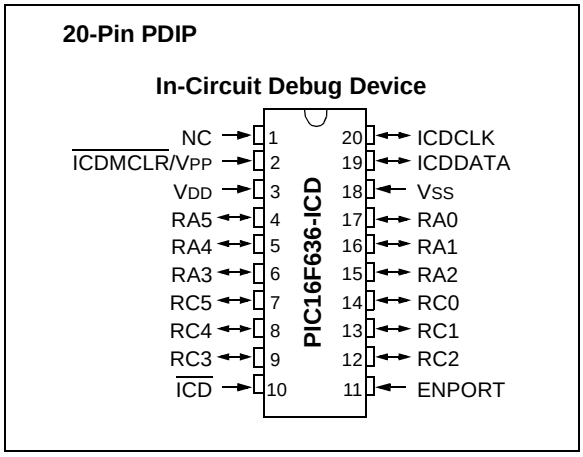
When the $\overline{\text{ICD}}$ pin on the PIC16F636 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger:

TABLE 12-9: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be `NOP` 700h-7FFh

For more information, see the "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 12-12: 20-PIN ICD PINOUT



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NOTES:

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13.0 INSTRUCTION SET SUMMARY

The PIC12F635/PIC16F636/639 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16FXXX instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

Table 13-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with future products, do not use the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

13.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF GPIO instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result of clearing the condition that set the GPIF flag.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13 … 8	7	6 … 0
OPCODE	d	f (FILE #)

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13 … 10	9 … 7	6 … 0
OPCODE	b (BIT #)	f (FILE #)

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13 … 8	7 … 0
OPCODE	k (literal)

k = 8-bit immediate value

CALL and GOTO instructions only

13 … 11	10 … 0
OPCODE	k (literal)

k = 11-bit immediate value

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TABLE 13-2: PIC12F635/PIC16F636/639 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	**1, 2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1, 2**
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	**2**
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1, 2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1, 2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1, 2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1, 2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1, 2**
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1, 2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1, 2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	**1, 2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1, 2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1, 2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1, 2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1, 2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF GPIO, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

Note: Additional information on the mid-range instruction set is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

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13.2 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

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CALL	Call Subroutine
Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits, $\overline{TO}$ and $\overline{PD}$, are set.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register ‘f’ are cleared and the Z bit is set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\bar{f})$ → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘`0`’, the result is stored in W. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) – 1 → (destination)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘`0`’, the result is stored in the W register. If ‘d’ is ‘`0`’, the result is stored back in register ‘f’.

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DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) – 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW	Inclusive OR Literal with W
Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

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MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Encoding:	00 | 1000 | dfff | ffff
Description:	The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register, since status flag Z is affected.
Words:	1
Cycles:	1
Example:	`MOVF FSR, 0` After Instruction W = value in FSR register Z = 1

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	(W) → (f)
Status Affected:	None
Encoding:	00 | 0000 | 1fff | ffff
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	`MOVWF OPTION` Before Instruction OPTION = 0xFF W = 0x4F After Instruction OPTION = 0x4F W = 0x4F

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Encoding:	11 | 00xx | kkkk | kkkk
Description:	The eight-bit literal 'k' is loaded into the W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	`MOVLW 0x5A` After Instruction W = 0x5A

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	00 | 0000 | 0xx0 | 0000
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

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RETFIE — Return from Interrupt

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Encoding:	00 | 0000 | 0000 | 1001
Description:	Return from interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting the Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	`RETFIE`

After Interrupt
PC = TOS
GIE = 1

RETURN — Return from Subroutine

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RETLW — Return with Literal in W

Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	11 | 01xx | kkkk | kkkk
Description:	The W register is loaded with the eight-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

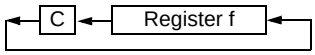
Example:

```
CALL TABLE ;W contains table
           ;offset value
•          ;W now has table value
•
•
TABLE
ADDWF PC   ;W = offset
RETLW k1   ;Begin table
RETLW k2   ;
•
•
•
RETLW kn   ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RLF — Rotate Left f through Carry

Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Encoding:	00 | 1101 | dfff | ffff
Description:	The contents of register ‘f’ are rotated one bit to the left through the CARRY flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



Words:	1
Cycles:	1

Example:

```
RLF     REG1,0
```

Before Instruction
REG1 = 1110 0110
C = 0
After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

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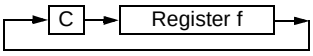
RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the CARRY flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SUBWF	Subtract W from f
Syntax:	[*label*] SUBWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - (W) → (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SLEEP	
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The Power-down Status bit, $\overline{PD}$, is cleared. Time-out Status bit, $\overline{TO}$, is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SWAPF	Swap Nibbles in f
Syntax:	[*label*] SWAPF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

SUBLW	Subtract W from Literal
Syntax:	[*label*] SUBLW k
Operands:	$0 \le k \le 255$
Operation:	k - (W) → (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

XORLW	Exclusive OR Literal with W
Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

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XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘`0`’, the result is stored in the W register. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’.

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14.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM.net™ Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 4 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KEELOQ®
  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - mixed assembly and C
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

14.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

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14.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, timekeeping and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high-level source debugging with the MPLAB IDE.

14.6 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it's object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

14.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high-speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

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14.9 MPLAB ICE 2000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.10 MPLAB ICE 4000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

14.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode.

14.13 MPLAB PM3 Device Programmer

The MPLAB PM3 is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode. MPLAB PM3 connects to the host PC via an RS-232 or USB cable. MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

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14.14 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

14.15 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

14.16 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

14.17 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18, 28 and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs and sample PIC18F452 and PIC16F877 Flash microcontrollers.

14.18 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

14.19 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8, 14 and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low power operation with the supercapacitor circuit and jumpers allow on-board hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2 x 16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

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14.20 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board Flash memory. A generous prototype area is available for user hardware expansion.

14.21 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/Demultiplexed and 16-bit Memory modes. The board includes 2 Mb external Flash memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

14.22 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 Flash microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

14.23 PICkit™ 1 Flash Starter Kit

A complete “development system in a box”, the PICkit Flash Starter Kit includes a convenient multi-section board for programming, evaluation and development of 8/14-pin Flash PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the User’s Guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware “Tips 'n Tricks for 8-pin Flash PIC® Microcontrollers” Handbook and a USB interface cable. Supports all current 8/14-pin Flash PIC microcontrollers, as well as many future planned devices.

14.24 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

14.25 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip’s HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA® development kit
- microID development and rfLab™ development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high-power IR driver, delta sigma ADC and flow rate sensor

Check the Microchip web page and the latest Product Selector Guide for the complete list of demonstration and evaluation kits.

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15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss ..... -0.3V to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS}/V_{SST} pin ..... 300 mA
Maximum current into V_{DD}/V_{DDT} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ± 20 mA
Output clamp current, IOK (V_O < 0 or V_O >V_{DD}) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by PORTA and PORTC (combined) ..... 200 mA
Maximum current sourced PORTA and PORTC (combined) ..... 200 mA
Maximum LC Input Voltage (LCX, LCY, LCZ)(2) loaded, with device ..... 10.0 V_{PP}
Maximum LC Input Voltage (LCX, LCY, LCZ)(2) unloaded, without device ..... 700.0 V_{PP}
Maximum Input Current (rms) into device per LC Channel(2) ..... 10 mA
Human Body ESD rating ..... 4000 (min.) V
Machine Model ESD rating ..... 400 (min.) V

Note 1: Power dissipation for PIC12F635/PIC16F636/639 (AFE section not included) is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.
Power dissipation for AFE section is calculated as follows:
$P_{DIS} = V_{DD} \times I_{ACT} = 3.6V \times 16\ \mu A = 57.6\ \mu W$

2: Specification applies to the PIC16F639 only.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a ‘low’ level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

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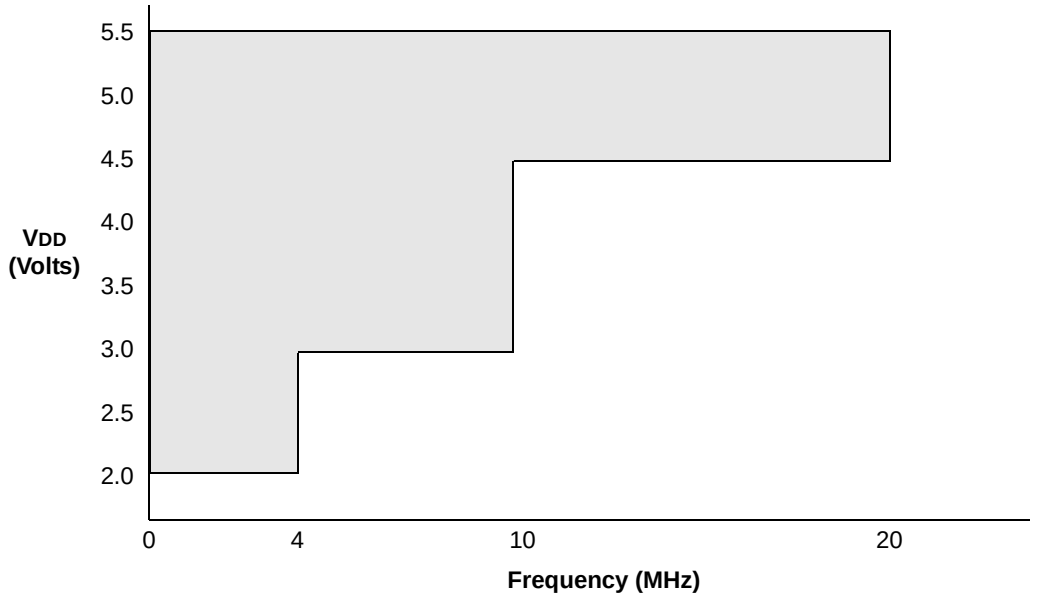
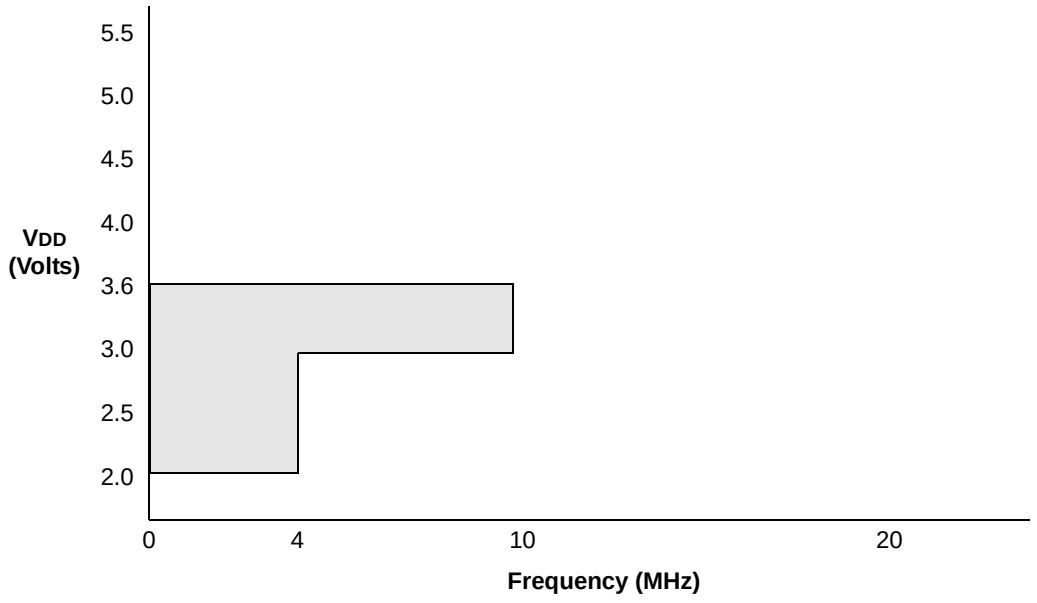
FIGURE 15-1: PIC12F635/PIC16F636 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: PIC16F639 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

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15.1 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001			2.0	—	5.5	V	FOSC < = 4 MHz
D001C			3.0	—	5.5	V	FOSC < = 10 MHz
D001D			4.5	—	5.5	V	FOSC < = 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3 "Power-on Reset"** for details.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 12.3 "Power-on Reset"** for details.
D005	VBOD	**Brown-out Detect**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

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15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current(1,2)**	—	9	TBD	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	TBD	µA	3.0	
			—	35	TBD	µA	5.0	
D011			—	110	TBD	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	190	TBD	µA	3.0	
			—	330	TBD	µA	5.0	
D012			—	220	TBD	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	370	TBD	µA	3.0	
			—	600	TBD	µA	5.0	
D013			—	70	TBD	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	140	TBD	µA	3.0	
			—	260	TBD	µA	5.0	
D014			—	180	TBD	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	320	TBD	µA	3.0	
			—	580	TBD	µA	5.0	
D015			—	TBD	TBD	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	TBD	TBD	µA	3.0	
			—	TBD	TBD	mA	5.0	
D016			—	340	TBD	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	TBD	µA	3.0	
			—	800	TBD	µA	5.0	
D017			—	180	TBD	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	320	TBD	µA	3.0	
			—	580	TBD	µA	5.0	
D018			—	2.1	TBD	mA	4.5	FOSC = 20 MHz HS Oscillator mode
			—	2.4	TBD	mA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.2 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Sym**	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
							VDD	**Note**
D020	IPD	**Power-down Base Current(4)**	—	0.99	TBD	nA	2.0	WDT, BOD, Comparators, VREF and T1OSC disabled
			—	1.2	TBD	nA	3.0	
			—	2.9	TBD	nA	5.0	
D021	ΔIWDT		—	0.3	TBD	μA	2.0	WDT Current(3)
			—	1.8	TBD	μA	3.0	
			—	8.4	TBD	μA	5.0	
D022A	ΔIBOD		—	58	TBD	μA	3.0	BOD Current(3)
			—	109	TBD	μA	5.0	
D022B	ΔILVD		—	TBD	TBD	μA	2.0	PLVD Current
			—	TBD	TBD	μA	3.0	
			—	TBD	TBD	μA	5.0	
D023	ΔICMP		—	3.3	TBD	μA	2.0	Comparator Current(3)
			—	6.1	TBD	μA	3.0	
			—	11.5	TBD	μA	5.0	
D024	ΔIVREF		—	58	TBD	μA	2.0	CVREF Current(3)
			—	85	TBD	μA	3.0	
			—	138	TBD	μA	5.0	
D025	ΔIT1OSC		—	4.0	TBD	μA	2.0	T1OSC Current(3)
			—	4.6	TBD	μA	3.0	
			—	6.0	TBD	μA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.3 DC Characteristics: PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Sym**	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
							VDD	**Note**
D010E	IDD	**Supply Current(1,2)**	—	9	TBD	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	TBD	µA	3.0	
			—	35	TBD	µA	5.0	
D011E			—	110	TBD	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	190	TBD	µA	3.0	
			—	330	TBD	µA	5.0	
D012E			—	220	TBD	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	370	TBD	µA	3.0	
			—	600	TBD	µA	5.0	
D013E			—	70	TBD	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	140	TBD	µA	3.0	
			—	260	TBD	µA	5.0	
D014E			—	180	TBD	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	320	TBD	µA	3.0	
			—	580	TBD	µA	5.0	
D015E			—	TBD	TBD	µA	2.0	FOSC = 31 kHz LFINTOSC
			—	TBD	TBD	µA	3.0	
			—	TBD	TBD	mA	5.0	
D016E			—	340	TBD	µA	2.0	FOSC = 4 MHz IHFINTOSC
			—	500	TBD	µA	3.0	
			—	800	TBD	µA	5.0	
D017E			—	180	TBD	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	320	TBD	µA	3.0	
			—	580	TBD	µA	5.0	
D018E			—	2.1	TBD	mA	4.5	FOSC = 20 MHz HS Oscillator mode
			—	2.4	TBD	mA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.3 DC Characteristics: PIC12F635/PIC16F636-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Sym**	**Device Characteristics**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**	
							VDD	**Note**
D020	IPD	**Power-down Base Current(4)**	—	0.0009	TBD	μA	2.0	WDT, BOD, Comparators, VREF and T1OSC disabled
			—	0.0012	TBD	μA	3.0	
			—	0.0029	TBD	μA	5.0	
D021	ΔIWDT		—	0.3	TBD	μA	2.0	WDT Current(3)
			—	1.8	TBD	μA	3.0	
			—	8.4	TBD	μA	5.0	
D022A	ΔIBOD		—	58	TBD	μA	3.0	BOD Current(3)
			—	109	TBD	μA	5.0	
D022B	ΔILVD		—	TBD	TBD	μA	2.0	PLVD Current
			—	TBD	TBD	μA	3.0	
			—	TBD	TBD	μA	5.0	
D023	ΔICMP		—	3.3	TBD	μA	2.0	Comparator Current(3)
			—	6.1	TBD	μA	3.0	
			—	11.5	TBD	μA	5.0	
D024	ΔIVREF		—	58	TBD	μA	2.0	CVREF Current(3)
			—	85	TBD	μA	3.0	
			—	138	TBD	μA	5.0	
D025	ΔIT1OSC		—	4.0	TBD	μA	2.0	T1OSC Current(3)
			—	4.6	TBD	μA	3.0	
			—	6.0	TBD	μA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.4 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	VSS	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			VSS	—	0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	VSS	—	0.2 VDD	V	Entire range
D032		$\overline{\text{MCLR}}$, OSC1 (RC mode)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)(1)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)(1)	VSS	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25 VDD + 0.8)	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	Entire range
D042		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	**(Note 1)**
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 1)**
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		Analog inputs	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D060B		VREF	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D061		$\overline{\text{MCLR}}$(3)	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070	IPUR	**PORTA Weak Pull-up Current**	50*	250	400*	µA	VDD = 5.0V, VPIN = VSS
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information.

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15.4 DC Characteristics: PIC12F635/PIC16F636-I (Industrial) PIC12F635/PIC16F636-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V (Ind.) IOH = -1.0 mA, VDD = 4.5V (Ext.)
D100	IULP	**Ultra Low-power Wake-up Current**	—	200	—	nA	
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information.

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15.5 DC Characteristics: PIC16F639-I (Industrial), PIC16F639-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0	—	3.6	V	FOSC ≤ 10 MHz
D001A	VDDT	**Supply Voltage (AFE)**	2.0	—	3.6	V	Analog Front-End VDD voltage. Treated as VDD in this document.
D002	VDR	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3 "Power-on Reset"** for details.
D003A	VPORT	**VDD Start Voltage (AFE)** to ensure internal Power-on Reset signal	—	—	1.8	V	Analog Front-End POR voltage.
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 12.3 "Power-on Reset"** for details.
D005	VBOD	**Brown-out Detect**	—	2.1	—	V	
D006	RM	**Turn-on Resistance** or Modulation Transistor	—	—	100	Ohm	VDD = 3.0V
D007	RPU	**Digital Input Pull-Up Resistor** $\overline{CS}$, SCLK	50	200	300	kOhm	VDD = 3.6V
D008	IAIL	**Analog Input Leakage Current** LCX, LCY, LCZ LCCOM	 — —	 — —	 ±1 ±1	 µA µA	 VDD = 3.6V, VSS ≤ VIN ≤ VDD, tested at Sleep mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

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15.6 DC Characteristics: PIC16F639-I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial Supply Voltage 2.0V ≤ VDD ≤ 3.6V					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010	IDD	**Supply Current**(1,2,3)	—	9	TBD	µA	2.0	FOSC = 32.768 kHz LP Oscillator mode
			—	18	TBD	µA	3.0	
D011			—	110	TBD	µA	2.0	FOSC = 1 MHz XT Oscillator mode
			—	190	TBD	µA	3.0	
D012			—	220	TBD	µA	2.0	FOSC = 4 MHz XT Oscillator mode
			—	370	TBD	µA	3.0	
D013			—	70	TBD	µA	2.0	FOSC = 1 MHz EC Oscillator mode
			—	140	TBD	µA	3.0	
D014			—	180	TBD	µA	2.0	FOSC = 4 MHz EC Oscillator mode
			—	320	TBD	µA	3.0	
D015			—	TBD	TBD	µA	2.0	FOSC = 31 kHz LFINTOSC mode
			—	TBD	TBD	µA	3.0	
D016			—	340	TBD	µA	2.0	FOSC = 4 MHz HFINTOSC mode
			—	500	TBD	µA	3.0	
D017			—	180	TBD	µA	2.0	FOSC = 4 MHz EXTRC mode
			—	320	TBD	µA	3.0	
D020	IPD	**Power-down Base Current**(4)	—	0.99	TBD	nA	2.0	WDT, BOD, Comparators, VREF and T1OSC disabled (excludes AFE)
			—	1.2	TBD	nA	3.0	
D021	ΔIWDT		—	0.3	TBD	µA	2.0	WDT Current(3)
			—	1.8	TBD	µA	3.0	
D022A	ΔIBOD		—	58	TBD	µA	3.0	BOD Current(3)
D022B	ΔILVD		—	TBD	TBD	µA	2.0	PLVD Current
			—	TBD	TBD	µA	3.0	
D023	ΔICMP		—	3.3	TBD	µA	2.0	Comparator Current(3)
			—	6.1	TBD	µA	3.0	
D024	ΔIVREF		—	58	TBD	µA	2.0	CVREF Current(3)
			—	85	TBD	µA	3.0	
D025	ΔIT1OSC		—	4.0	TBD	µA	2.0	T1OSC Current(3)
			—	4.6	TBD	µA	3.0	
D026	IACT	**Active Current** of AFE only (receiving signal) 1 LC Input Channel Signal 3 LC Input Channel Signals	 — —	 10 —	 — 16	 µA µA	 3.6 3.6	$\overline{CS}$ = VDD; Input = Continuous Wave (CW); Amplitude = 300 mVPP. All channels enabled.
D027	ISTDBY	**Standby Current** of AFE only (not receiving signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	 — — —	 3 4 5	 5 6 7	 µA µA µA	 3.6 3.6 3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD
D028	ISLEEP	**Sleep Current** of AFE only	—	0.2	1	µA	3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD

Legend: TBD = To Be Determined
† Data in 'Typ' column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled. MCU only, Analog Front-End not included.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. MCU only, Analog Front-End not included.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.7 DC Characteristics: PIC16F639-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended Supply Voltage 2.0V ≤ VDD ≤ 3.6V					
Param No.	Sym	Device Characteristics	Min	Typ†	Max	Units	Conditions	
							VDD	Note
D010E	IDD	**Supply Current**(1,2)	—	9	TBD	μA	2.0	
			—	18	TBD	μA	3.0	
D011E			—	110	TBD	μA	2.0	
			—	190	TBD	μA	3.0	
D012E			—	220	TBD	μA	2.0	
			—	370	TBD	μA	3.0	
D013E			—	70	TBD	μA	2.0	
			—	140	TBD	μA	3.0	
D014E			—	180	TBD	μA	2.0	
			—	320	TBD	μA	3.0	
D015E			—	TBD	TBD	μA	2.0	
			—	TBD	TBD	μA	3.0	
D016E			—	340	TBD	μA	2.0	
			—	500	TBD	μA	3.0	
D017E			—	180	TBD	μA	2.0	
			—	320	TBD	μA	3.0	
D020	IPD	**Power-down Base Current**(4)	—	0.99	TBD	nA	2.0	WDT, BOD, Comparators, VREF and T1OSC disabled (excludes AFE)
			—	1.2	TBD	nA	3.0	
D021	ΔIWDT		—	0.3	TBD	μA	2.0	WDT Current(3)
			—	1.8	TBD	μA	3.0	
D022A	ΔIBOD		—	58	TBD	μA	3.0	BOD Current(3)
D022B	ΔILVD		—	TBD	TBD	μA	2.0	PLVD Current
			—	TBD	TBD	μA	3.0	
D023	ΔICMP		—	3.3	TBD	μA	2.0	Comparator Current(3)
			—	6.1	TBD	μA	3.0	
D024	ΔIVREF		—	58	TBD	μA	2.0	CVREF Current(3)
			—	85	TBD	μA	3.0	
D025	ΔIT1OSC		—	4.0	TBD	μA	2.0	T1OSC Current(3)
			—	4.6	TBD	μA	3.0	
D026	IACT	**Active Current** of AFE only (receiving signal) 1 LC Input Channel Signal 3 LC Input Channel Signals	 — —	 10 —	 — 16	 μA μA	 3.6 3.6	$\overline{CS}$ = VDD; Input = Continuous Wave (CW); Amplitude = 300 mVPP. All channels enabled.
D027	ISTDBY	**Standby Current** of AFE only (not receiving signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	 — — —	 3 4 5	 5 6 7	 μA μA μA	 3.6 3.6 3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD
D028	ISLEEP	**Sleep Current** of AFE only	—	0.2	1	μA	3.6	$\overline{CS}$ = VDD; $\overline{ALERT}$ = VDD

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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15.8 DC Characteristics: PIC16F639-I (Industrial), PIC16F639-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer					
D030A			VSS	—	0.15 VDD	V	
D031		with Schmitt Trigger buffer	VSS	—	0.2 VDD	V	
D032		$\overline{\text{MCLR}}$, OSC1 (RC mode)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)(1)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)(1)	VSS	—	0.3 VDD	V	
D034		**Digital Input Low Voltage**	VSS	—	0.3 VDD	V	Analog Front-End section
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer					
D040A			(0.25 VDD + 0.8)	—	VDD	V	
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	
D042		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	**(Note 1)**
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	**(Note 1)**
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	
		Digital Input High Voltage					Analog Front-End section
D044		SCLK, $\overline{\text{CS}}$, SDIO for Analog Front-End (AFE)	0.7 VDD	—	VDD	V	
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		Analog inputs	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D060B		VREF	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD
D061		$\overline{\text{MCLR}}$(3)	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
		Digital Input Leakage Current(2)					VDD = 3.6V, Analog Front-End section
D064		SDI for Analog Front-End (AFE)	—	—	± 1	µA	VSS ≤ VPIN ≤ VDD
D064A		SCLK, $\overline{\text{CS}}$ for Analog Front-End (AFE)	—	—	± 1	µA	VPIN ≤ VDD
D070	IPUR	**PORTA Weak Pull-up Current**	50*	250	400*	µA	VDD = 3.6V, VPIN = VSS
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 3.6V (Ind.)
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 3.6V (Ind.) IOL = 1.2 mA, VDD = 3.6V (Ext.)
		Digital Output Low Voltage					Analog Front-End section
D084		$\overline{\text{ALERT}}$, LFDATA/SDIO for Analog Front-End (AFE)	—	—	VSS + 0.4	V	IOL = 1.0 mA, VDD = 2.0V

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

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15.8 DC Characteristics: PIC16F639-I (Industrial), PIC16F639-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Supply Voltage 2.0V ≤ VDD ≤ 3.6V				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 3.6V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 3.6V (Ind.) IOH = -1.0 mA, VDD = 3.6V (Ext.)
		Digital Output High Voltage					Analog Front-End (AFE) section
D093		LFDATA/SDIO for Analog Front-End (AFE)	VDD – 0.5	—	—	V	IOH = -400 µA, VDD = 2.0V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D102	IULP	**Ultra Low-power Wake-up Current**	—	200	—	nA	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(1)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 9.4.1 "Using the Data EEPROM"** for additional information

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15.9 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

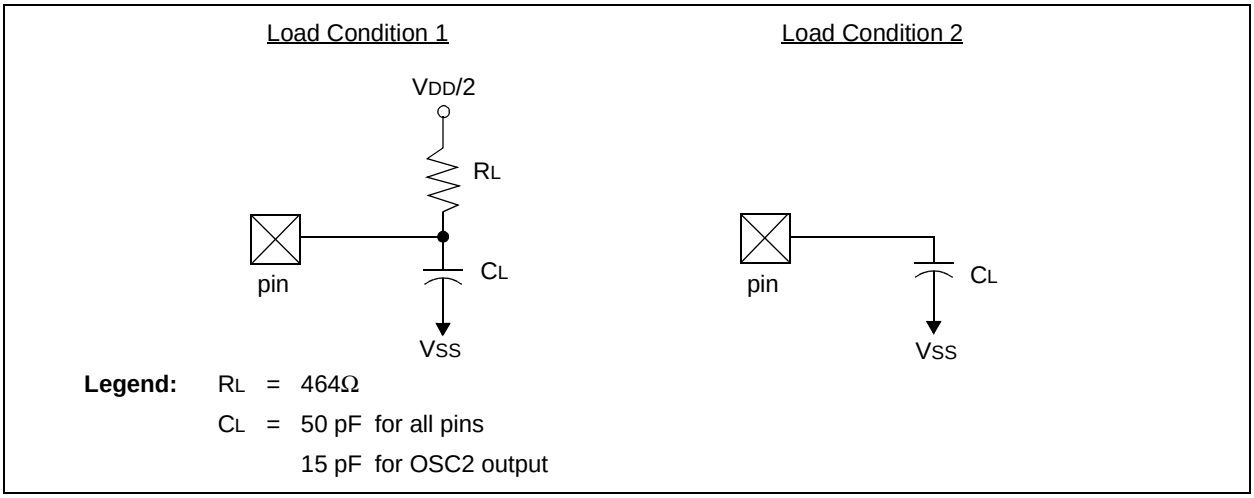
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCLK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 15-3: LOAD CONDITIONS



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15.10 AC Characteristics: PIC12F635/PIC16F636/639 (Industrial, Extended)

FIGURE 15-4: EXTERNAL CLOCK TIMING

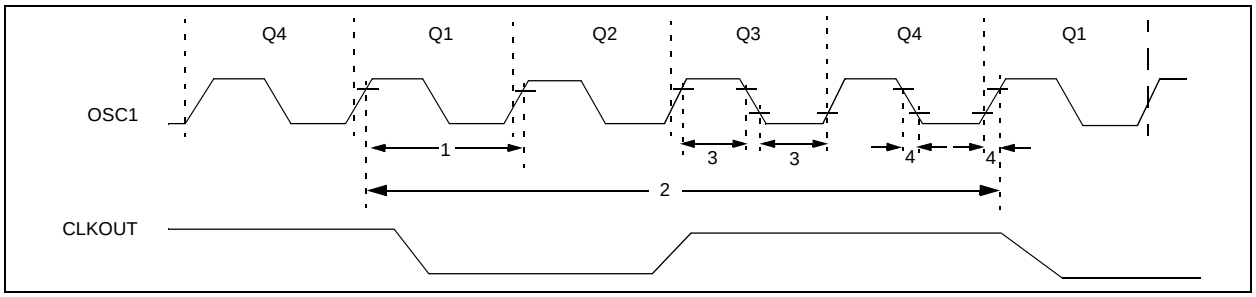

TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency(1)	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency(1)	5	—	37	kHz	LP Oscillator mode
			—	—	—	MHz	HFINTOSC Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
1	TOSC	External CLKIN Period(1)	27	—	—	µs	LP Oscillator mode
			50	—	—	ns	HS Oscillator mode
			50	—	—	ns	EC Oscillator mode
			250	—	—	ns	XT Oscillator mode
		Oscillator Period(1)	27		200	µs	LP Oscillator mode
			—	125	—	ns	INTOSC Oscillator mode
			250	—	—	ns	RC Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	External CLKIN (OSC1) High External CLKIN Low	2*	—	—	µs	LP oscillator, TOSC L/H duty cycle
			20*	—	—	ns	HS oscillator, TOSC L/H duty cycle
			100*	—	—	ns	XT oscillator, TOSC L/H duty cycle
4	TosR, TosF	External CLKIN Rise External CLKIN Fall	—	—	50*	ns	LP oscillator
			—	—	25*	ns	XT oscillator
			—	—	15*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

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TABLE 15-2: PRECISION INTERNAL OSCILLATOR PARAMETERS

Param No.	Sym	Characteristic	Freq Tolerance	Min	Typ†	Max	Units	Conditions
F10	FOSC	Internal Calibrated INTOSC Frequency(1) HFINTOSC	±1%	—	8.00	TBD	MHz	VDD and Temperature (TBD)
			±2%	—	8.00	TBD	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			±5%	—	8.00	TBD	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)
F14	TIOSCST	Oscillator Wake-up from Sleep Start-up Time*	—	—	TBD	TBD	µs	VDD = 2.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 3.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 5.0V, -40°C to +85°C

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 15-5: CLKOUT AND I/O TIMING

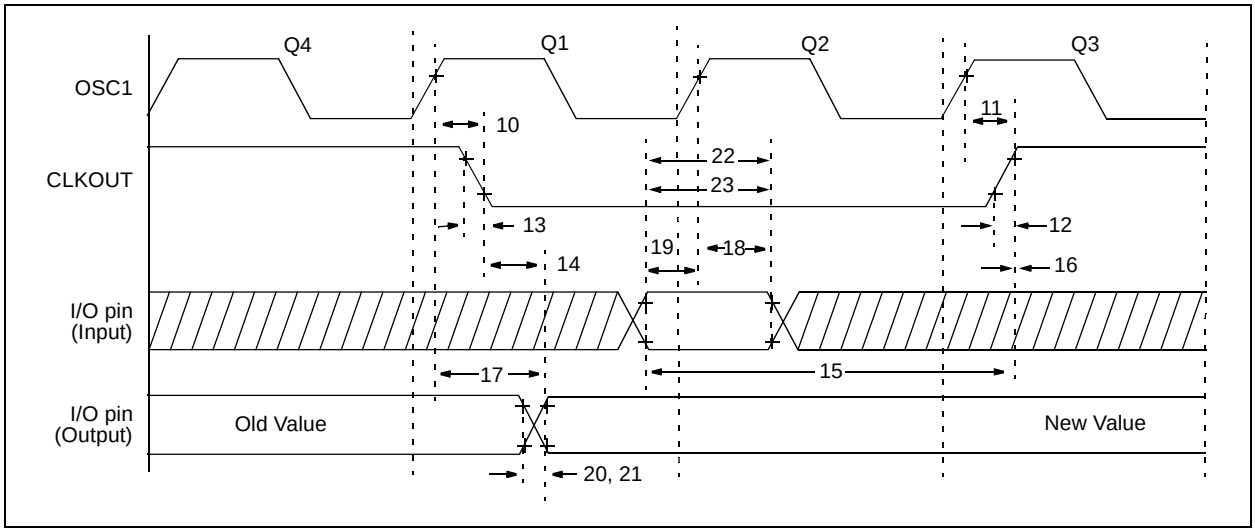

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TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TOSH2CKL	OSC1↑ to CLKOUT↓	—	75	200	ns	**(Note 1)**
11	TOSH2CKH	OSC1↑ to CLKOUT↑	—	75	200	ns	**(Note 1)**
12	TCKR	CLKOUT Rise Time	—	35	100	ns	**(Note 1)**
13	TCKF	CLKOUT Fall Time	—	35	100	ns	**(Note 1)**
14	TCKL2IOV	CLKOUT↓ to Port Out Valid	—	—	20	ns	**(Note 1)**
15	TIOV2CKH	Port In Valid before CLKOUT↑	TOSC + 200 ns	—	—	ns	**(Note 1)**
16	TCKH2IOI	Port In Hold after CLKOUT↑	0	—	—	ns	**(Note 1)**
17	TOSH2IOV	OSC1↑ (Q1 cycle) to Port Out Valid	—	50	150*	ns	
			—	—	300	ns	
18	TOSH2IOI	OSC1↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	100	—	—	ns	
19	TIOV2OSH	Port Input Valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TIOR	Port Output Rise Time	—	10	40	ns	
21	TIOF	Port Output Fall Time	—	10	40	ns	
22	TINP	INT pin High or Low Time	25	—	—	ns	
23	TRBP	PORTA Change INT High or Low Time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

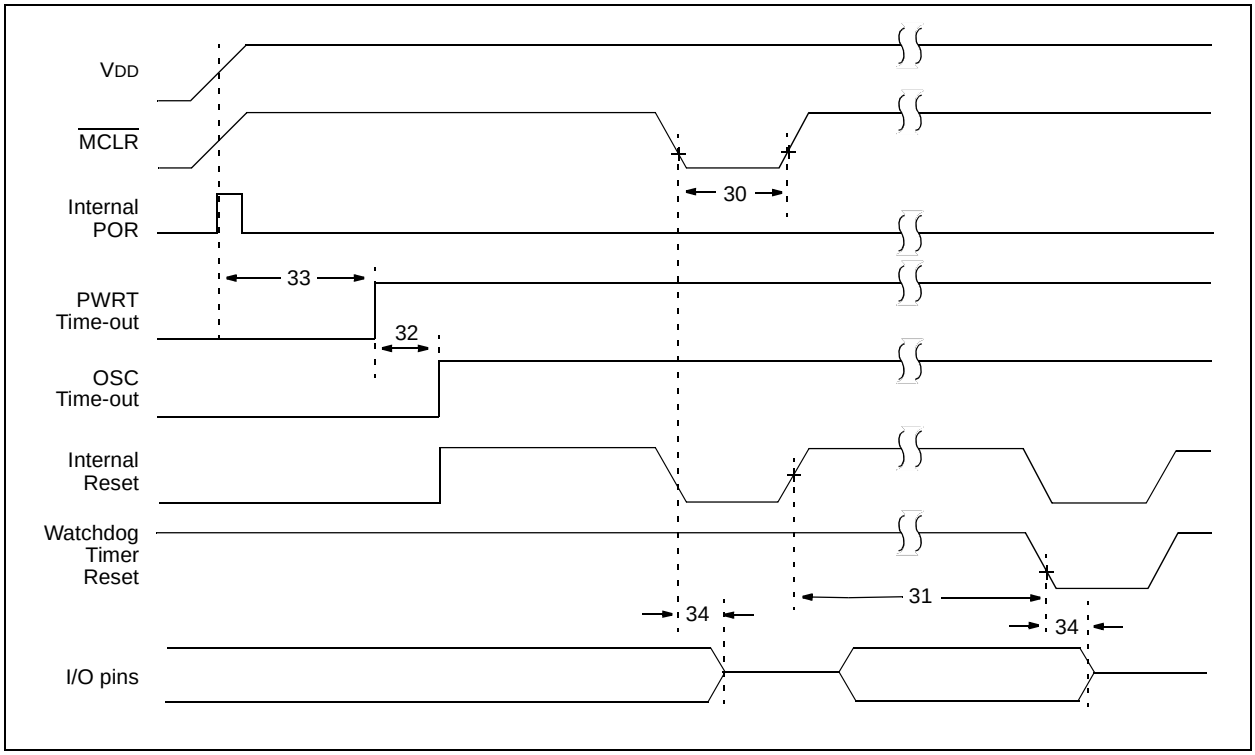

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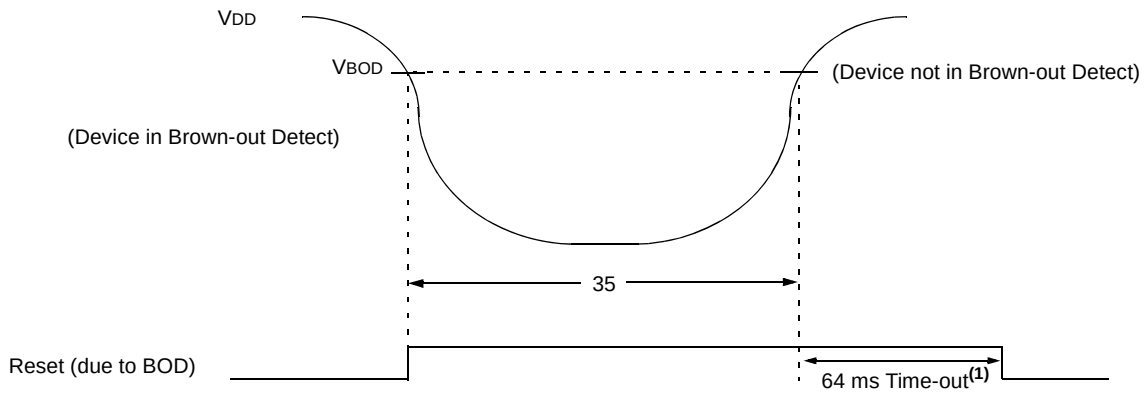
FIGURE 15-7: BROWN-OUT DETECT TIMING AND CHARACTERISTICS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in Configuration Word register is programmed to '0'.

TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2 11	— 18	— 24	µs ms	VDD = 5.0V, -40°C to +85°C Extended temperature
31	TWDT	Watchdog Timer Time-out Period (no prescaler)	10 10	17 17	25 30	ms ms	VDD = 5.0V, -40°C to +85°C Extended temperature
32	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	64 TBD	132* TBD	ms ms	VDD = 5.0V, -40°C to +85°C Extended Temperature
34	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	VBOD	Brown-out Detect Voltage	2.025	—	2.175	V	
36	TBOD	Brown-out Detect Pulse Width	100*	—	—	µs	VDD ≤ VBOD (D005)

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 15-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

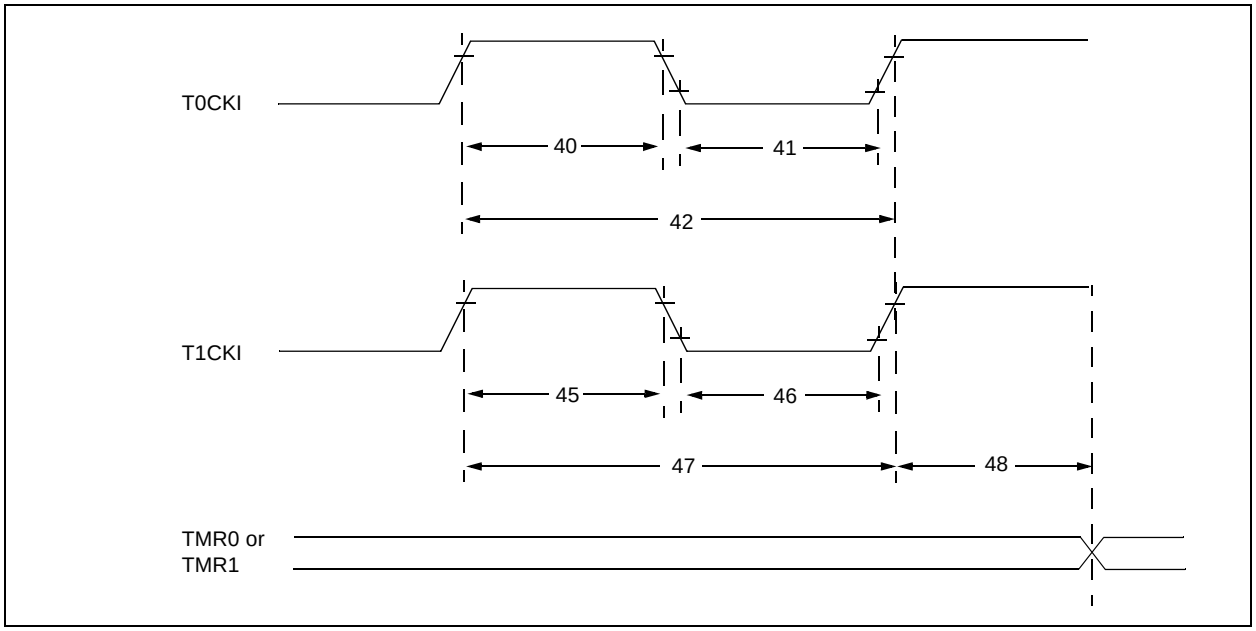

TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4,..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		DC	—	200*	kHz	
49	TCKEZTMR1	Delay from External Clock Edge to Timer increment		2 TOSC*	—	7 TOSC*	—	

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 15-6: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Sym	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VOS	Input Offset Voltage	—	±5.0	±10	mV	
VCM	Input Common Mode Voltage	0	—	VDD – 1.5	V	
CMRR	Common Mode Rejection Ratio	+55*	—	—	db	
TRT	Response Time(1)	—	150	400*	ns	
TMC2COV	Comparator Mode Change to Output Valid	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2 while the other input transitions from VSS to VDD – 1.5V.

TABLE 15-7: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
Sym.	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low range (VRR = 1) High range (VRR = 0)
	Absolute Accuracy	— —	— —	±1/4* ±1/2*	LSb LSb	Low range (VRR = 1) High range (VRR = 0)
	Unit Resistor Value (R)	—	2K*	—	Ω	
	Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

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15.11 AC Characteristics: Analog Front-End for PIC16F639 (industrial, extended)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial -40°C ≤ TAMB ≤ +125°C for extended LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param No.	**Sym.**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VSENSE	LC Input Sensitivity	1	3.0	6	mVPP	VDD = 3.0V Output enable filter disabled AGCSIG = 0; MODMIN = 00 (50% modulation depth setting) Input = Continuous Wave (CW) Output = Logic level transition from low-to-high at sensitivity level for CW input.
	VDE_Q	Coil de-Q'ing Voltage - RF Limiter (RFLM) must be active	3	—	5	V	VDD = 3.0V, Force IIN = 5 µA
	RFLM	RF Limiter Turn-on Resistance (LCX, LCY, LCZ)	—	—	700	Ohm	VDD = 2.0V, VIN = 8 VDC
	SADJ	Sensitivity Reduction	— —	0 -30	— —	dB dB	VDD = 3.0V No sensitivity reduction selected Max reduction selected Monotonic increment in attenuation value from setting = 0000 to 1111 by design
	VIN_MOD	Minimum Modulation Depth 75% ± 12% 50% ± 12% 25% ± 12% 12% ± 12%	 63 38 13 0	 75 50 25 12	 87 62 37 24	 % % % %	VDD = 3.0V
	CTUNX	LCX Tuning Capacitor	— 44.1	0 63	— 81.9	pF pF	VDD = 3.0V, Config. Reg. 1, bits <6:1> Setting = 000000 63 pF +/- 30% Config. Reg. 1, bits <6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
	CTUNY	LCY Tuning Capacitor	— 44.1	0 63	— 81.9	pF pF	VDD = 3.0V, Config. Reg. 2, bits <6:1> Setting = 000000 63 pF +/- 30% Config. Reg. 2, bits <6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
	FCARRIER	Carrier frequency	—	125	—	kHz	Characterized at bench.
	FMOD	Input modulation frequency	—	—	4	kHz	Input data rate, characterized at bench.

* Parameter is characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays = **TOEH** - TDR + TDF
2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF)

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15.11 AC Characteristics: Analog Front-End for PIC16F639 (industrial, extended) (Continued)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial -40°C ≤ TAMB ≤ +125°C for extended LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param No.	**Sym.**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	CTUNZ	LCZ Tuning Capacitor	—	0	—	pF	VDD = 3.0V, Config. Reg. 3, bits<6:1> Setting = 000000
			44.1	63	81.9	pF	63 pF +/- 30% Config. Reg. 3, bits<6:1> Setting = 111111 63 steps, 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
	C_Q	Q of Trimming Capacitors	50*	—	—	pF	Characterized at bench test
	TDR	Demodulator Charge Time (delay time of demodulated output to rise)	—	50	—	µs	VDD = 3.0V MOD depth setting = 50% Input conditions: Amplitude = 300 mVPP Modulation depth = 80%
	TDF	Demodulator Discharge Time (delay time of demodulated output to fall)	—	50	—	µs	VDD = 3.0V MOD depth setting = 50% Input conditions: Amplitude = 300 mVPP Modulation depth = 80%
	TLFDATAR	Rise time of LFDATA	—	0.5	—	µs	VDD = 3.0V Time is measured from 10% to 90% of amplitude
	TLFDATAF	Fall time of LFDATA	—	0.5	—	µs	VDD = 3.0V Time is measured from 10% to 90% of amplitude
	TAGC	AGC stabilization time	—	3.5*	—	ms	Time required for AGC stabilization
	TPAGC	High time after AGC settling time	—	62.5	—	µs	Equivalent to two Internal clock cycle (FOSC)
	TSTAB	AGC stabilization time plus high time (after AGC settling time) (TAGC + TPAGC)	4	—	—	ms	AGC stabilization time
	TGAP	Gap time after AGC settling time	200	—	—	µs	Typically 1 TE
	TRDY	Time from exiting Sleep or POR to being ready to receive signal	—	—	50*	ms	
	TPRES	Minimum time AGC level must be held after receiving AGC Preserve command	5*	—	—	ms	AGC level must not change more than 10% during TPRES.
	FOSC	Internal RC oscillator frequency (±10%)	28.8	32	35.2	kHz	Internal clock trimmed at 32 kHz during test
	TINACT	Inactivity timer time-out	14.4	16	17.6	ms	512 cycles of RC oscillator @ FOSC
	TALARM	Alarm timer time-out	28.8	32	35.2	ms	1024 cycles of RC oscillator @ FOSC
	RLC	**LC Pin Input Impedance** LCX, LCY, LCZ	—	1*	—	MOhm	Device in Standby mode

* Parameter is characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays = **TOEH** - TDR + TDF
2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF)

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15.11 AC Characteristics: Analog Front-End for PIC16F639 (industrial, extended) (Continued)

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage: 2.0V ≤ VDD ≤ 3.6V Operating temperature: -40°C ≤ TAMB ≤ +85°C for industrial; -40°C ≤ TAMB ≤ +125°C for extended LC Signal Input: Sinusoidal 300 mVPP Carrier Frequency: 125 kHz LCCOM connected to VSS				
Param No.	**Sym.**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	TE	Time element of pulse	200	—	—	µs	
	TOEH	Minimum output enable filter high time **OEH (Bits Config0<7:6>)** 01 = 1 ms 10 = 2 ms 11 = 4 ms 00 = Filter Disabled	 32 (~1ms) 64 (~2ms) 128 (~ms) —	 — — — —	 — — — —	 clock count	RC oscillator = FOSC Viewed from the pin input: **(Note 1)**
	TOEL	Minimum output enable filter low time **OEL (Bits Config0<5:4>)** 00 = 1 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms	 32 (~1ms) 32 (~1ms) 64 (~2ms) 128 (~4ms)	 — — — —	 — — — —	 clock count	RC oscillator = FOSC Viewed from the pin input: **(Note 2)**
	TOET	Maximum output enable filter period **OEH OEL TOEH TOEL** 01 00 = 1 ms 1 ms 01 01 = 1 ms 1 ms 01 10 = 1 ms 2 ms 01 11 = 1 ms 4 ms 10 00 = 2 ms 1 ms 10 01 = 2 ms 1 ms 10 10 = 2 ms 2 ms 10 11 = 2 ms 4 ms 11 00 = 4 ms 1 ms 11 01 = 4 ms 1 ms 11 10 = 4 ms 2 ms 11 11 = 4 ms 4 ms 00 XX = Filter Disabled	 — — — — — — — — — — — — —	 — — — — — — — — — — — — —	 96 (~3ms) 96 (~3ms) 128 (~4ms) 192 (~6ms) 128 (~4ms) 128 (~4ms) 160 (~5ms) 250 (~8ms) 192 (~6ms) 192 (~6ms) 256 (~8ms) 320 (~10ms) —	 clock count	RC oscillator = FOSC LFDATA output appears as long as input signal level is greater than VSENSE.
	IRSSI	RSSI current output	— — — —	100 1 10 100	— — — —	µA µA µA µA	VDD = 3.0V, VIN = 0 to 4 VPP Linearly increases with input signal amplitude. Tested at VIN = 40 mVPP, 400 mVPP, and 4 VPP VIN = 40 mVPP VIN = 400 mVPP VIN = 4 VPP
	IRSSILR	RSSI current linearity	—	TBD	—	—	

* Parameter is characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
Note 1: Required output enable filter high time must account for input path analog delays = **TOEH** - TDR + TDF
2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF)

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15.12 SPI Timing: Analog Front-End (AFE) for PIC16F639

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Supply Voltage 2.0V ≤ VDD ≤ 3.6V Operating temperature -40°C ≤ TAMB ≤ +85°C for industrial -40°C ≤ TAMB ≤ +125°C for extended LC Signal Input Sinusoidal 300 mVPP Carrier Frequency 125 kHz LCCOM connected to VSS				
Param	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	FSCLK	SCLK Frequency	—	—	3	MHz	
	Tcssc	$\overline{CS}$ fall to first SCLK edge setup time	100	—	—	ns	
	TSU	SDI setup time	30	—	—	ns	
	THD	SDI hold time	50	—	—	ns	
	THI	SCLK high time	150	—	—	ns	
	TLO	SCLK low time	150	—	—	ns	
	TDO	SDO setup time	—	—	150	ns	
	TSCCS	SCLK last edge to $\overline{CS}$ rise setup time	100	—	—	ns	
	TCSH	$\overline{CS}$ high time	500	—	—	ns	
	TCS1	$\overline{CS}$ rise to SCLK edge setup time	50	—	—	ns	
	TCS0	SCLK edge to $\overline{CS}$ fall setup time	50	—	—	ns	SCLK edge when $\overline{CS}$ is high
	TSPIR	Rise time of SPI data (SPI Read command)	—	10	—	ns	VDD = 3.0V. Time is measured from 10% to 90% of amplitude
	TSPIF	Fall time of SPI data (SPI Read command)	—	10	—	ns	VDD = 3.0V. Time is measured from 90% to 10% of amplitude

* Parameter is characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays = **TOEH** - TDR + TDF

2: Required output enable filter low time must account for input path analog delays (= **TOEL** + TDR - TDF)

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16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs and Tables are not available at this time.

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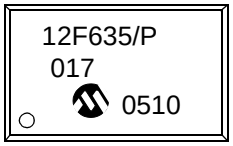
17.0 PACKAGING INFORMATION

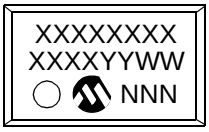
17.1 Package Marking Information

8-Lead PDIP

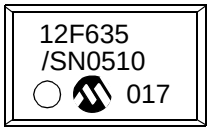
Example



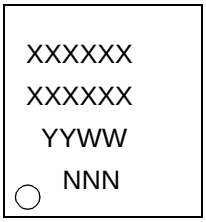
8-Lead SOIC



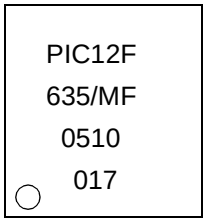
Example



8-Lead DFN-S

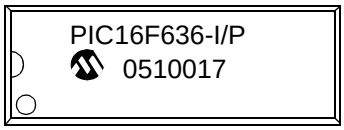


Example



14-Lead PDIP

Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

* Standard PICmicro device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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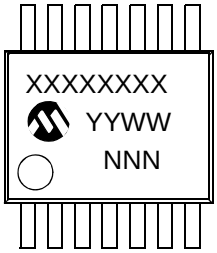
17.1 Package Marking Information (Continued)

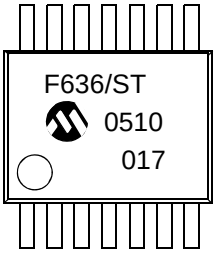
14-Lead SOIC

Example

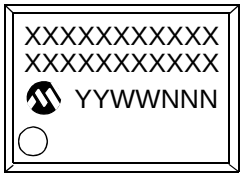
14-Lead TSSOP



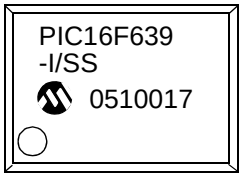
Example



20-Lead SSOP



Example



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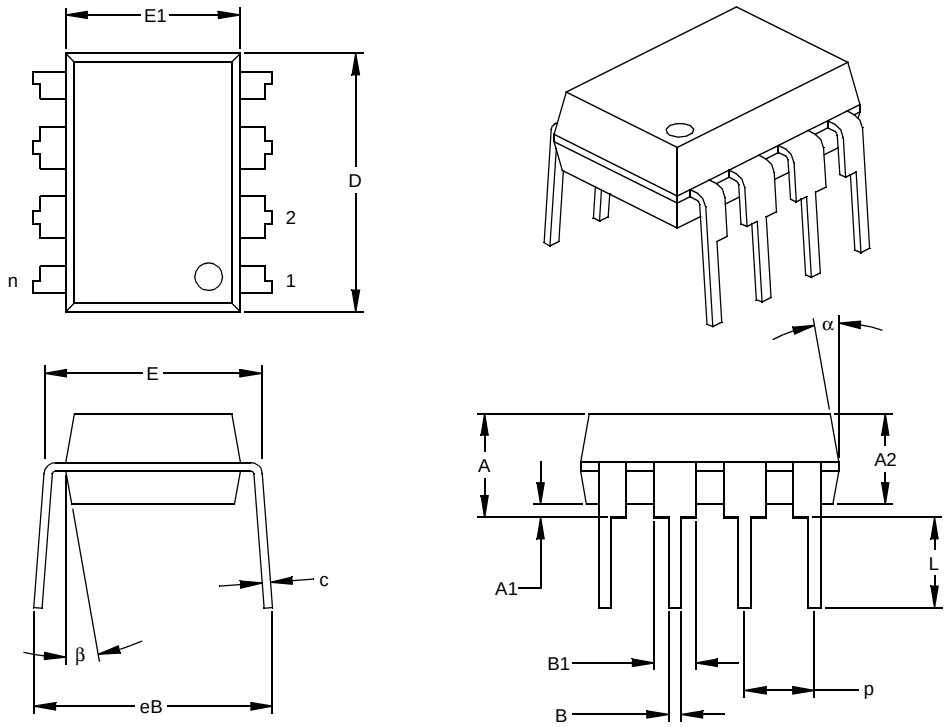
17.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

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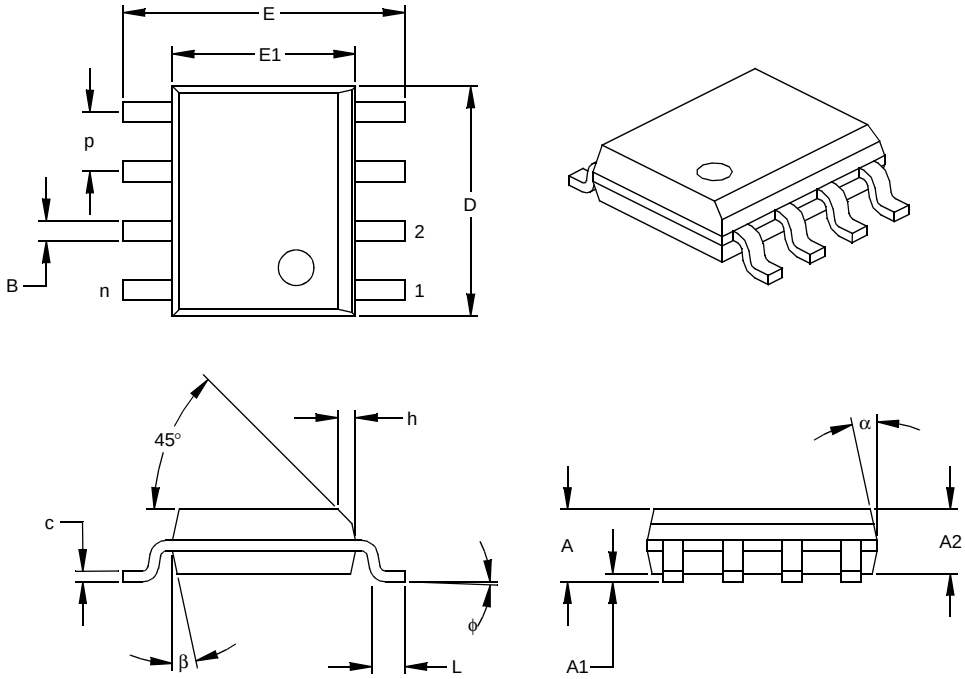
8-Lead Plastic Small Outline (SN) – Narrow, 150 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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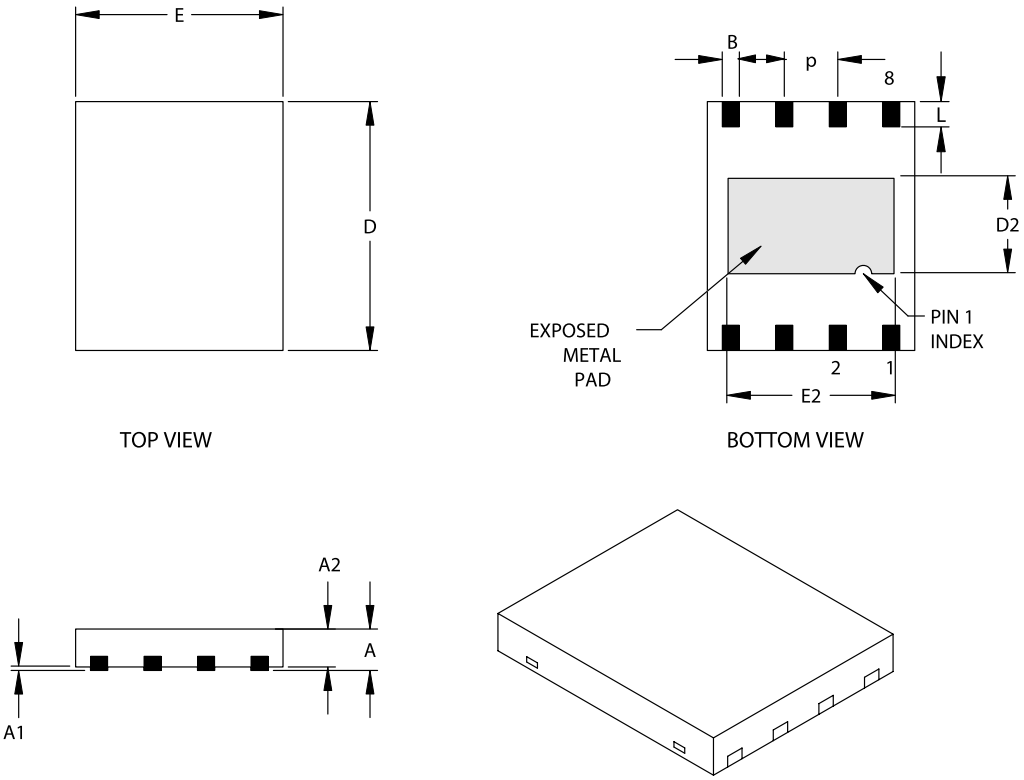
8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.050 BSC			1.27 BSC		
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

Notes:

JEDEC equivalent: MO-220

Drawing No. C04-122 Revised 11/3/03

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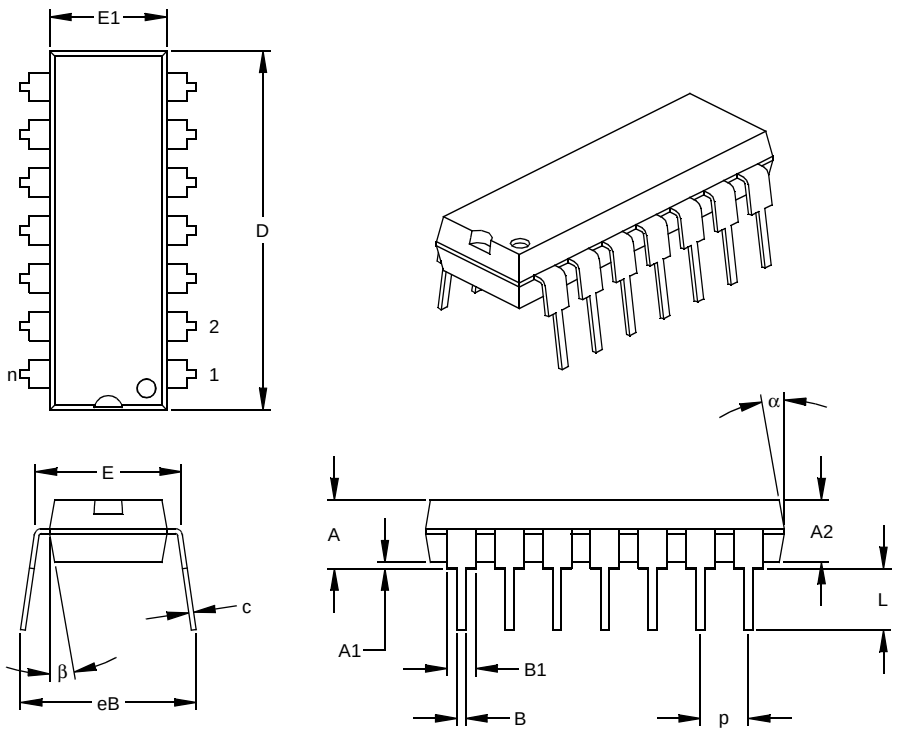
14-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

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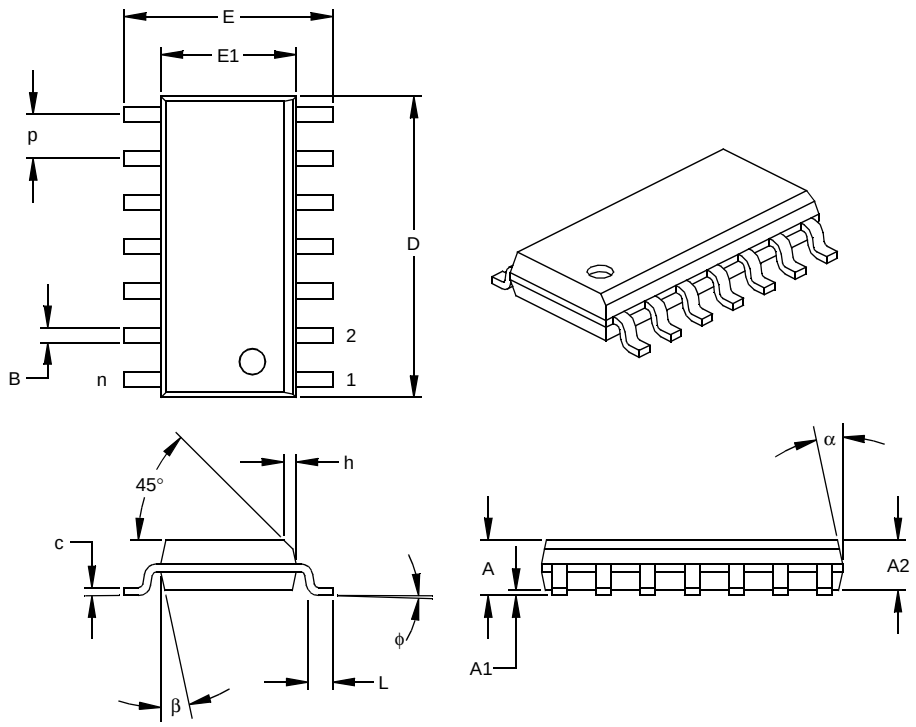
14-Lead Plastic Small Outline (SL) – Narrow, 150 mil Body (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

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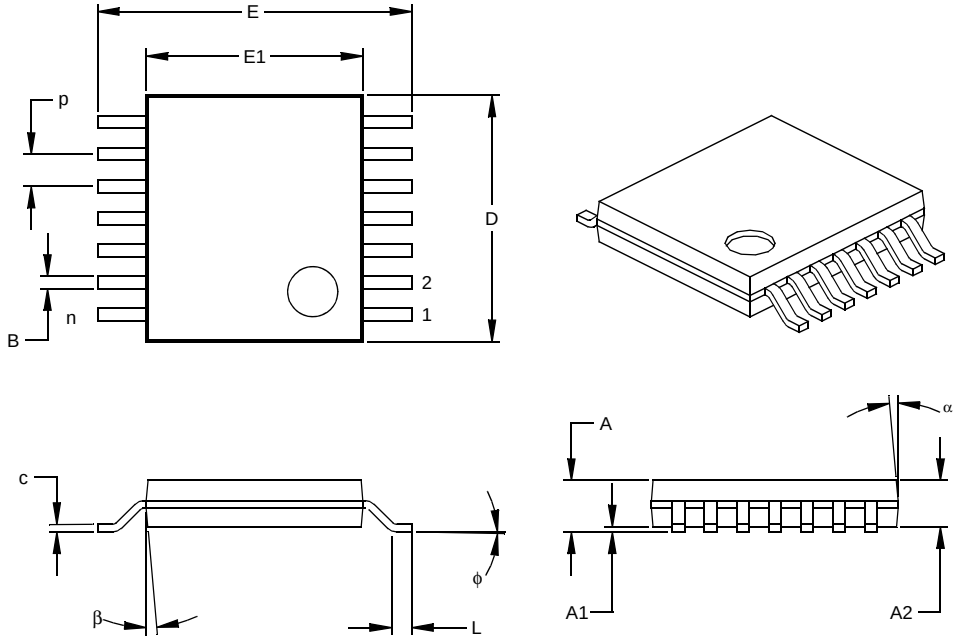
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

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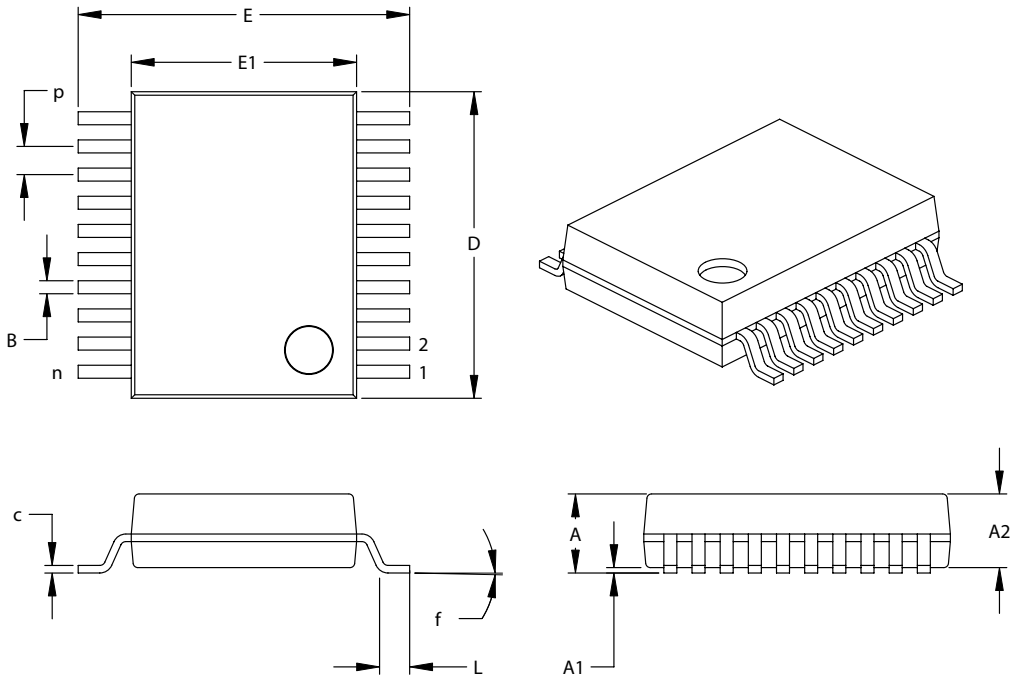
20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95
Lead Thickness	c	.004	-	.010	0.09	-	0.25
Foot Angle	f	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	-	.015	0.22	-	0.38

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Added PIC16F639 to the data sheet.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC12F635: Standard VDD range PIC12F635T: (Tape and Reel) PIC16F636: Standard VDD range PIC16F636T: (Tape and Reel) PIC16F639: Standard VDD range PIC16F639T: (Tape and Reel)
Temperature Range	I = -40°C to +85°C E = -40°C to +125°C
Package	MF = DFN-S (6x5 mm, 8-pin) P = PDIP (300 mil) SN = SOIC (Gull wing, 150 mil body, 8-pin) SL = SOIC (Gull wing, 150 mil body, 14-pin) SS = SSOP (209 mil, 20-pin) ST = TSSOP (4.4 mm, 14-pin)
Pattern	3-Digit Pattern Code for QTP (blank otherwise)

Examples:

a) PIC12F635-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC12F635-I/S = Industrial Temp., SOIC package, 20 MHz

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