# Block Diagram

Figure 1: Block Diagram

Pin Configuration
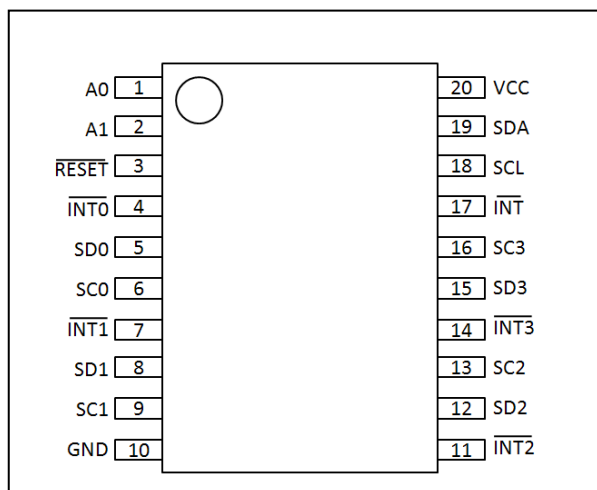
Pin Description

Pin No	Pin Name	Type	Description
1	A0	Input	address input 0
2	A1	Input	address input 1
3	$\overline{\text{RESET}}$	Input	active LOW reset pin
4	$\overline{\text{INT0}}$	Input	active LOW interrupt input 0
5	SD0	I/O	serial data 0
6	SC0	I/O	serial clock 0
7	$\overline{\text{INT1}}$	Input	active LOW interrupt input 1
8	SD1	I/O	serial data 1
9	SC1	I/O	serial clock 1
10	GND	Ground	supply ground
11	$\overline{\text{INT2}}$	Input	active LOW interrupt input 2
12	SD2	I/O	serial data 2
13	SC2	I/O	serial clock 2
14	$\overline{\text{INT3}}$	Input	active LOW interrupt input 3
15	SD3	I/O	serial data 3
16	SC3	I/O	serial clock 3
17	$\overline{\text{INT}}$	Output	active LOW interrupt output
18	SCL	I/O	serial clock line
19	SDA	I/O	serial data line
20	VCC	Power	Supply Power

Maximum Ratings

Storage Temperature	–55℃ to +125℃
Supply Voltage port B	–0.5V to +6.0V
Supply Voltage port A	–0.5V to +6.0V
DC Input Voltage	–0.5V to +6.0V
Control Input Voltage (EN)…	–0.5V to +6.0V
Total power dissipation [1]	100mW
Input current(EN,VCCA,VCCB,GND)...................................	50mA
ESD: HBM Mode	8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	1.65	-	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	-	5.5	V
V_{IO}	I/O Pin Voltage	GND	-	5.5	V
$\Delta t / \Delta V$	Input transition rise or fall time	-	-	10	ns/V
T_A	Operating Temperature Range	−40	-	+85	℃

DC Electrical Characteristics

Unless otherwise specified, -40℃≤T$_A$≤85℃, 1.1V≤Vcc≤3.6V

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
Supply							
VCC	Supply Voltage			1.65		5.5	V
ICC	supply current	operating mode; no load; V$_I$ = VCC or GND; fSCL = 100 kHz	3.6V to 5.5V		65	100	uA
			2.3V to 3.6V		20	50	uA
			1.65V to 2.3V		10	30	uA
Istb	standby current	standby mode; VCC = 3.6 V; no load; V$_I$ = VCC or GND; fSCL = 0 kHz	3.6V to 5.5V		0.3	1	uA
			2.3V to 3.6V		0.1	1	uA
			1.65V to 2.3V		0.1	1	uA
VPOR[1]	power-on reset voltage	no load; V$_I$ = VCC or GND	3.6V to 5.5V		1.3	1.5	V
Input SCL; input/output SDA							
V$_{IL}$	LOW-level input voltage		1.65V to 5.5V	-0.5		+0.3V$_{CC}$	V
V$_{IH}$	HIGH-level input voltage		1.65V to 2V	0.75V$_{CC}$		6	V
			2V to 5.5V	0.7V$_{CC}$		6	V
I$_{OL}$	LOW-level output current	V$_{OL}$ = 0.4 V	1.65V to 5.5V	3		-	mA
		V$_{OL}$ = 0.6 V	1.65V to 5.5V	6		-	mA
I$_{IL}$	LOW-level input current	V$_I$ = GND	1.65V to 5.5V	-1		+1	uA
I$_{IH}$	HIGH-level input current	V$_I$ = VCC	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	VI = GND	3.6V to 5.5V	-	12	13	pF
Pass Gate							
Ron	ON-state resistance	V$_O$ = 0.4 V; I$_O$ = 15 mA	4.5 V to 5.5 V	4	9	24	Ω
			3V to 3.6V	5	11	31	Ω
		V$_O$ = 0.4 V; I$_O$ = 10mA	2.3V to 2.7V	7	16	55	Ω
			1.65V to 2V	9	20	70	Ω
Vpass	switch output voltage	Vin =VCC; Iout = -100uA	5V		3.6		V
			4.5 V to 5.5 V	2.8		4.5	V
			3.3V		2.2		V
			3V to 3.6V	1.6		2.8	V
			2.5V		1.5		V
			2.3V to 2.7V	1.1		2	V
			1.8V		0.9		V
			1.65V to 2V	0.54		1.3	V
I$_L$	leakage current	VI = VCC or GND	1.65V to 5.5V	-1		+1	uA
Cio	input/output capacitance	VI = VCC or GND	1.65V to 5.5V		3	5	pF
Select inputs A0, A1,INT0, INT1,INT2,INT3							
V$_{IL}$	LOW-level input voltage		1.65V to 5.5V	-0.5		+0.3V$_{CC}$	V
V$_{IH}$	HIGH-level input voltage		1.65V to 5.5V	0.7V$_{CC}$		6	V
I$_{IL}$	LOW-level input current	V$_I$ = GND	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	V$_I$ = GND	1.65V to 5.5V		3	5	pF
INT output							
I$_{OL}$	LOW-level output current	V$_{OL}$ = 0.4 V	1.65V to 5.5V	3			mA
I$_{OH}$	HIGH-level output current		1.65V to 5.5V			+10	uA

Note: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.

AC Electrical characteristics

Tamb = - 40 ^{o} C to +85 ^{o} C; unless otherwise specified.

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
t_{PD}[1]	propagation delay	from SDA to SDx, or SCL to SCx	1.65V to 5.5V			0.3	ns
INT[2]							
t_{V_INT}	valid time from INTn to INT signal		1.65V to 5.5V			4	us
t_{D_INT}	delay time from INTn to INT inactive		1.65V to 5.5V			2	us
t_{REJ_L}	LOW-level rejection time		1.65V to 5.5V	1			us
t_{REJ_H}	HIGH-level rejection time		1.65V to 5.5V	0.5			us
RESET							
tw(rst)L	LOW-level reset time			4			ns
trst	reset time	SDA clear		500			ns
$t_{REC;STA}$	recovery time to START condition			0			ns

Note:
1. Pass gate propagation delay is calculated from the 20Ω typical Ron and the 15 pF load capacitance.
2. Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

I2C Interface Timing Requirements

Symbol	Parameter	Standard Mode I2C Bus		Fast Mode I2C Bus		Unit
		Min	Max	Min	Max	
fscl	I2C clock frequency	0	100	0	400	kHz
t_{Low}	I2C clock high time	4.7		1.3		μs
t_{High}	I2C clock low time	4		0.6		μs
t_{SP}	I2C spike time		50		50	ns
$t_{SU:DAT}$	I2C serial-data setup time	250		100		ns
$t_{HD:DAT}$	I2C serial-data hold time	0 [1]		0 [1]		μs
tr	I2C input rise time		1000		300	ns
tf	I2C input fall time		300		300	ns
t_{BUF}	I2C bus free time between stop and start	4.7		1.3		μs
$t_{SU:STA}$	I2C start or repeated start condition setup	4.7		0.6		μs
$t_{HD:STA}$	I2C start or repeated start condition hold	4		0.6		μs
$t_{SU:STO}$	I2C stop condition setup	4		0.6		μs
$t_{VD:DAT}$	Valid-data time (high to low) [2] SCL low to SDA output low valid		1		1	μs
	Valid-data time (low to high) [2] SCL low to SDA output high valid		0.6		0.6	μs
$t_{VD:ACK}$	Valid-data time of ACK condition ACK signal from SCL low to SDA output low		1		1	μs
Cb	I2C bus capacitive load		400		400	pF

Notes:
1. A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
2. Data taken using a 1-kΩ pullup resistor and 50-pF load Notes
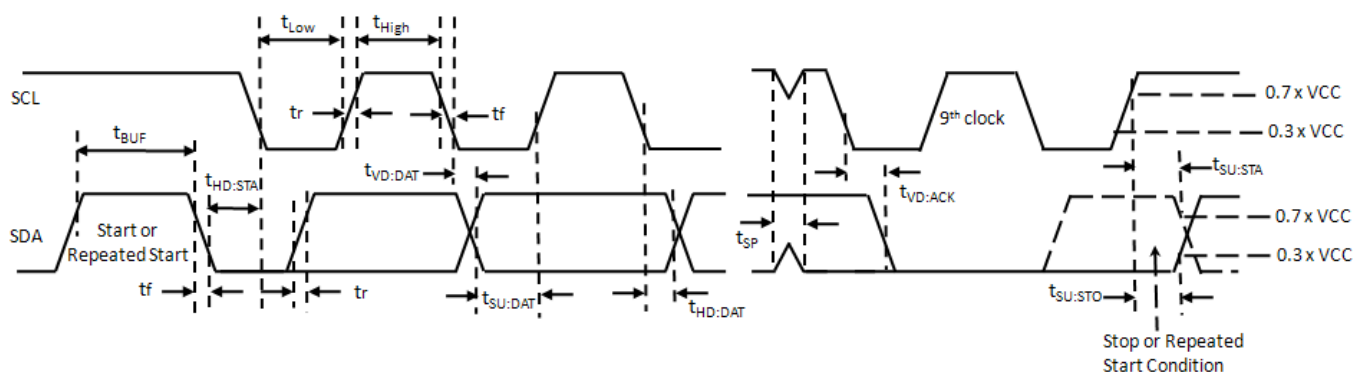
**Figure 2. Definition of timing on the I2C-bus**

Application Diagram
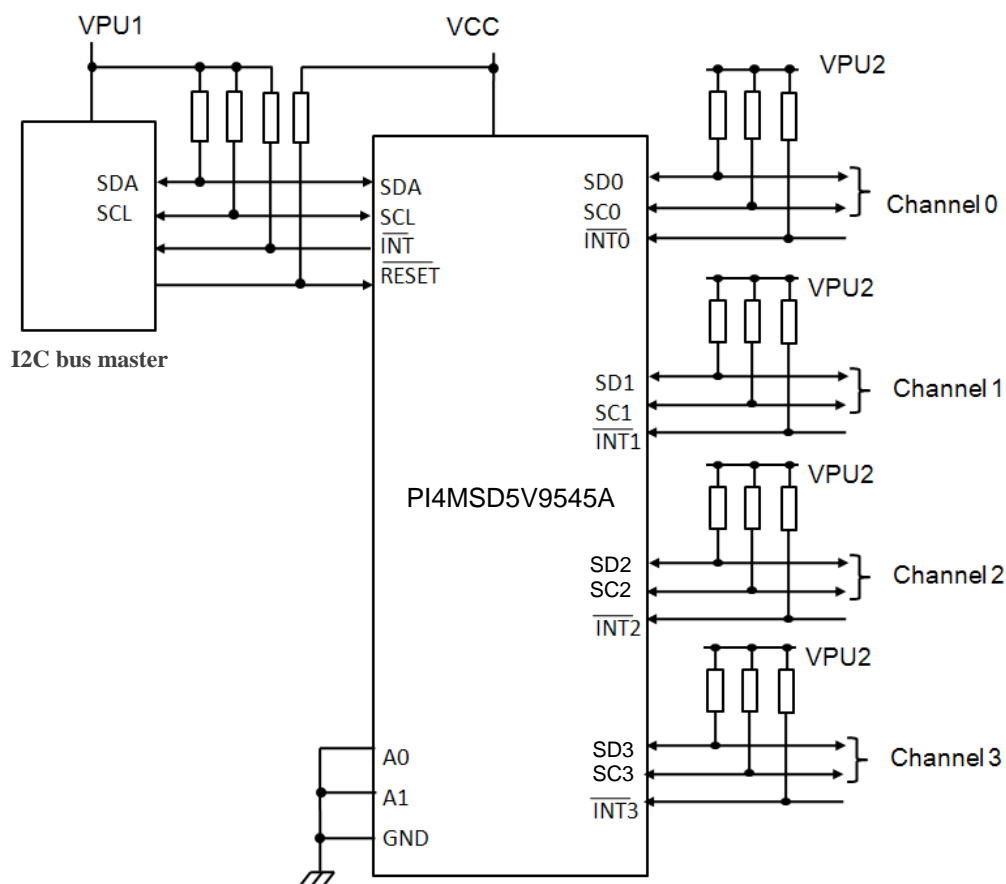
Figure 3. Typical Application

VCC	VPU1	VPU2
1.8V	1.5V-5.5V	1.2V-5.5V
2.5V	1.8V-5.5V	1.8V-5.5V
3.3V	2.7V-5.5V	2.7V-5.5V
5V	4.5V-5.5V	4.5V-5.5V

Note:
If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.
If the device generating the interrupt has a totem pole output structure and cannot be 3-stated, a pull-up resistor is not required.
The interrupt inputs should not be left floating.

Device Addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PI4MSD5V9545A is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.
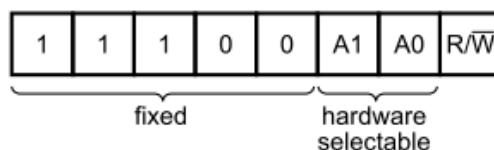
Figure 4: Device Address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

Control Register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PI4MSD5V9545A, which will be stored in the control register. If multiple bytes are received by the PI4MSD5V9545A, it will save the last byte received. This register can be written and read via the I2C-bus.
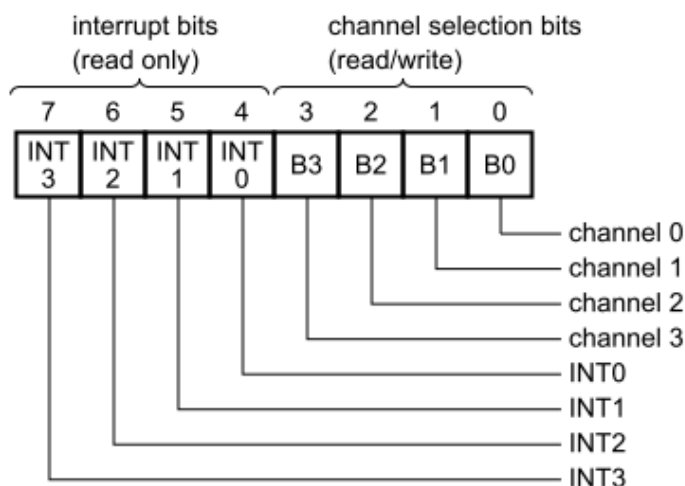
Figure 5: Control Register

Control Register Definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PI4MSD5V9545A has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

Control register: Write—channel selection; Read—channel status.

Interrupt Handling

The PI4MSD5V9545A provides 4 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PI4MSD5V9545A and the interrupt output will be driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 through bit 7 of the control register corresponds to channel 0 through channel 3 of the PI4MSD5V9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PI4MSD5V9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PI4MSD5V9545A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt. The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to VCC through a pull-up resistor.

INT3	INT2	INT1	INT0	B3	D2	B1	B0	Command
X	X	X	0	X	X	X	X	no interrupt on channel 0
X	X	X	1	X	X	X	X	interrupt on channel 0
X	X	0	X	X	X	X	X	no interrupt on channel 1
X	X	1	X	X	X	X	X	interrupt on channel 1
X	0	X	X	X	X	X	X	no interrupt on channel 2
X	1	X	X	X	X	X	X	interrupt on channel 2
0	X	X	X	X	X	X	X	no interrupt on channel 3
1	X	X	X	X	X	X	X	interrupt on channel 3

Control register read — interrupt

Remark: Several interrupts can be active at the same time. For example: INT3 = 0,INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channel 0 and channel 3, and there is an interrupt on channel 1 and on channel 2.

__RESET__ Input

The RESET input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of tw(rst)L, the PI4MSD5V9545A will reset its registers and I2C-bus state machine and will deselect all channels. The RESET input must be connected to VCC through a pull-up resistor.

Power-on Reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4MSD5V9545A in a reset condition until VCC has reached VPOR. At this point, the reset condition is released and the PI4MSD5V9545A registers and I2C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, VCC must be lowered below 0.2 V to reset the device.

Voltage Translation

The pass gate transistors of the PI4MSD5V9545A are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I2C-bus to another.
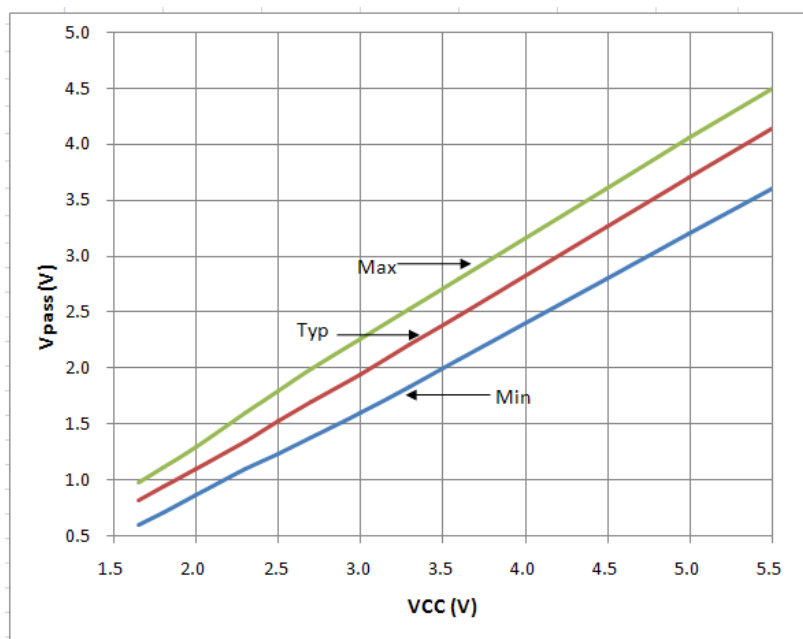
Figure 6:Vpass voltage VS Vcc

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section "DC Electrical characteristics" of this data sheet).

In order for the PI4MSD5V9545A to act as a voltage translator, the Vpass voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then Vpass should be equal to or below 2.7 V to clamp the downstream bus voltages effectively.

Looking at Figure 6, we see that Vpass (max) is at 2.7 V when the PI4MSD5V9545A supply voltage is 3.5 V or lower so the PI4MSD5V9545A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels

I2C Bus

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals.
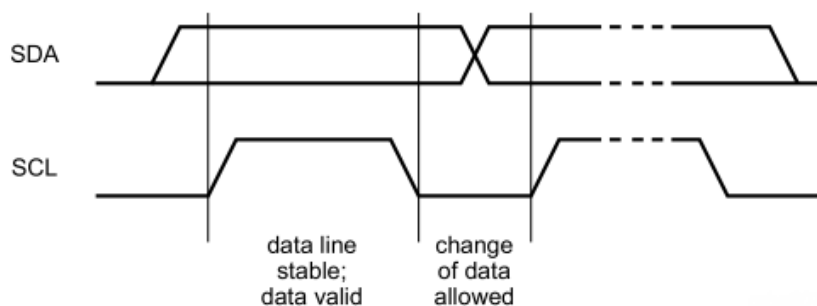
Figure 7: Bit Transfer

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).
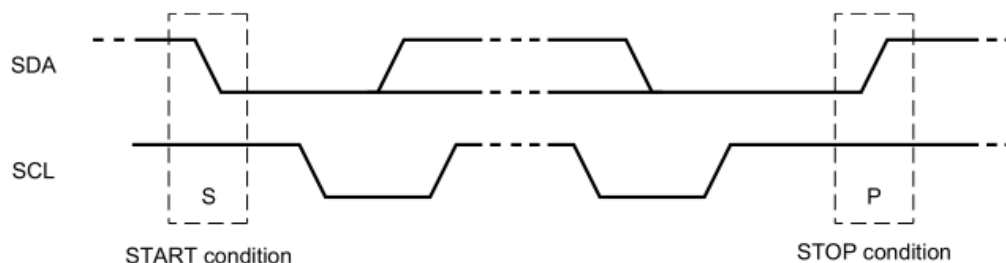
Figure 8. Definition of Start and Stop Conditions

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'
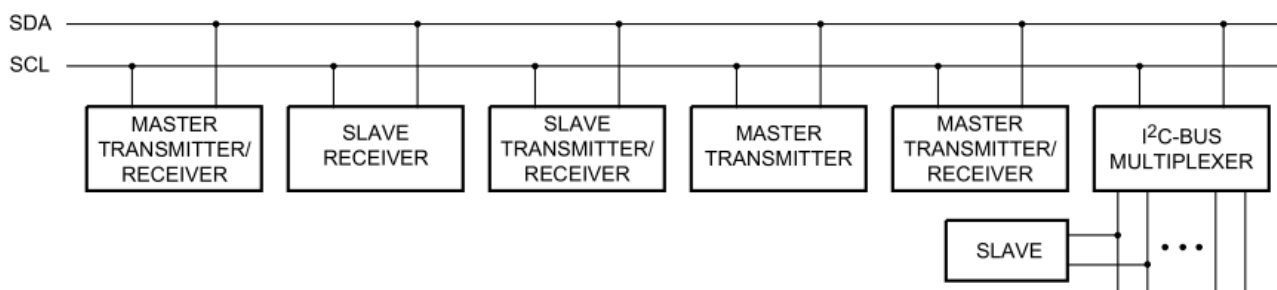
Figure 9. System Configuration

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an

acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
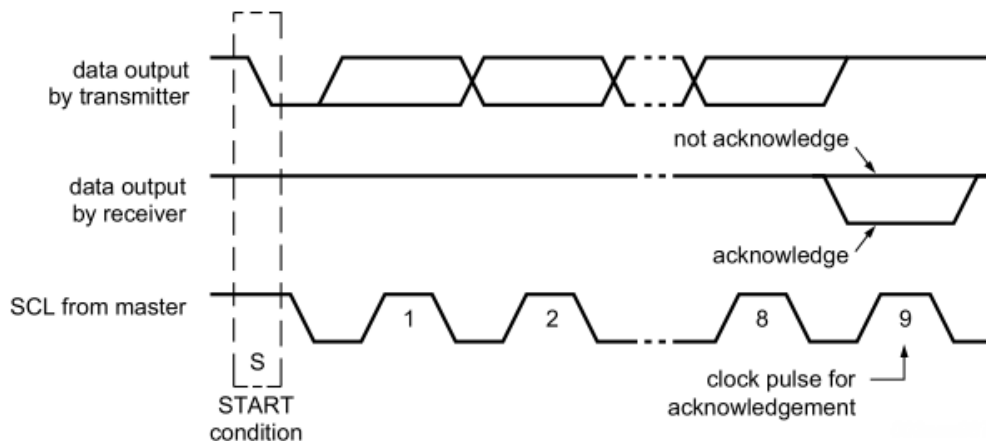
Figure 10. Acknowledgment on I2C Bus

Data is transmitted to the PI4MSD5V9545A control register using the write mode shown in bellow
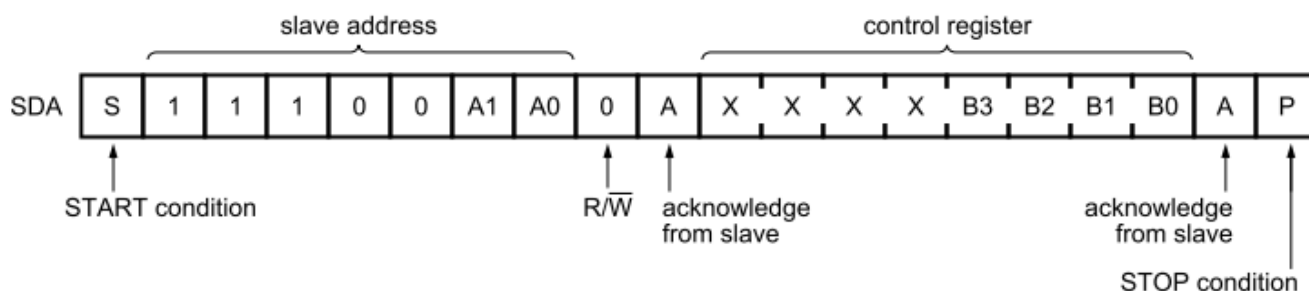
Figure 11. Write Control Register

Data is transmitted to the PI4MSD5V9545A control register using the write mode shown in bellow
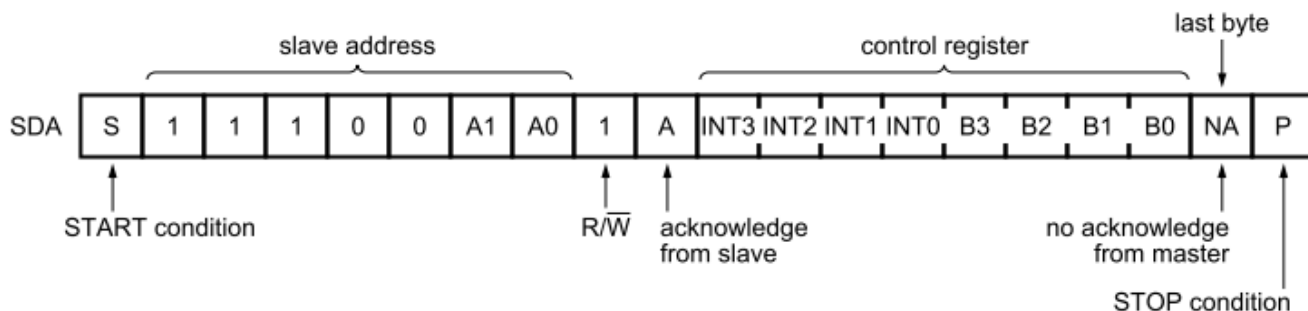
Figure 12. Read Control Register

Part Marking

PĪ4MSD5V
9545ALE
○ YYYWWGḠ

1st Y: Die Rev
YYWW: Date Code (Year & Workweek)
1st G: Assembly Site Code
2nd G: Wafer Fab Site Code
The Bar above "I" means Fab3 of MGN
The Bar above "G" means Cu wire

Packaging Mechanical:

20-TSSOP (L)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO−153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DATE: 03/31/16
DESCRIPTION: 20-Pin, 173mil Wide TSSOP
PACKAGE CODE: L (L20)
DOCUMENT CONTROL #: PD-1311
REVISION: G

16-0074

For latest package information:
Please see http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Part Number	Package Code	Package Description
PI4MSD5V9545ALEX	L	20-Pin,173 mil Wide (TSSOP)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE