# Contents

# 1. FEATURES

- 2G-bit/4G-bit SLC NAND Flash
  - Bus: x8
  - Page size: (2048+64)byte
  - Block size: (128K+4K)byte
  - Plane size:
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **Multiplexed Command/Address/Data**
- **User Redundancy**
  - 64-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 45us (typ.)
  - Sequential read: 25ns
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7~1.95V
- **Low Power Dissipation**
  - Max. 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max.) standby current
- **Hardware Data Protection:** WP# pin
- **Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature**
- **High Reliability**
  - Internal ECC logic always enabling
  - Typical 100K P/E endurance cycle
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  63-ball 9mmx11mm VFBGA
  All packaged devices are RoHS Compliant.

# 2. GENERAL DESCRIPTIONS

The MX30UFxGE8AB is a 2Gb & 4Gb SLC NAND Flash memory device. Its standard NAND Flash features and reliable quality make it most suitable for embedded system code and data storage.

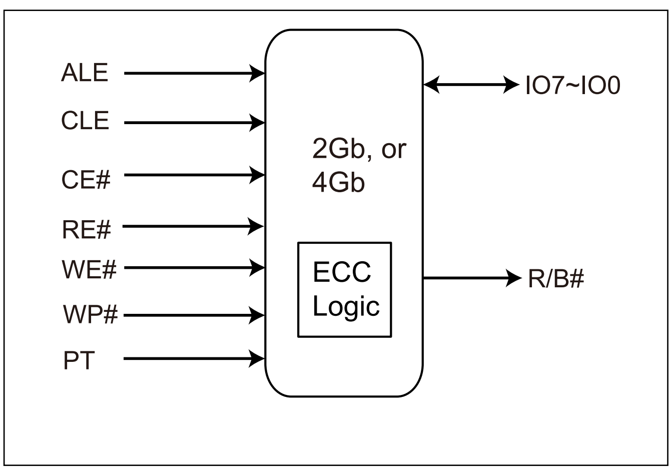
The product family does not require the host controller to support ECC since there is an internal ECC logic inside the Flash device for the error correction and detection.

The MX30UFxGE8AB is typically accessed in pages of 2,112 bytes both for read and for program operations.

The MX30UFxGE8AB array is organized as thousands of blocks, which is composed by 64 pages of (2,048+64) bytes in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for bad block marks and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access.

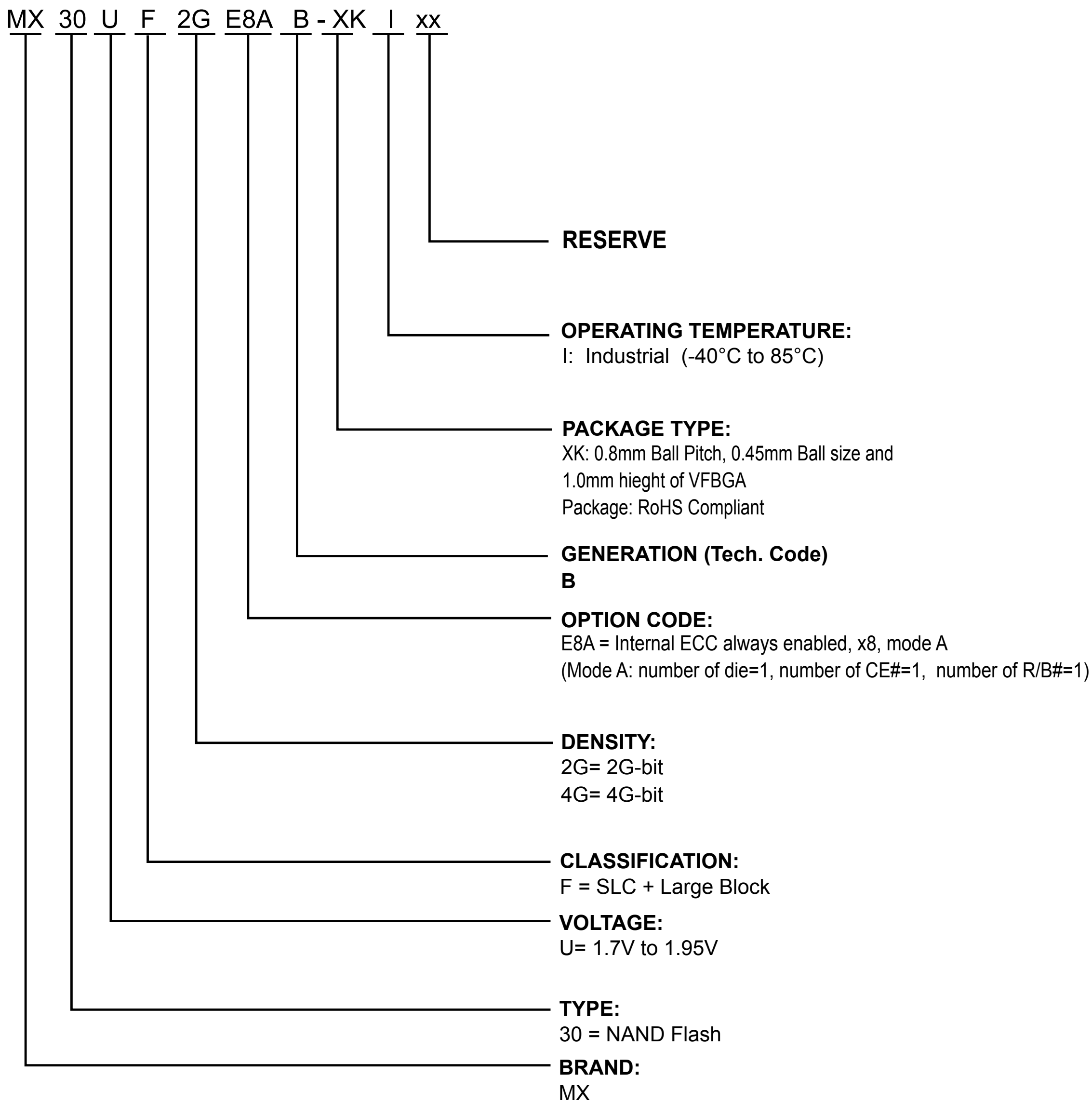
The MX30UFxGE8AB power consumption is 30mA during all modes of operations (Read/Program/Erase), and 50uA in standby mode.

**Figure 1. Logic Diagram**



## 2-1. ORDERING INFORMATION

### Part Name Description




| Part Number | Density | Organization | VCC Range | Package | Temperature Grade |
|---|---|---|---|---|---|
| MX30UF2GE8AB-XKI | 2Gb | x8 | 1.8V | 63-VFBGA | Industrial |
| MX30UF4GE8AB-XKI | 4Gb | x8 | 1.8V | 63-VFBGA | Industrial |

# 3. PIN CONFIGURATIONS

## 63-ball 9mmx11mm VFBGA (x8)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | NC | | | | | | | NC | NC |
| B | NC | | | | | | | | NC | NC |
| C | | | WP# | ALE | Vss | CE# | WE# | R/B# | | |
| D | | | Vcc[1] | RE# | CLE | NC | NC | NC | | |
| E | | | NC | NC | NC | NC | NC | NC | | |
| F | | | NC | NC | NC | NC | Vss[1] | NC | | |
| G | | | NC | Vcc[1] | PT | NC | NC | NC | | |
| H | | | NC | I/O0 | NC | NC | NC | Vcc | | |
| J | | | NC | IO1 | NC | Vcc | IO5 | IO7 | | |
| K | | | Vss | IO2 | IO3 | IO4 | I/O6 | Vss | | |
| L | NC | NC | | | | | | | NC | NC |
| M | NC | NC | | | | | | | NC | NC |

***Note 1.*** *These pins might not be connected internally; however, it is recommended to connect these pins to power (or ground) as designated for ONFI compatibility.*

## 3-1. PIN DESCRIPTIONS

| SYMBOL | PIN NAME |
|---|---|
| **IO7 - IO0** | Data I/O port: IO7-IO0 |
| **CE#** | Chip Enable (Active Low) |
| **RE#** | Read Enable (Active Low) |
| **WE#** | Write Enable (Active Low) |
| **CLE** | Command Latch Enable |
| **ALE** | Address Latch Enable |
| **WP#** | Write Protect (Active Low) |
| **R/B#** | Ready/Busy (Open Drain) |
| **VSS** | Ground |
| **VCC** | Power Supply for Device Operation |
| **NC** | Not Connected Internally |
| **DNU** | Do Not Use (Do Not Connect) |
| **PT** | Protection (Active High) for entire chip protection. A weak pull-down internally |

### PIN FUNCTIONS

The MX30UFxGE8AB device is a sequential access memory that utilizes multiplexing input of Command/Address/Data.

### I/O PORT: IO7- IO0

The IO7 to IO0 pins are for address/command input and data output to and from the device.

### CHIP ENABLE: CE#

The device goes into low-power Standby Mode when CE# goes high during a read operation and not at busy stage.

The CE# goes low to enable the device to be ready for standard operation. When the CE# goes high, the device is deselected. However, when the device is at busy stage, the device will not go to standby mode when CE# pin goes high.

### READ ENABLE: RE#

The RE# (Read Enable) allows the data to be output by a tREA time after the falling edge of RE#. The internal address counter is automatically increased by one at the falling edge of RE#.

### WRITE ENABLE: WE#

When the WE# goes low, the address/data/command are latched at the rising edge of WE#.

### COMMAND LATCH ENABLE: CLE

The CLE controls the command input. When the CLE goes high, the command data is latched at the rising edge of the WE#.

### ADDRESS LATCH ENABLE: ALE

The ALE controls the address input. When the ALE goes high, the address is latched at the rising edge of WE#.

### WRITE PROTECT: WP#

The WP# signal keeps low and then the memory will not accept the program/erase operation. It is recommended to keep WP# pin low during power on/off sequence. Please refer to **"Figure 42. Power On/Off Sequence"**.

### READY/Busy: R/B#

The R/B# is an open-drain output pin. The R/B# outputs the ready/busy status of read/program/erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

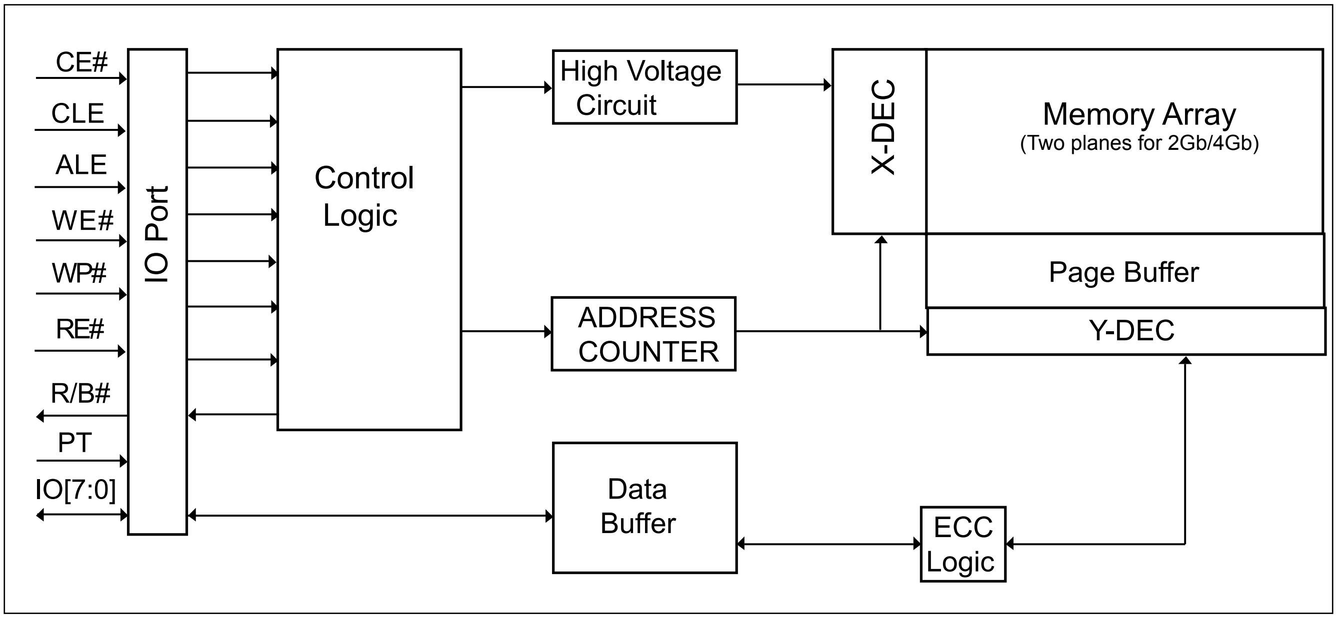
Please refer to **"8-1. R/B#: Termination for The Ready/Busy# Pin (R/B#)"** for details.

### PROTECTION: PT

The PT pin is the hardware method to protect the whole chip from program/erase operation. When the PT pin is at high at power-on, the whole chip is protected even the WP# is at high; the un-protect command and procedure is necessary before any program/erase operation. When the PT pin is connected to low or floating, the Protection function is disabled.

Please refer to Section - **"6-17. Block Protection"** for details.

## 4. BLOCK DIAGRAM



# 5. SCHEMATIC CELL LAYOUT AND ADDRESS ASSIGNMENT

MX30UFxGE8AB NAND device is divided into two planes, which is composed by 64 pages of (2,048+64)-byte in two NAND strings structure with 32 serial connected cells in each string. Each page has an additional 64 bytes for bad block marks and other purposes. The device has an on-chip buffer of 2,112 bytes for data load and access. Each 2K-Byte page has the two area, one is the main area which is 2048-bytes and the other is spare area which is 64-byte.

There are five address cycles for the address allocation, please refer to the table below.

**Table 1. Address Allocation: MX30UFxGE8AB**

| Addresses | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|
| **Column address - 1st cycle** | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| **Column address - 2nd cycle** | L | L | L | L | A11 | A10 | A9 | A8 |
| **Row address - 3rd cycle** | A19 | A18[1] | A17 | A16 | A15 | A14 | A13 | A12 |
| **Row address - 4th cycle** | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 |
| **Row address - 5th cycle[2]** | L | L | L | L | L | L | A29[2] | A28 |

***Notes:***

1. *A18 is the plane selection.*
2. *A29 is for 4Gb, "L" (Low) is for 2Gb.*

# 6. DEVICE OPERATIONS

## 6-1. Address Input/Command Input/Data Input

Address input bus operation is for address input to select the memory address. The command input bus operation is for giving command to the memory. The data input bus is for data input to the memory device.

**Figure 2. AC Waveforms for Command / Address / Data Latch Timing**

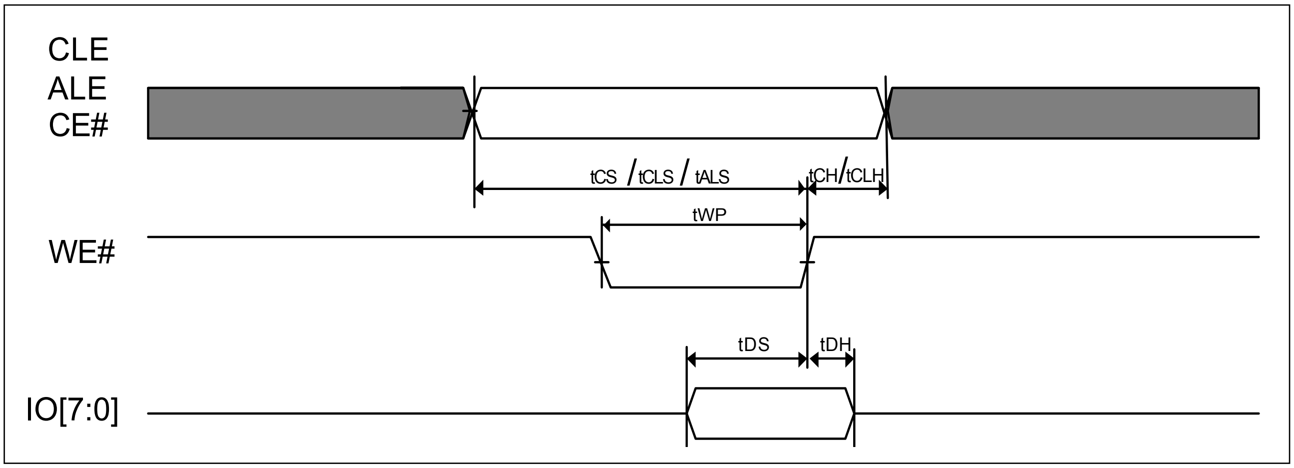
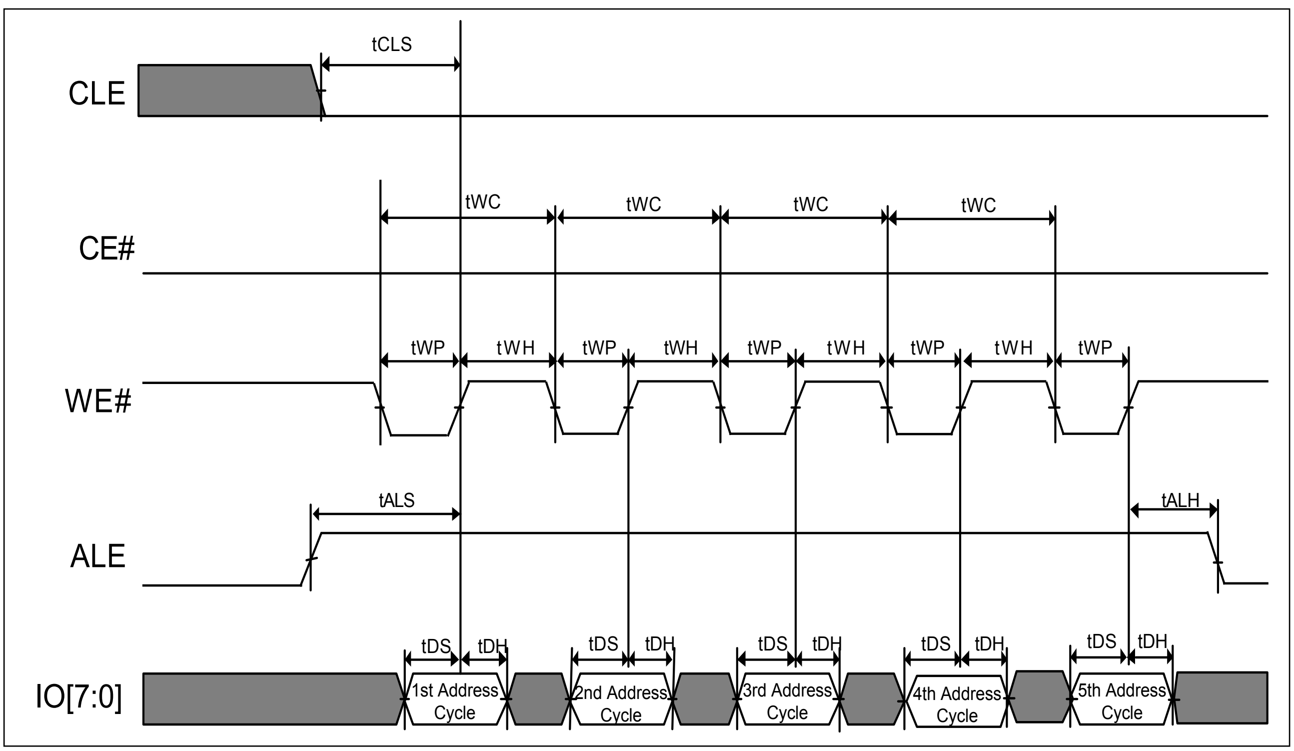
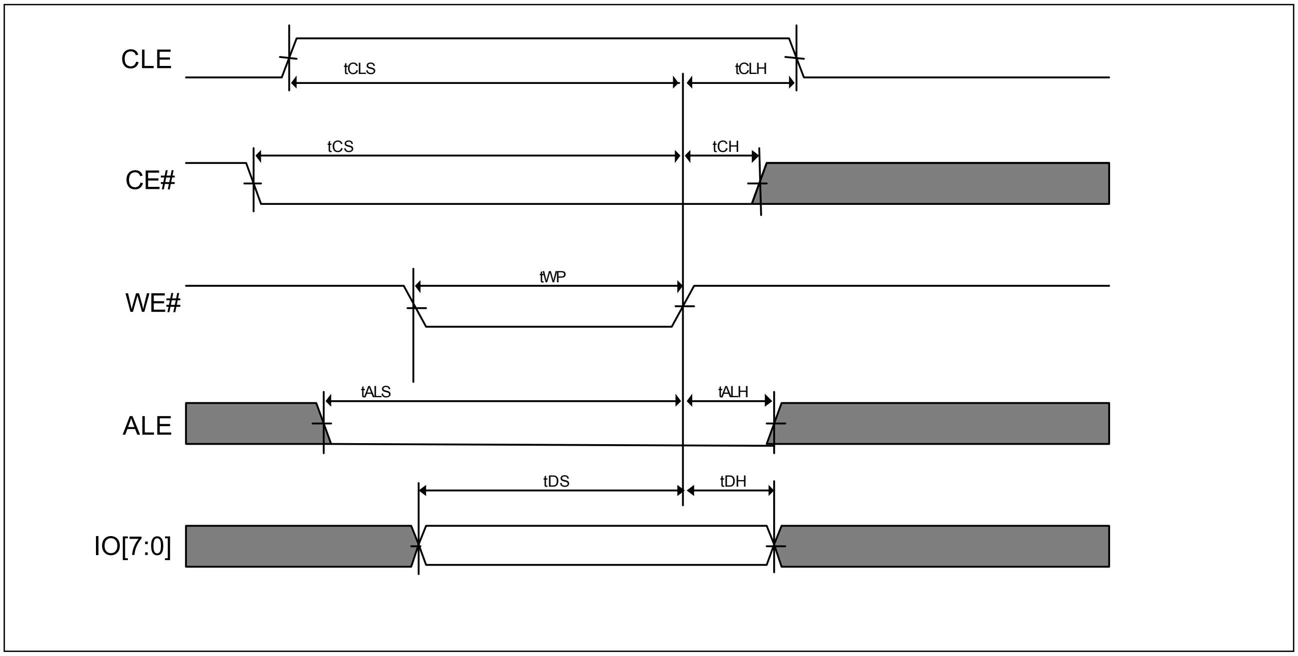


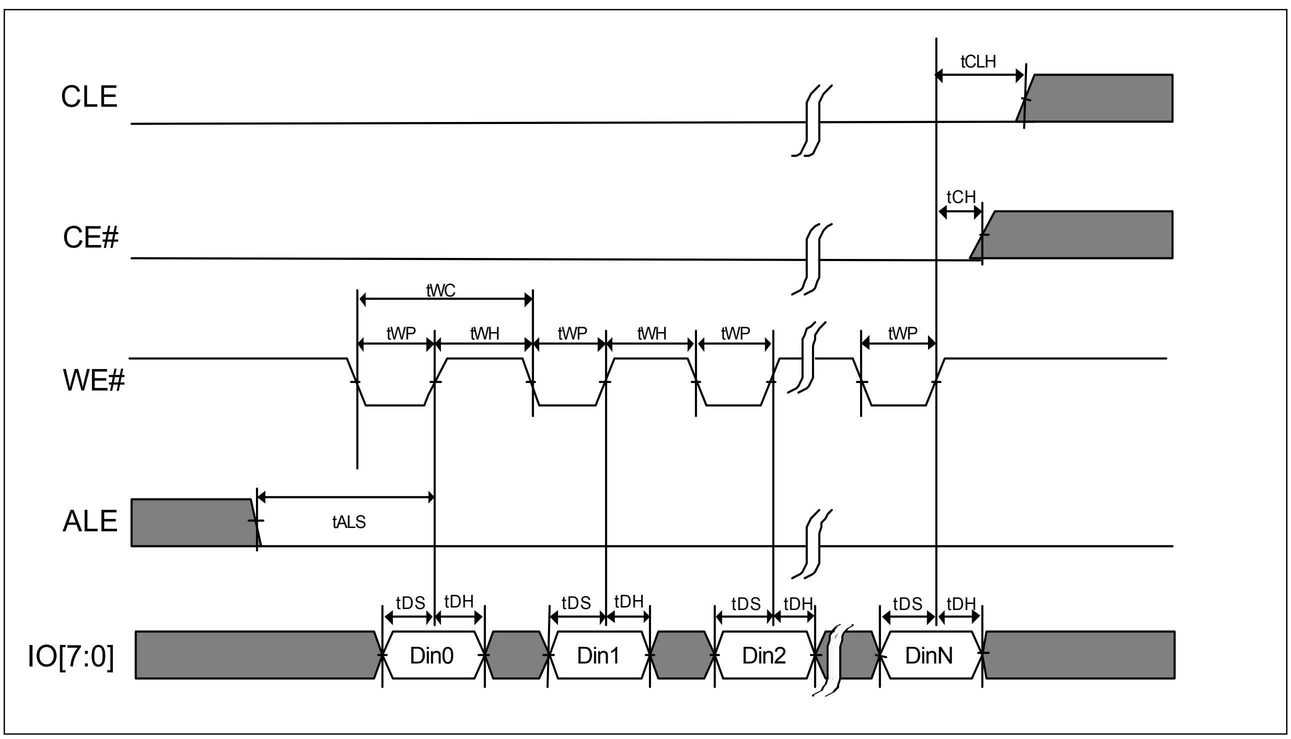

**Figure 3. AC Waveforms for Address Input Cycle**



### Figure 4. AC Waveforms for Command Input Cycle




### Figure 5. AC Waveforms for Data Input Cycle



## 6-2. Page Read

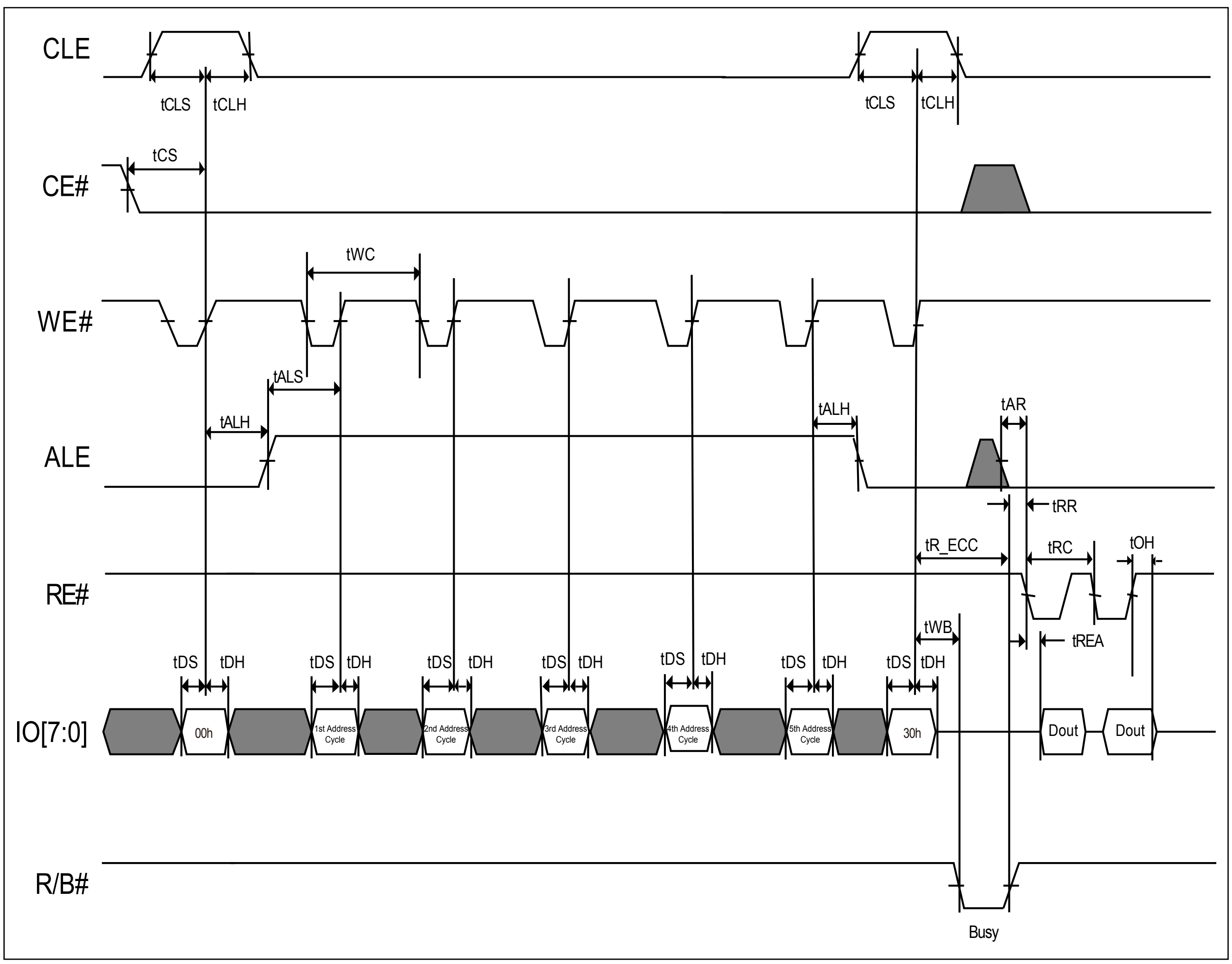
The MX30UFxGE8AB array is accessed in Page of 2,112 bytes. External reads begins after the R/B# pin goes to READY.

The Read operation may also be initiated by writing the 00h command and giving the address (column and row address) and being confirmed by the 30h command, the MX30UFxGE8AB begins the internal read operation and the chip enters busy state. The data can be read out in sequence after the chip is ready. Refer to the waveform for Read Operation as below.

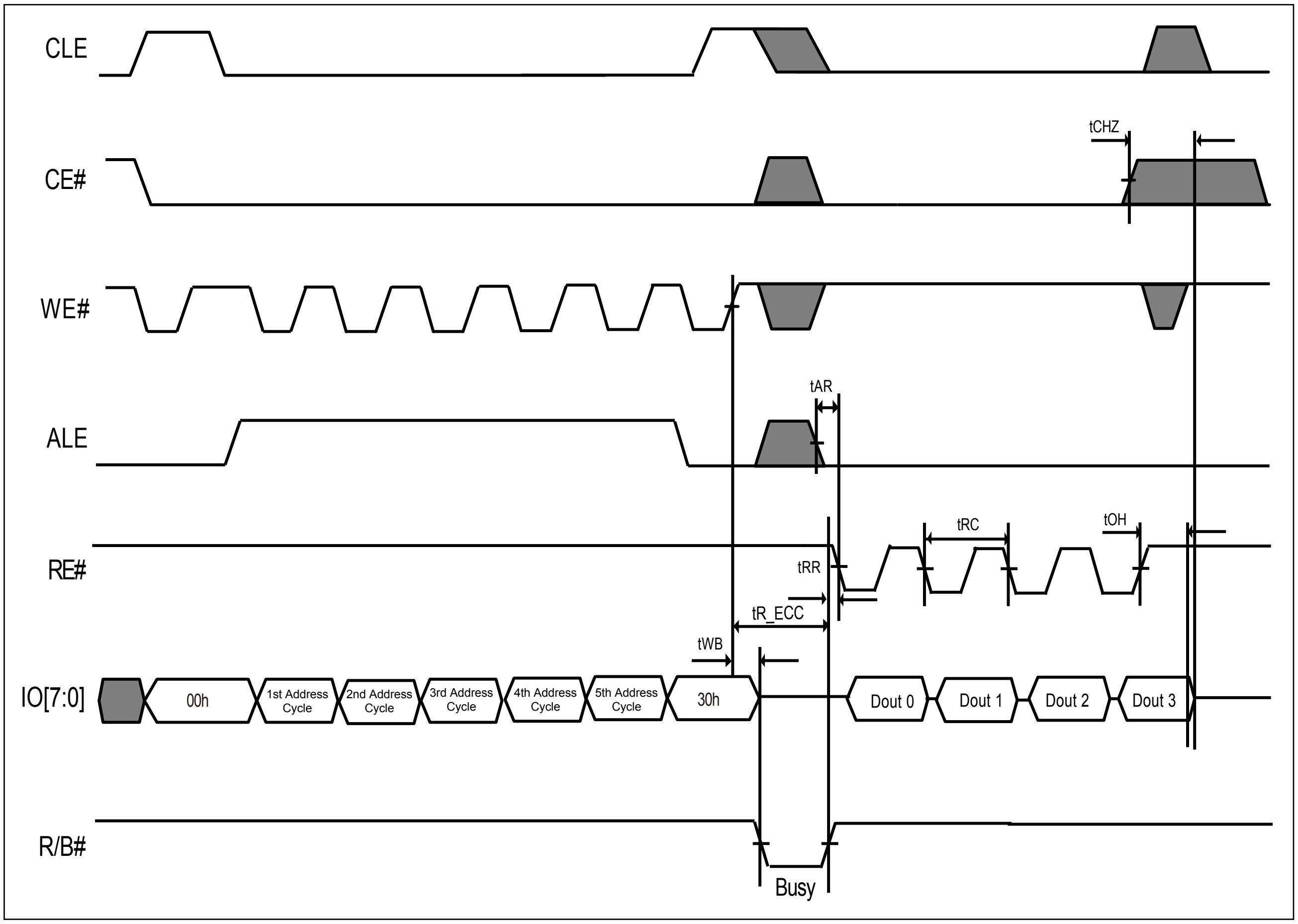
If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode (**"Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode"**).

To access the data in the same page randomly, a command of 05h may be written and only column address following and then confirmed by E0h command.

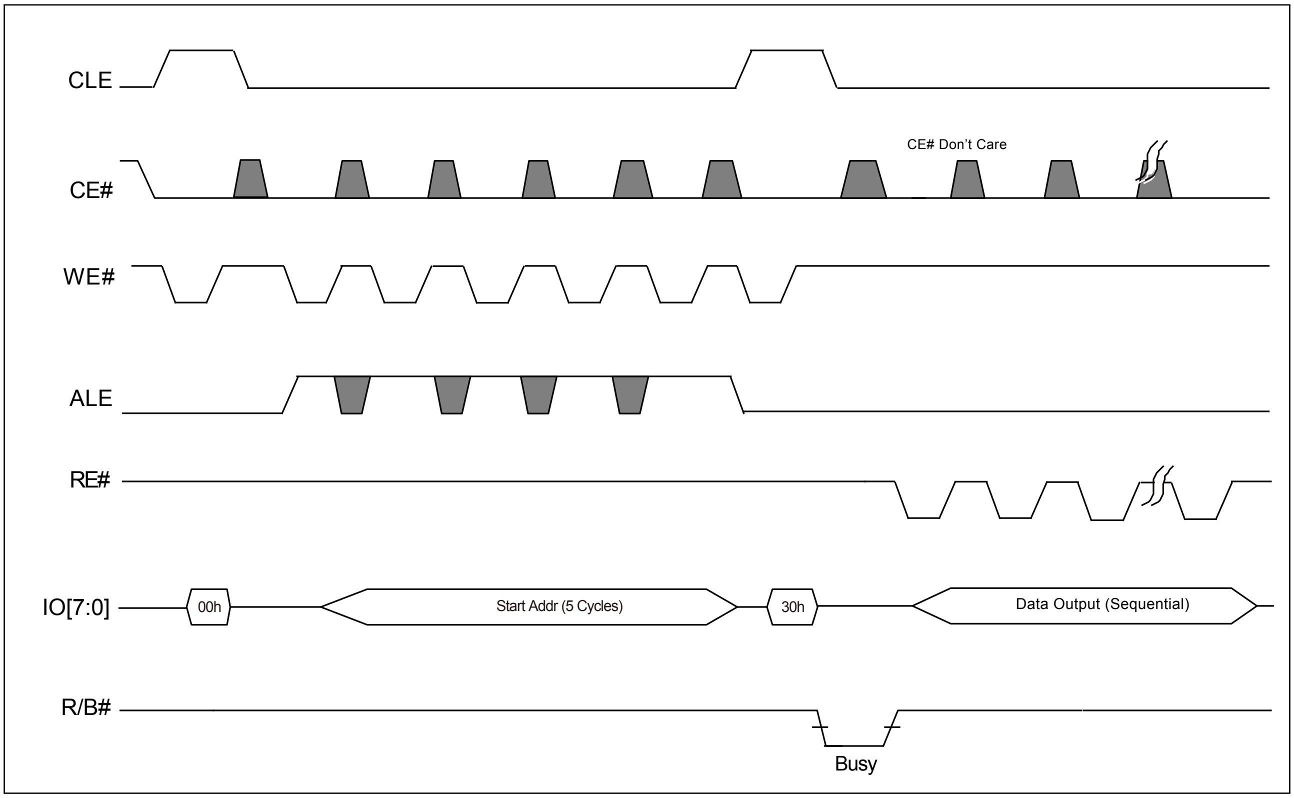
**Figure 6. AC Waveforms for Read Cycle**



### Figure 7. AC Waveforms for Read Operation (Intercepted by CE#)

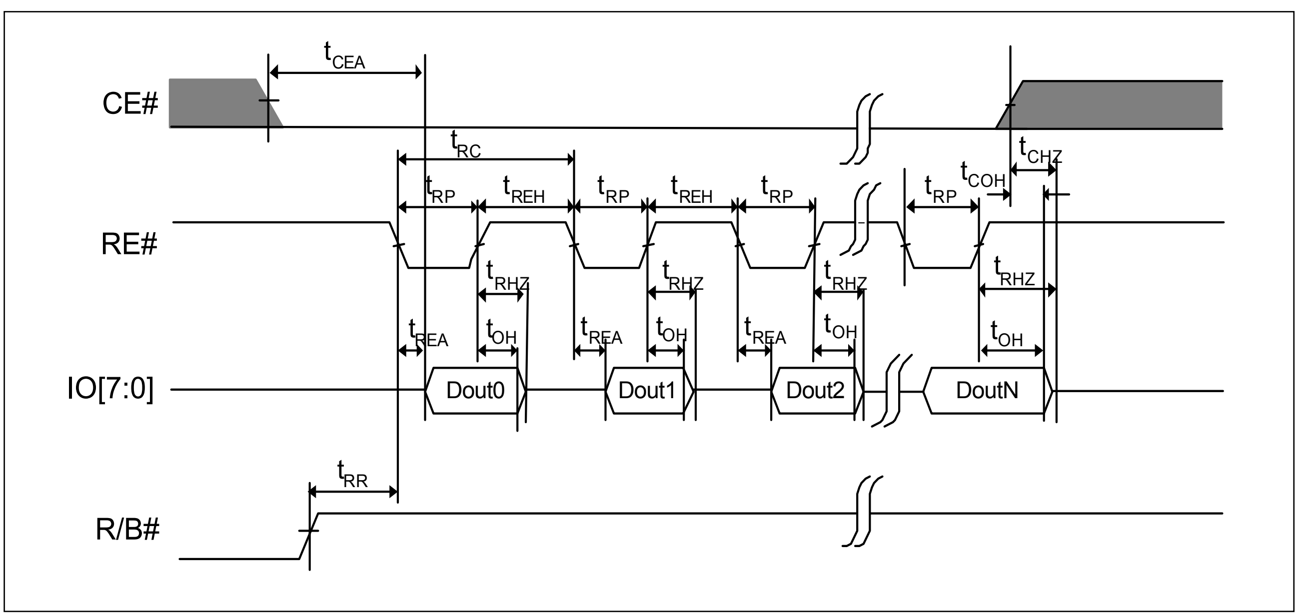


### Figure 8. AC Waveforms for Read Operation (with CE# Don't Care)

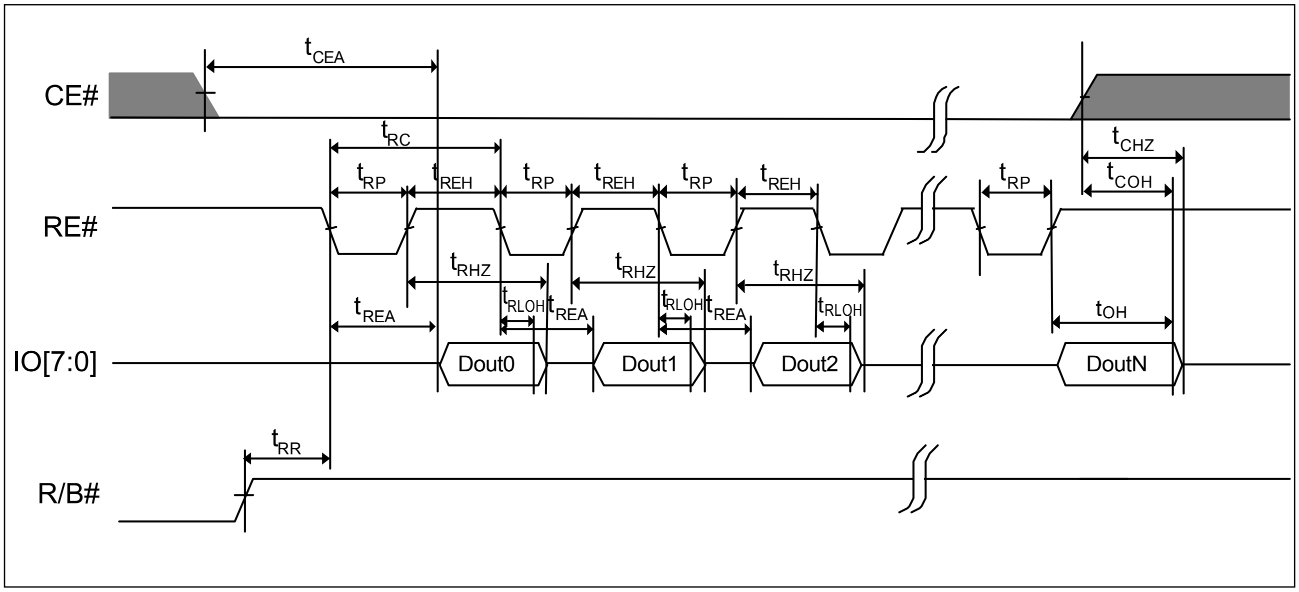



**Note:** *The CE# "Don't Care" feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.*

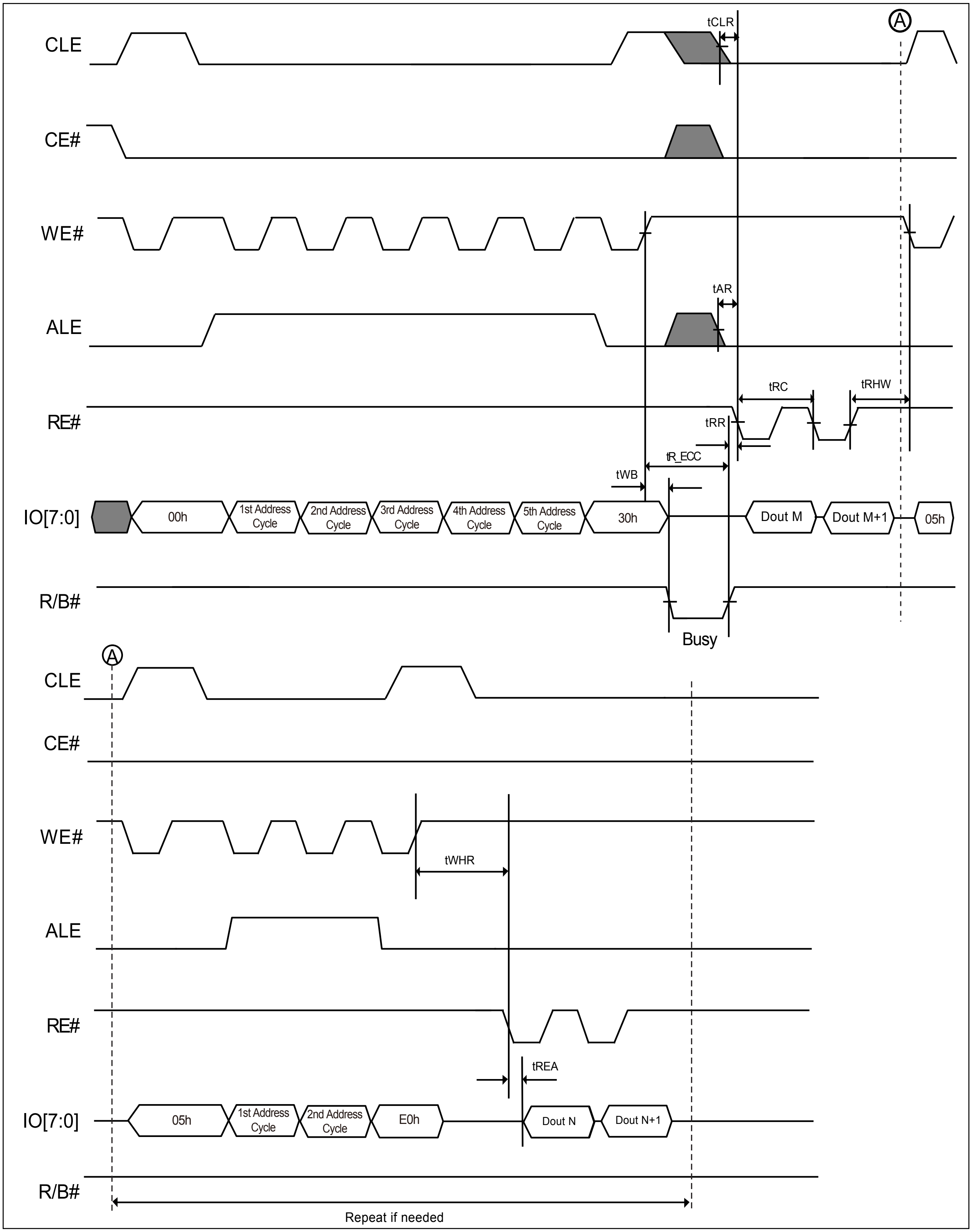
### Figure 9-1. AC Waveforms for Sequential Data Out Cycle (After Read)



## Figure 9-2. AC Waveforms for Sequential Data Out Cycle (After Read) - EDO Mode



## Figure 10. AC Waveforms for Random Data Output



## 6-3. Page Program

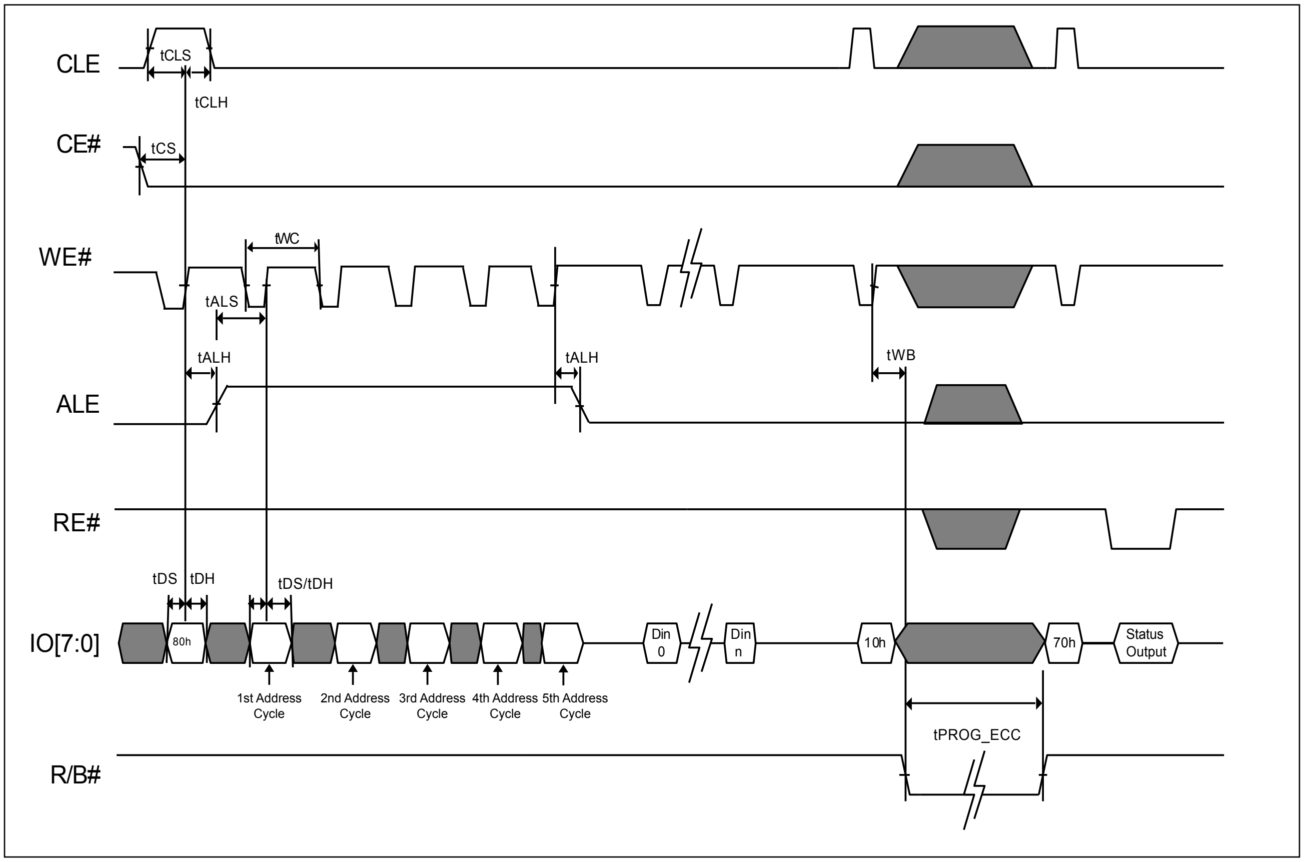
The memory is programmed by page, which is 2,112 bytes. After Program load command (80h) is issued and the row and column address is given, the data will be loaded into the chip sequentially. Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is complete, program confirm command (10h) is issued to start the page program operation. The page program operation in a block should start from the low address to high address (A[17:12]). Partial program in a page is allowed up to 4 times. However, the random data input mode for programming a page is allowed and number of times is not limited.

The status of the program completion can be detected by R/B# pin or Status register bit SR[6].

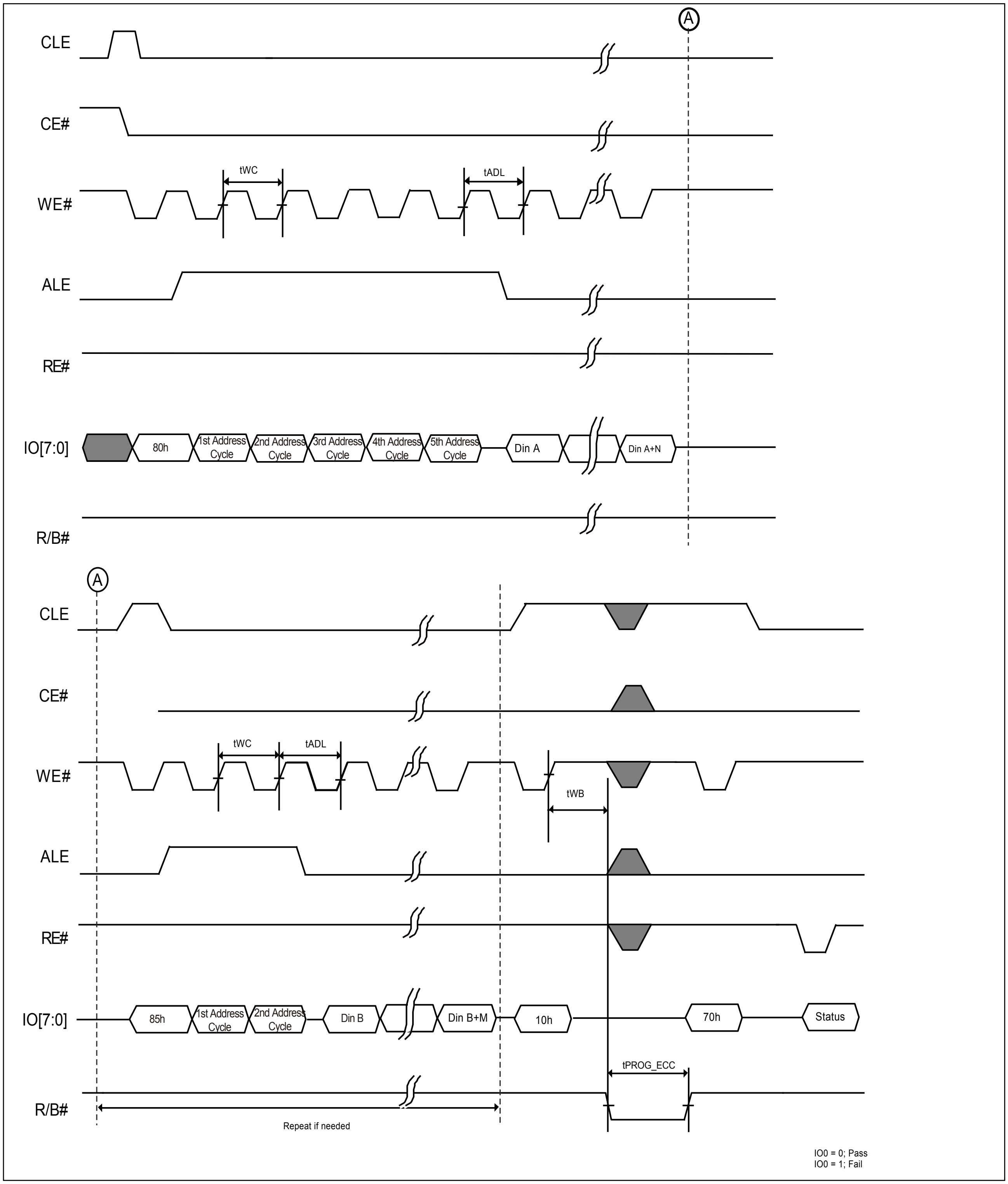
The program result is shown in the chip status bit (SR[0]). SR[0] = 1 indicates the Page Program is not successful and SR[0] = 0 means the program operation is successful.

During the Page Program progressing, only the read status register command and reset command are accepted, others are ignored.

### Figure 11. AC Waveforms for Program Operation after Command 80H

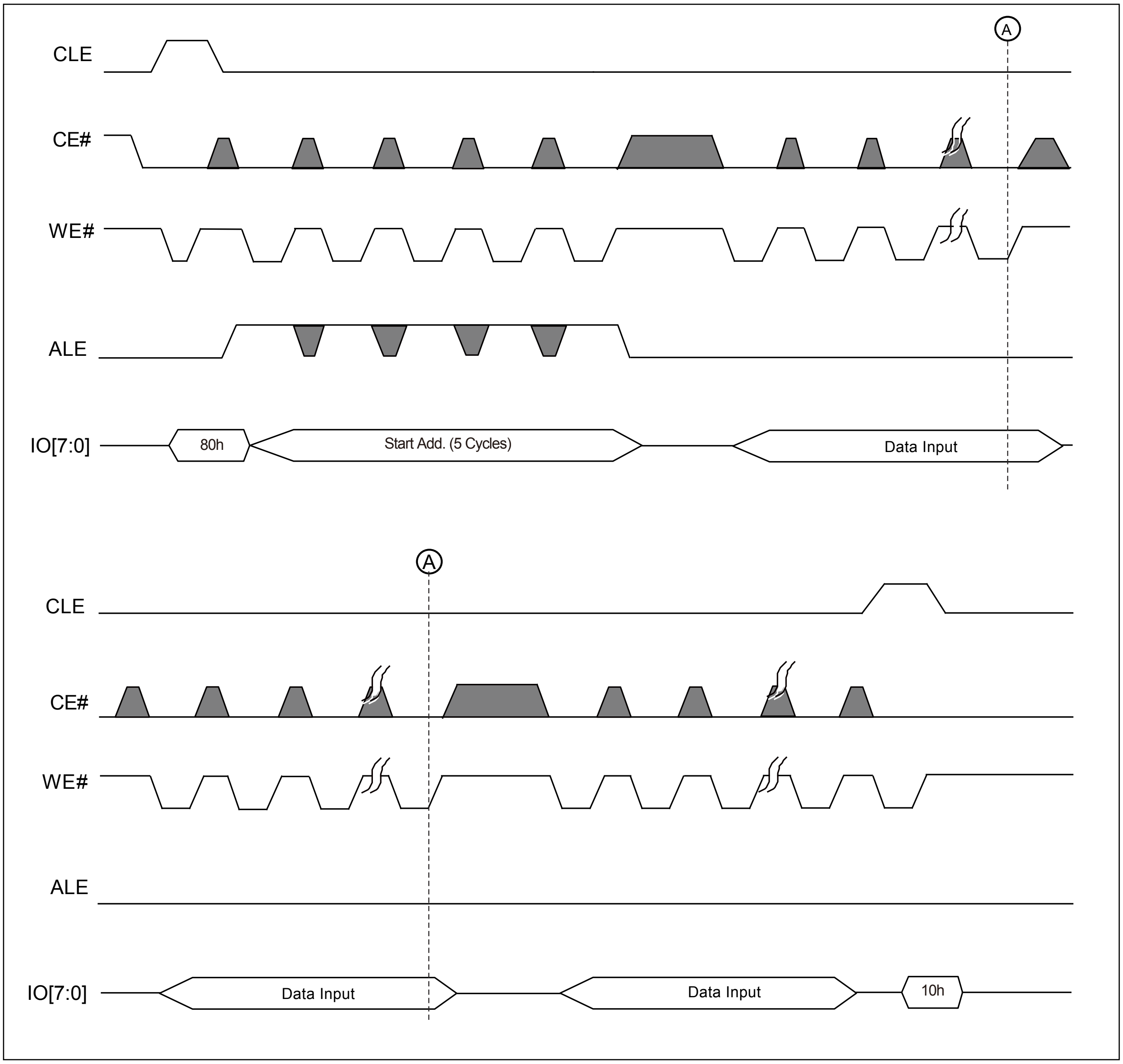


## Figure 12. AC Waveforms for Random Data In (For Page Program)




***Note:*** *Random Data In is also supported in cache program.*

**Figure 13. AC Waveforms for Program Operation with CE# Don't Care**




***Note:*** *The CE# "Don't Care" feature may simplify the system interface, which allows the controller to directly write data into flash device, and the CE# transitions will not stop the program operation during the latency time.*

## 6-4. Cache Program

The cache program feature enhances the program performance by using the cache buffer of 2,112-byte. The serial data can be input to the cache buffer while the previous data stored in the buffer are programming into the memory cell. Cache Program command sequence is almost the same as page program command sequence. Only the Program Confirm command (10h) is replaced by cache Program command (15h).

After the Cache Program command (15h) is issued. The user can check the status by the following methods.

- R/B# pin

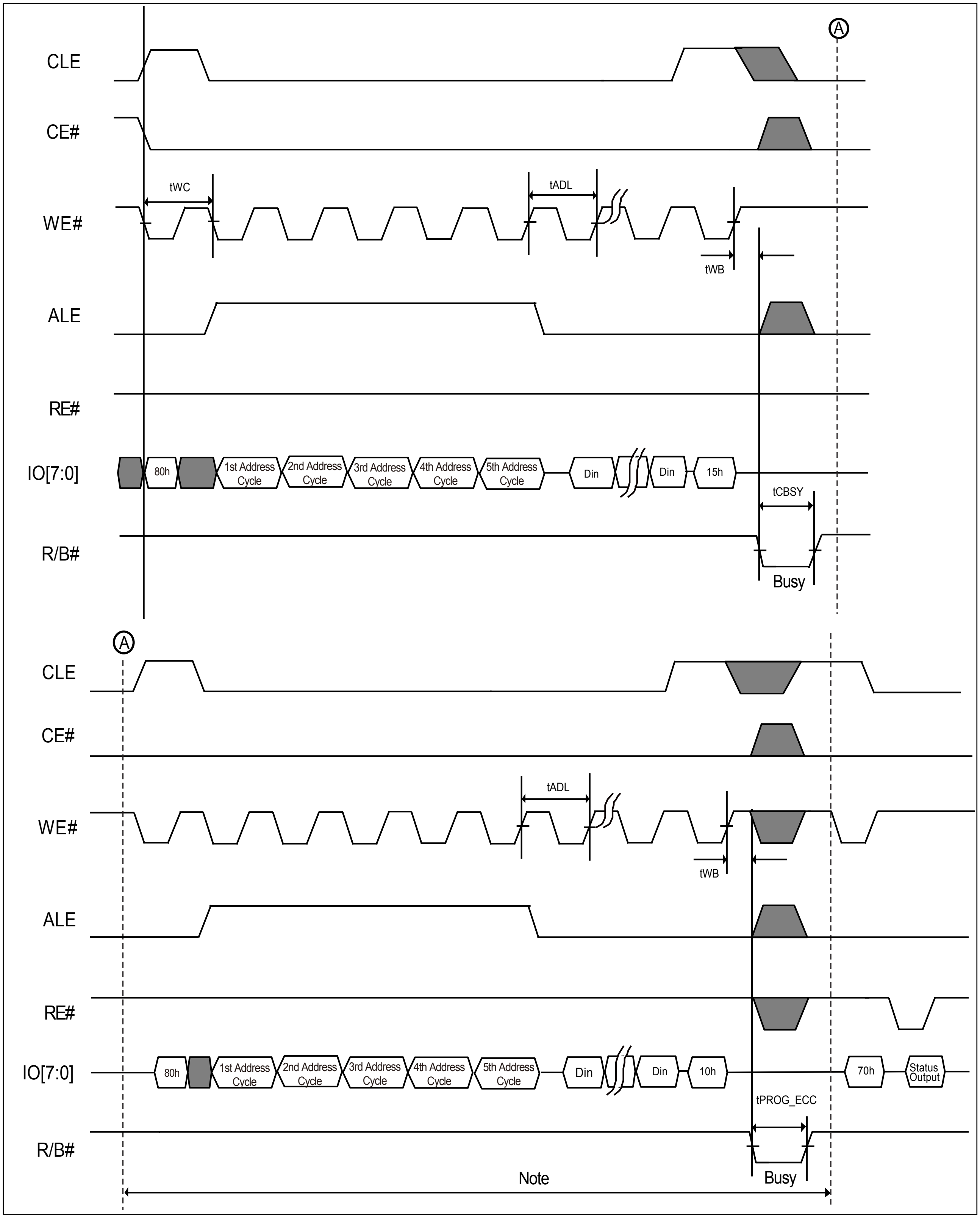
- Cache Status Bit (SR[6] = 0 indicates the cache is busy; SR[6] = 1 means the cache is ready).

The user can issue another Cache Program Command Sequence after the Cache is ready. The user can always monitor the chip state by Ready/Busy Status Bit (SR[5]). The user can issues either program confirm command (10h) or cache program command (15h) for the last page if the user monitor the chip status by issuing Read Status Command (70h).

However, if the user only monitors the R/B# pin, the user needs to issue the program confirm command (10h) for the last page.

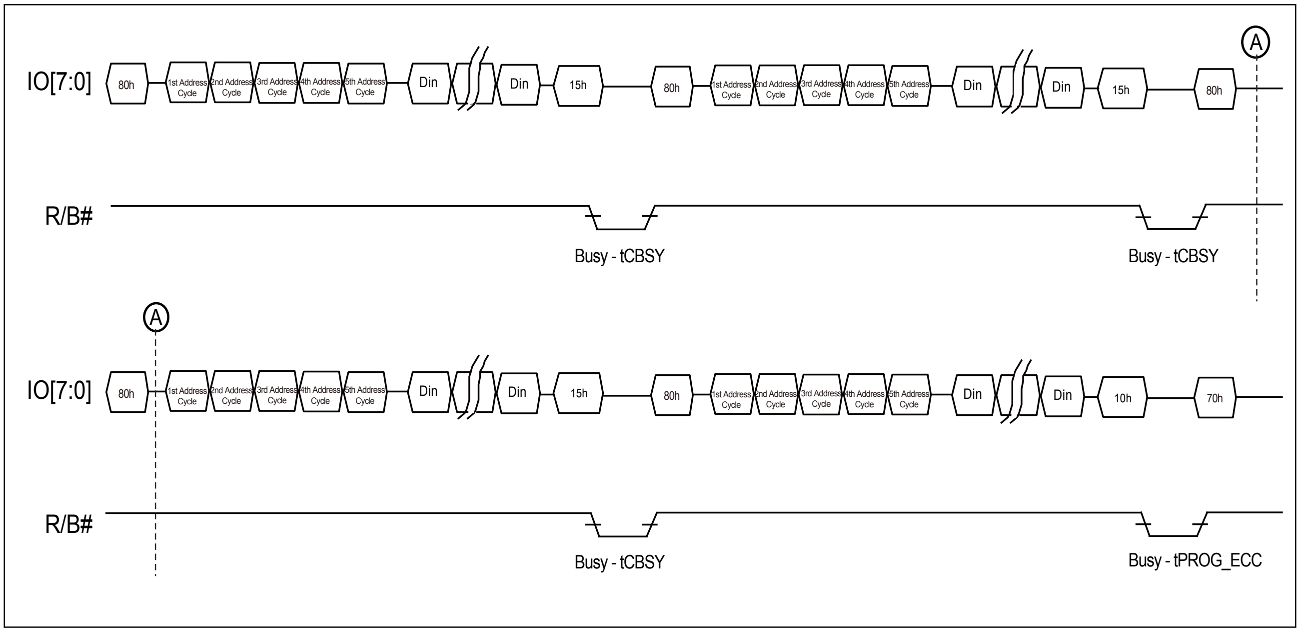
The user can check the Pass/Fail Status through P/F Status Bit (SR[0]) and Cache P/F Status Bit (SR[1]). SR[1] represents Pass/Fail Status of the previous page. SR[1] is updated when SR[6] change from 0 to 1 or Chip is ready. SR[0] shows the Pass/Fail status of the current page. It is updated when SR[5] change from "0" to "1" or the end of the internal programming.  For more details, please refer to the related waveforms.

## Figure 14-1. AC Waveforms for Cache Program




***Note:*** *It indicates the last page Input & Program.*

### Figure 14-2. AC Waveforms for Sequence of Cache Program




***Note:*** *tPROG_ECC = Page $_{(Last)}$ programming + Page $_{(Last-1)}$ programming time - Input cycle time of command & address - Data loading time of Page $_{(Last)}$.*

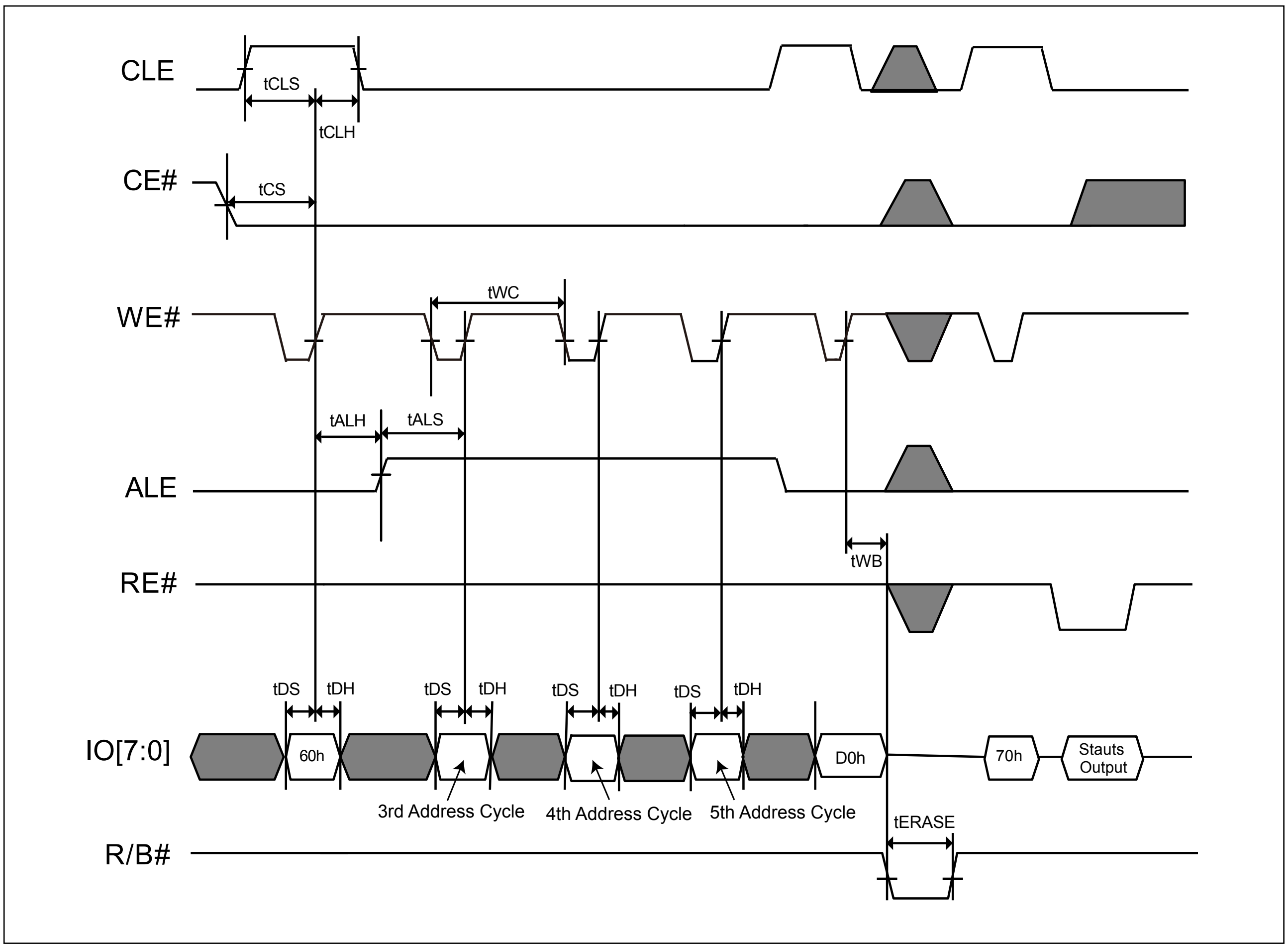
## 6-5. Block Erase

The MX30UFxGE8AB supports a block erase command. This command will erase a block of 64 pages associated with the most significant address bits.

The completion of the erase operation can be detected by R/B# pin or Status register bit (IO6). Recommend to check the status register bit IO0 after the erase operation completes.

During the erasing process, only the read status register command and reset command can be accepted, others are ignored.

### Figure 15. AC Waveforms for Erase Operation



## 6-6. ID Read

The device contains ID codes that identify the device type and the manufacturer. The ID READ command sequence includes one command Byte (90h), one address byte (00h). The Read ID command 90h may provide the manufacturer ID (C2h) of one-byte and device ID of one-byte, also Byte2, Byte3, and Byte4 ID code are followed.

The device support ONFI Parameter Page Read, by sending the ID Read (90h) command and following one byte address (20h), the four-byte data returns the value of 4Fh-4Eh-46h-49h for the ASCII code of "O"-"N"-"F"-"I" to identify the ONFI parameter page.

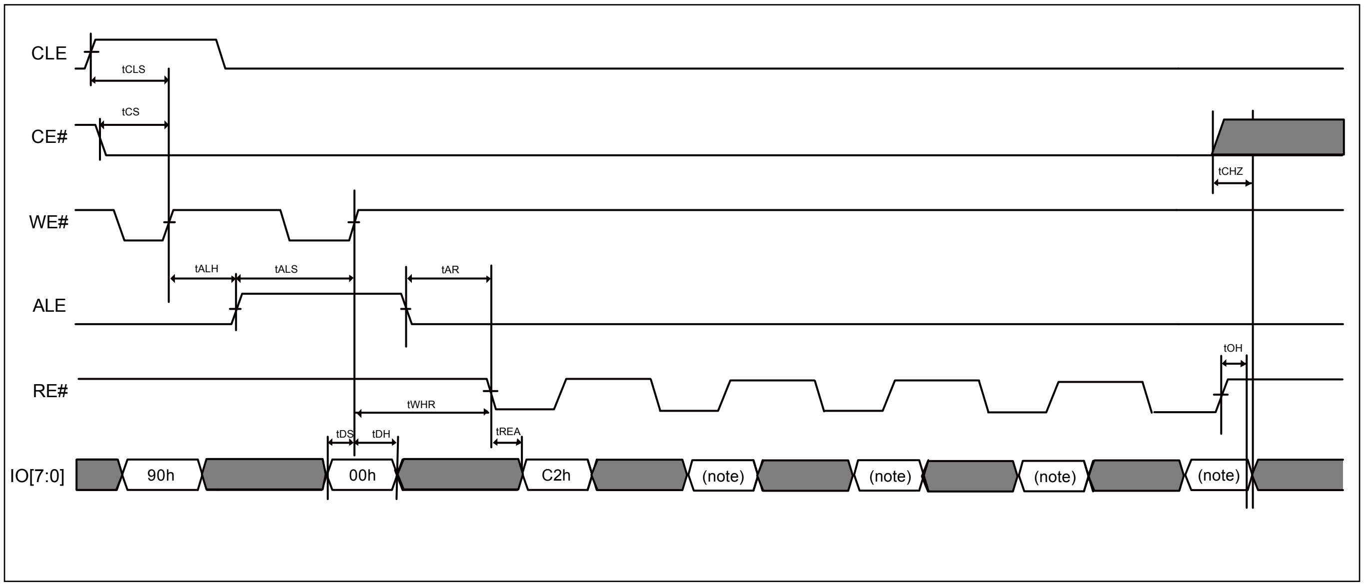
### Table 2. ID Codes Read Out by ID Read Command 90H

| **2Gb** | **2Gb, x8, 1.8V** |
|---|---|
| Byte0-Manufacturer | C2h |
| Byte1: Device ID | AAh |
| Byte2 | 90h |
| Byte3 | 15h |
| Byte4 | 86h |
| **4Gb** | **4Gb, x8, 1.8V** |
| Byte0-Manufacturer | C2h |
| Byte1: Device ID | ACh |
| Byte2 | 90h |
| Byte3 | 15h |
| Byte4 | D6h |

### Table 3. The Definition of Byte2~Byte4 of ID Table

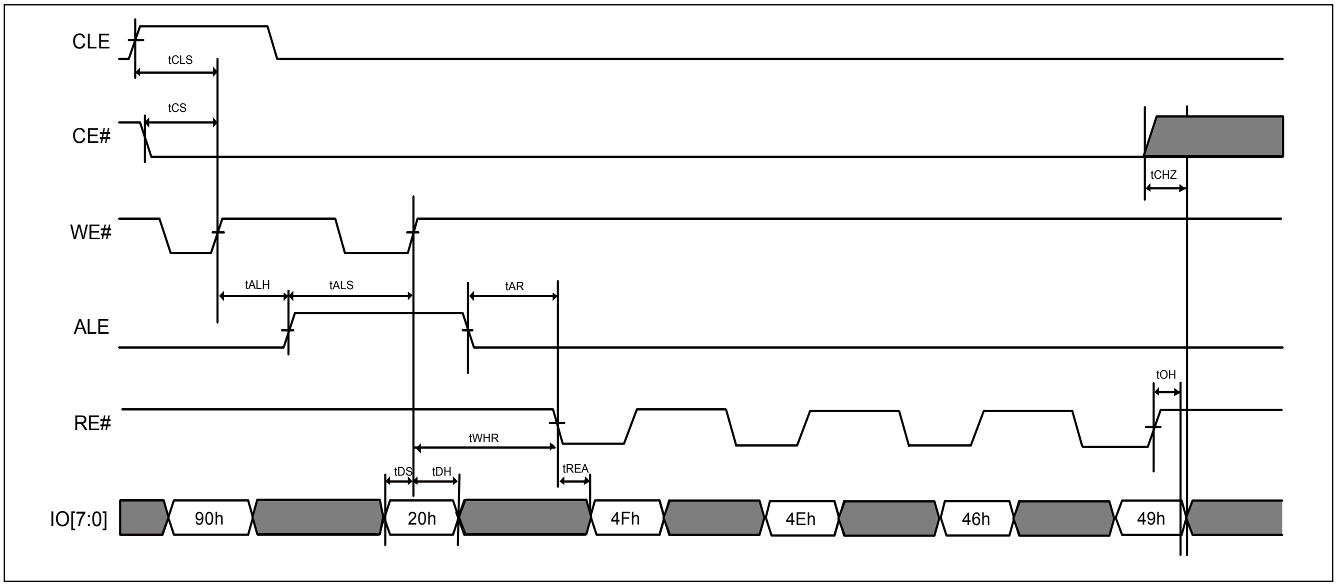
| Terms | Description | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|---|
| **Byte 2** | | | | | | | | | |
| **Die# per CE** | 1 | | | | | | | 0 | 0 |
| | 2 | | | | | | | 0 | 1 |
| **Cell type** | SLC | | | | | 0 | 0 | | |
| **# of Simultaneously Programmed page** | 1 | | | 0 | 0 | | | | |
| | 2 | | | 0 | 1 | | | | |
| **Interleaved operations between Multiple die** | Not supported | | 0 | | | | | | |
| **Cache Program** | Supported | 1 | | | | | | | |
| **Byte 3** | | | | | | | | | |
| **Page size** | 2KB | | | | | | | 0 | 1 |
| **Spare area size** | 64B | | | | | | 1 | | |
| **Block size (without spare)** | 128KB | | | 0 | 1 | | | | |
| **Organization** | x8 | | 0 | | | | | | |
| **Sequential access (min.)** | 25ns | 0 | | | | 0 | | | |
| **Byte 4** | | | | | | | | | |
| **Internal ECC level** | 4-bit ECC/524B | | | | | | | 1 | 0 |
| **#Plane per CE** | 1 | | | | | 0 | 0 | | |
| | 2 | | | | | 0 | 1 | | |
| | 4 | | | | | 1 | 0 | | |
| **Plane size** | | | 1 | 0 | 1 | | | | |
| **Internal ECC state** | ECC enabled | 1 | | | | | | | |

### Figure 16-1. AC Waveforms for ID Read Operation




***Note***: *See also* ***Table 2. ID Codes Read Out by ID Read Command 90H****.*

### Figure 16-2. AC Waveforms for ID Read (ONFI Identifier) Operation



## 6-7. Status Read

The MX30UFxGE8AB provides a status register that outputs the device status by writing a command code 70h, and then the IO pins output the status at the falling edge of CE# or RE# which occurs last. Even though when multiple flash devices are connecting in system and the R/B#pins are common-wired, the two lines of CE# and RE# may be checked for individual devices status separately.

The status read command 70h will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in **Table 4-1** and **Table 4-2.**

### Table 4-1. Status Output

| Pin | Status | Related Mode | Value | |
|---|---|---|---|---|
| **SR[0]** | Chip Status | Page Read, Page Program, Cache Program (Page N), Block Erase (Note 1) | 0: Passed | 1: Failed |
| **SR[1]** | Cache Program Result | Cache Program (Page N-1) | 0: Passed | 1: Failed |
| **SR[2]** | Not Used | | | |
| **SR[3]** | Internal ECC Status | Page Read (Note 1) | See ECC bits Table below | |
| **SR[4]** | Internal ECC Status | Page Read (Note 1) | See ECC bits Table below | |
| **SR[5]** | Ready / Busy (For P/E/R Controller) | Cache Program, other Page Program/Block Erase/Read are same as IO6 (Note 2) | 0: Busy | 1: Ready |
| **SR[6]** | Ready / Busy | Page Program, Block Erase, Cache Program, Read (Note 3) | 0: Busy | 1: Ready |
| **SR[7]** | Write Protect | Page Program, Block Erase, Cache Program, Read | 0: Protected | 1: Unprotected |

***Notes:***

1. *ECC status for current output page.*
2. *During the actual programming operation, the SR[5] is "0" value; however, when the internal operation is completed during the cache mode, the SR[5] returns to "1".*
3. *The SR[6] returns to "1" when the internal cache is available to receive new data. The SR[6] value is consistent with the R/B#.*

### Table 4-2. ECC Bits Status

| SR Bits and Value | | | Status of Error Bits Correction |
|---|---|---|---|
| SR[4] | SR[3] | SR[0] | |
| 0 | 0 | 1 | Uncorrectable |
| 0 | 0 | 0 | 0-1 bits error and been corrected |
| 1 | 0 | 0 | 2 bits error and been corrected |
| 0 | 1 | 0 | 3 bits error and been corrected |
| 1 | 1 | 0 | 4 bits error and been corrected |

The following is an example of a HEX data bit assignment:

**Figure 17. Bit Assignment (HEX Data)**

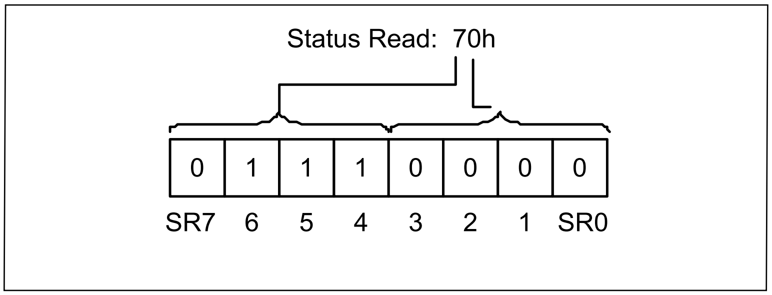
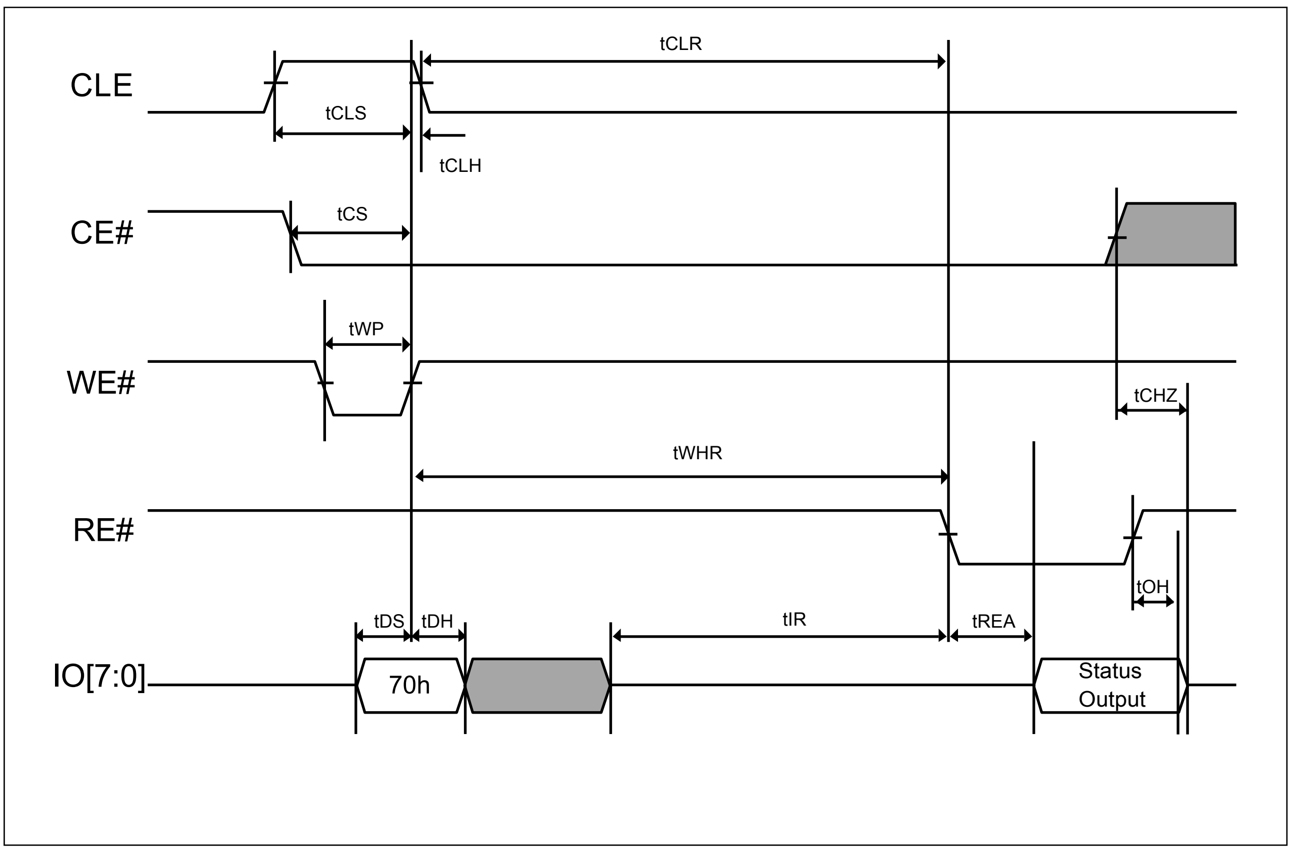



**Figure 18. AC Waveforms for Status Read Operation**

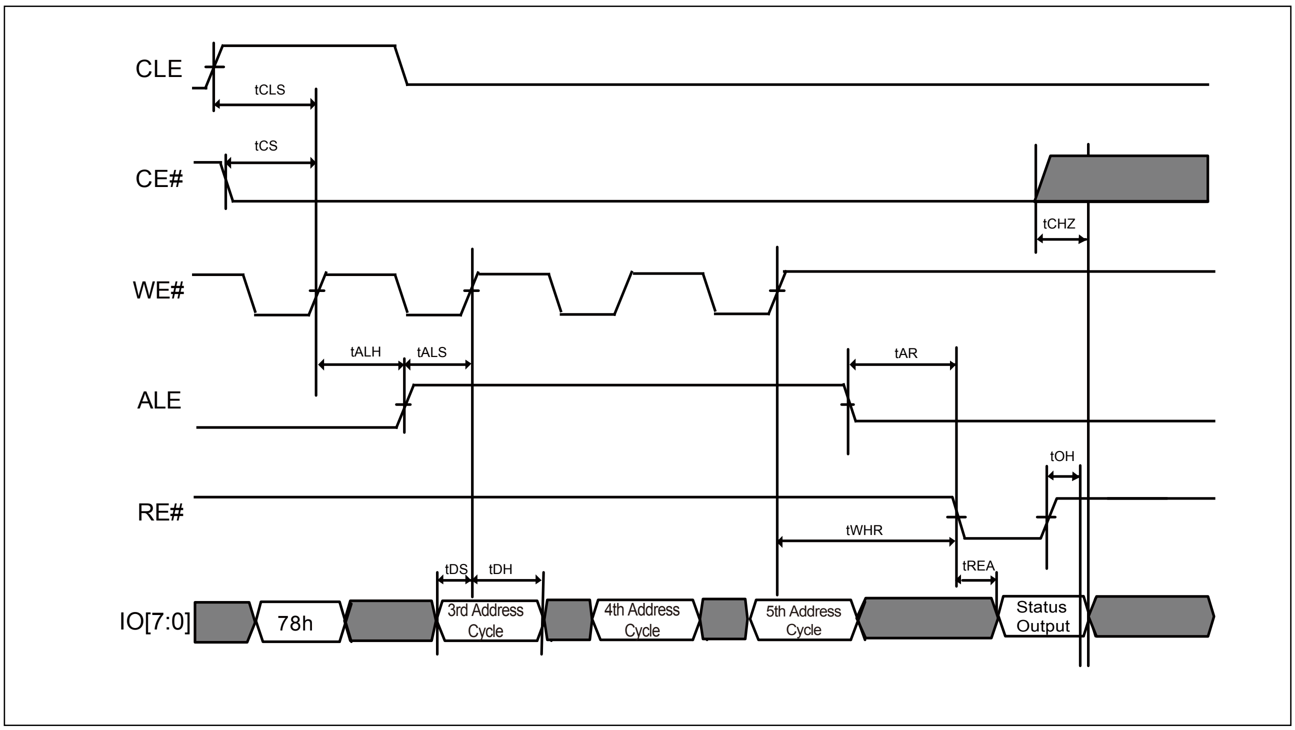


## 6-8. Status Enhance Read

The 2Gb and 4Gb support the two-plane operation, the Status Enhanced Read command (78h) offers the alternative method besides the Status Read command to get the status of specific plane in the same NAND Flash device. The result information is outlined in **Table 4-1** and **Table 4-2.**

The SR[6] and SR[5] bits are shared with all planes. However, the SR[0], SR[1], SR[3], SR[4] are for the status of specific plane in the row address. The Status Enhanced Read command is not allowed at power-on Reset (FFh) command and OTP enabled.

**Figure 19. AC Waveforms for Status Enhance Operation**

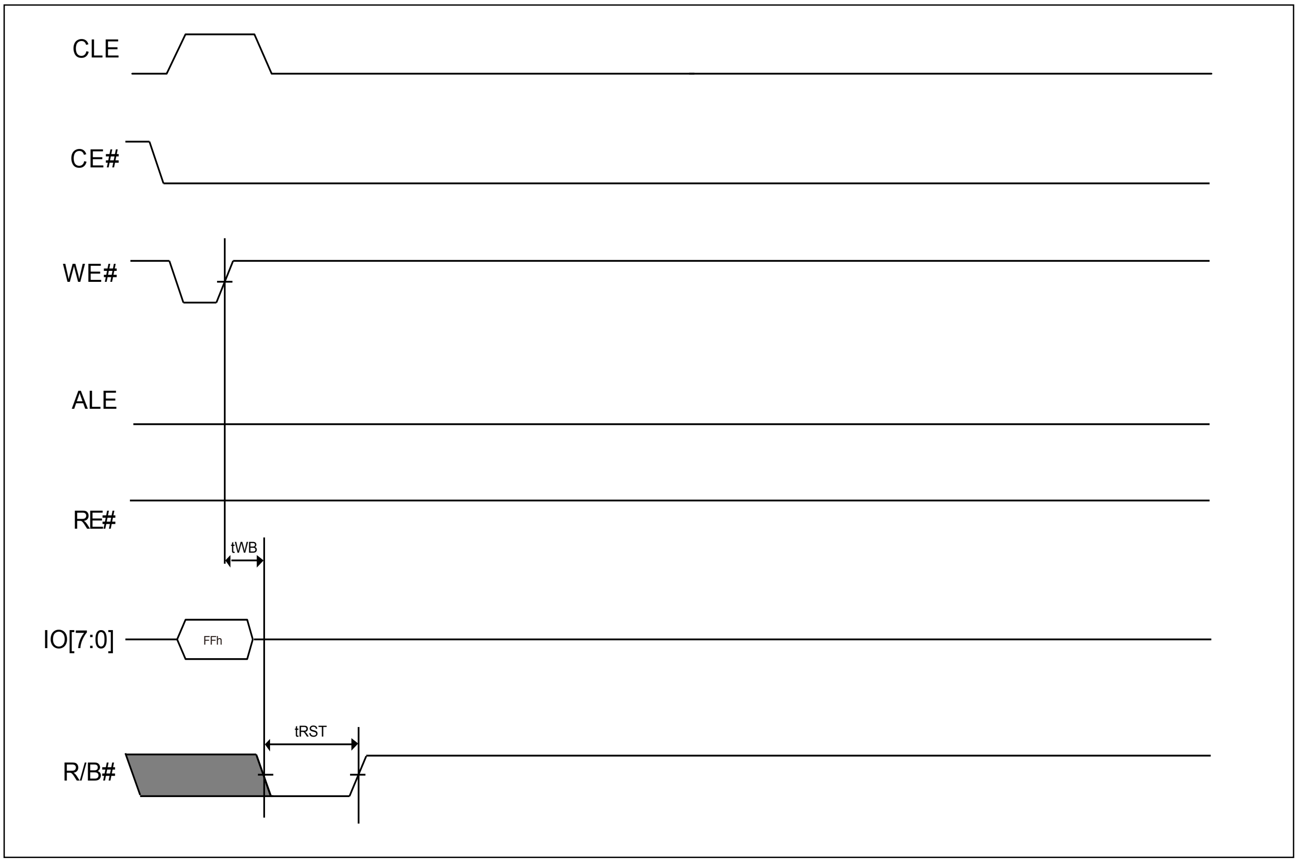


## 6-9. Reset

The reset command FFh resets the read/program/erase operation and clear the status register to be E0h (when WP# is high). The reset command during the program/erase operation will result in the content of the selected locations(perform programming/erasing) might be partially programmed/erased.

If the Flash memory has already been set to reset stage with reset command, the additional new reset command is invalid.

### Figure 20. AC waveforms for Reset Operation



## 6-10. Parameter Page Read (ONFI)

The NAND Flash device support ONFI Parameter Page Read and the parameter can be read out by sending the command of ECh and giving the address 00h. The NAND device information may refer to the table of parameter page(ONFI), there are three copies of 256-byte data and additional redundant parameter pages.

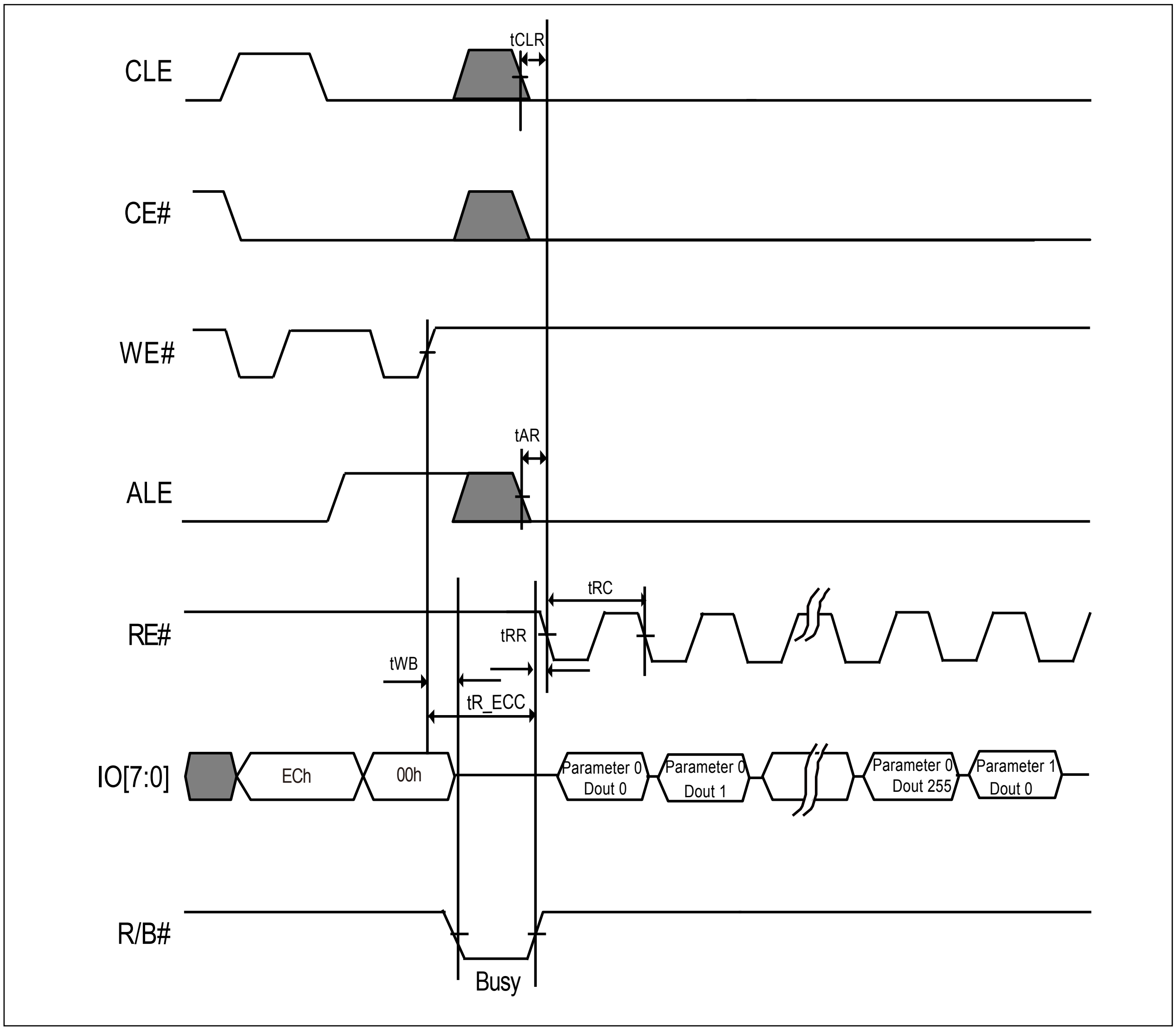
Once sending the ECh command, the NAND device will remain in the Parameter Page Read mode until next valid command is sent.

The Random Data Out command set (05h-E0h) can be used to change the parameter location for the specific parameter data random read out.

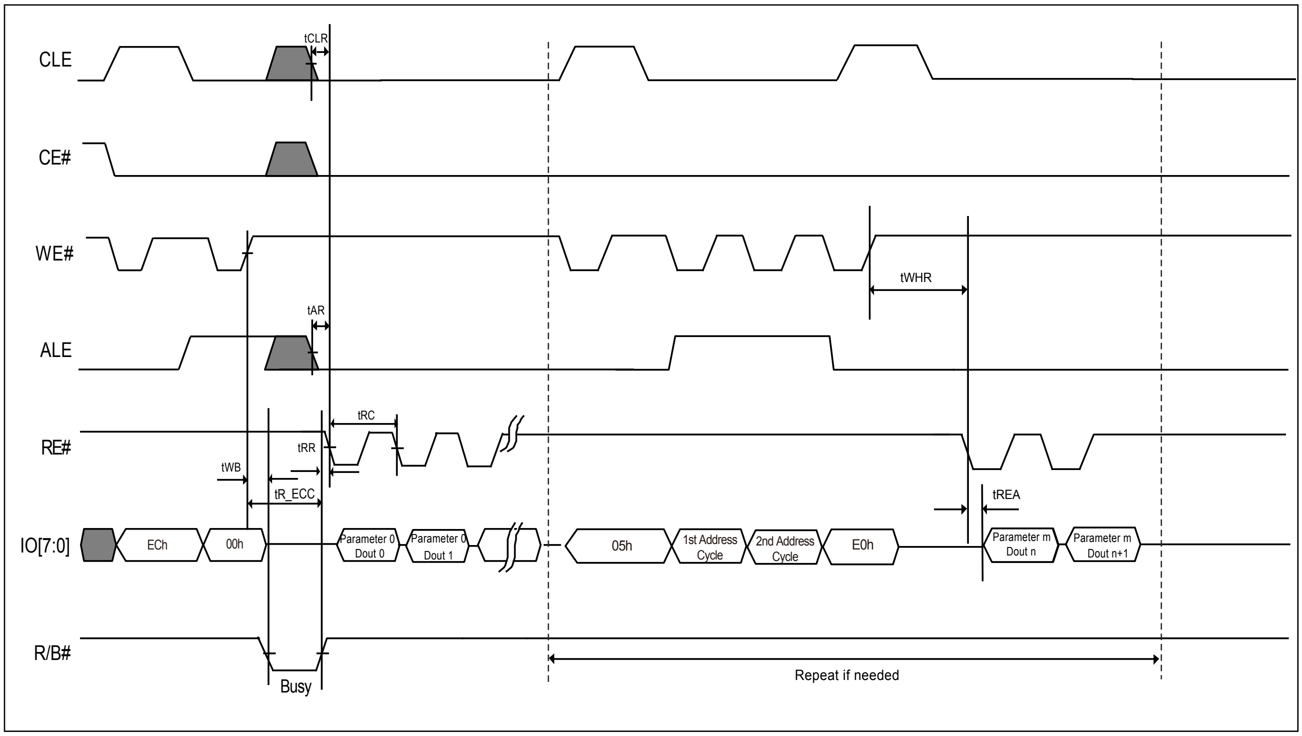
The Status Read command (70h) can be used to check the completion with a following read command (00h) to enable the data out.

The internal ECC is disabled on the parameter page.

**Figure 21. AC waveforms for Parameter Page Read (ONFI) Operation**



## Figure 22. AC Waveforms for Parameter Page Read (ONFI) Random Operation (For 05h-E0h)



## Table 5. Parameter Page (ONFI)

**ONFI Table below is for MX30UF2GE8AB-XKI**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | Parameter Page Signature | | 4Fh,4Eh,46h,49h |
| **4-5** | Revision Number | | 02h,00h |
| **6-7** | Features Supported | | 18h,00h |
| **8-9** | Optional Commands Supported | | 3Dh,00h |
| **10-31** | Reserved | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | Device Manufacturer (12 ASCII characters) | | 4Dh,41h,43h,52h,4Fh,4Eh,49h,58h, 20h,20h,20h,20h |
| **44-63** | Device Model (20 ASCII Characters) | MX30UF2GE8AB | 4Dh,58h,33h,30h,55h,46h,32h,47h,45h,38h,41h,42h,20h,20h,20h,20h,20h,20h,20h,20h |
| **64** | JEDEC Manufacturer ID | | C2h |
| **65-66** | Date Code | | 00h,00h |
| **67-79** | Reserved | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 2048-byte | 00h,08h,00h,00h |
| **84-85** | Number of Spare Bytes per Page | 64-byte | 40h,00h |
| **86-89** | Number of Data Bytes per Partial Page | 512-byte | 00h,02h,00h,00h |
| **90-91** | Number of Spare Bytes per Partial Page | 16-byte | 10h,00h |
| **92-95** | Number of Pages per Block | | 40h,00h,00h,00h |
| **96-99** | Number of Blocks per Logical Unit | | 00h,08h,00h,00h |
| **100** | Number of Logical Units (LUNs) | | 01h |
| **101** | Number of Address Cycles | | 23h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per LUN | | 28h,00h |
| **105-106** | Block endurance | | 01h,05h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 01h |
| **108-109** | Block endurance for guaranteed valid blocks | | 01h,03h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partial Programming Attributes | | 00h |
| **112** | Number of Bits ECC Correctability | | 00h |
| **113** | Number of Interleaved Address Bits | | 01h |
| **114** | Interleaved Operation Attributes | | 0Eh |
| **115-127** | Reserved | | 00h |

| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support | | 1Fh,00h |
| **131-132** | Program Cache Timing Mode Support | | 1Fh,00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 600us | 58h,02h |
| **135-136** | tBERS(tERASE) Maximum Block Erase Time (uS) | 3500us | ACh,0Dh |
| **137-138** | tR Maximum Page Read Time (uS) | 70us | 46h,00h |
| **139-140** | tCCS Minimum Change Column Setup Time (ns) | 80ns | 50h,00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h,00h |
| **166** | Security feature (permanently block-locked) support | | 00h |
| **167-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **512-767** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **768+** | Additional Redundant Parameter Pages | | |

***Note***:

*The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*
$G(X) = X^{16} + X^{15} + X^2 + 1$

**ONFI Table below is for MX30UF4GE8AB-XKI**

| | Revision Information and Features Block | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **0-3** | Parameter Page Signature | | 4Fh,4Eh,46h,49h |
| **4-5** | Revision Number | | 02h,00h |
| **6-7** | Features Supported | | 18h,00h |
| **8-9** | Optional Commands Supported | | 3Dh,00h |
| **10-31** | Reserved | | 00h |
| | **Manufacturer Information Block** | | |
| **Byte#** | **Description** | | **Data** |
| **32-43** | Device Manufacturer (12 ASCII characters) | | 4Dh,41h,43h,52h,4Fh,4Eh,49h,58h,20h,20h,20h,20h |
| **44-63** | Device Model<br>(20 ASCII Characters) | MX30UF4GE8AB | 4Dh,58h,33h,30h,55h,46h,34h,47h,45h,38h,41h,42h,20h,20h,20h,20h,20h,20h,20h,20h |
| **64** | JEDEC Manufacturer ID | | C2h |
| **65-66** | Date Code | | 00h,00h |
| **67-79** | Reserved | | 00h |

| Memory Organization Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **80-83** | Number of Data Bytes per Page | 2048-byte | 00h,08h,00h,00h |
| **84-85** | Number of Spare Bytes per Page | 64-byte | 40h,00h |
| **86-89** | Number of Data Bytes per Partial Page | 512-byte | 00h,02h,00h,00h |
| **90-91** | Number of Spare Bytes per Partial Page | 16-byte | 10h,00h |
| **92-95** | Number of Pages per Block | | 40h,00h,00h,00h |
| **96-99** | Number of Blocks per Logical Unit | | 00h,10h,00h,00h |
| **100** | Number of Logical Units (LUNs) | | 01h |
| **101** | Number of Address Cycles | | 23h |
| **102** | Number of Bits per Cell | | 01h |
| **103-104** | Bad Blocks Maximum per LUN | | 50h,00h |
| **105-106** | Block endurance | | 01h,05h |
| **107** | Guarantee Valid Blocks at Beginning of Target | | 01h |
| **108-109** | Block endurance for guaranteed valid blocks | | 01h,03h |
| **110** | Number of Programs per Page | | 04h |
| **111** | Partial Programming Attributes | | 00h |
| **112** | Number of Bits ECC Correctability | | 00h |
| **113** | Number of Interleaved Address Bits | | 01h |
| **114** | Interleaved Operation Attributes | | 0Eh |
| **115-127** | Reserved | | 00h |

| Electrical Parameters Block | | | |
|---|---|---|---|
| **Byte#** | **Description** | | **Data** |
| **128** | I/O Pin Capacitance | | 0Ah |
| **129-130** | Timing Mode Support | | 1Fh,00h |
| **131-132** | Program Cache Timing Mode Support | | 1Fh,00h |
| **133-134** | tPROG Maximum Page Program Time (uS) | 600us | 58h,02h |
| **135-136** | tBERS(tERASE) Maximum Block Erase Time (uS) | 3500us | ACh,0Dh |
| **137-138** | tR Maximum Page Read Time (uS) | 70us | 46h,00h |
| **139-140** | tCCS Minimum Change Column Setup Time (ns) | 80ns | 50h,00h |
| **141-163** | Reserved | | 00h |
| **Vendor Blocks** | | | |
| **Byte#** | **Description** | | **Data** |
| **164-165** | Vendor Specific Revision Number | | 00h,00h |
| **166** | Security feature (permanently block-locked) support | | 00h |
| **167-253** | Vendor Specific | | 00h |
| **254-255** | Integrity CRC | | Set at Test ***(Note)*** |
| **Redundant Parameter Pages** | | | |
| **Byte#** | **Description** | | **Data** |
| **256-511** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **512-767** | Value of Bytes 0-255 | | Same as 0~255 Byte |
| **768+** | Additional Redundant Parameter Pages | | |

***Note***:
*The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.*

*The CRC shall be calculated using the following 16-bit generator polynomial:*
$G(X) = X^{16} + X^{15} + X^2 + 1$

## 6-11. Unique ID Read (ONFI)

The unique ID is 32-byte and with 16 copies for back-up purpose. After writing the Unique ID read command (EDh) and following the one address byte (00h), the host may read out the unique ID data. The host need to XOR the 1st 16-byte unique data and the 2nd 16-byte complement data to get the result, if the result is FFh, the unique ID data is correct; otherwise, host need to repeat the XOR with the next copy of Unique ID data.

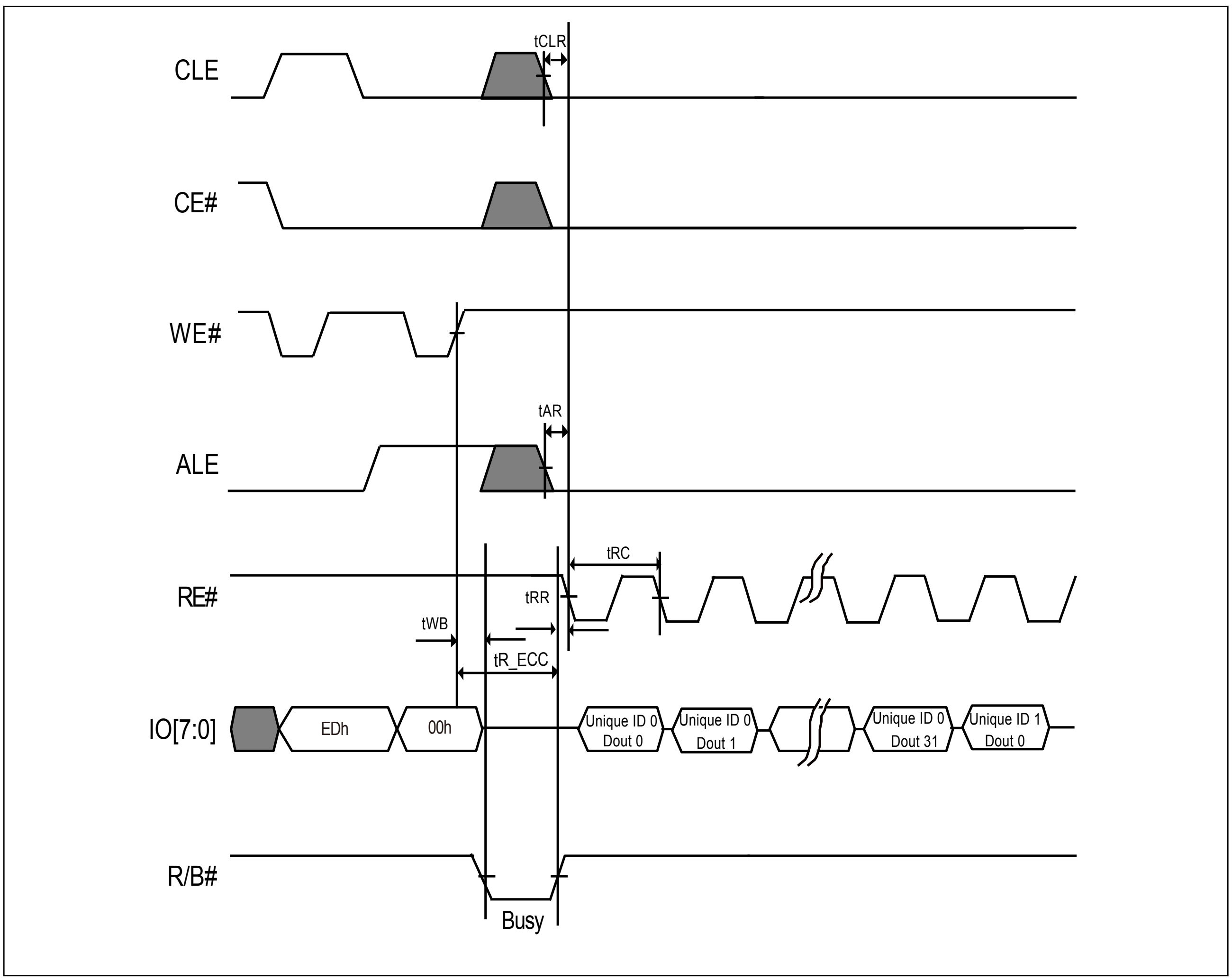
Once sending the EDh command, the NAND device will remain in the Unique ID read mode until next valid command is sent.

To change the data output location, it is recommended to use the Random Data Out command set (05h-E0h).

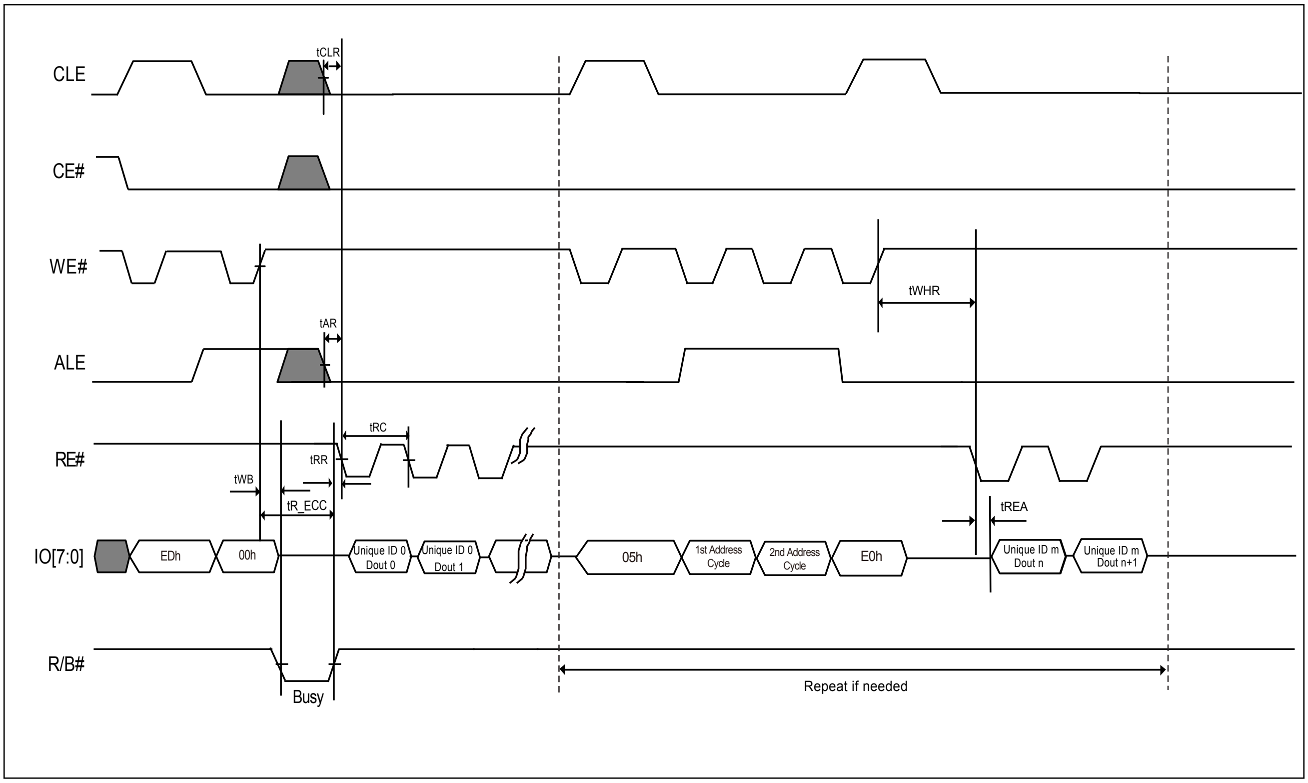
The Status Read command (70h) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

The internal ECC is disabled on the unique ID.

**Figure 23. AC waveforms for Unique ID Read Operation**



### Figure 24. AC waveforms for Unique ID Read Operation (For 05h-E0h)



## 6-12. Feature Set Operation (ONFI)

The Feature Set operation is to change the default power-on feature sets by using the Set Feature and Get Feature command and writing the specific parameter data (P1-P4) on the specific feature addresses. The NAND device may remain the current feature set until next power cycle since the feature set data is volatile. However, the reset command (FFh) can not reset the current feature set.

### Table 6-1. Definition of Feature Address

| Feature Address | Description |
|---|---|
| 00h-8Fh, 91h-FFh | Reserved |
| 90h | Array Operation Mode |

### Table 6-2. Sub-Feature Parameter Table of Feature Address - 90h (Array Operation Mode)

| Sub Feature Parameter | Definition | | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | Values | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P1 | Array Operation Mode | Normal | Reserved (0) | | | | 1 | 0 | 0 | 0 | 0000 1000b | 1 |
| | | OTP Operation | Reserved (0) | | | | 1 | 0 | 0 | 1 | 0000 1001b | |
| | | OTP Protection | Reserved (0) | | | | 1 | 0 | 1 | 1 | 0000 1011b | |
| P2 | | | Reserved (0) | | | | | | | | 0000 0000b | |
| P3 | | | Reserved (0) | | | | | | | | 0000 0000b | |
| P4 | | | Reserved (0) | | | | | | | | 0000 0000b | |

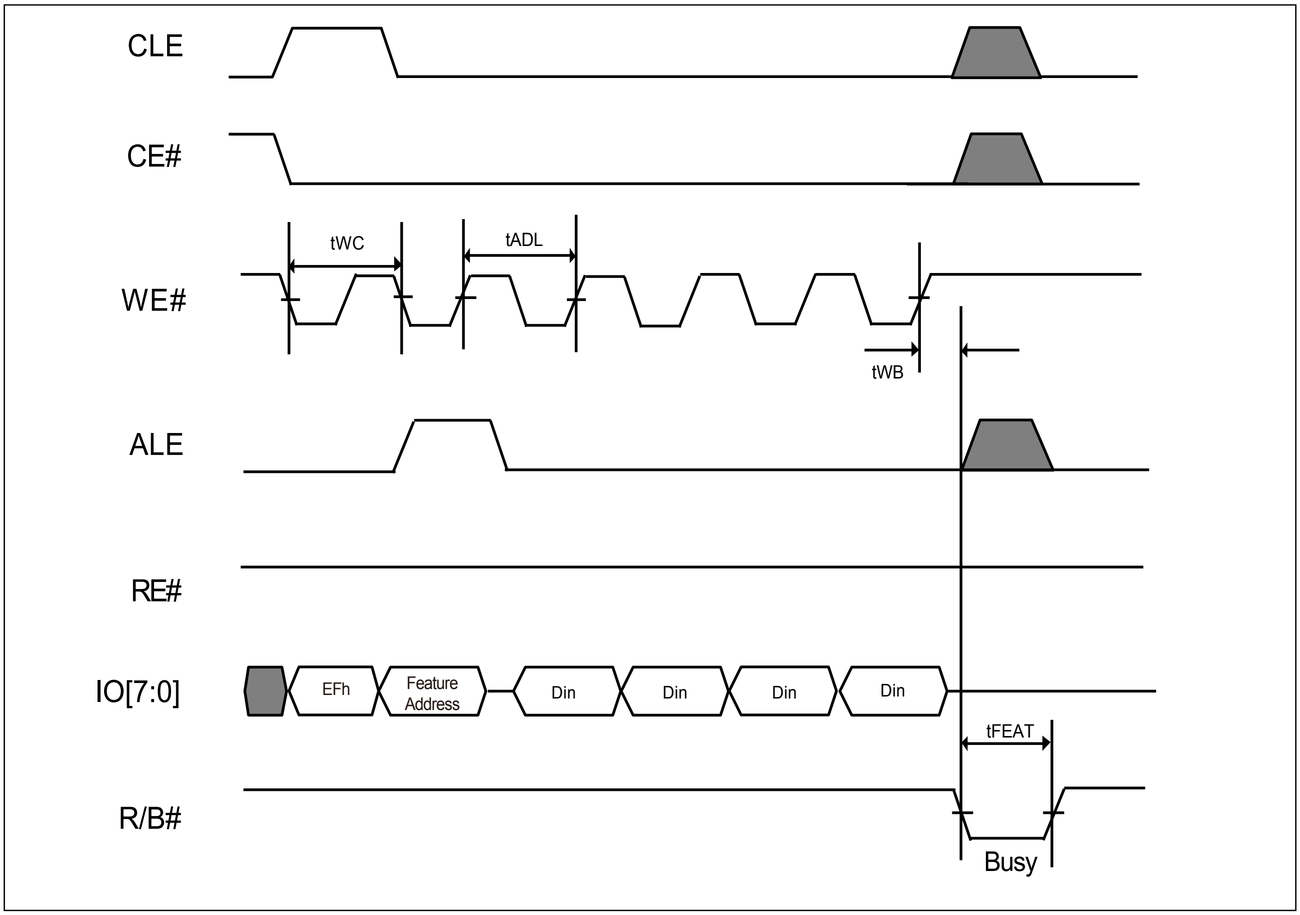
***Note 1:*** *The value is clear to 08h at power cycle.*

### 6-12-1. Set Feature (ONFI)

The Set Feature command is to change the power-on default feature set. After sending the Set Feature command (EFh) and following specific feature and then input the P1-P4 parameter data to change the default power-on feature set. Once sending the EFh command, the NAND device will remain in the Set Feature mode until next valid command is sent.

The Status Read command (70h) may check the completion of the Set Feature.

#### Figure 25. AC Waveforms for Set Feature (ONFI) Operation



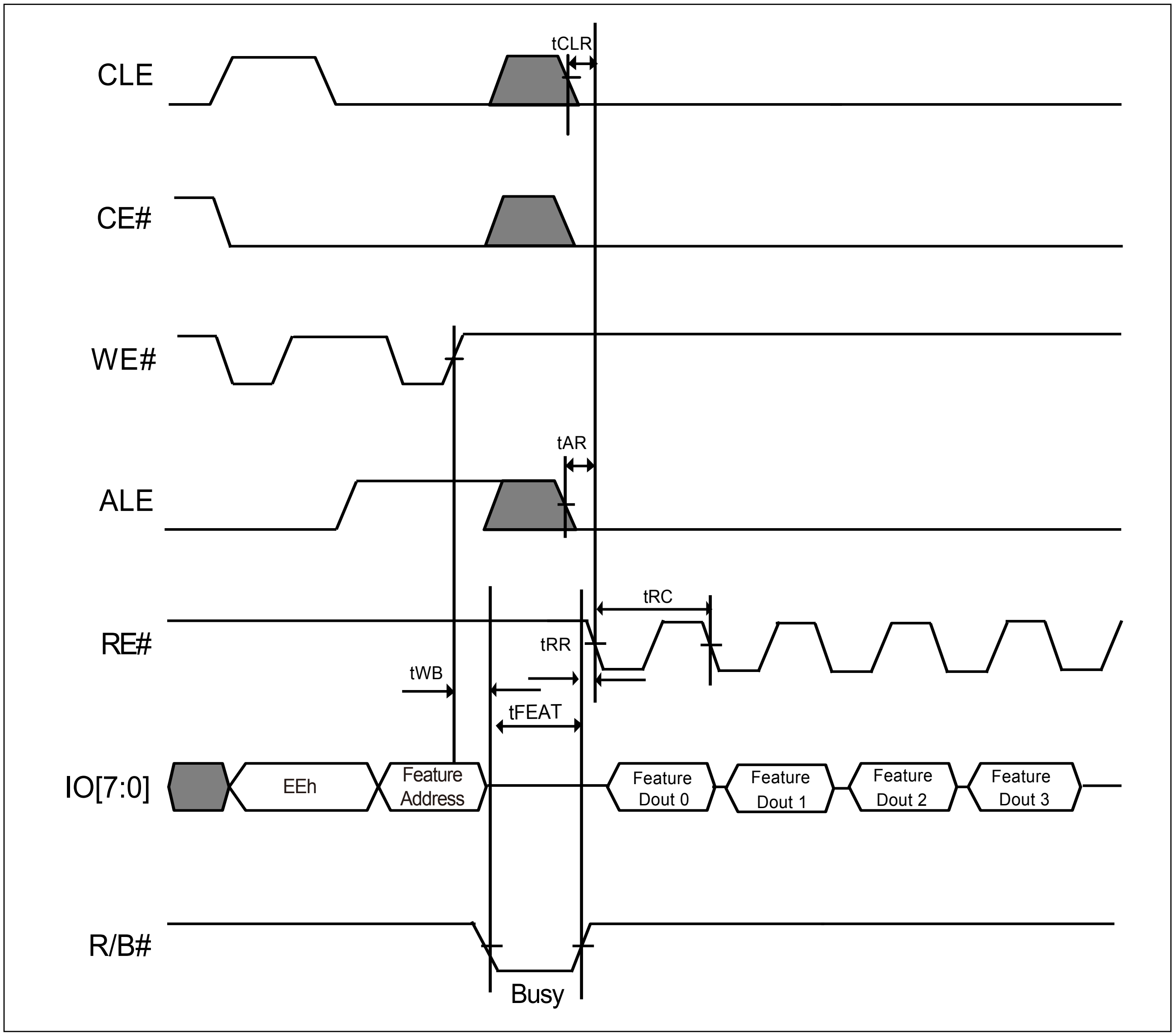
## 6-12-2. Get Feature (ONFI)

The Get Feature command is to read sub-feature parameter. After sending the Get Feature command (EEh) and following specific feature, the host may read out the P1-P4 sub- feature parameter data. Once sending the EEh command, the NAND device will remain in the Get Feature mode until next valid command is sent.

The Status Read command (70h) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Please refer to the following waveform of **Get Feature Operation** for details.

### Figure 26. AC Waveforms for Get Feature (ONFI) Operation



### 6-12-3. Secure OTP (One-Time-Programmable) Feature

There is an OTP area which has thirty full pages (30 x 2112-byte) guarantee to be good for system device serial number storage or other fixed code storage. The OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows whole page or partial page program to be “0”, once the OTP protection mode is set, the OTP area becomes read-only and cannot be programmed again.

The OTP operation is operated by the Set Feature/ Get Feature operation to access the OTP operation mode and OTP protection mode.

To check the NAND device is ready or busy in the OTP operation mode, either checking the R/B# or writing the Status Read command (70h) may collect the status.

To exit the OTP operation or protect mode, it can be done by writing 08h to P1 at feature address 90h.

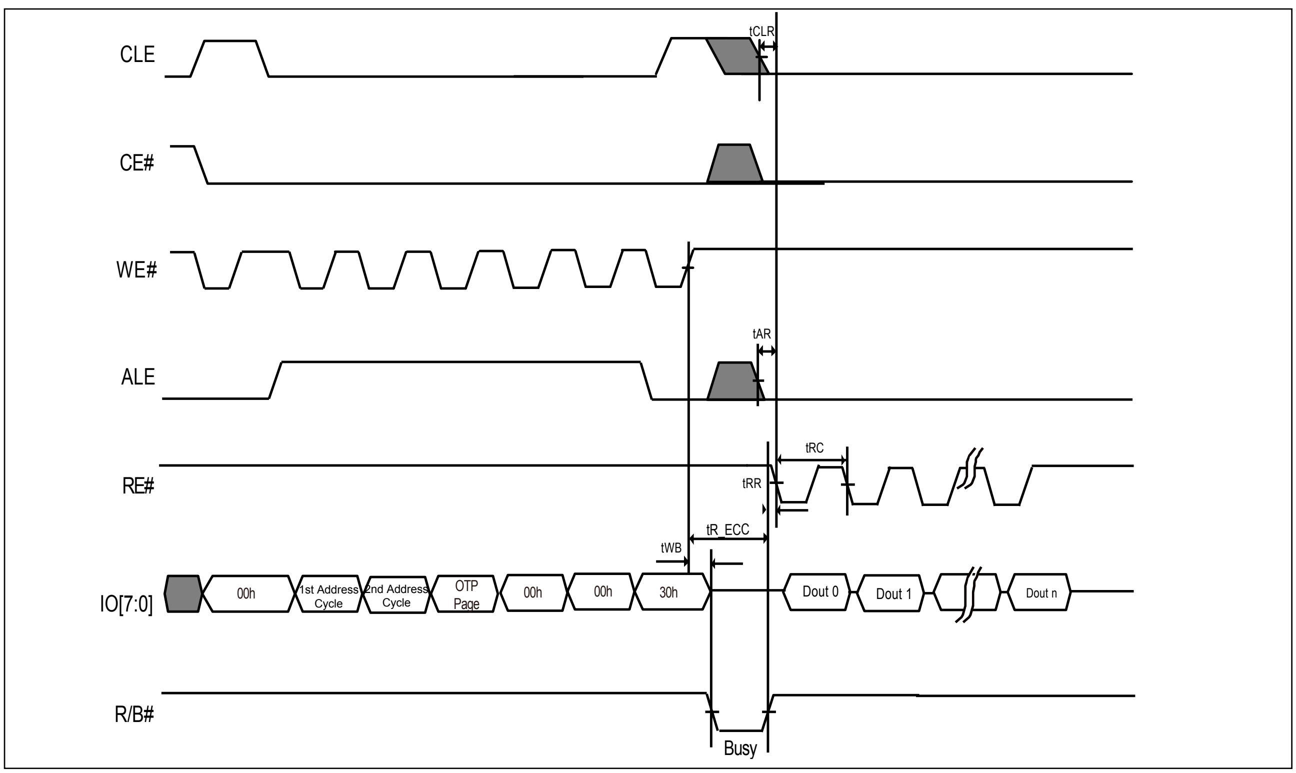
#### OTP Read/Program Operation

To enter the OTP operation mode, it is by using the Set Feature command (EFh) and followed by the feature address (90h) and then input the 01h to P1 and 00h to P2-P4 of sub-Feature Parameter data( please refer to the sub-Feature Parameter table). After enter the OTP operation mode, the normal Read command (00h-30h) or Page program( 80h-10h) command can be used to read the OTP area or program it. The address of OTP is located on the 02h-1Fh of page address.

Besides the normal Read command, the Random Data Output command (05h-E0h) can be used for read OTP data.

Besides the normal page program command, the Random Data Input command (85h) allows multi-data load in non-sequential address. After data load is completed, a program confirm command (10h) is issued to start the page program operation. The number of partial-page OTP program is 4 per each OTP page.

**Figure 27. AC Waveforms for OTP Data Read**



## Figure 28. AC Waveforms for OTP Data Read with Random Data Output

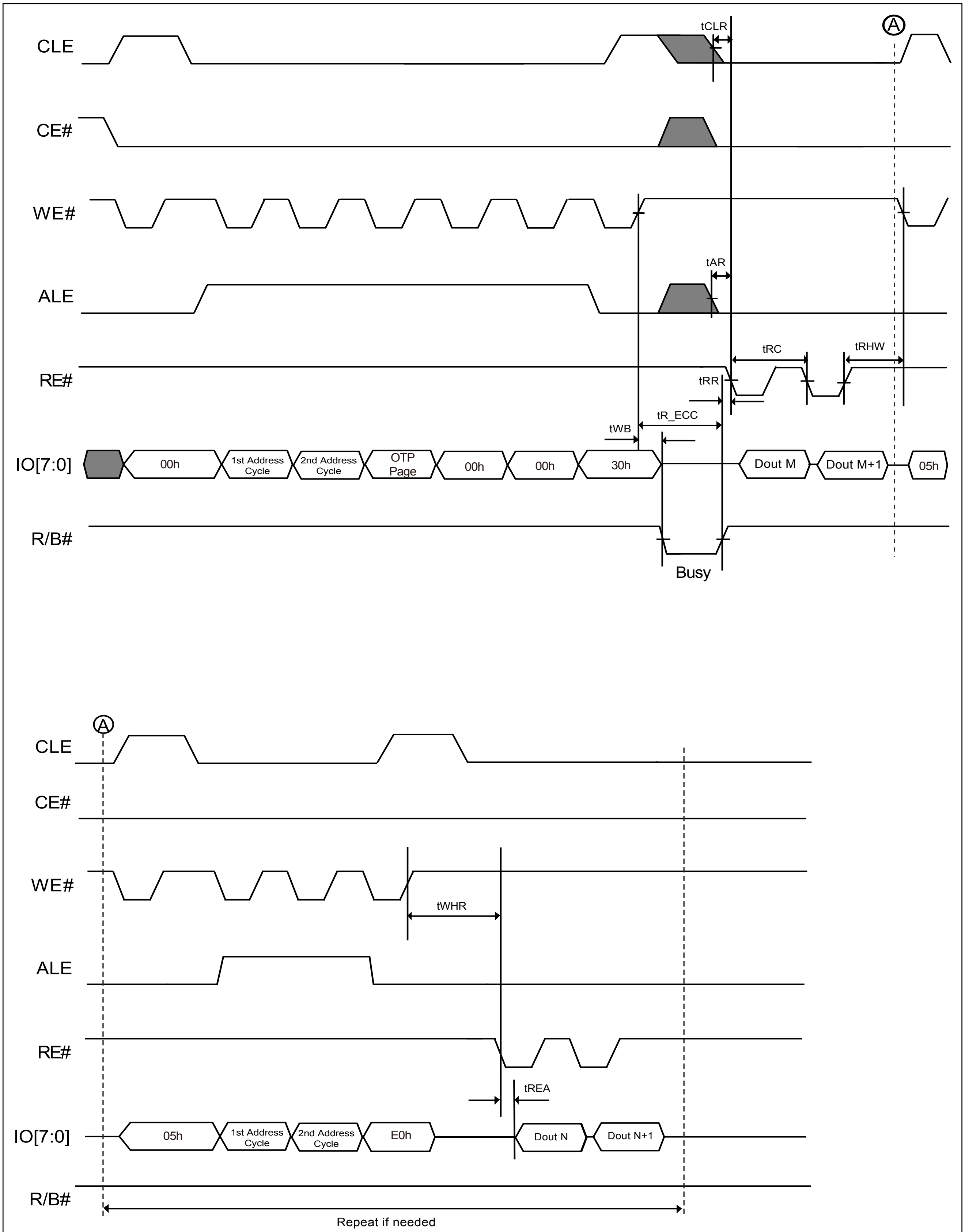
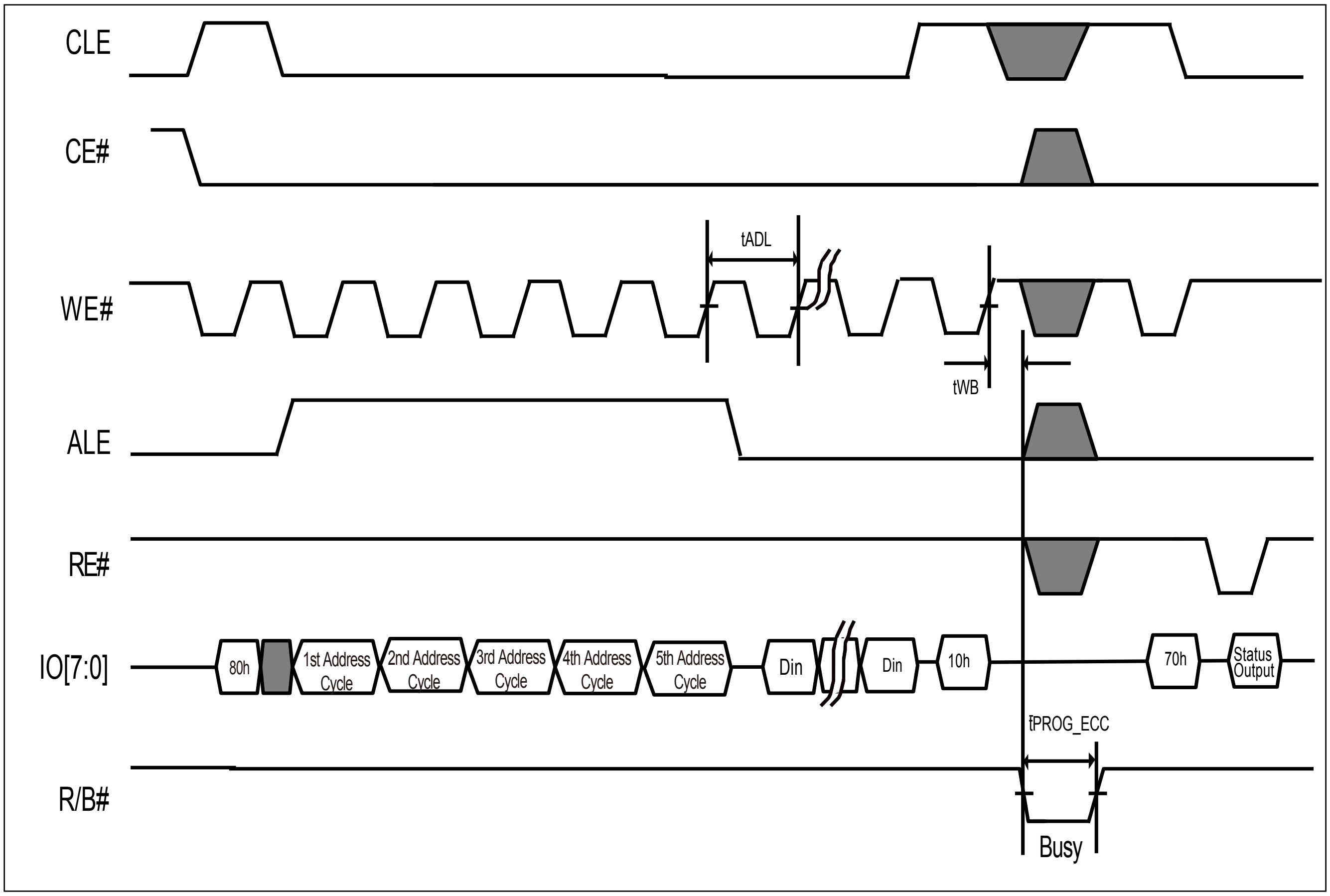
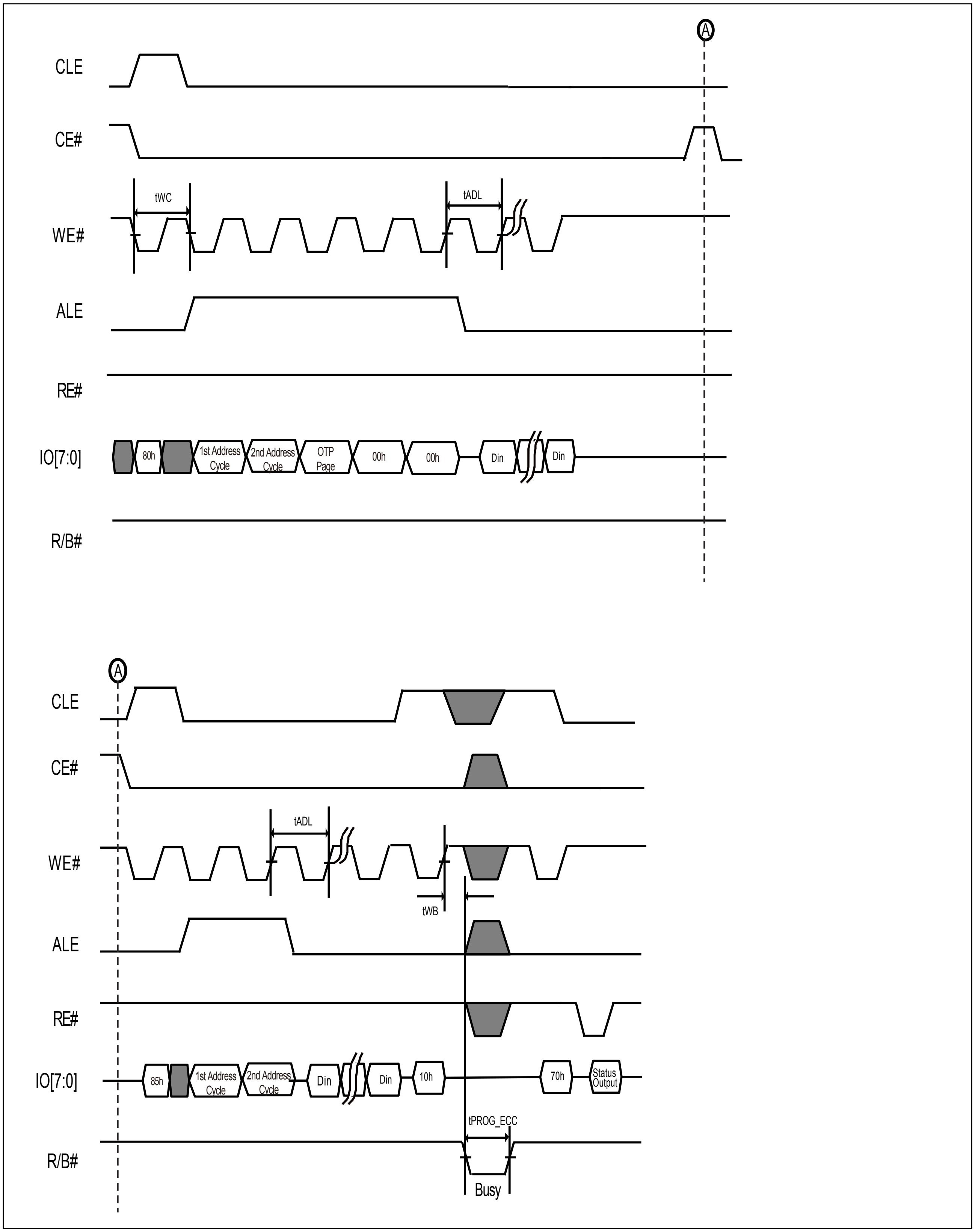


**Figure 29. AC Waveforms for OTP Data Program**



### Figure 30. AC Waveforms for OTP Data Program with Random Data Input

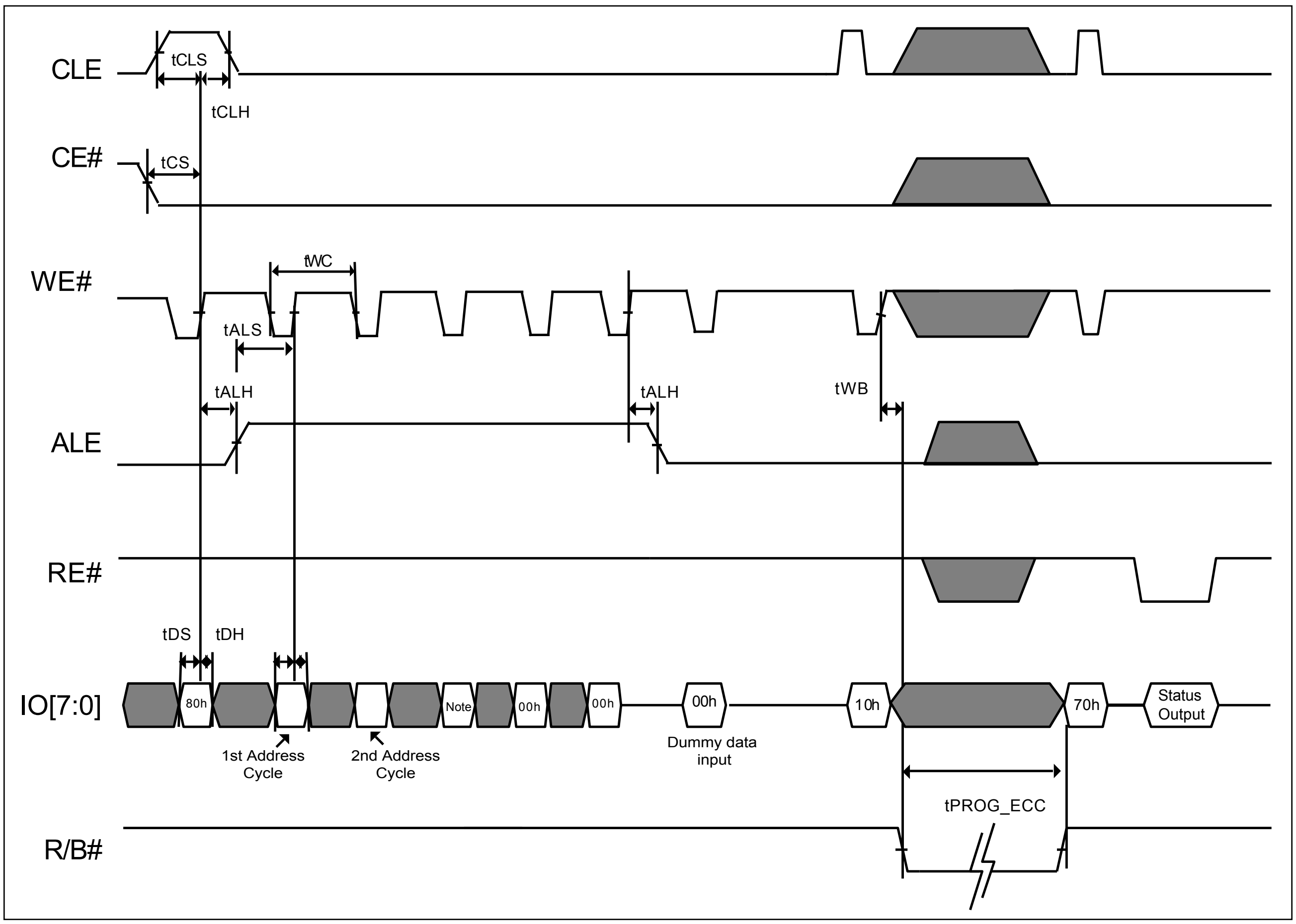


## OTP Protection Operation

To prevent the further OTP data to be changed, the OTP protection mode operation is necessary. To enter the OTP protection mode, it can be done by using the Set Feature command (EFh) and followed by the feature address (90h) and then input the 03h to P1 and 00h to P2-P4 of sub-Feature Parameter data (please refer to the sub-Feature Parameter table). And then the normal page program command (80h-10h) with the address 00h before the 10h command is required.

The OTP Protection mode is operated by the whole OTP area instead of individual OTP page. Once the OTP protection mode is set, the OTP area cannot be programmed or unprotected again.

### Figure 31. AC Waveforms for OTP Protection Operation




***Note***: *This address cycle can be any value since the OTP protection protects the entire OTP area instead of individual OTP page*

### 6-12-4. Internal ECC Always Enabled

The internal ECC logic may detect 5-bit error and correct 4-bit error. The internal ECC is always enabled. After the data transfer time (tR_ECC) is completed, a Status Read command (70h) is required to check any uncorrectable read error happened. Please refer to **"Table 4-1. Status Output" and "Table 4-2. ECC Bits Status".**

The constraint of the internal ECC operation:

- The ECC protection coverage: please refer to **Table 7-1 & 7-2. The Distribution of ECC Segment and Spare Area**. Only the grey areas are under internal ECC protection when the internal ECC is enabled.
- The number of partial-page program is not 4 in an ECC segment, the user need to program the main area (512B) + spare area (1st 8-byte for 4Gb and whole 16-byte for 2Gb) together at one time of program operation, so the ECC parity code can be calculated properly and stored in the additional hidden spare area.

#### Table 7-1 For 4Gb, the Distribution of ECC Segment and Spare Area in a Page

| **Main Area (2KB)** | | | | **Spare Area (64B)** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Main0 | Main1 | Main2 | Main3 | Spare0(16B) | | Spare1(16B) | | Spare2(16B) | | Spare3(16B) | |
| (512B) | (512B) | (512B) | (512B) | 8B | 8B (Reserved) | 8B | 8B (Reserved) | 8B | 8B (Reserved) | 8B | 8B (Reserved) |

***Note***: *Grey color area: Under ECC protection*

#### Table 7-2 For 2Gb, the Distribution of ECC Segment and Spare Area in a Page

| **Main Area (2KB)** | | | | **Spare Area (64B)** | | | |
|---|---|---|---|---|---|---|---|
| Main0 | Main1 | Main2 | Main3 | Spare0(16B) | Spare1(16B) | Spare2(16B) | Spare3(16B) |
| (512B) | (512B) | (512B) | (512B) | 16B | 16B | 16B | 16B |

***Note***: *Grey color area: Under ECC protection*

## 6-13. Two-Plane Operations

The 2Gb/4Gb NAND device is divided into two planes for performance improvement. In the two-plane operation, the NAND device may proceed the same type operation (for example- Program, or Erase) on the two planes concurrent or overlapped by the two-plane command sets. The different type operations cannot be done in the two-plane operations; for example, it cannot be done to erase one plane and program the other plane concurrently.

The plane address A18 must be different from each selected plane address. The page address A12-A17 of individual plane must be the same for two-plane operation.

The Status Read command( 70h) may check the device status in the two-plane operation, if the result is failed and then the Status Enhanced Read (78h) may check which plane is failed.

## 6-14. Two-plane Program (ONFI) and Two-plane Cache Program (ONFI)

The two-plane program command (80h-11h) may input data to cache buffer and wait for the final plane data input with command (80h-10h) and then transfer all data to NAND array. As for the two-plane cache program operation, it can be achieved by a two-plane program command (80h-11h) with a cache program command (80h-15h), and the final address input with the confirm command (80h-10h). Please refer to the waveforms of two-plane program (**"Figure 32-1. AC Waveforms for Two-plane Program (ONFI)"**) and two-plane cache program (**"Figure 33. AC Waveforms for Two-plane Cache Program (ONFI)"**) for details. The random data input command (85h) can be also used in the two-plane program operation for changing the column address, please refer to the waveform of two-plane program with random data input.

***Notes:***

*1. Page number should be the same for both planes.*

*2. Block address [29:18] can be different.*

*For examples:*

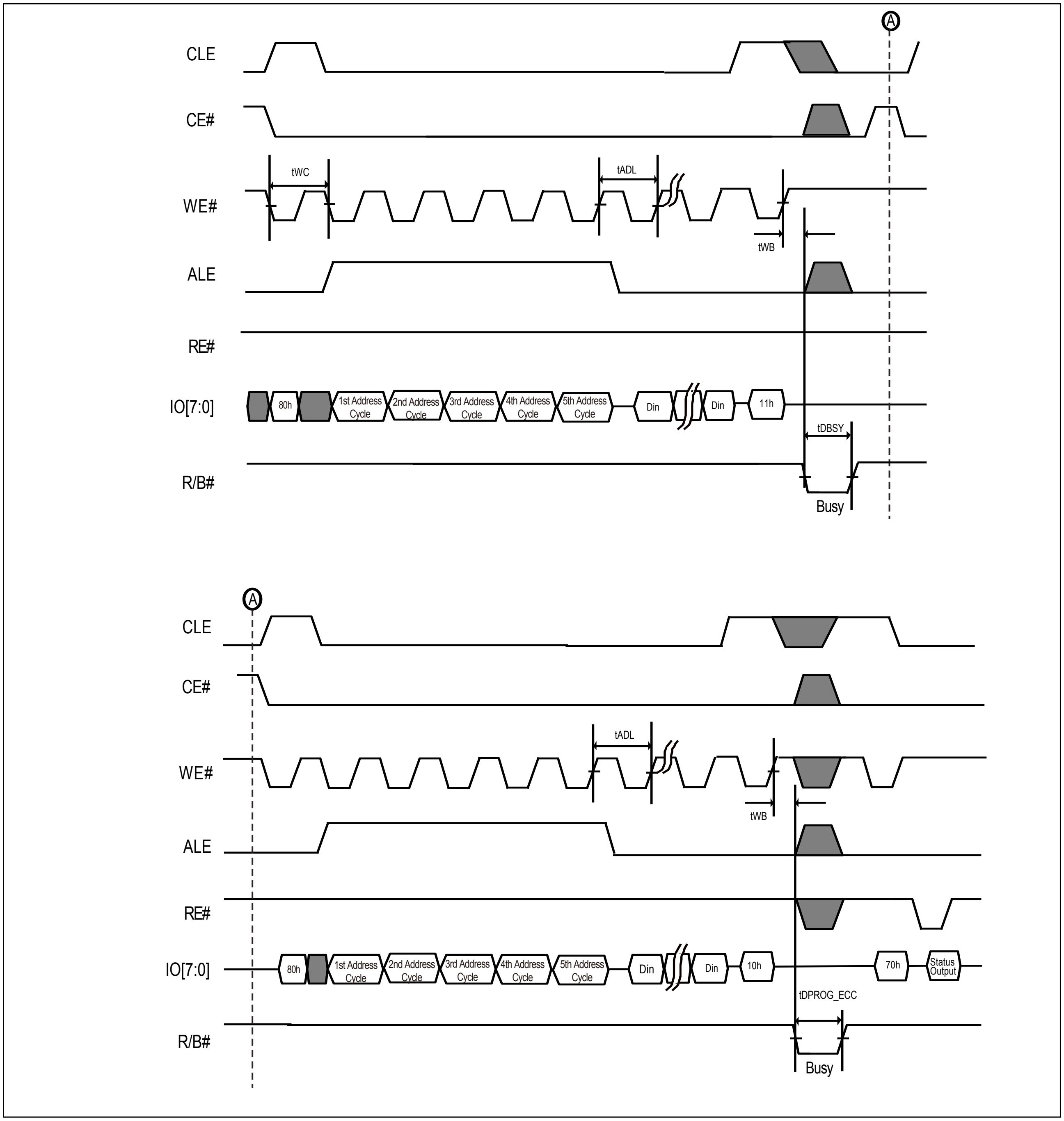
*If the user issues 80h-(block address 5h, page address 5h) -11h - 80h - (block address - 18h, page address 5h) - 10h, the programmed page is*

*- Plane 0: block address 18h, page address 5h*

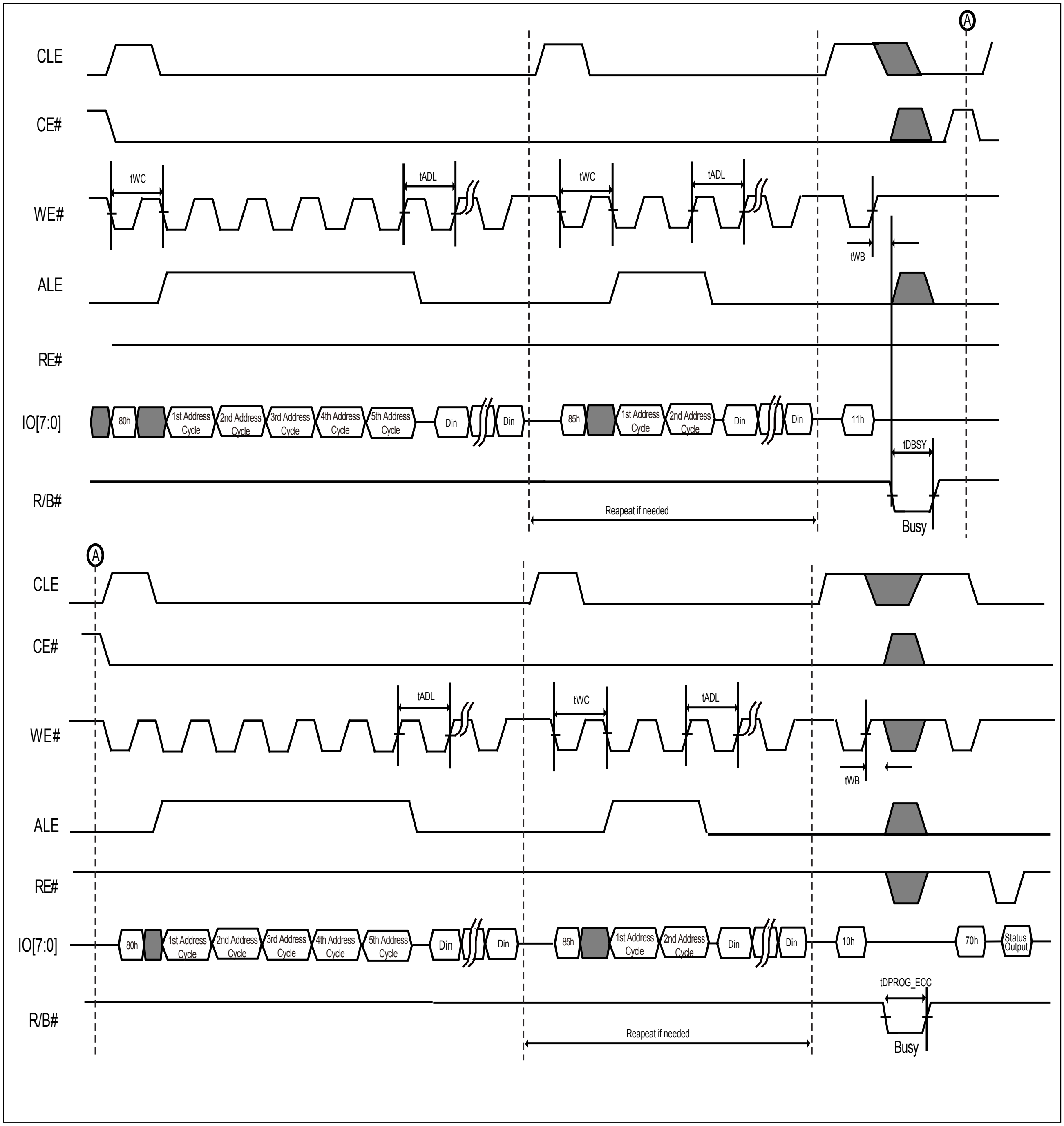
*- Plane 1: block address 5h, page address 5h*

*(**Note**: Block address = A [29:18], page address = A [17:12])*

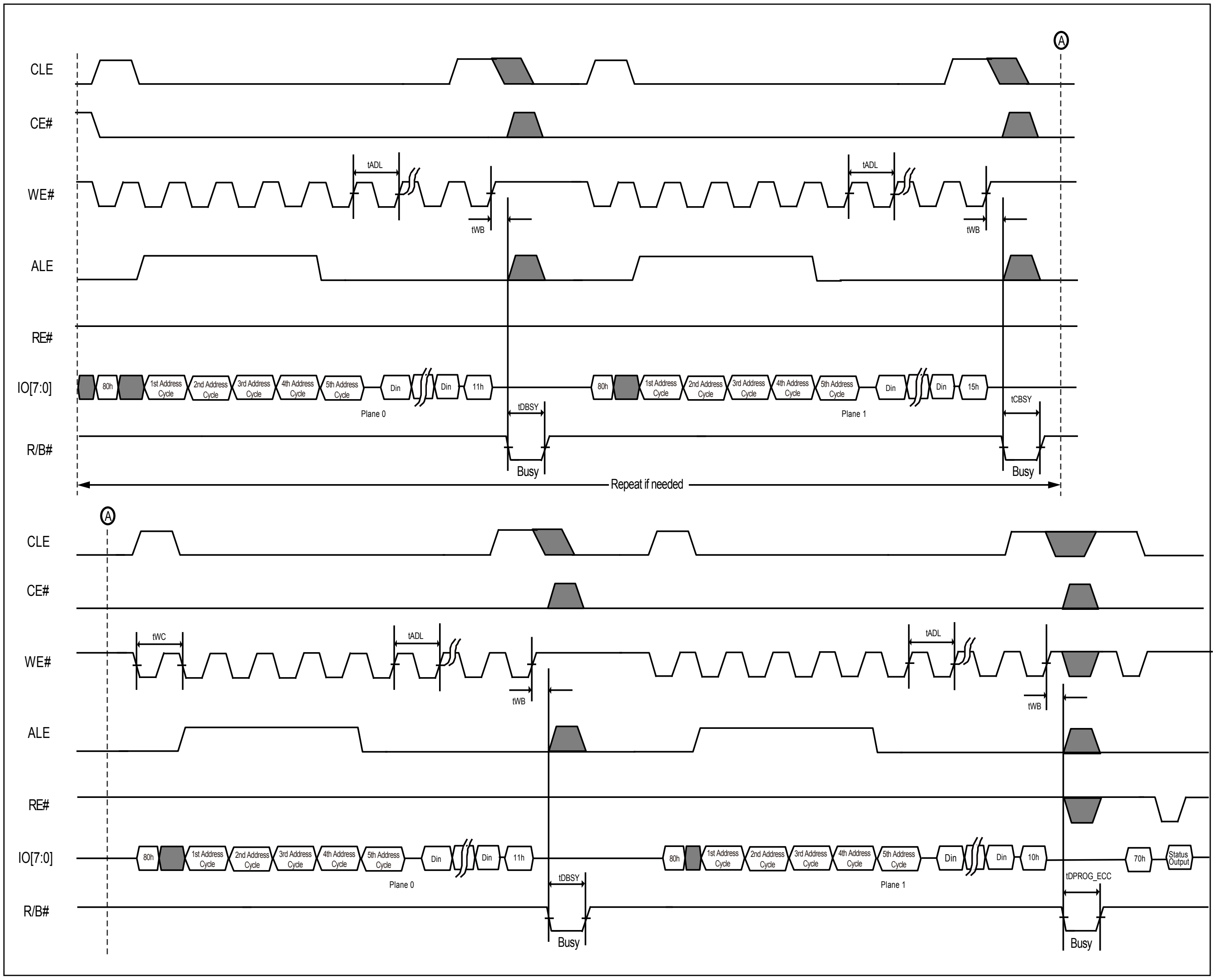
## Figure 32-1. AC Waveforms for Two-plane Program (ONFI)



## Figure 32-2. AC Waveforms for Page Program Random Data Two-plane (ONFI)



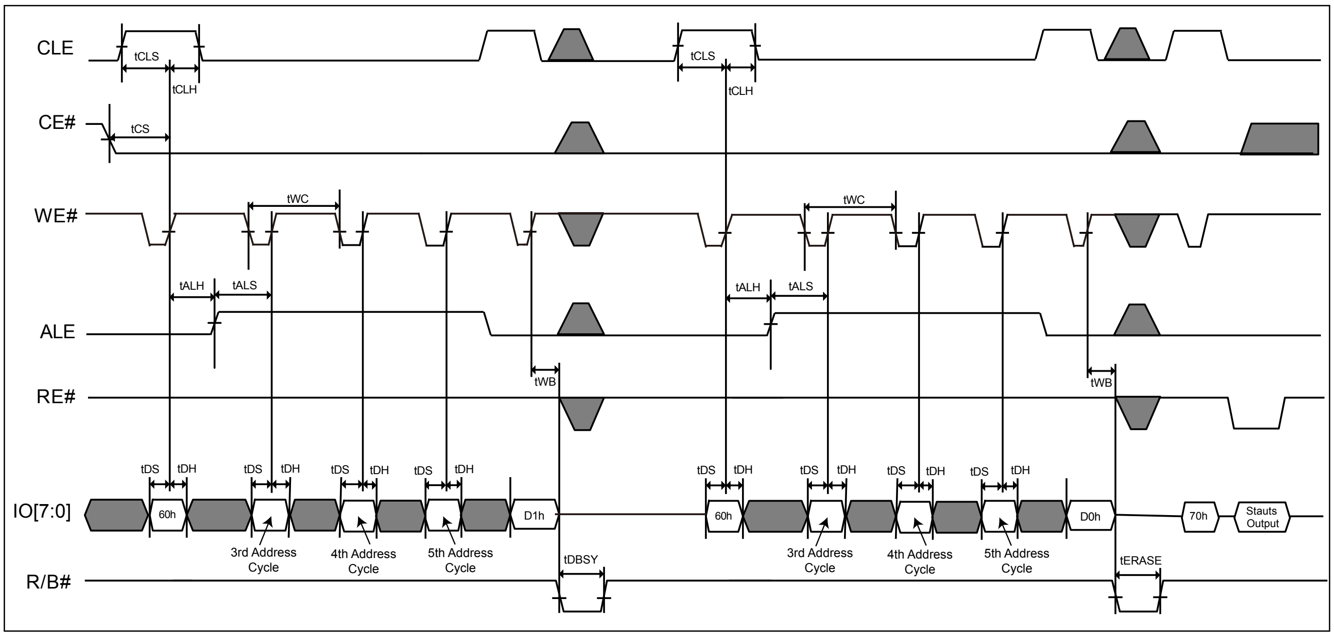
## Figure 33. AC Waveforms for Two-plane Cache Program (ONFI)



## 6-15. Two-plane Block Erase (ONFI)

The two-plane erase command (60h-D1h) may erase the selected blocks in parallel from each plane, with setting the 1st and 2nd block address by (60h-D1h) & (60h-D0h) command and then erase two selected blocks from NAND array. Please refer to the waveforms of two-plane erase for details.

### Figure 34. AC Waveforms for Two-plane Erase (ONFI)

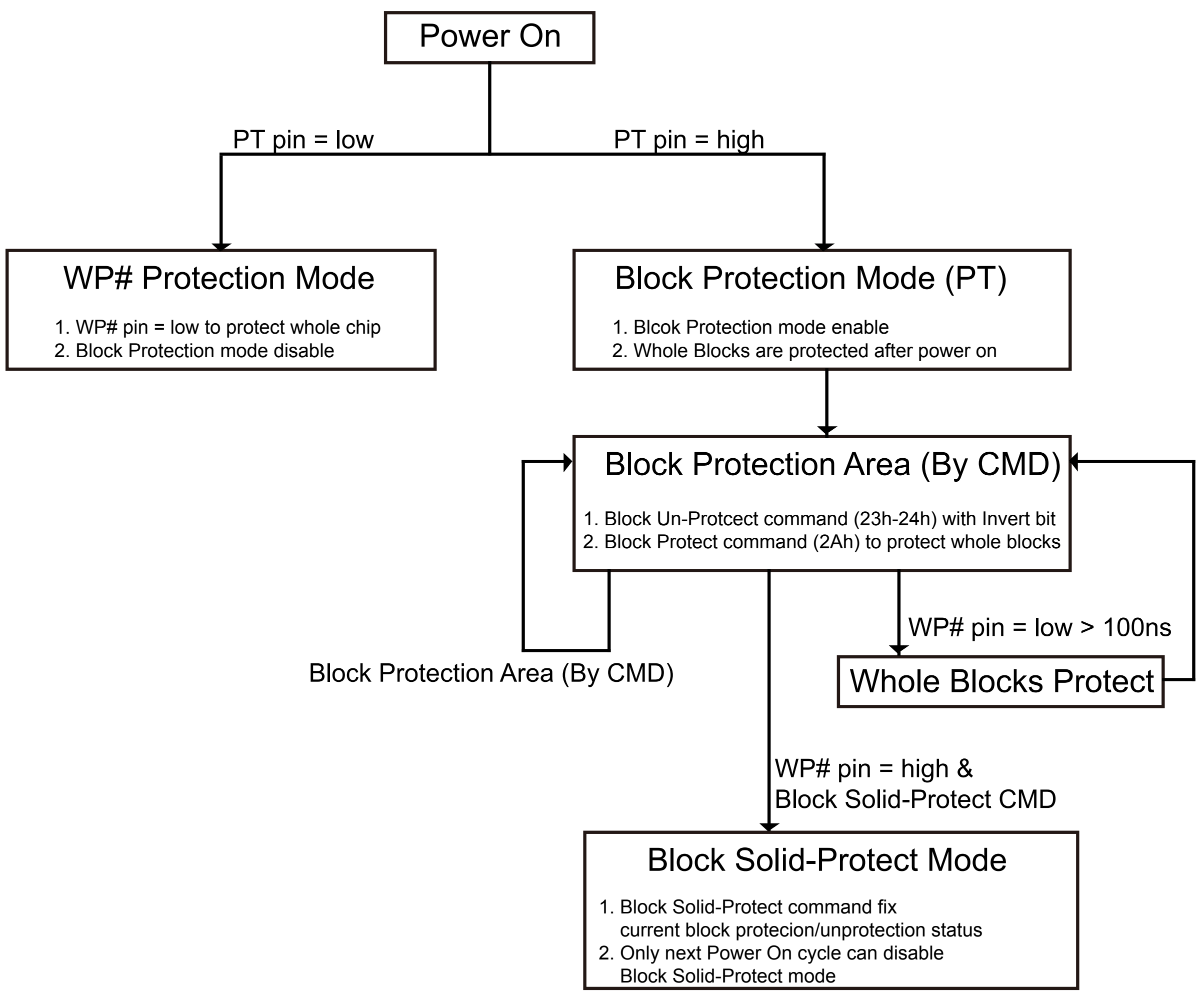


## 6-17. Block Protection

The block protect operation can protect the whole chip or selected blocks from erasing or programming. Through the PT pin at power-on stage, it decides the block protect command is enabled or disabled. At power-on, if the PT pin is connected to high, the related Block Protect command sets are enabled; in contrast, if the PT pin is low, all the block protect command sets are disabled. If the PT pin is connected to high at power-on, all the blocks are default to be protected from programming/erasing even the WP# is disabled, the block un-protect command is necessary to un-protect those selected blocks before those selected blocks to be updated. Once the selected blocks are un-protected, those blocks can be protected again. Besides the Block protect operation, there is “Block Solid-Protect” command (2Ch) may provide a solid block protection; once the block is solid-protected, the block is protected from programming or erasing and cannot be up-protected until next power cycle.

The functional block protection flow chart is shown in the figure below:

### Figure 35. Block Protection Flow Chart



### 6-17-1. Block Un-Protect

When PT pin is connected to high at the power-on stage, all blocks are default to be protected from programming or erasing. The Block Un-Protect command set (23h-24h) may define the range of blocks to be un-protected. The Block Un-Protect Lower command (23h) may set the lower boundary address and followed by the Block Un-Protect Upper command (24h) setting the upper boundary address and the invert-bit to define the un-protect blocks range. The invert-bit defines the un-Protect block area, if the invert-bit is set to "0" which sets the un-Protected area is within the upper and lower boundary address; in contrast, the bit is set to "1" which means the un-protected area is outside the upper and lower boundary address. Please refer to the waveforms below (**"Figure 37 AC Waveforms for Block Unprotection"**) for details.

**Table 8. Address Cycle Definition of Block Un-Protect**

| Address Cycle | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
|---|---|---|---|---|---|---|---|---|
| **Block Address 1** | A19 | A18 | L | L | L | L | L | Invert Bit[1] |
| **Block Address 2** | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 |
| **Block Address 3** | L | L | L | L | L | L | A29 | A28 |

***Note 1**. The Invert bit is set by 24h command to decide the Un-protect range is inside or outside of the boundary. The bit can be H/L for 23h command.*

**Figure 36. Invert-Bit to Define Un-Protected Area Options**

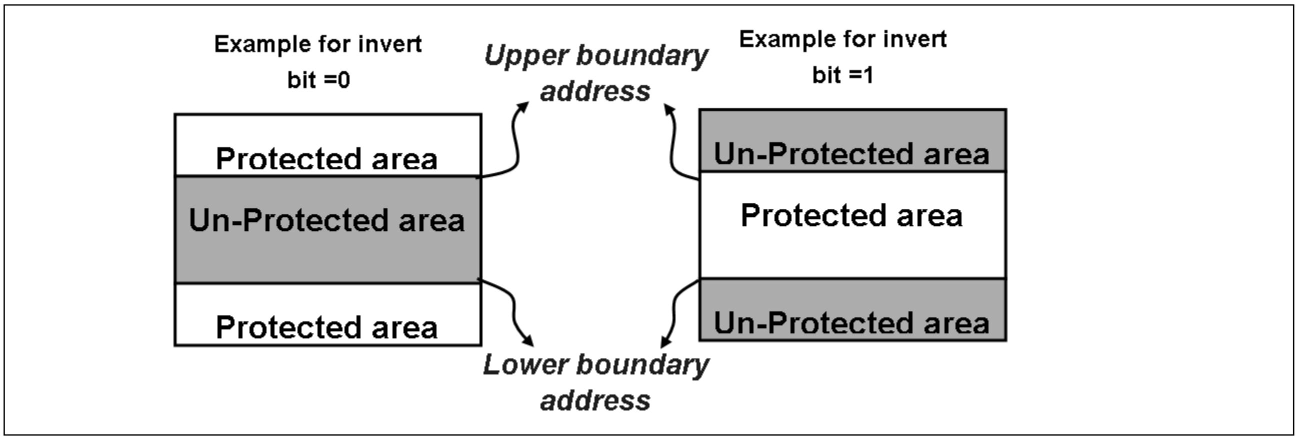
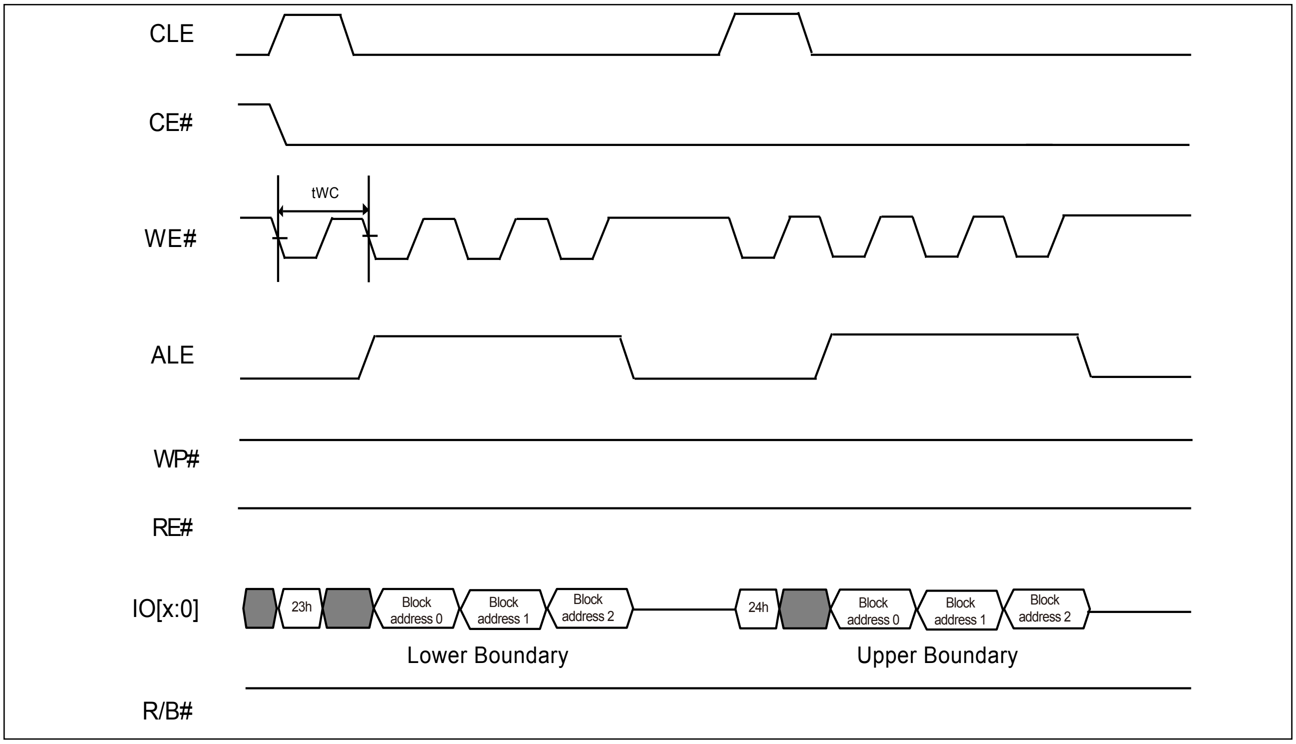


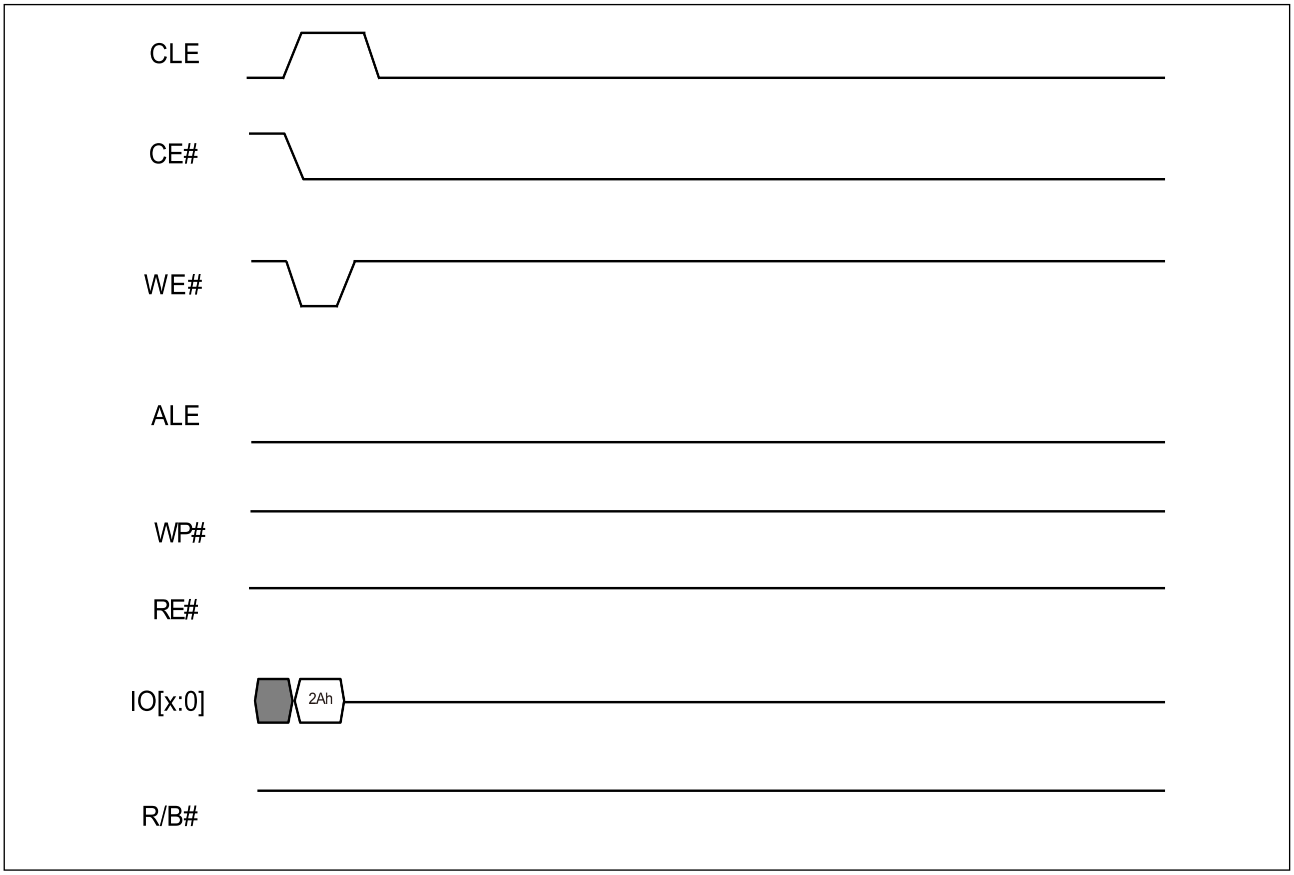

**Figure 37 AC Waveforms for Block Unprotection**



### 6-17-2. Block Protect

When some blocks are un-protected by the Block Un-Protect command set (23h-24h), those blocks can be protected again from the program/erase operation by writing the Block Protect command (2Ah), which may protect all blocks together.

**Figure 38. AC Waveforms for Block Protection**

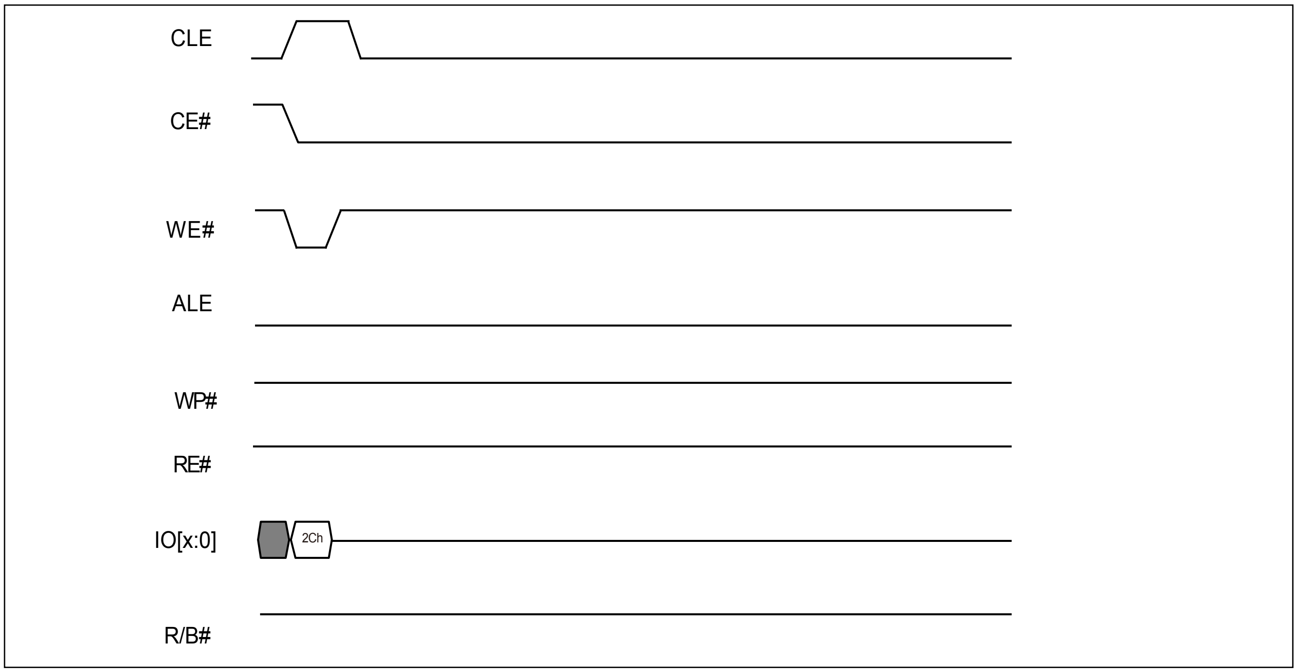


### 6-17-3. Block Solid-Protect

The Block Solid-Protect Command (2Ch) may firmly maintain the previous block protect status; which means the protected blocks cannot be un-protected and the un-protected blocks cannot be protected. Once the Block Solid-Protect command is set, only a new power cycle may change the states of blocks protection/un-protection. The WP# needs to be connected to high before writing the Block Solid-Protect command, and the command is valid only when the PT pin is connected to high.

The Block Solid-Protect command was issued, only the un-protected blocks may accept the program/erase operation. To program or erase the protected block, the R/B# keeps low for the time of tLPSY, and the Status Read command (70h) may get the 60h result.

**Figure 39. AC Waveforms for Block Solid-Protect**



## 6-17-4. Block Protection Status Read

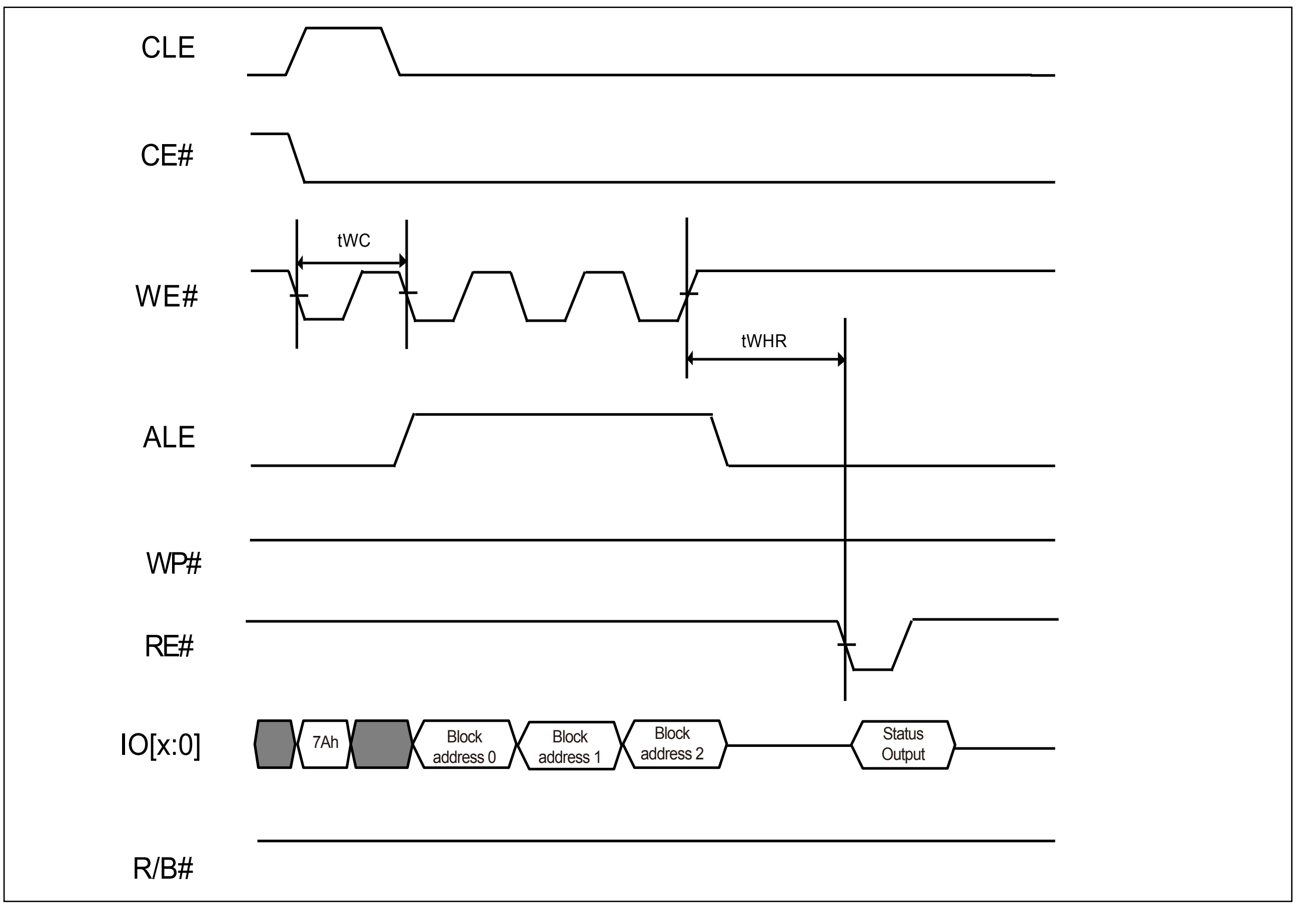
The Block Protection Status Read command (7Ah) may check the protect/un-protect status of individual blocks. The address cycle is referred to **"Table 8. Address Cycle Definition of Block Un-Protect"**.

### Table 9. The Block-Protection Status Output

| Block-Protection Status | IO[15:3] or IO[7:3] | IO2(PT#) | IO1(SP#) | IO0(SP) |
|---|---|---|---|---|
| Block is protected, and device is solid-protected | x | 0 | 0 | 1 |
| Block is protected, and device is not solid-protected | x | 0 | 1 | 0 |
| Block is un-protected, and device is solid-protected | x | 1 | 0 | 1 |
| Block is un-protected, and device is not solid-protected | x | 1 | 1 | 0 |

***Note:*** *PT stands for Block Protection, SP stands for Solid-Protection.*

### Figure 40. AC Waveforms for Block Protection Status Read



# 7. PARAMETERS

## 7-1. ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Temperature under Bias** | -50°C to +125°C |
| **Storage temperature** | -65°C to +150°C |
| **All input voltages with respect to ground (Note 2)** | -0.6V to 4.6V |
| **VCC supply voltage with respect to ground (Note 2)** | -0.6V to 4.6V |
| **ESD protection** | >2000V |

***Notes:***

1. *The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.*
2. *Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.*
3. *During voltage transitions, all pins may overshoot to VCC +1.0V or -1.0V for period up to 20ns. See the two waveforms as below.*

**Figure 41. Maximum Negative Overshoot Waveform**

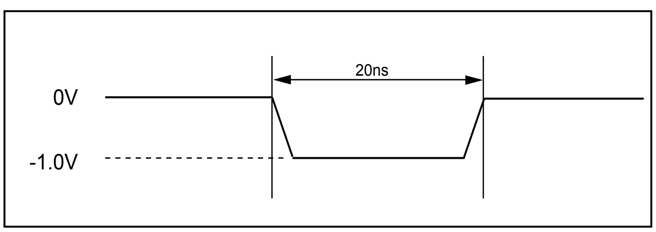



**Figure 42. Maximum Positive Overshoot Waveform**

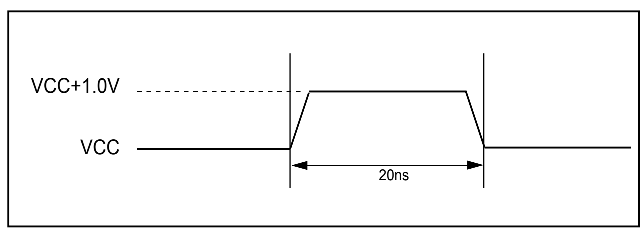


**Table 10. Operating Range**

| Temperature | VCC | Tolerance |
|---|---|---|
| -40°C to +85°C | +1.8V | 1.7~1.95V |

**Table 11. DC Characteristics**

| Symbol | Parameter | Test Conditions | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| VIL | Input low level | | -0.3 | | 0.2VCC | V | |
| VIH | Input high level | | 0.8VCC | | VCC + 0.3 | V | |
| VOL | Output low voltage | IOL= 100uA, VCC= VCC Min. | | | 0.1 | V | |
| VOH | Output high voltage | IOH= -100uA, VCC= VCC Min. | VCC-0.1V | | | V | |
| ISB1 | VCC standby current (CMOS) | CE# = VCC -0.2V, WP# = 0/VCC | | 10 | 50 | uA | |
| ISB2 | VCC standby current (TTL) | CE# = VIH Min., WP# = 0/VCC | | | 1 | mA | |
| ICC0 | Power on current (Including POR current) | | | | 30 | mA | |
| ICC1 | VCC active current (Sequential Read) | tRC Min., CE# = VIL, IOUT= 0mA | | 23 | 30 | mA | |
| ICC2 | VCC active current (Program) | | | 23 | 30 | mA | 1 |
| ICC3 | VCC active current (Erase) | | | 15 | 30 | mA | |
| ILI | Input leakage current | VIN= 0 to VCC Max. | | | +/- 10 | uA | |
| ILO | Output leakage current | VOUT= 0 to VCC Max. | | | +/- 10 | uA | |
| ILO (R/B#) | Output current of R/B# pin | VOL=0.2V | 3 | 4 | | mA | |

***Notes:***

1. *The typical program current (ICC2) for two-plane program operation is 28mA.*

### Table 12. Capacitance

TA = +25°C, F = 1 MHz

| Symbol | Parameter | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| CIN | Input capacitance | | 10 | pF | VIN = 0 V |
| COUT | Output capacitance | | 10 | pF | VOUT = 0 V |

### Table 13. AC Testing Conditions

| Testing Conditions | Value | Unit |
|---|---|---|
| **Input pulse level** | 0 to VCC | V |
| **Output load capacitance** | 1TTL+CL(30) | pF |
| **Input rise and fall time** | 2.5 | ns |
| **Input timing measurement reference levels** | VCC/2 | V |
| **Output timing measurement reference levels** | VCC/2 | V |

### Table 14. Program and Erase Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| **tPROG_ECC** | Page programming time under internal ECC enalbed | | 340 | 600 | us | |
| **tDPROG_ECC** | Two-plane programming time under internal ECC enalbed | | 360 | 600 | us | |
| **tCBSY (Program)** | Dummy busy time for cache program | | 3 | 600 | us | |
| **tDBSY** | The busy time for two-plane program/erase operation | | 0.5 | 1 | us | |
| **tFEAT** | The busy time for Set Feature/ Get Feature | | | 1 | us | |
| **tOBSY_ECC** | The busy time for OTP program at OTP protection mode under internal ECC enabled | | | 50 | us | |
| **NOP** | Number of partial program cycles in same page | | | 4 | cycles | |
| **tERASE (Block)** | Block erase time | | 1 | 3.5 | ms | |

### Table 15. AC Characteristics

| Symbol | Parameter | Min. | Typical | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| **tCLS** | CLE setup time | 10 | | | ns | 1 |
| **tCLH** | CLE hold time | 5 | | | ns | 1 |
| **tCS** | CE# setup time | 20 | | | ns | 1 |
| **tCH** | CE# hold time | 5 | | | ns | 1 |
| **tWP** | Write pulse width | 12 | | | ns | 1 |
| **tALS** | ALE setup time | 10 | | | ns | 1 |
| **tALH** | ALE hold time | 5 | | | ns | 1 |
| **tDS** | Data setup time | 10 | | | ns | 1 |
| **tDH** | Data hold time | 5 | | | ns | 1 |
| **tWC** | Write cycle time | 25 | | | ns | 1 |
| **tWH** | WE# high hold time | 10 | | | ns | 1 |
| **tADL** | Last address latched to data loading time during program operations | 70 | | | ns | 1 |
| **tWW** | WP# transition to WE# high | 100 | | | ns | 1 |
| **tRR** | Ready to RE# falling edge | 20 | | | ns | 1 |
| **tRP** | Read pulse width | 12 | | | ns | 1 |
| **tRC** | Read cycle time | 25 | | | ns | 1 |
| **tREA** | RE# access time (serial data access) | | | 22 | ns | 1 |
| **tCEA** | CE# access time | | | 25 | ns | 1 |
| **tRLOH** | RE#-low to data hold time (EDO) | 5 | | | ns | |
| **tOH** | Data output hold time | 15 | | | ns | 1 |
| **tRHZ** | RE#-high to output-high impedance | | | 60 | ns | 1 |
| **tCHZ** | CE#-high to output-high impedance | | | 50 | ns | 1 |
| **tCOH** | CE# high to output hold time | 15 | | | ns | |
| **tREH** | RE# high hold time | 10 | | | ns | 1 |
| **tIR** | Output high impedance to RE# falling edge | 0 | | | ns | 1 |
| **tRHW** | RE# high to WE# low | 60 | | | ns | 1 |
| **tWHR** | WE# high to RE# low | 80 | | | ns | 1 |
| **tR_ECC** | The data transfering from array to buffer under internal ECC enabled | | 45 | 70 | us | 1 |
| **tWB** | WE# high to busy | | | 100 | ns | 1 |
| **tCLR** | CLE low to RE# low | 10 | | | ns | 1 |
| **tAR** | ALE low to RE# low | 10 | | | ns | 1 |
| **tRST** | Device reset time (Idle/ Read/ Program/ Erase) | | | 5/10/500 | us | 1 |

***Notes:*** *ONFI Mode 5 compliant.*

# 8. OPERATION MODES: LOGIC AND COMMAND TABLES

Address input, command input and data input/output are managed by the CLE, ALE, CE#, WE#, RE# and WP# signals, as shown in **"Table 16. Logic Table"** below.

Program, Erase, Read and Reset are four major operations modes controlled by command sets, please refer to **"Table 17-1. HEX Command Table"** and **"Table 17-2. Two-plane Command Set"**.

**Table 16. Logic Table**

| Mode | CE# | RE# | WE# | CLE | ALE | WP# |
|---|---|---|---|---|---|---|
| Address Input (Read Mode) | L | H | ↑ | L | H | X |
| Address Input (Write Mode) | L | H | ↑ | L | H | H |
| Command Input (Read Mode) | L | H | ↑ | H | L | X |
| Command Input (Write Mode) | L | H | ↑ | H | L | H |
| Data Input | L | H | ↑ | L | L | H |
| Data Output | L | ↓ | H | L | L | X |
| During Read (Busy) | X | H | H | L | L | X |
| During Programming (Busy) | X | X | X | X | X | H |
| During Erasing (Busy) | X | X | X | X | X | H |
| Program/Erase Inhibit | X | X | X | X | X | L |
| Stand-by | H | X | X | X | X | 0V/VCC |

***Notes:***

1. *H = VIH;   L = VIL;   X = VIH or VIL*
2. *WP# should be biased to CMOS high or CMOS low for stand-by.*

### Table 17-1. HEX Command Table

| | First Cycle | Second Cycle | Acceptable While Busy |
|---|---|---|---|
| **Read Mode** | 00H | 30H | |
| **Random Data Input** | 85H | - | |
| **Random Data Output** | 05H | E0H | |
| **ID Read** | 90H | - | |
| **Parameter Page Read (ONFI)** | ECH | - | |
| **Unique ID Read (ONFI)** | EDH | - | |
| **Set Feature (ONFI)** | EFH | - | |
| **Get Feature (ONFI)** | EEH | - | |
| **Reset** | FFH | - | V |
| **Page Program** | 80H | 10H | |
| **Cache Program** | 80H | 15H | |
| **Block Erase** | 60H | D0H | |
| **Block Un-Protect Lower** | 23H | - | |
| **Block Un-Protect Upper** | 24H | - | |
| **Block Protect** | 2AH | - | |
| **Block Solid-Protect** | 2CH | - | |
| **Status Read** | 70H | - | V |
| **Status Enhanced Read (ONFI)** | 78H | - | V |
| **Block Protection Status Read** | 7AH | - | |

### Table 17-2. Two-plane Command Set

| | First Cycle | Second Cycle | Third Cycle | Fourth Cycle |
|---|---|---|---|---|
| **Two-plane Program (ONFI)** | 80H | 11H | 80H | 10H |
| **Two-plane Cache Program (ONFI)** | 80H | 11H | 80H | 15H |
| **Two-plane Block Erase (ONFI)** | 60H | D1H | 60H | D0H |

***Caution:*** *None of the undefined command inputs can be accepted except for the command set in the above table.*

## 8-1. R/B#: Termination for The Ready/Busy# Pin (R/B#)

The R/B# is an open-drain output pin and a pull-up resistor is necessary to add on the R/B# pin. The R/B# outputs the ready/busy status of read/program/ erase operation of the device. When the R/B# is at low, the device is busy for read or program or erase operation. When the R/B# is at high, the read/program/erase operation is finished.

### Rp Value Guidence

The rise time of the R/B# signal depends on the combination of Rp and capacitive loading of the R/B# circuit. It is approximately two times constants (Tc) between the 10% and 90% points on the R/B# waveform.

$$T_C = R \times C$$

Where $R = R_p$ (Resistance of pull-up resistor), and $C = C_L$ (Total capacitive load)

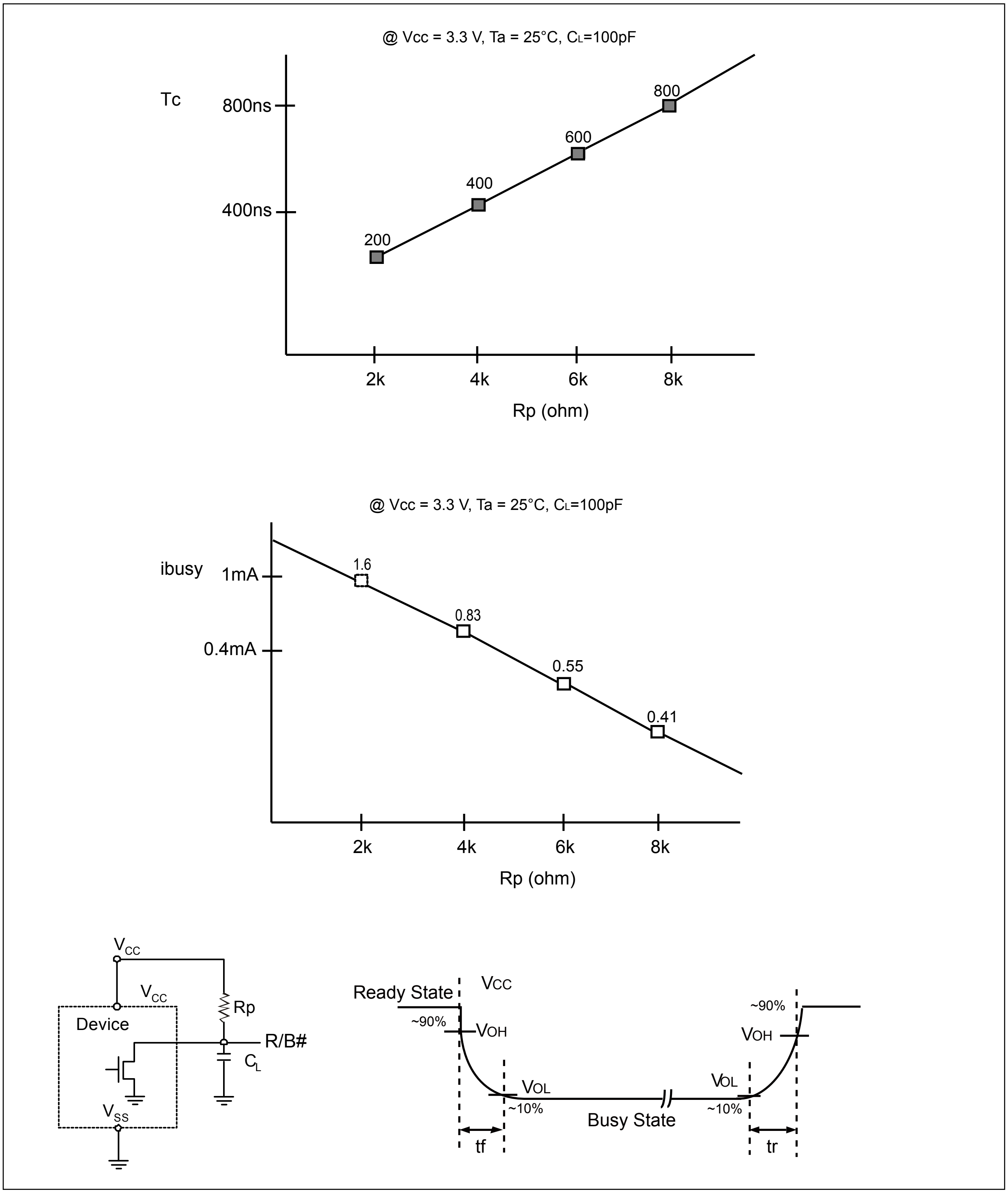
The fall time of the R/B# signal majorly depends on the output impedance of the R/B# signal and the total load capacitance.

$$Rp\ (Min.) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{I_{OL} + \Sigma IL}$$

***Notes:***

1. *Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.*
2. *Rp maximum value depends on the maximum permissible limit of tr.*
3. *IL is the total sum of the input currents of all devices tied to the R/B pin.*

### Figure 43. R/B# Pin Timing Information



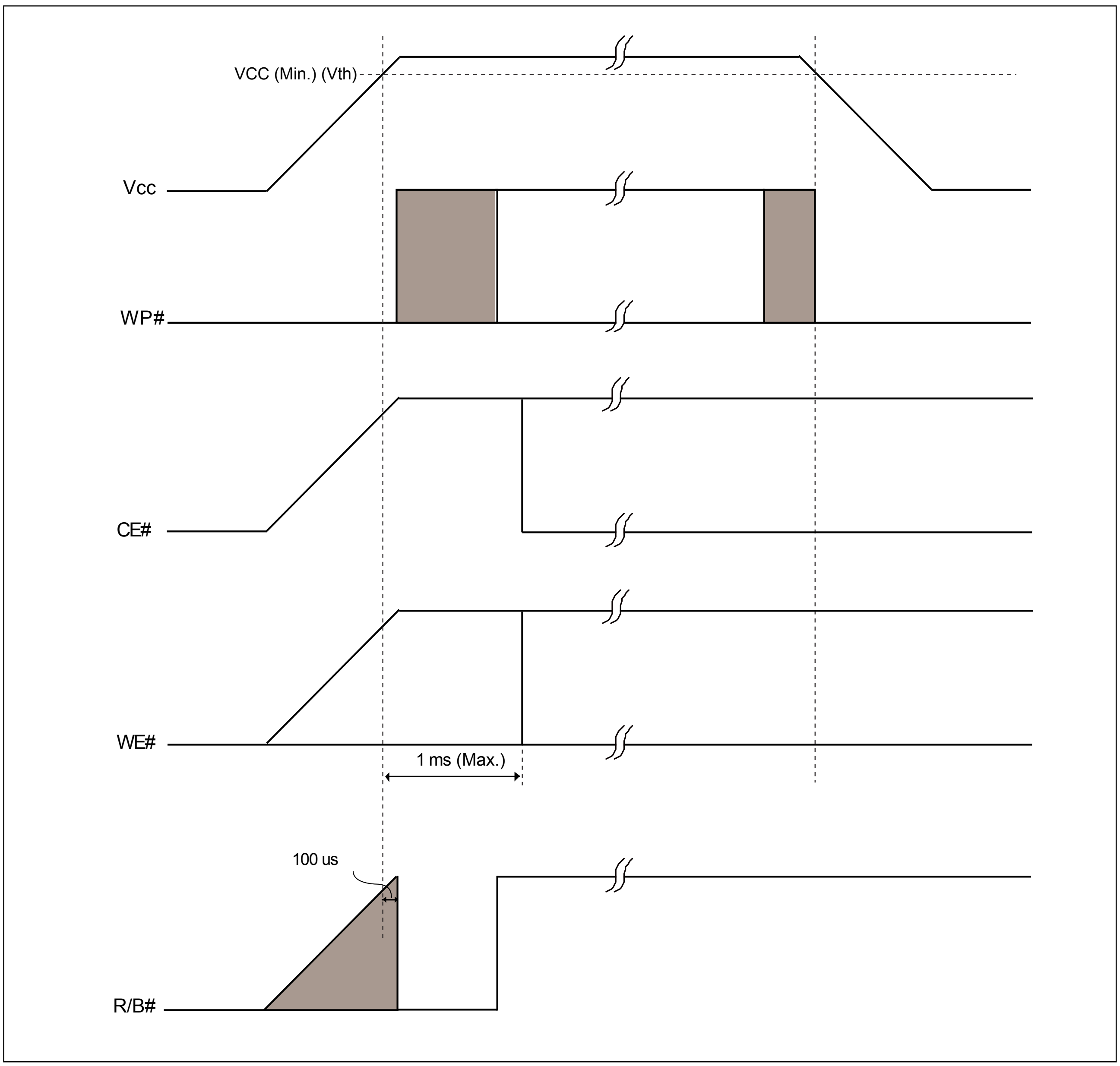
## 8-2. Power On/Off Sequence

After the Chip reaches the power on level (Vth = Vcc min.), the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. There are two ways to identify the termination of the internal power on reset sequence. Please refer to **"Figure 44. Power On/Off Sequence"**.

- R/B# pin
- Wait 1 ms

During the power on and power off sequence, it is recommended to keep the WP# = Low for internal data protection.

### Figure 44. Power On/Off Sequence



### 8-2-1. WP# Signal

WP# going Low can cause program and erase operations automatically reset.

The enabling & disabling of the both operations are as below:

**Figure 45-1. Enable Programming of WP# Signal**

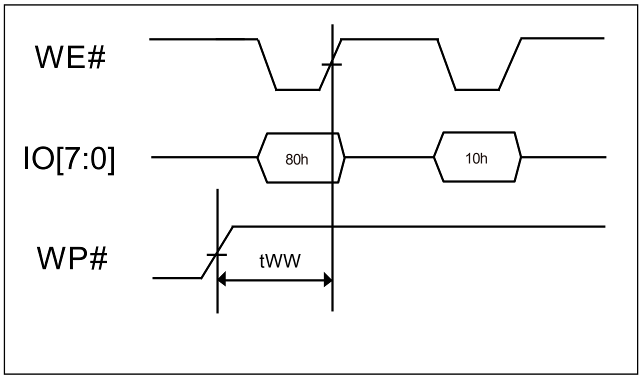



**Figure 45-2. Disable Programming of WP# Signal**

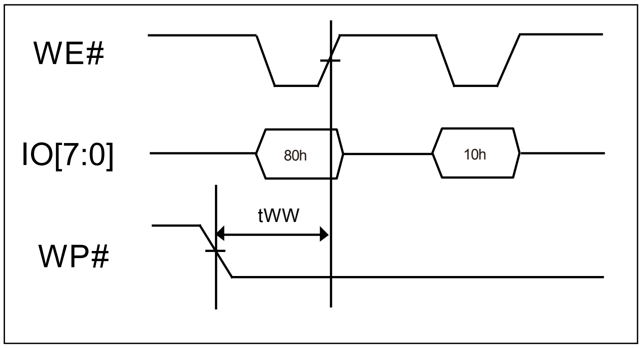



**Figure 45-3. Enable Erasing of WP# Signal**

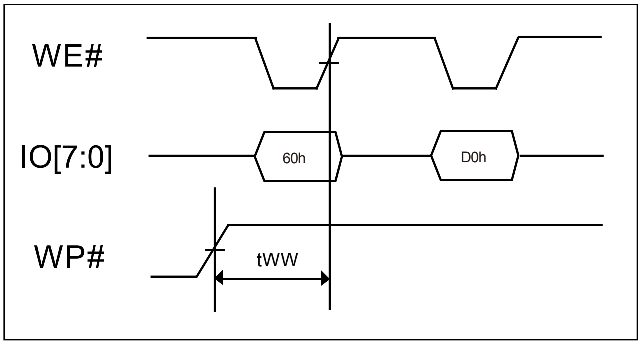
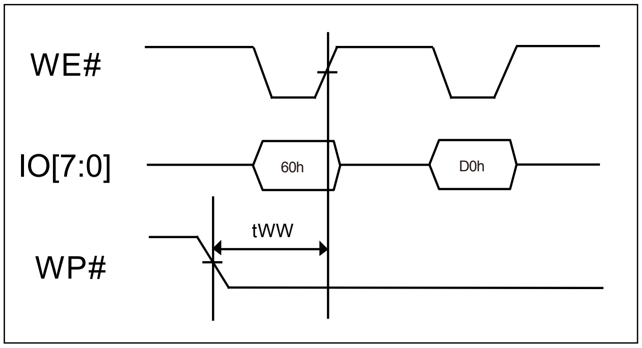



**Figure 45-4. Disable Erasing of WP# Signal**

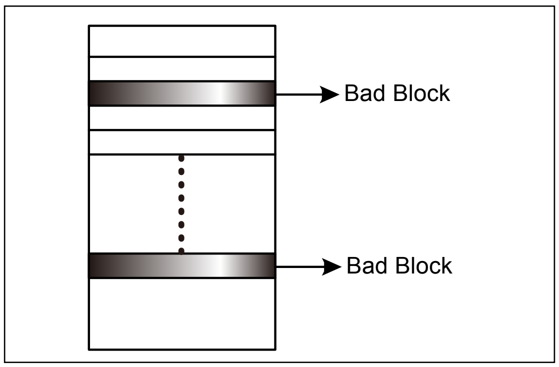


# 9. SOFTWARE ALGORITHM

## 9-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is recommended to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since it may be cleared by any erase operation.

**Figure 46. Bad Blocks**




While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st bytes of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. The figure shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

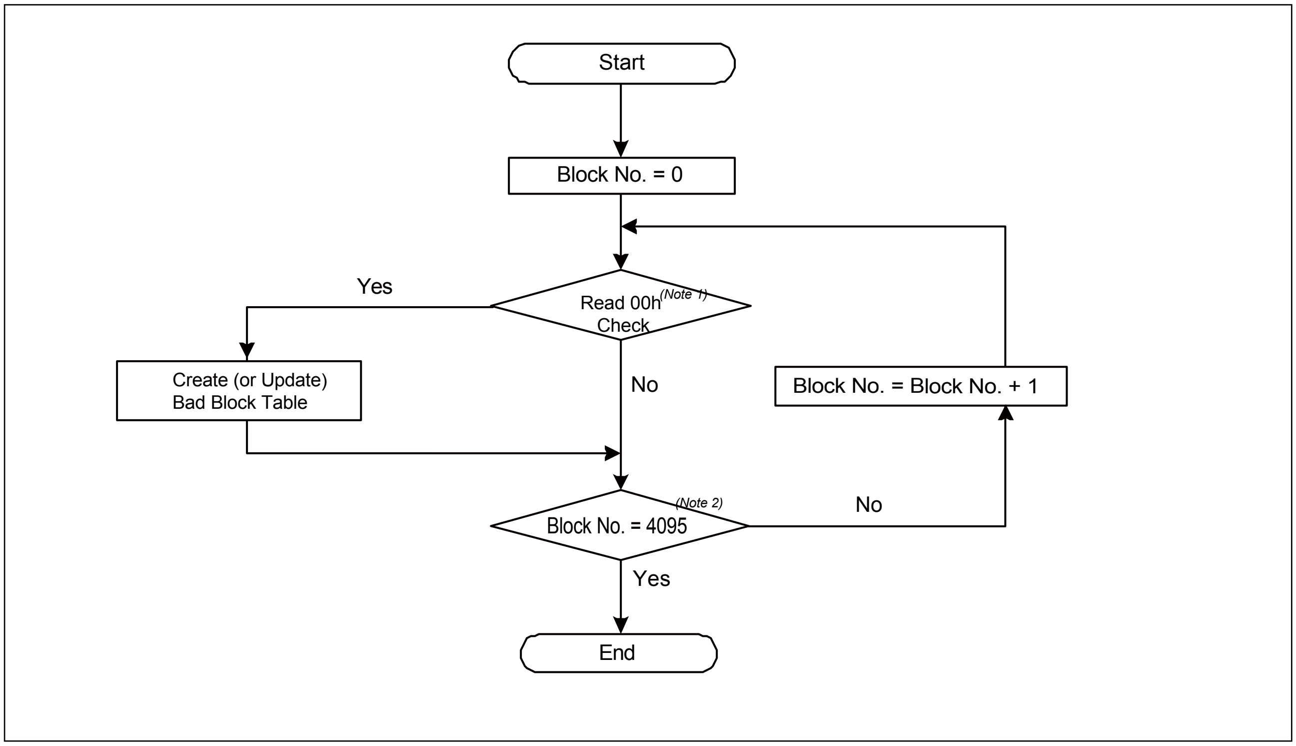
**Table 18. Valid Blocks**

| | Density | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Valid (Good) Block Number | 2Gb | 2008 | | 2048 | Block | Block 0 is guaranteed to be good (with ECC) |
| | 4Gb | 4016 | | 4096 | Block | |

## 9-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. The following section shows the recommended flow for creating a bad block table.

**Figure 47. Bad Block Test Flow**




***Notes:***

1. *Read 00h check is at the 1st bytes of the 1st and 2nd pages of the block spare area.*
2. *The Block No. = 2047 for 2Gb, 4095 for 4Gb.*

## 9-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

### Table 19. Failure Modes

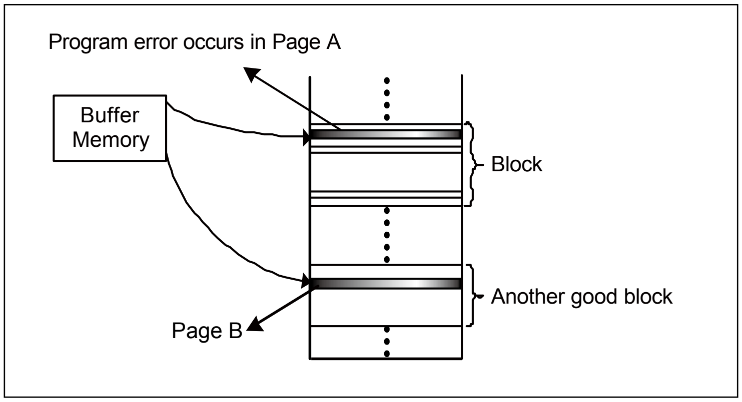
| Failure Mode | Detection and Countermeasure | Sequence |
|---|---|---|
| **Erase Failure** | Status Read after Erase | Block Replacement |
| **Programming Failure** | Status Read after Program | Block Replacement |
| **Read Failure**[1] | Read Failure | ECC |

***Note 1****: The internal ECC is always enabled, the internal ECC will handle the Read failure.*

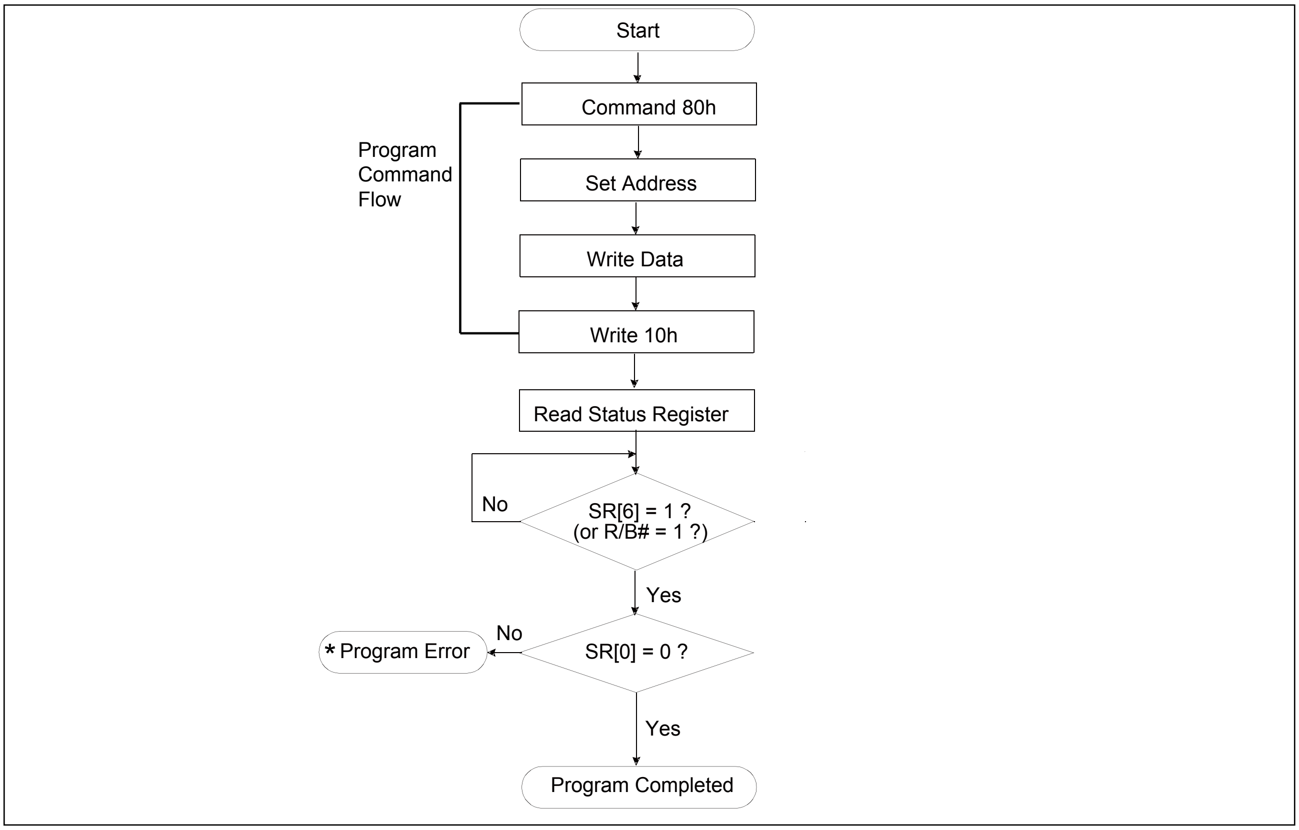
## 9-4. Program

It is feasible to reprogram the data into another page (Page B) when an error occurred in Page A by loading from an external buffer. Then create a bad block table or by using another appropriate scheme to prevent further system accesses to Page A.

### Figure 48. Failure Modes



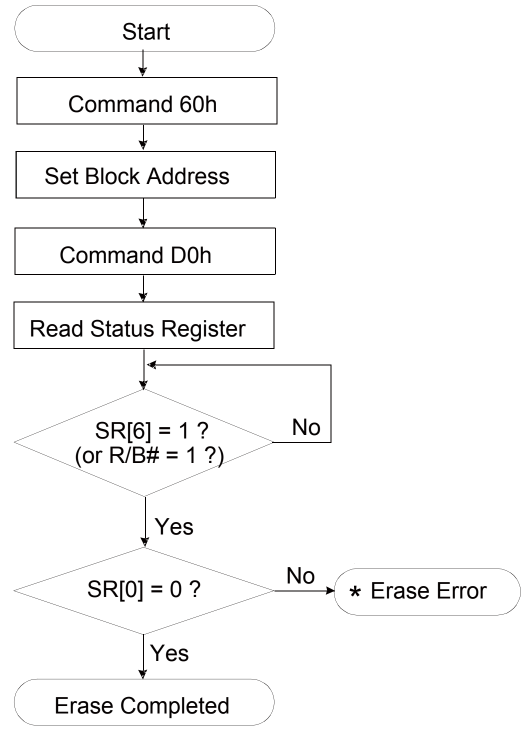

### Figure 49. Program Flow Chart




## 9-5. Erase

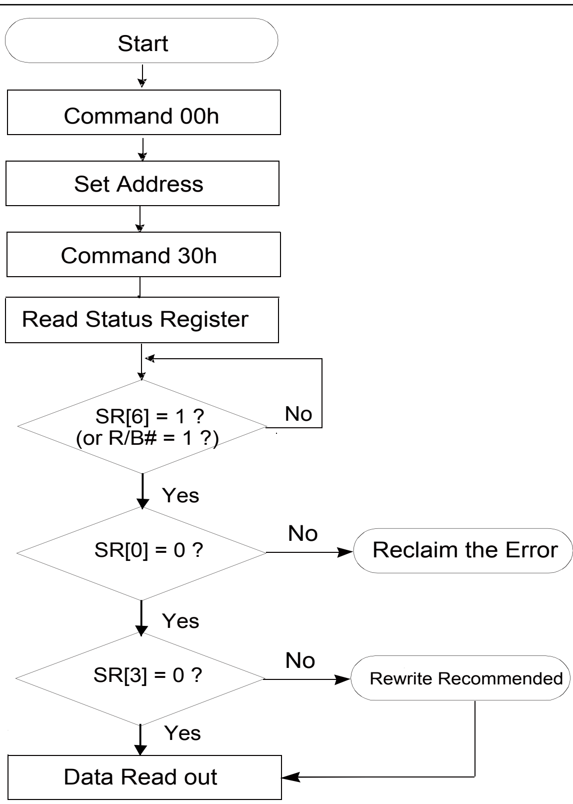
To prevent future accesses to this bad block, it is feasible to create a table within the system or by using another appropriate scheme when an error occurs in an Erase operation.

## Figure 50. Erase Flow Chart



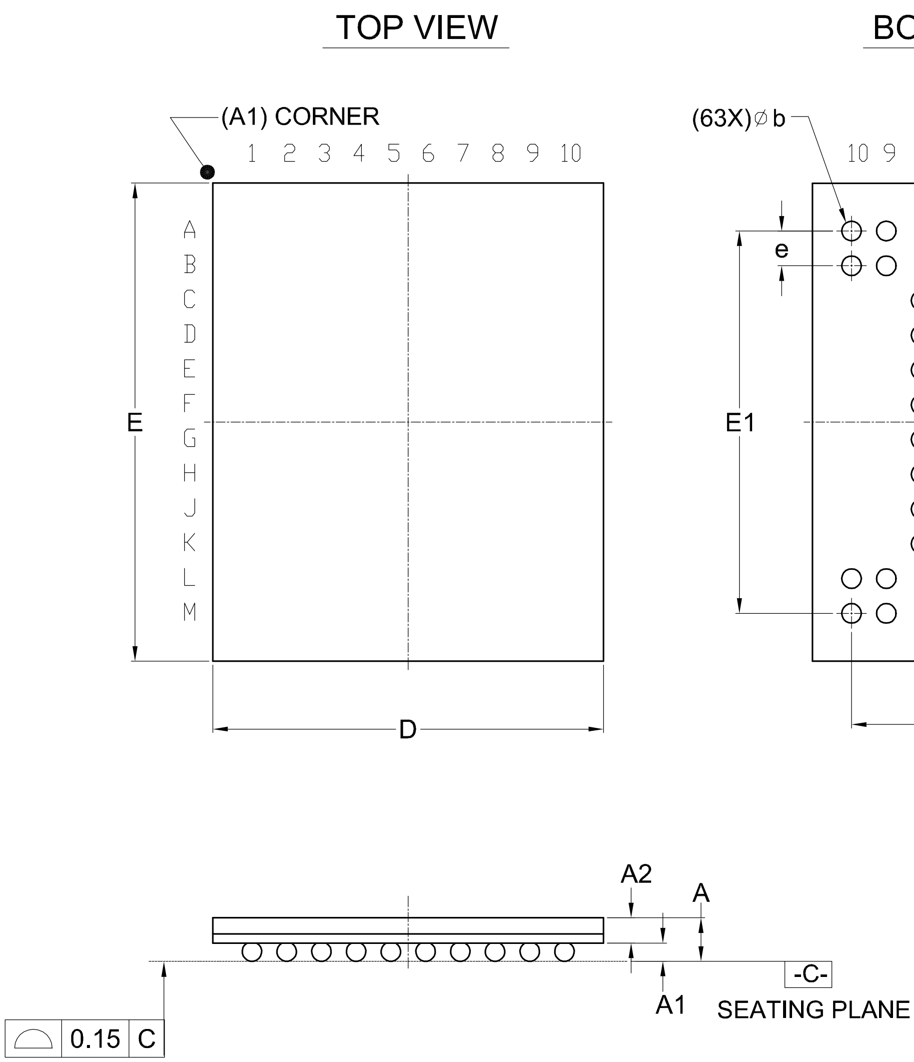

* The failed blocks will be identified and given errors in status register bits for attempts on erasing them.

## Figure 51. Read Flow Chart



# 10. PACKAGE INFORMATION

**Title:** Package Outline for 63-VFBGA (9x11x1.0mm, Ball-pitch: 0.8mm, Ball-diameter: 0.45mm)




Dimensions (inch dimensions are derived from the original mm dimensions)

| UNIT \ SYMBOL | | A | A1 | A2 | b | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.25 | 0.55 | 0.40 | 8.90 | --- | 10.90 | --- | --- |
| | Nom. | --- | 0.30 | --- | 0.45 | 9.00 | 7.20 | 11.00 | 8.80 | 0.80 |
| | Max. | 1.00 | 0.40 | --- | 0.50 | 9.10 | --- | 11.10 | --- | --- |
| Inch | Min. | --- | 0.010 | 0.022 | 0.016 | 0.350 | --- | 0.429 | --- | --- |
| | Nom. | --- | 0.012 | --- | 0.018 | 0.354 | 0.283 | 0.433 | 0.346 | 0.031 |
| | Max. | 0.039 | 0.016 | --- | 0.020 | 0.358 | --- | 0.437 | --- | --- |

| Dwg. No. | Revision | Reference | | | |
|---|---|---|---|---|---|
| | | JEDEC | EIAJ | | |
| 6110-4267 | 0 | | | | |

# 11. REVISION HISTORY

| Rev. No. | Descriptions | Page | Date |
|---|---|---|---|
| 0.00 | 1. Initial Released | ALL | FEB. 02, 2015 |
| 1.0 | 1. Removed "Advanced Information" title | ALL | MAR. 24, 2015 |
| | 2. Corrected tALS timing waveform as ALE high till WE# high | P21 | |
| | 3. Corrected waveform of OTP protection tWB timing from WE# high to busy | P21,P50 | |
| | 4. Typographical error | P12,P74 | |
| 1.1 | 1. Supplement "the internal ECC is disable on the parameter page and unique ID" | P35, P41 | DEC. 18, 2015 |
| | 2. Aligned the term of "plane 1" & "plane 2" as "plane 0" & "plane 1" | P55 | |
| | 3. Added overshoot/undershoot waveforms | P63 | |
| | 4. Modification of the power-on/off sequence: supplement the CE# signal, supplement the WE# single waveform with WE#=0 without toggle during the power-on period. | P71 | |

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