1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

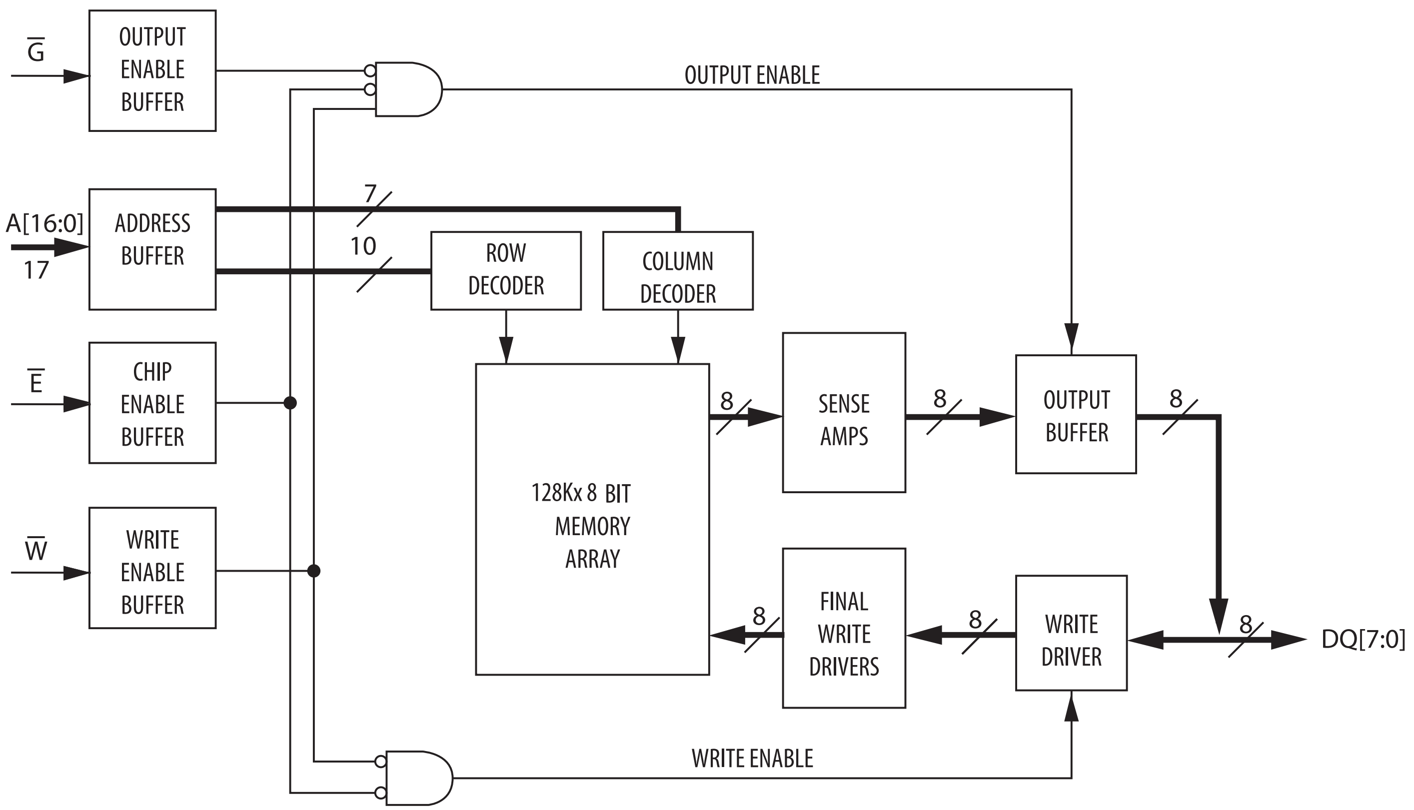
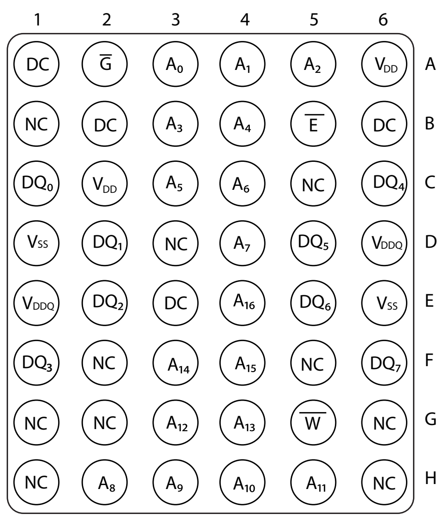


Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{DDQ}	I/O Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection, Ball D3, H1, H6, G2 Reserved for Future Expansion

Figure 1.2 Pin Diagrams for Available Packages (Top View)



48 Pin FBGA

Table 1.2 Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	Mode	V_{DD} Current	DQ[7:0][2]
H	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z
L	H	H	Output disabled	I_{DDR}	Hi-Z
L	L	H	Byte Read	I_{DDR}	D_{Out}
L	X	L	Byte Write	I_{DDW}	D_{in}

[1] H = high, L = low, X = don't care

[2] Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Core Supply voltage[2]	V_{DD}	-0.5 to 4.0	V
I/O Power Supply voltage[2]	V_{DDQ}	-0.5 to 4.0	V
Voltage on any pin[2]	V_{IN}	-0.5 to +4.0 or V_{DDQ} + 0.5 *whichever is less*	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation [3]	P_D	0.600	W
Temperature under bias	T_{BIAS}	-10 to 85	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write	H_{max_write}	2000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

1 Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

2 All voltages are referenced to V_{SS}.

3 Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Core Power supply voltage	V_{DD}	3.0 [1]	3.3	3.6	V
I/O Power supply voltage	V_{DDQ}	1.65 [1]	-	3.6	V
Write inhibit voltage	V_{WIDD}	2.5	2.7	3.0 [1]	V
Write inhibit voltage	V_{WIDDQ}	1.2	1.4	1.65 [1]	V
Input high voltage (V_{DDQ}=1.65-2.2V)	V_{IH}	1.4	-	$V_{DDQ} + 0.2$ [2]	V
Input high voltage (V_{DDQ}=2.2-2.7V)	V_{IH}	1.8	-	$V_{DDQ} + 0.2$ [2]	V
Input high voltage (V_{DDQ}=2.7-3.6V)	V_{IH}	2.2	-	$V_{DDQ} + 0.2$ [2]	V
Input low voltage (V_{DDQ}=1.65-2.2V)	V_{IL}	-0.2 [3]	-	0.4	V
Input low voltage (V_{DDQ}=2.2-2.7V)	V_{IL}	-0.2 [3]	-	0.6	V
Input low voltage (V_{DDQ}=2.7-3.6V)	V_{IL}	-0.2 [3]	-	0.8	V
Temperature under bias	T_A	0		70	°C

1 $V_{DDQ} \leq V_{DD}$. Write inhibit occurs when either V_{DD} or V_{DDQ} drops below its write inhibit voltage. There is a 2 ms startup time once V_{DD} exceeds V_{DD}(min). See **Power Up and Power Down Sequencing**.

2 V_{IH}(max) = V_{DDQ} + 0.2 V DC ; V_{IH}(max) = V_{DDQ} + 0.5 V AC (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

3 V_{IL}(min) = -0.2 V DC ; V_{IL}(min) = -2.0 V AC (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WIDD} or V_{DDQ} is less than V_{WIDDQ}. As soon as V_{DD} exceeds V_{DD}(min) and V_{DDQ} exceeds V_{DDQ}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD} - 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where either V_{DD} goes below V_{WIDD} or V_{DDQ} goes below V_{WIDDQ}, writes are protected and a startup time must be observed when power returns above V_{DD}(min) and / or V_{DDQ}.

Figure 2.1 Power Up and Power Down Diagram

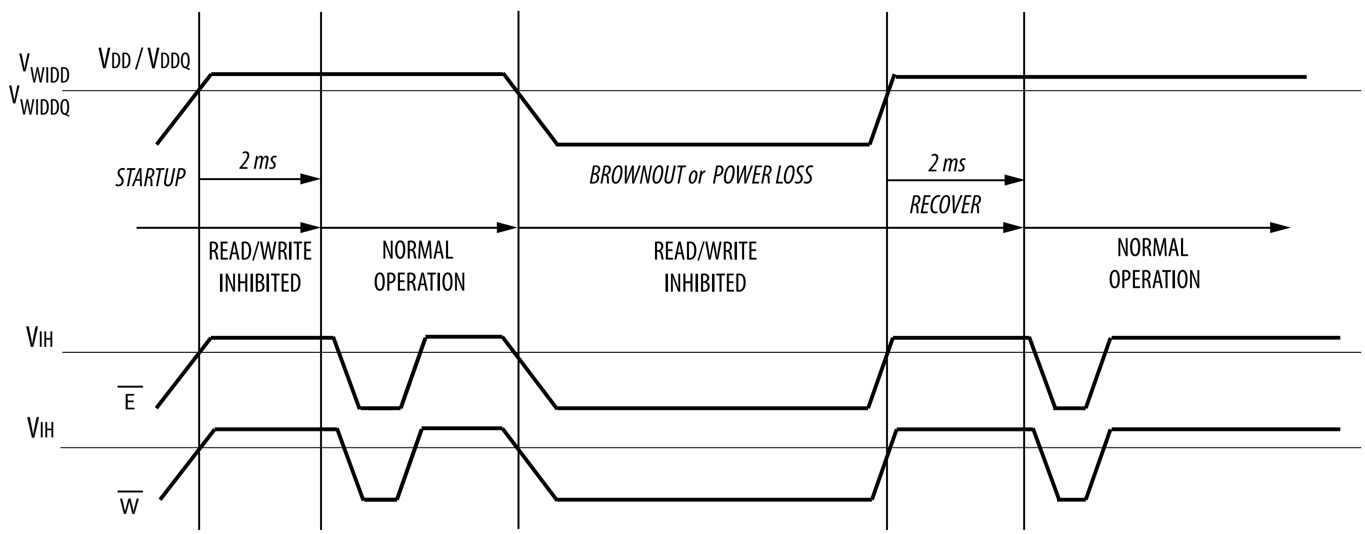


Table 2.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	-	±1	µA
Output leakage current	$I_{lkg(O)}$	-	-	±1	µA
Output low voltage (V_{DDQ}=1.65-2.2V@ 0.1mA)	V_{OL}	-	-	0.2	V
Output low voltage (V_{DDQ}=2.2-2.7V@ 0.1mA)	V_{OL}	-	-	0.4	V
Output low voltage (V_{DDQ}=2.7-3.6V@ 2.1 mA)	V_{OL}	-	-	0.4	V
Output high voltage (V_{DDQ}=1.65-2.2V@ - 0.1 mA)	V_{OH}	1.4	-	-	V
Output high voltage (V_{DDQ}=2.2-2.7V@ -0.1 mA)	V_{OH}	2	-	-	V
Output high voltage (V_{DDQ}=2.7-3.6V@ -1.0 mA)	V_{OH}	2.4	-	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes[1] (I_{OUT}= 0 mA, V_{DD}= max)	I_{DDR}	25	30	mA
AC active supply current - write modes[1] (V_{DD}= max)	I_{DDW}	55	65	mA
AC active operating current ($V_{DDQ} = V_{IH}$= 3.6V, V_{IL}= 0V) *input transitions <2ns, no output load*	I_{DDQ}	0.50	2	mA
AC standby current (V_{DD}= max, $\overline{E} = V_{IH}$) *no other restrictions on other inputs*	I_{SB1}	6	8	mA
CMOS standby current ($\overline{E} \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or $\geq V_{DDQ}$ - 0.2 V) (V_{DD} = max, f = 0 MHz)	I_{SB2}	5	7	mA

[1] All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	-	6	pF
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

[1] f = 1.0 MHz, VDDQ=VDDQ(typ), T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	V_{DDQ}=1.8	V_{DDQ}=2.5	V_{DDQ}=3.3	Unit
Logic input timing measurement reference level	0.8	0.8	0.8	V
Logic output timing measurement reference level	0.8	0.8	0.8	V
Logic input pulse levels	0 or 1.8	0 or 2.5	0 or 3.3	V
Output load voltage (V_L) for low & high impedance parameters (Figure 3.1)	0.8	1.2	1.75	V
Output load resistor (R1) for all other timing	13,500	16,600	1,103	Ω
Output load resistor (R2) for all other timing	10,800	15,400	1,554	Ω

Figure 3.1 Output Load Test Low and High

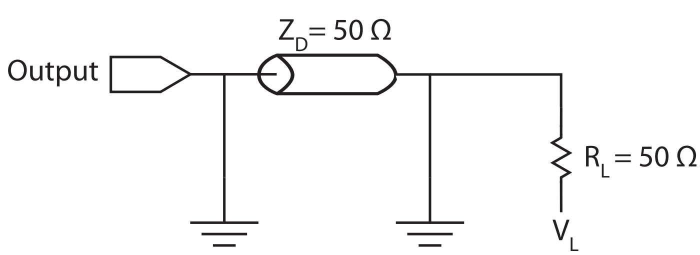
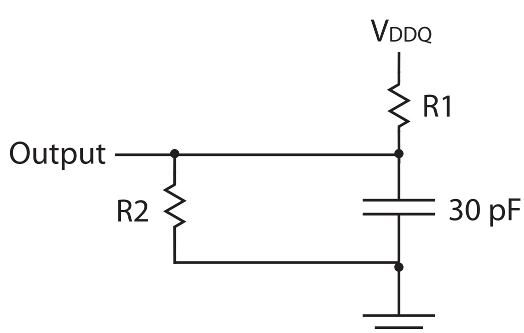


Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing[1]

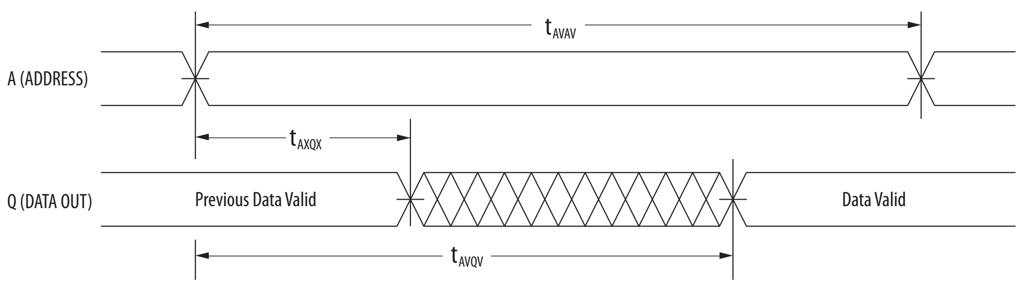
Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	45	-	ns
Address access time	t_{AVQV}	-	45	ns
Enable access time[2]	t_{ELQV}	-	45	ns
Output enable access time	t_{GLQV}	-	20	ns
Output hold from address change	t_{AXQX}	3	-	ns
Enable low to output active[3]	t_{ELQX}	3	-	ns
Output enable low to output active[3]	t_{GLQX}	0	-	ns
Enable high to output Hi-Z[3]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[3]	t_{GHQZ}	0	15	ns

1 $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

2 Addresses valid before or at the same time $\overline{E}$ goes low.

3 This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



NOTE: Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$)

Figure 3.3B Read Cycle 2

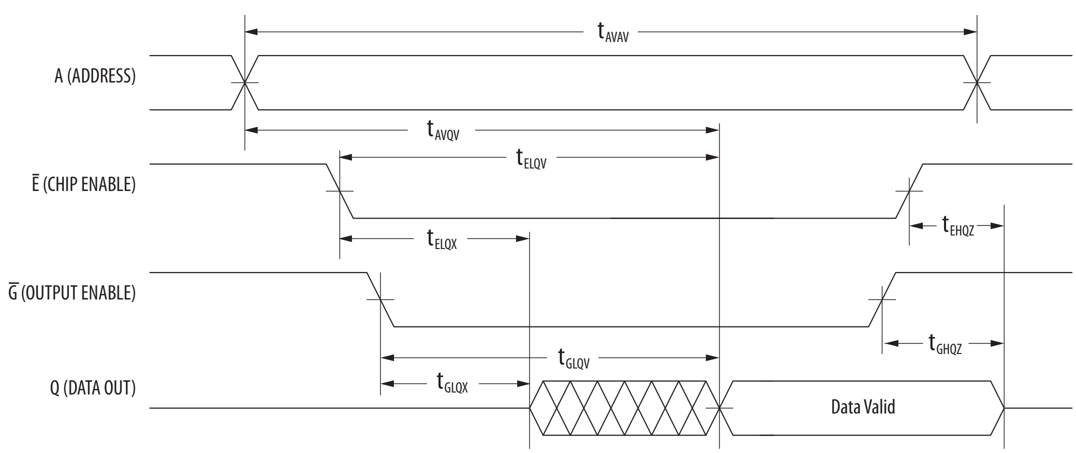


Table 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	45	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	25	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	25	-	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	20	-	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	20	-	ns
Data valid to end of write	t_{DVWH}	15	-	ns
Data hold time	t_{WHDX}	0	-	ns
Write low to data Hi-Z[3]	t_{WLQZ}	0	15	ns
Write high to output active[3]	t_{WHQX}	3	-	ns
Write recovery time	t_{WHAX}	12	-	ns

1 All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

2 All write cycle timings are referenced from the last valid address to the first transition address.

3 This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperature, t_{WLQZ}(max) < t_{WHQX}(min)

Figure 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)

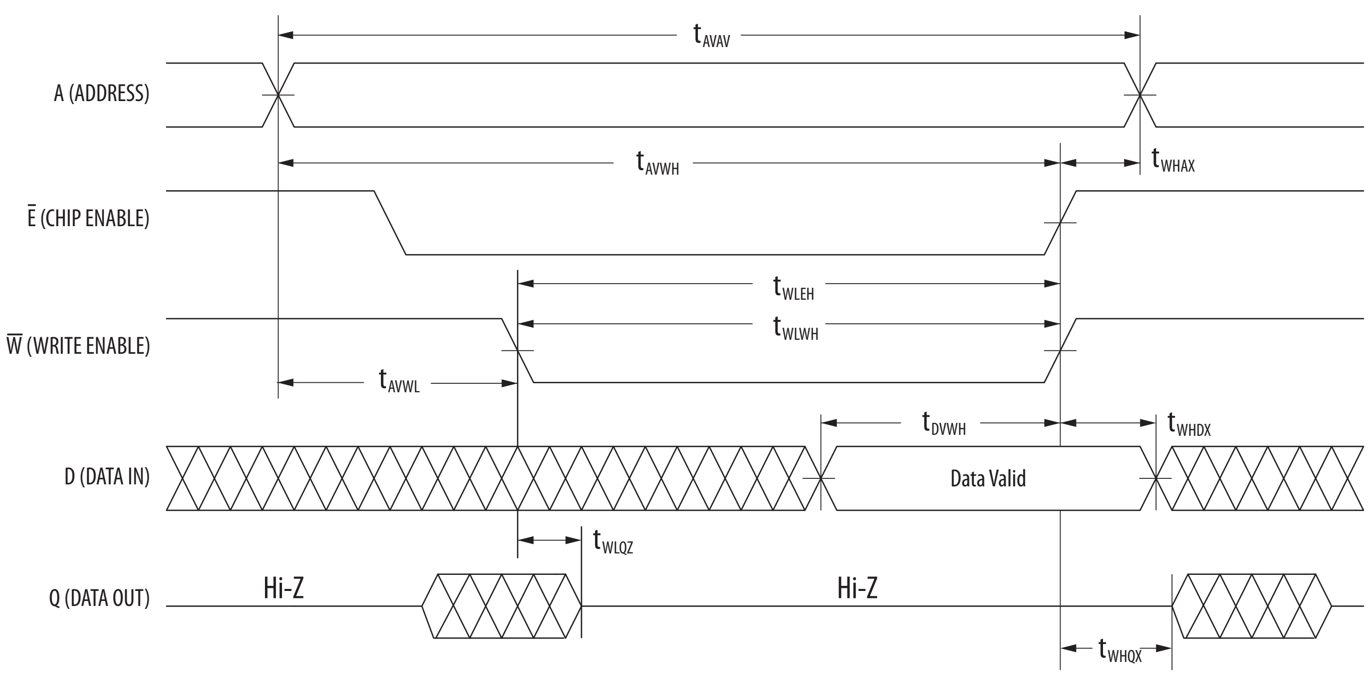


Table 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	45	-	ns
Address set-up time	t_{AVEL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	25	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	25	-	ns
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	20	-	ns
Enable to end of write ($\overline{G}$ low)[3]	t_{ELEH} t_{ELWH}	20	-	ns
Data valid to end of write	t_{DVEH}	15	-	ns
Data hold time	t_{EHDX}	0	-	ns
Write recovery time	t_{EHAX}	12	-	ns

1 All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

2 All write cycle timings are referenced from the last valid address to the first transition address.

3 If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)

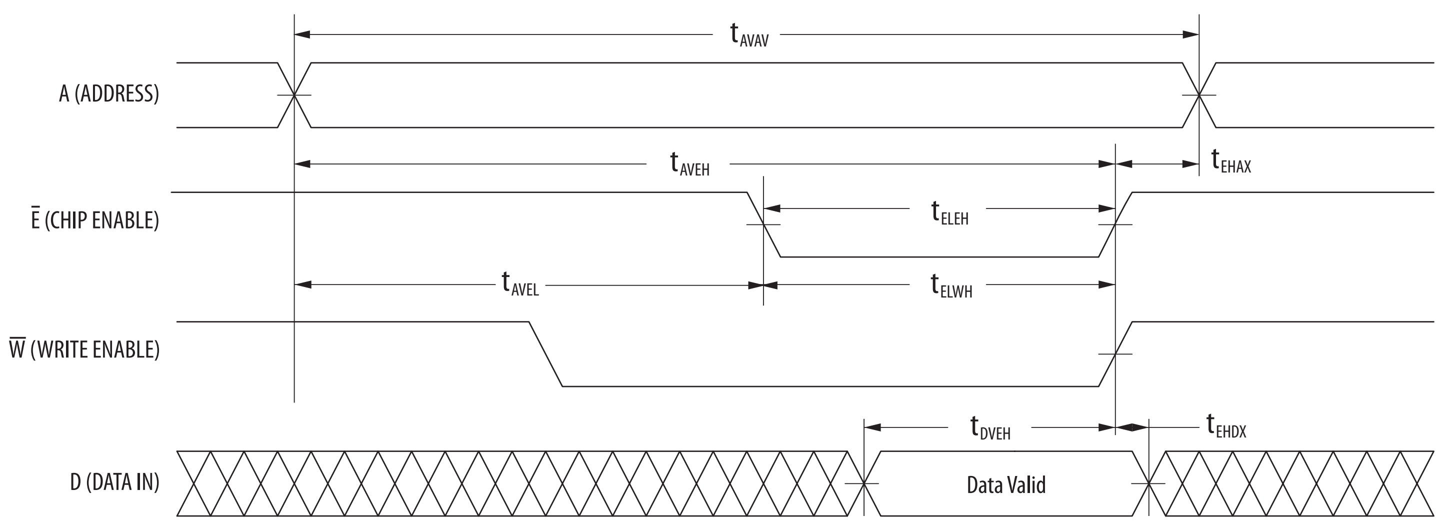
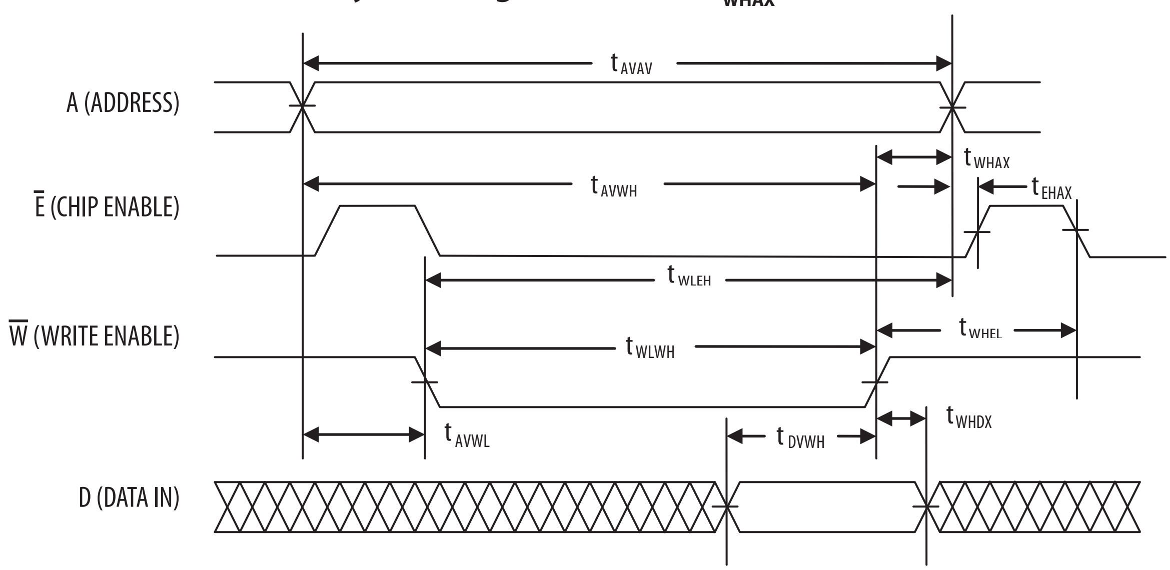


Table 3.6 Write Cycle Timing 3 (Shortened t_{WHAX}, $\overline{W}$ and $\overline{E}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	45	-	ns
Address set-up time —	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	25	-	ns
Address valid to end of write (G low)	t_{AVWH}	25	-	ns
Write pulse width	t_{WLWH} t_{WLEH}	20	-	ns
Data valid to end of write	t_{DVWH}	15	-	ns
Data hold time	t_{WHDX}	0	-	ns
Enable recovery time	t_{EHAX}	-2	-	ns
Write recovery time[3]	t_{WHAX}	6	-	ns
Write to enable recovery time[3]	t_{WHEL}	12	-	ns

1. All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
2. All write cycle timings are referenced from the last valid address to the first transition address.
3. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Table 3.6 Write Cycle Timing 3 (Shortened t_{WHAX}, $\overline{W}$ and $\overline{E}$ Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

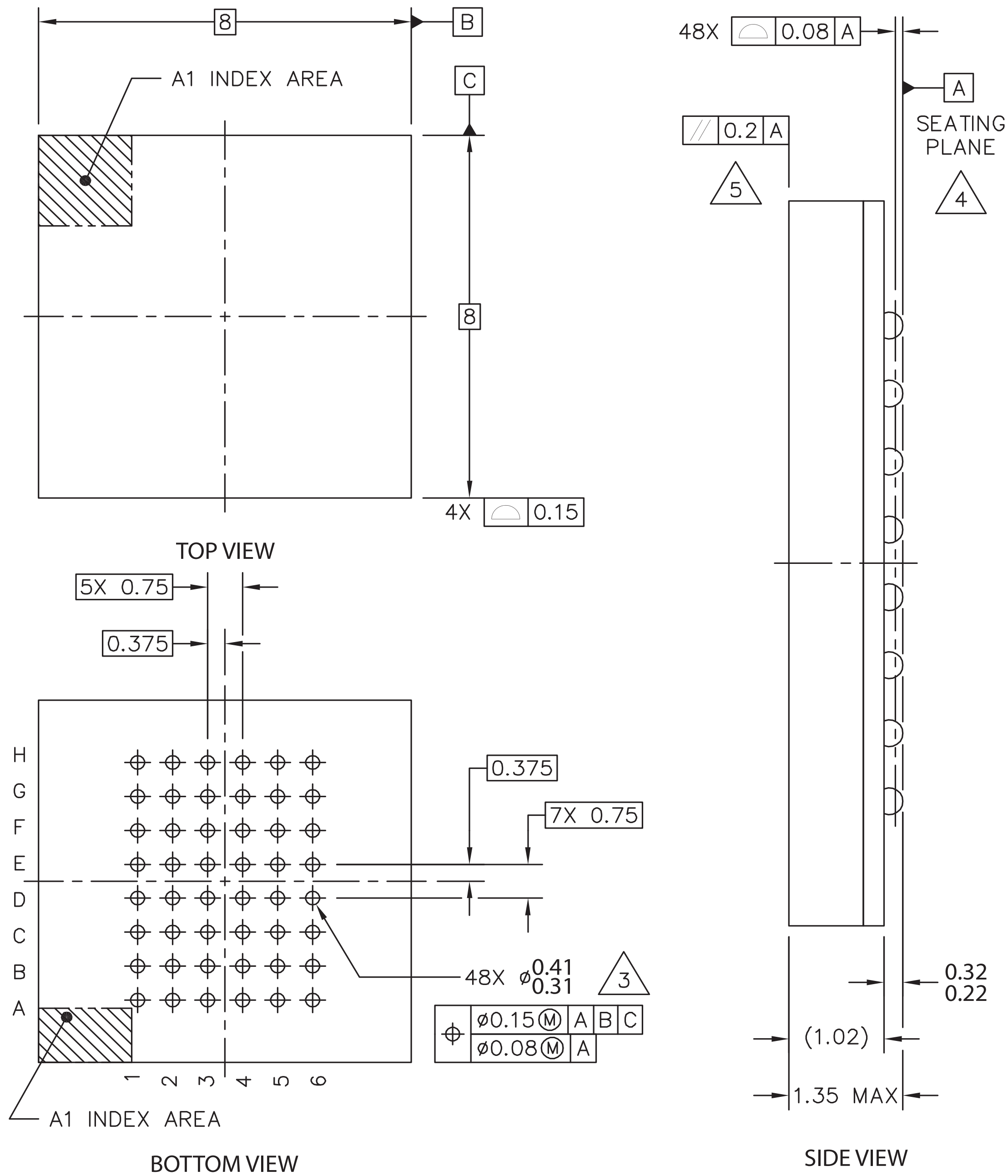
MR	0	D	08	B		MA	45	R

Carrier	(Blank= Tray,R=Tape & Reel)
Speed	(45 = 45 ns)
Package	(MA = FBGA)
Temperature Range	(Blank= 0 to +70 °C)
Revision	(B = Revision)
Data Width	(08 = 8-Bit)
Type	(D = Dual Supply)
Density	(0 = 1Mb)
Part Type	(MR = Magnetoresistive RAM)

Table 4.1 Available Parts

Part Number	Description	Temperature
MR0D08BMA45	Dual Supply 128x8 MRAM 48-BGA	Commercial
MR0D08BMA45R	Dual Supply 128x8 MRAM 48-BGA Tape & Reel	Commercial

Figure 5.1 FBGA



Print Version Not To Scale

1. Dimensions in Millimeters.
2. Dimensions and tolerances per ASME Y14.5M - 1994.
3. Maximum solder ball diameter measured parallel to DATUM A
4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

6. REVISION HISTORY

Revision	Date	Description of Change
0	Aug 24, 2009	Initial Product Concept
1	Oct 22, 2009	Added Write Cycle Timing 3. In table 2.4, I_{SB1} max changes from 7 to 8 mA and I_{SB2} from 6 to 7 mA. Added Tape & Reel Option in table 4.1. Changed to Production Level
2	Apr 7, 2010	Added I_{DDQ} specification in table 2.4.
3	Dec 9, 2011	Corrected Figure 5.1 FBGA drawing ball dimensions.
3.1	May 19, 2015	Revised contact information on Contact US page.
3.2	June 11, 2015	Correction to Japan Sales Office telephone number.
3.3	March 22, 2018	Updated the Contact Us table

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MR0D08B_Datasheet_EST370_Rev3.3 032218