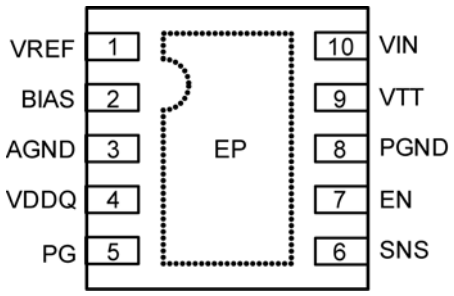
Ordering Information

Part Number	Output Voltage	Junction Temperature Range[1]	Package	Lead Finish
MIC5166YML	½VDDQ	–40°C to +125°C	10-Pin 3mm × 3mm MLF®	Pb-Free

Note:

1. MLF® is a GREEN RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free..

Pin Configuration



10-Pin 3mm × 3mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Description
1	VREF	Reference Voltage. This output provides an output of the internal reference voltage $V_{DDQ}/2$. The V_{REF} output is used to provide the reference voltage for the memory chip. Connect a 1.0µF capacitor to ground at this pin. This pin can sink and source 10mA.
2	BIAS	BIAS Supply Voltage. The BIAS supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. The BIAS voltage must be greater than (V_{TT} + 2.2V). A 1.0µF ceramic capacitor from the BIAS pin to PGND must be placed next to the IC.
3	AGND	Analog Ground. Internal signal ground for all low-power circuits.
4	VDDQ	Input Supply. VDDQ is connected to an internal precision divider which provides the V_{REF}. Connect a 4.7µF capacitor to ground at this pin.
5	PG	Power Good. This is an open drain output that indicates when the output voltage is within ±10% of the reference voltage. The PG flag is asserted typically with 65µs delay when the enable is set low or when the output goes outside ±10% the window threshold.
6	SNS	Feedback. Input to the error amplifier.
7	EN	Enable. Logic level control of the output. Logic HIGH enables the MIC5166 and a logic LOW shuts down the MIC5166. In the off state, supply current of the device is greatly reduced (typically 0.2µA). The EN pin should not be left open.
8	PGND	Power Ground. Internal ground connection to the source of the internal, low-side drive, N-channel MOSFET.
9	VTT	Power Output. This is the connection to the source of the internal high-side N-channel MOSFET and drain of the low-side N-channel MOSFET. This is a high-frequency, high-power connection, therefore two 10µF output capacitors must be placed as close to the IC as possible.
10	VIN	High-Side N-Channel MOSFET Drain Connection. The V_{IN} operating voltage range is from 0.9V to 3.6V. An input capacitor between the VIN pin and the PGND is required as close to the chip as possible.
EP	ePad	Exposed Pad. Must be connected to a GND plane for best thermal performance.

Absolute Maximum Ratings[1]

V_{BIAS} ..... –0.3V to 6V
V_{IN} ..... –0.3V to V_{BIAS}
V_{DDQ} ..... –0.3V to V_{IN}
V_{TT} ..... –0.3V to V_{IN}
V_{EN} ..... –0.3V to V_{BIAS}
V_{PG} ..... –0.3V to V_{BIAS}
PGND to AGND ..... –0.3V to 0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10s)..... 260°C
Continuous Power Dissipation (T_A = 25°C)
(De-rated 16.4mW/°C above 25°C)..... 1.64W
Continuous Power Dissipation (T_A = 85°C) 656mW
ESD[2] ..... 2kV(HBM)

Operating Ratings[3]

Supply Voltage (V_{BIAS})..... 2.5V to 5.5V
Supply Voltage (V_{IN})..... 0.9V to 3.6V[4]
Supply Voltage (V_{DDQ})..... 0.9V to V_{IN} [5]
Power Good Voltage (V_{PG})..... 0V to V_{BIAS}
Enable Input (V_{EN})..... 0V to V_{BIAS}
Junction Temperature (T_J) ..... –40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
3mm x 3mm MLF®-10 (θ_{JC})..... 28.7°C/W
3mm x 3mm MLF®-10 (θ_{JA})..... 60.7°C/W

Electrical Characteristics[6]

V_{IN} = 1.5V, V_{BIAS} = 3.3V, V_{DDQ} = 1.5V, T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (V_{IN})		**0.9**		**3.6**	V
Undervoltage Lockout Trip Level	V_{IN} Rising	**0.625**	0.8	**0.9**	V
UVLO Hysteresis			150		mV
Quiescent Supply Current (I_{IN})	I_{OUT} = 0A		0.1	10	µA
Shutdown Current (I_{IN})	V_{EN} = 0V		0.1	5	µA
Bias Supply					
Bias Voltage Range (V_{BIAS})		**2.5**		**5.5**	V
Undervoltage Lockout Trip Level	V_{BIAS} Rising	**1.9**	2.23	**2.33**	V
UVLO Hysteresis			70		mV
Quiescent Supply Current (I_{BIAS})	I_{OUT} = 1mA		1.6	**3**	mA
	I_{OUT} = 1A		1.6	**3**	
Shutdown Current (I_{BIAS})	V_{EN} = 0V		0.1	5	µA
V_{TT} Output					
V_{TT} Accuracy	Variation from V_{REF}, I_{OUT} = -3A to 3A	**–40**		**40**	mV
Load Regulation	V_{SNS} =0.75V, I_{OUT} = 10mA to +3A		1.5	**2.1**	%
	V_{SNS} =0.75V, I_{OUT} = -10mA to -3A	**–1.8**	–1.4		
Line Regulation	V_{IN} = 1.5V to 3.6V, V_{BIAS} = 5.5V, I_{OUT} = 100mA	**–0.05**	0.005	**0.05**	%/V
	V_{IN} = 1.5V, V_{BIAS} = 2.5V to 5.5V, I_{OUT} = 100mA	**–0.1**	0.015	**0.17**	

Electrical Characteristics[6] (Continued)

V_{IN} = 1.5V, V_{BIAS} = 3.3V, V_{DDQ} = 1.5V, T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

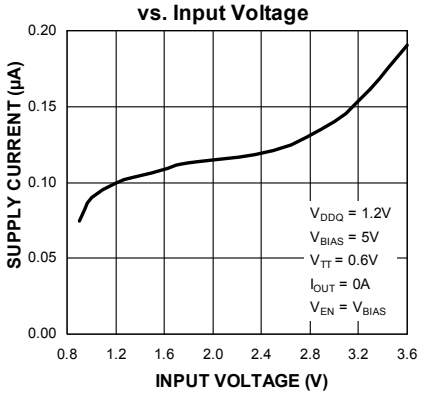
Parameter	Condition	Min.	Typ.	Max.	Units
V_{REF} Output					
V_{REF} Voltage Accuracy	Variation from (V_{DDQ}/2), I_{REF} = -10mA to 10mA	**–1**		**1**	%
Bias Supply Dropout Voltage					
Dropout Voltage (V_{BIAS} – V_{TT})	I_{OUT} = 100mA		1.15		V
Dropout Voltage (V_{BIAS} – V_{TT})	I_{OUT} = 500mA		1.25		V
Dropout Voltage (V_{BIAS} – V_{TT})	I_{OUT} = 3.0A		1.65	**2.2**	V
Enable Control					
EN Logic High Level	Logic High	**1.2**			V
EN Logic Low Level	Logic Low			**0.2**	V
EN Current	V_{EN} = 0.2V		1.0		µA
	V_{EN} = 1.2V		6.0		
Start-Up Time	From EN pin going high to V_{TT} 90% of V_{REF}		55		µs
Short-Current Protection					
Sourcing Current Limit	V_{IN} = 2.7V, V_{TT} = 0V	**3.1**	4.9	**7.8**	A
Sinking Current Limit	V_{IN} = 2.7V, V_{TT} = V_{IN}	**–3.1**	–4.9	**–7.8**	A
Internal FETs					
Top-MOSFET $R_{DS(ON)}$	Source, I_{OUT} = 3A (V_{TT} to PGND)		130	**190**	mΩ
Bottom-MOSFET $R_{DS(ON)}$	Sink, I_{OUT} = -3A (V_{IN} to V_{TT})		130	**190**	mΩ
Power Good (PG)					
PG Window	Threshold % of V_{TT} from V_{REF}	≥90		≤110	%
Hysteresis			2		%
PG Output Low Voltage	I_{PG} = 4mA (sinking)		430		mV
PG Leakage Current	V_{PG} = 5.5V, V_{SNS} = V_{REF}			**1.0**	µA
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		150		°C
Over-Temperature Shutdown Hysteresis			10		°C

Notes:

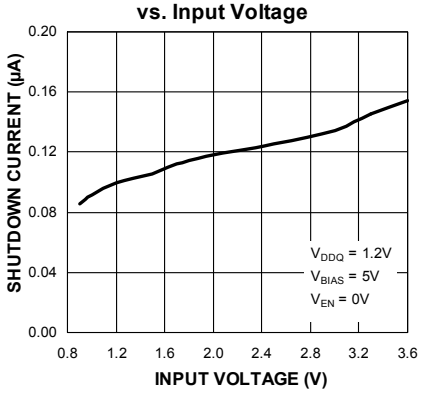
1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside its operating rating.
4. If $V_{BIAS} \le 3.6V$, then $V_{IN(MAX)} = V_{BIAS}$.
5. If $V_{BIAS} \le 4V$, then $V_{DDQ(MAX)} = 2 \times (V_{BIAS} - 2.2V)$. If $V_{BIAS} > 4V$, then $V_{DDQ(MAX)} = 3.6V$.
6. Specification for packaged product only.

Typical Characteristics

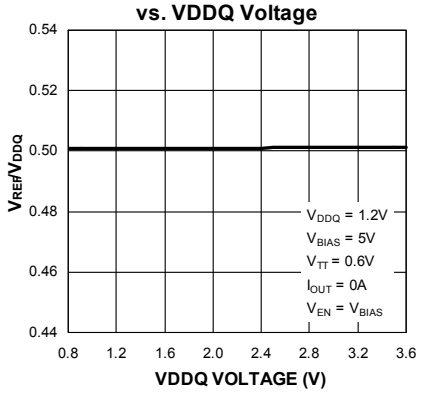
V_{IN} Operating Supply Current vs. Input Voltage



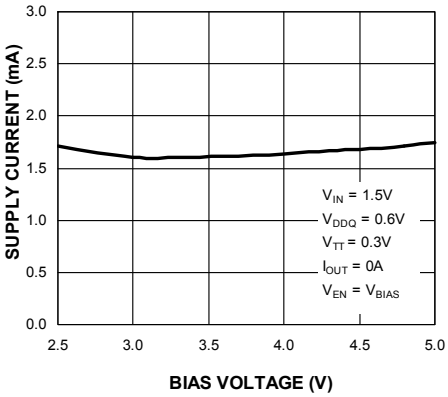
V_{IN} Shutdown Current vs. Input Voltage



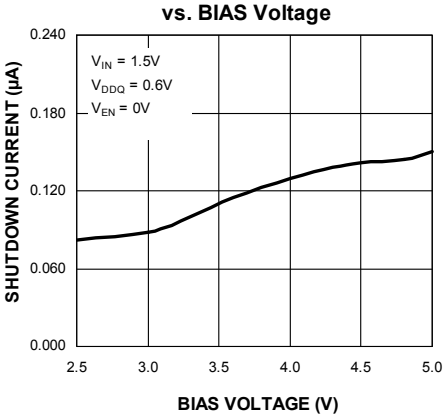
V_{REF}/V_{DDQ} Tracking Ratio vs. VDDQ Voltage



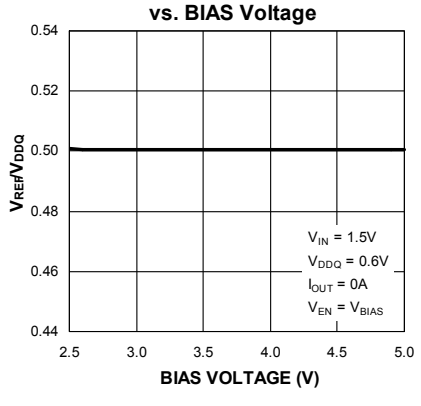
V_{BIAS} Operating Supply Current vs. BIAS Voltage



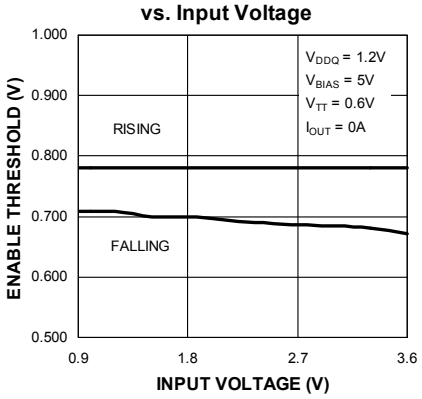
V_{BIAS} Shutdown Current vs. BIAS Voltage



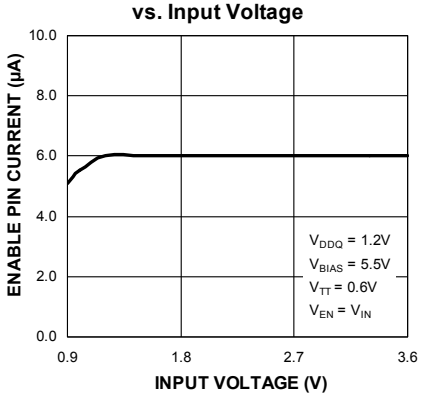
V_{REF}/V_{DDQ} Tracking Ratio vs. BIAS Voltage



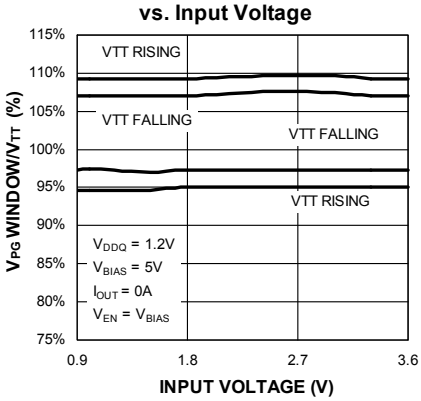
Enable Threshold vs. Input Voltage



Enable Pin Current vs. Input Voltage

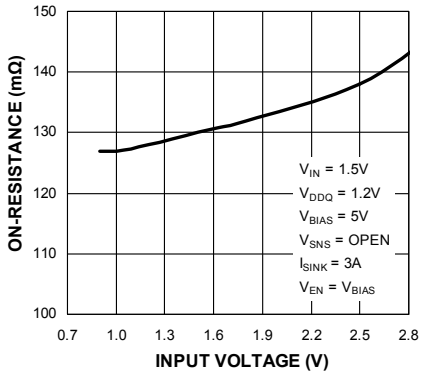


Power Good Window/V_{TT} Ratio vs. Input Voltage

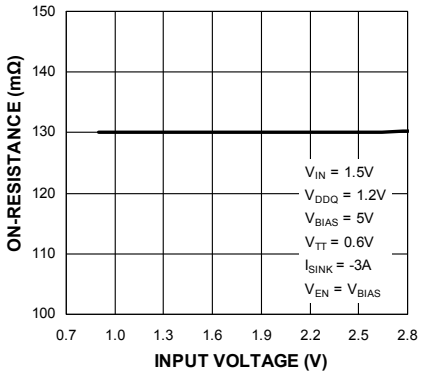


Typical Characteristics (Continued)

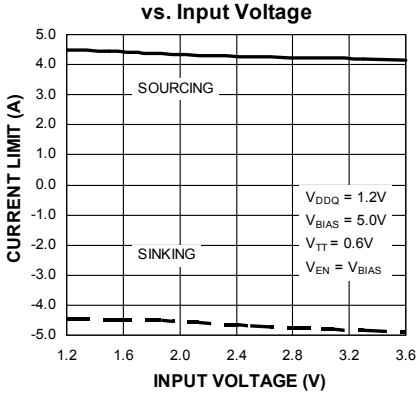
Top MOSFET On-Resistance vs. Input Voltage



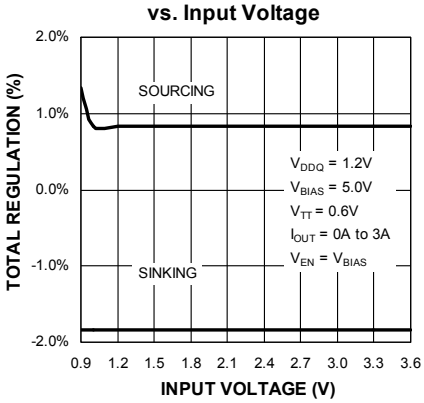
Bottom MOSFET On-Resistance vs. Input Voltage



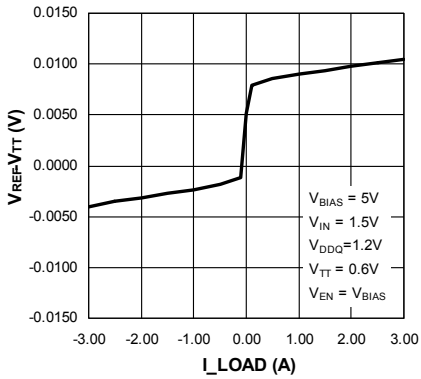
Current Limit vs. Input Voltage



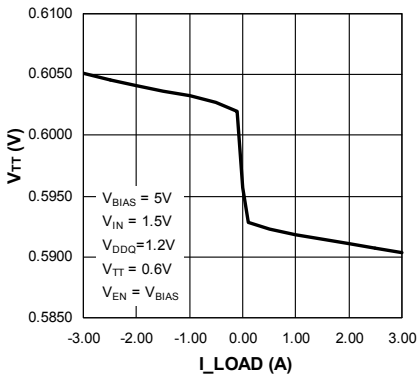
Load Regulation vs. Input Voltage



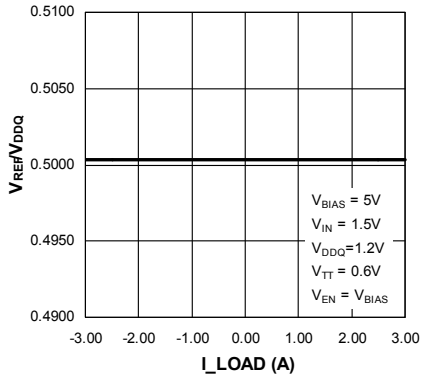
V_{REF}-V_{TT} vs. I_Load



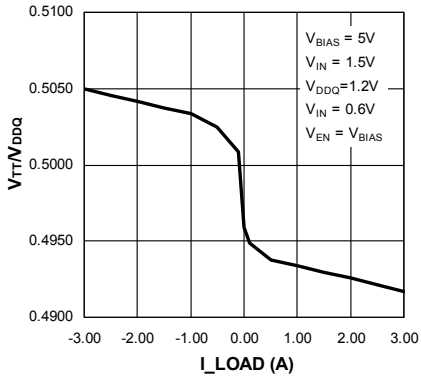
V_{TT} vs. I_Load



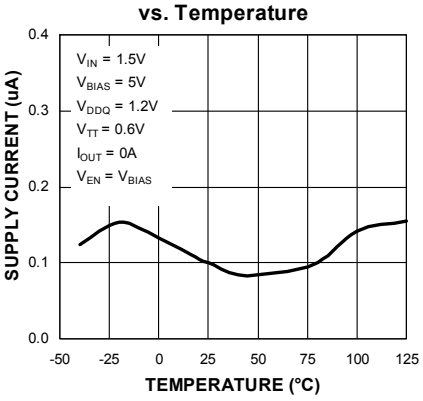
V_{REF}/V_{DDQ} vs. I_Load



V_{TT}/V_{DDQ} vs. I_Load

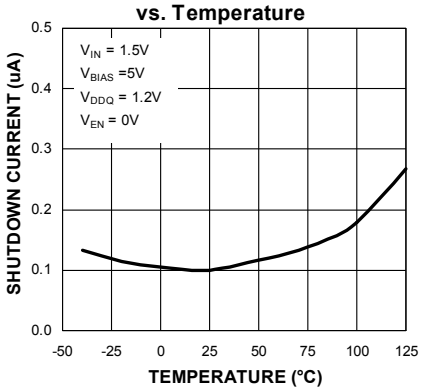


V_{IN} Operating Supply Current vs. Temperature

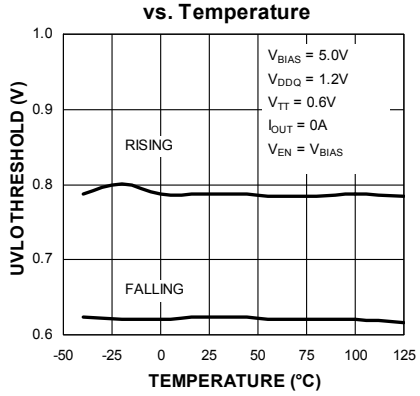


Typical Characteristics (Continued)

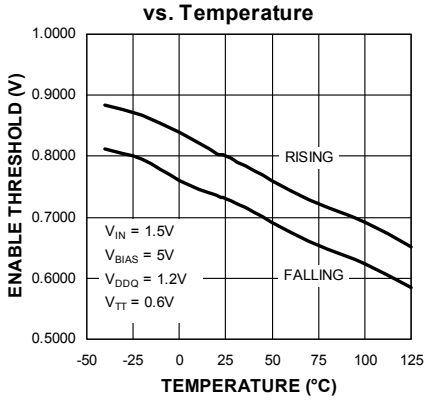
V_{IN} Shutdown Current vs. Temperature



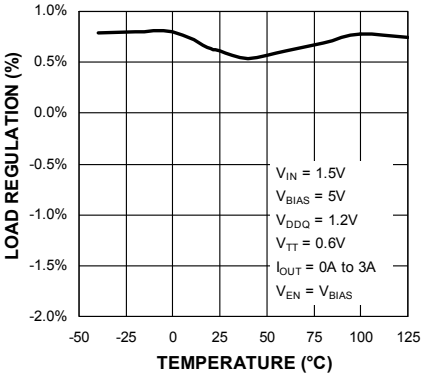
V_{IN} UVLO Threshold vs. Temperature



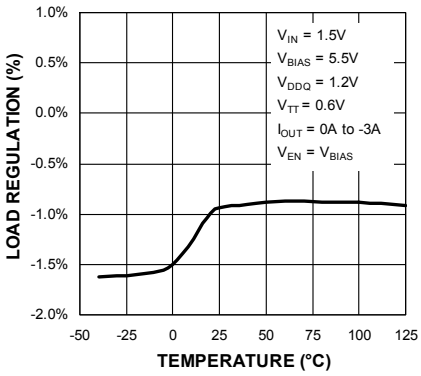
Enable Threshold vs. Temperature



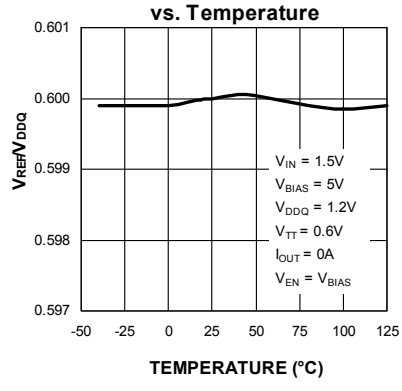
Sourcing Load Regulation vs. Temperature



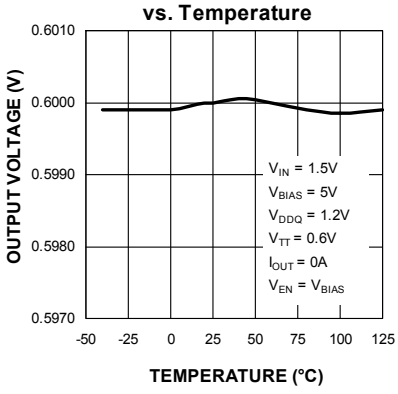
Sinking Load Regulation vs. Temperature



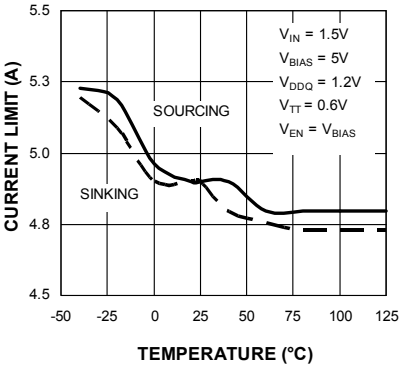
V_{REF}/V_{DDQ} Tracking Ratio vs. Temperature



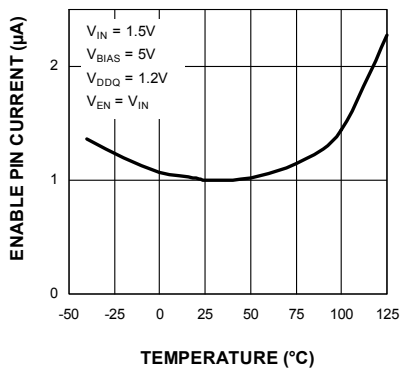
Output Voltage vs. Temperature



Current Limit vs. Temperature

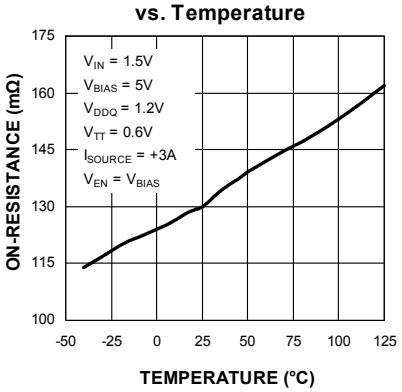


Enable Pin Current vs. Temperature

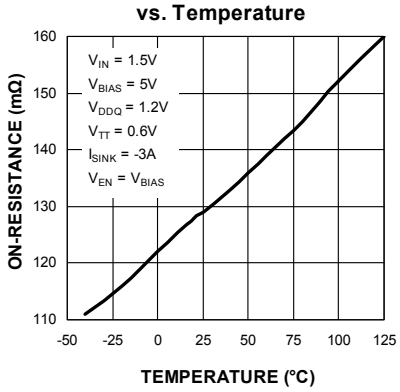


Typical Characteristics (Continued)

Top MOSFET On-Resistance vs. Temperature

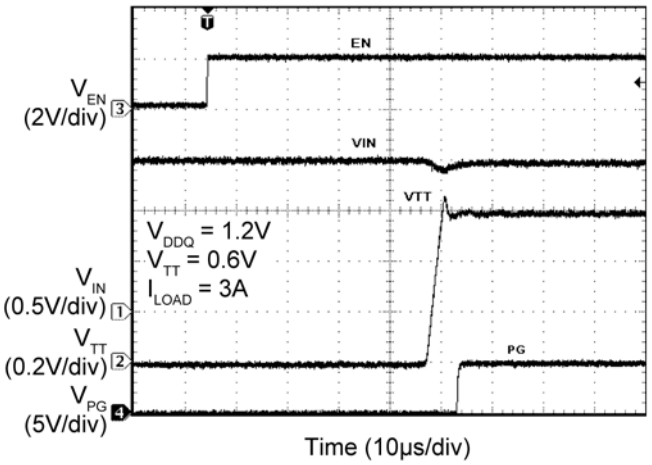


Bottom MOSFET On-Resistance vs. Temperature

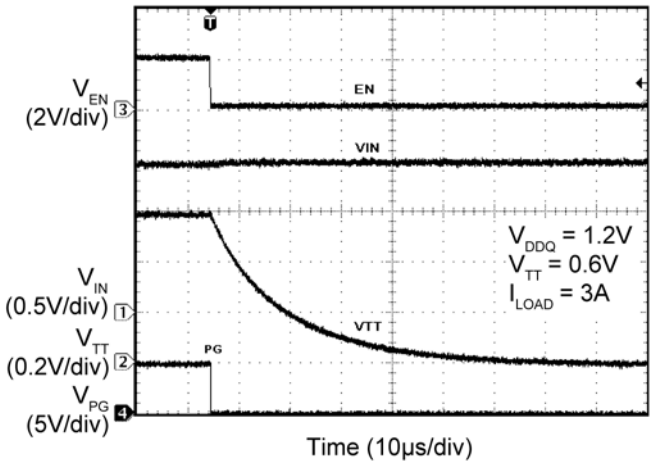


Functional Characteristics

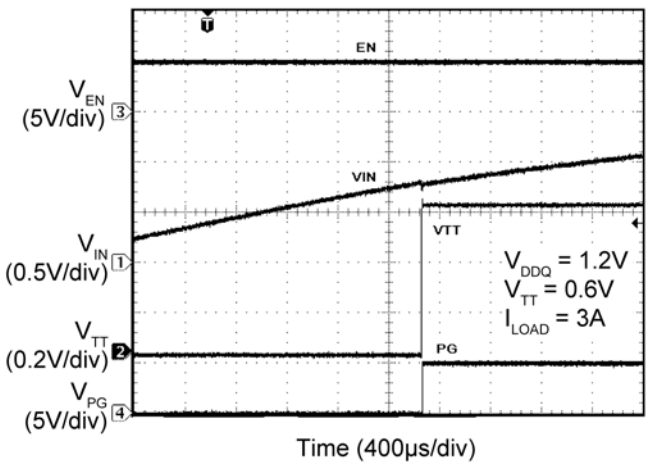
EN Turn-On



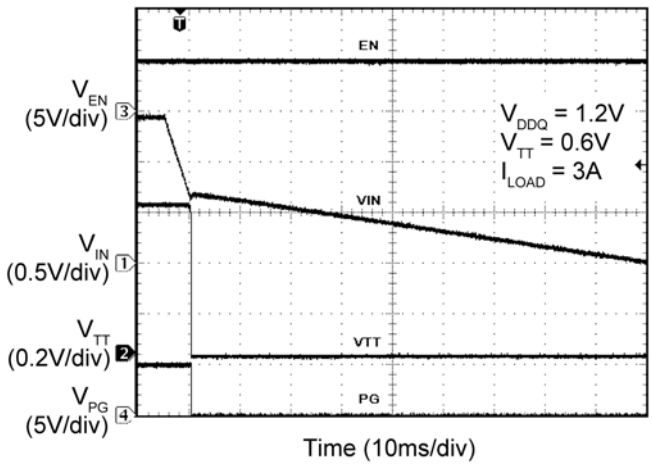
EN Turn-Off



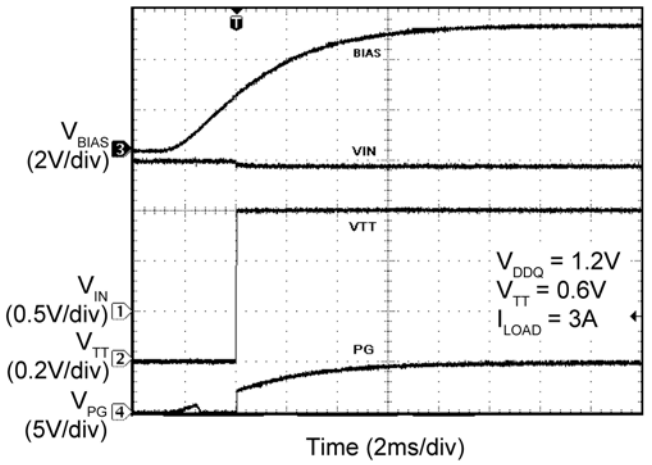
V_{IN} Turn-On (UVLO)



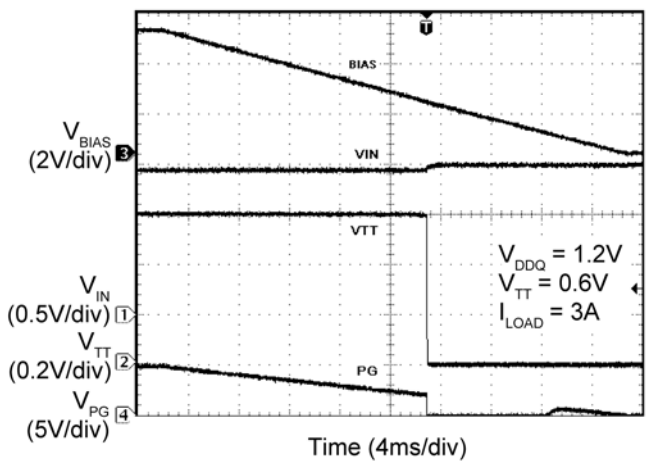
V_{IN} Turn-Off (UVLO)



V_{BIAS} Turn-On (UVLO)

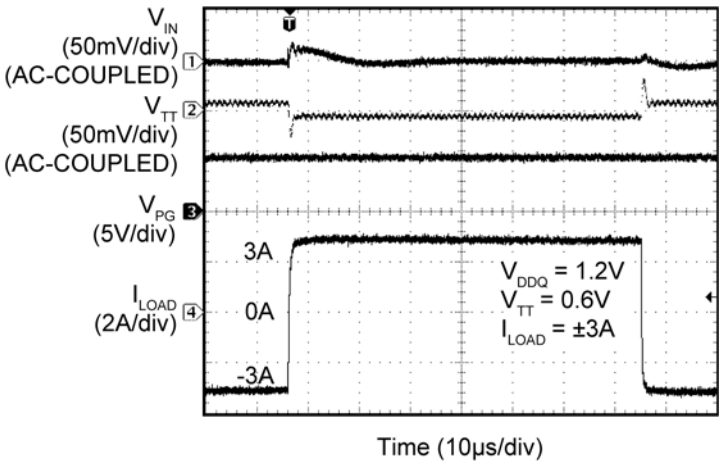


V_{BIAS} Turn-Off (UVLO)

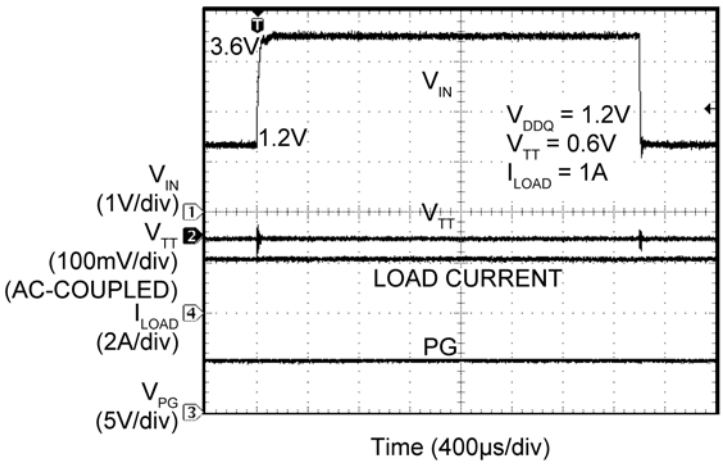


Functional Characteristics (Continued)

Load Transient (±3A)



Line Transient



Functional Diagram

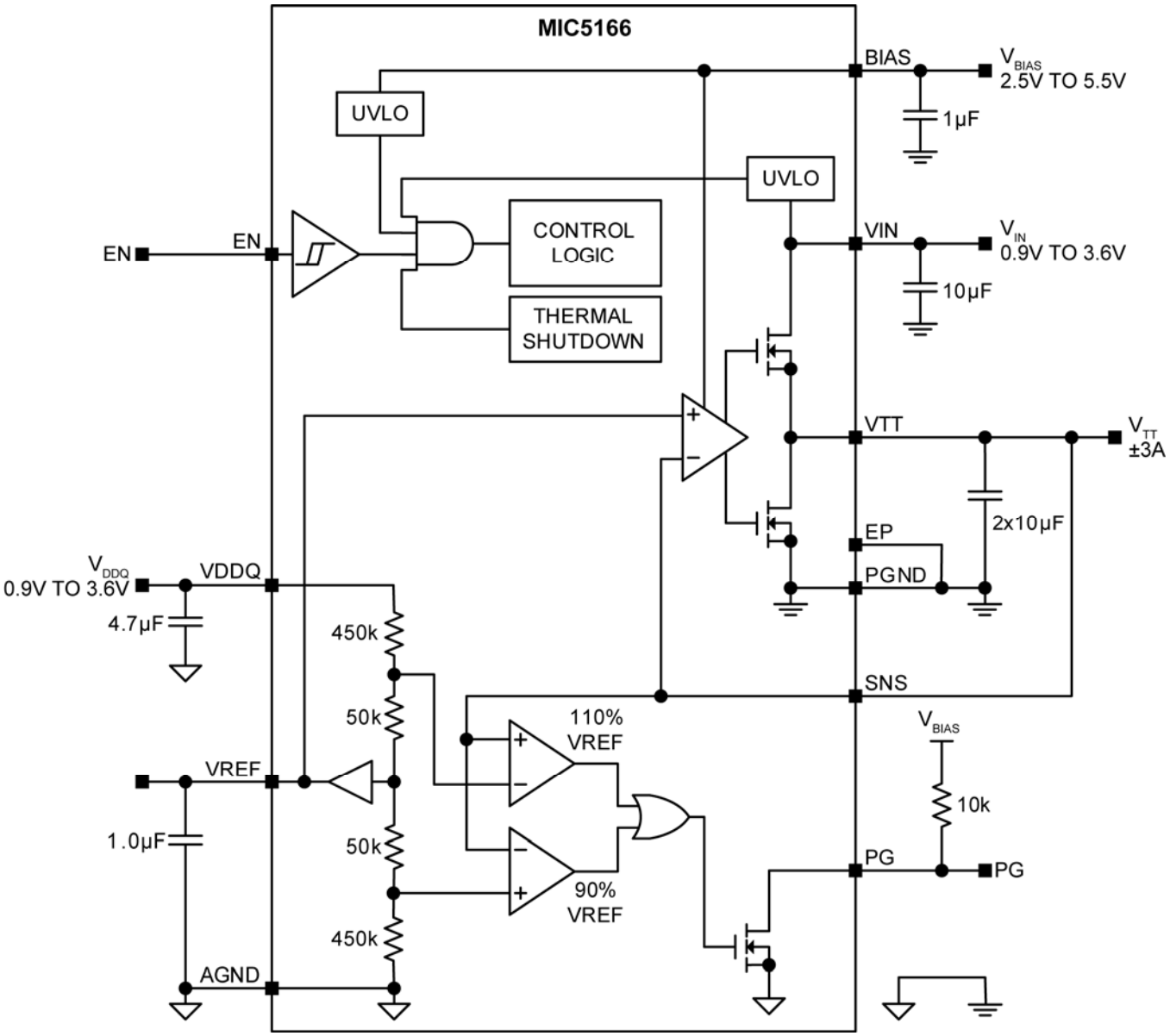


Figure 1. MIC5166 Block Diagram

Application Information

DDR memory requires two power supplies, one for the memory chip, referred to as V_{DDQ} and the other for a termination supply V_{TT}, which is one-half V_{DDQ}. With memory speeds in excess of 300MHz, the memory system bus must be treated as a transmission line. To maintain good signal integrity the memory bus must be terminated to minimize signal reflections. Figure 2 shows the simplified termination circuit. Each control, address and data lines have these termination resistors RS and RT connected to them.

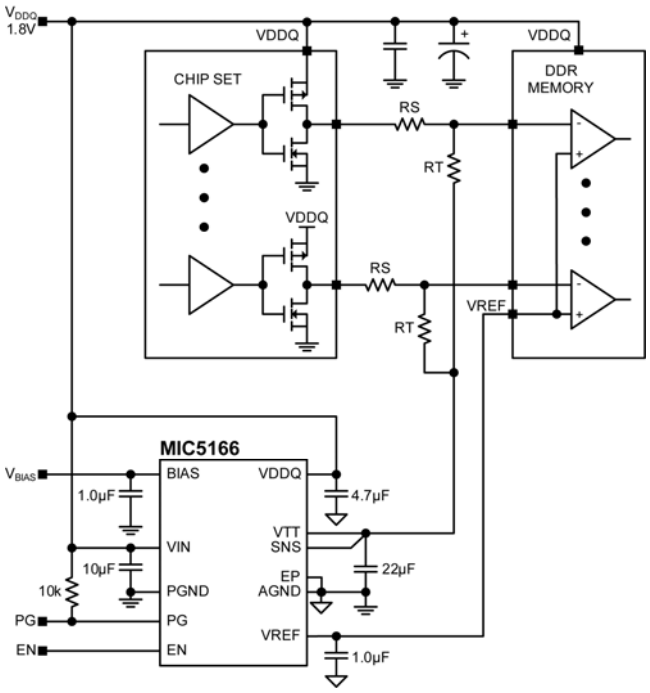


Figure 2. DDR Memory Termination Circuit

Bus termination provides a means to increase signaling speed while maintaining good signal integrity. The termination network consists of a series resistor (R_S) and a terminating resistor (R_T). Values of R_S range between 10Ω to 30Ω with a typical of 22Ω, while R_T ranges from 22Ω to 28Ω with a typical value of 25Ω. V_{REF} must maintain half V_{DDQ} with a ±1% tolerance, while V_{TT} will dynamically sink and source current to maintain a termination voltage of ±40mV from the V_{REF} line under all conditions. This method of bus termination reduces common-mode noise, settling time, voltage swings, EMI/RFI and improves slew rates.

V_{DDQ} powers all the memory ICs, memory drivers and receivers for all the memory bits in the DDR memory system. The MIC5166 regulates V_{TT} to $V_{DDQ/2}$ during sourcing or sinking current.

The memory bits are not usually all at a logic high or logic low at the same time so the V_{TT} supply is usually not sinking or sourcing –3A or +3A current continuously.

V_{TT}

V_{TT} is regulated to V_{REF}. Due to high-speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate transient response, two 10µF ceramic capacitors are required. The proper placement of ceramic capacitors is important to reduce both ESR and ESL such that high-current and high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is important to reduce the effects of PCB trace inductance.

V_{DDQ}

The V_{DDQ} input on the MIC5166 is used to create the internal reference voltage for V_{TT}. The reference voltage is generated from an internal resistor divider network of two 500kΩ resistors, generating a reference voltage V_{REF} that is $V_{DDQ/2}$. The V_{DDQ} input should be Kelvin connected as close as possible to the memory supply voltage.

Since the reference is simply $V_{DDQ/2}$, any perturbations on V_{DDQ} will also appear at half the amplitude on the reference. For this reason a 4.7µF ceramic capacitor is required on the V_{DDQ} supply. This will aid performance by improving the source impedance over a wide frequency range.

Sense

The sense (SNS) pin provides the path for the error amplifier to regulate V_{TT}. The SNS input must also be Kelvin connected to the V_{TT} bypass capacitors. If the SNS input is connected to close to the MIC5166, the IR drop of the PCB trace can cause the V_{TT} voltage at the memory chip to be too low. Placing the MIC5166 as close as possible to the DDR memory will improve the load regulation performance.

Enable

The MIC5166 features an active-high enable input (EN) that allows on-off control of the regulator. The current through the device reduces to near “zero” when the device is shutdown, with only <0.2µA of leakage current. The EN input may be directly tied to V_{BIAS}. The active high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

Power Good (PG)

The power-good (PG) output provides an under and over voltage fault flag for the V_{TT} output. The PG output remains high as long as V_{TT} is within ±10% range of V_{REF} and goes low if the output moves beyond this range.

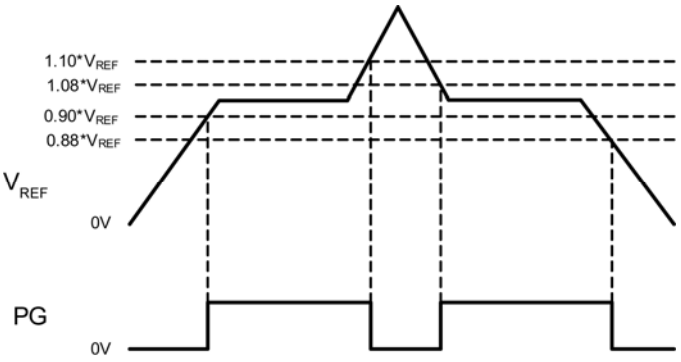


Figure 3. Power Good Threshold

The PG has an open-drain output. A pull-up resistor must be connected to V_{IBIAS}, V_{IN} or an external source. The external source voltage must not exceed the maximum rating of the pin. The PG pin can be connected to another regulator's enable pin for sequencing of the outputs.

V_{BIAS} Requirement

A 1µF ceramic input capacitor is required on V_{BIAS} pin. To achieve the ultra-fast transient response, the MIC5166 uses an all N-channel power output stage as shown in the Functional Diagram. The high-side N-channel MOSFET requires the V_{BIAS} voltage to be 2.2V higher than the V_{TT} to be able to fully enhance the high-side MOSFET.

V_{IN} Requirement

V_{IN} is used to supply the rail voltage for the high-side N-channel power output stage. It is normally connected to V_{DDQ}, but it can be connected to a lower voltage to reduce power dissipation. In this case, the input voltage must be higher than the V_{TT} voltage to ensure that the output stage is not operating in dropout.

Component Selection

Input Capacitor

A 10µF ceramic input capacitor is all that is required for most applications if it is close to a bulk capacitance.

The input capacitor must be placed on the same side of the board and next to the MIC5166 to minimize the dropout voltage and voltage ringing during transient and short circuit conditions. It is also recommended that each capacitor to be connected to the PGND directly, not through vias. X7R or X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic.

Output Capacitor

As part of the frequency compensation, the MIC5166 requires two 10µF ceramic output capacitors for best transient performance. To improve transient response, any other type of capacitor can be placed in parallel as long as the two 10µF ceramic output capacitors are placed next to the MIC5166.

The output capacitor type and placement criteria are the same as the input capacitor. See the input capacitor section for a detailed description.

Thermal Considerations

The MIC5166 is packaged in the 3mm x 3mm MLF®, a package that has excellent thermal performance. This maximizes heat transfer from the junction to the exposed pad (ePad) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board.

Thermal Design

The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application-specific parameters:

- Maximum ambient temperature (T_A)
- Output current (I_{OUT})
- Output voltage (V_{OUT})
- Input voltage (V_{IN})
- Ground current (I_{GND})

First, calculate the power dissipation of the regulator from these numbers and the device parameters from this datasheet.

$$P_D = (V_{IN} – V_{TT}) \times I_{OUT +} (V_{BIAS} \times I_{GND}) \quad \text{Eq. 1}$$

where the ground current is approximated by using numbers from the “Electrical Characteristics” or “Typical Characteristics.”

For example, given an expected maximum ambient temperature (T_A) of 70°C with V_{IN} = 1.2V, V_{BIAS} = 3.3V, V_{TT} = 0.9V, and I_{OUT} = 3A, first calculate the expected P_D using Equation 1:

$$P_D = (1.2V – 0.9V) \times 3A + 3.3V \times 0.0016A$$
$$= 0.90528W \quad \text{Eq. 2}$$

Next, determine the junction temperature for the expected power dissipation above using the thermal resistance (θ_{JA}) of the 10-pin 3mm × 3mm MLF® (YML) adhering to the following criteria for the PCB design (1oz. copper and 100mm^2 copper area for the MIC5166):

$$T_J = (\theta_{JA} \times P_D) + T_A = (60.7°C/W \times 0.90528W) + 70°C$$
$$= 124.95°C \quad \text{Eq. 3}$$

To determine the maximum power dissipation allowed that would not exceed the IC’s maximum junction temperature (125°C) when operating at a maximum ambient temperature of 70°C:

$$P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA} = (125°C – 70°C)/(60.7°C/W)$$
$$= 0.9061W \quad \text{Eq. 4}$$

Thermal Measurements

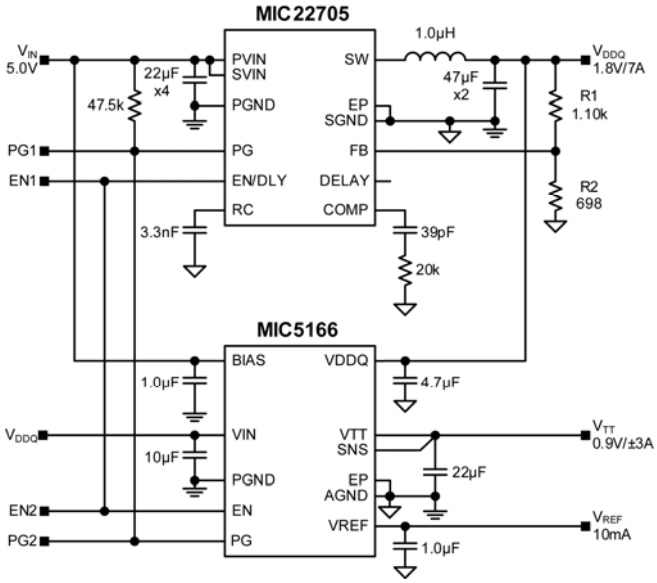
It is always wise to measure the IC’s case temperature to make sure that it is within its operating limits. Although this might seem like a very elementary task, it is very easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with the thermal voltage meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

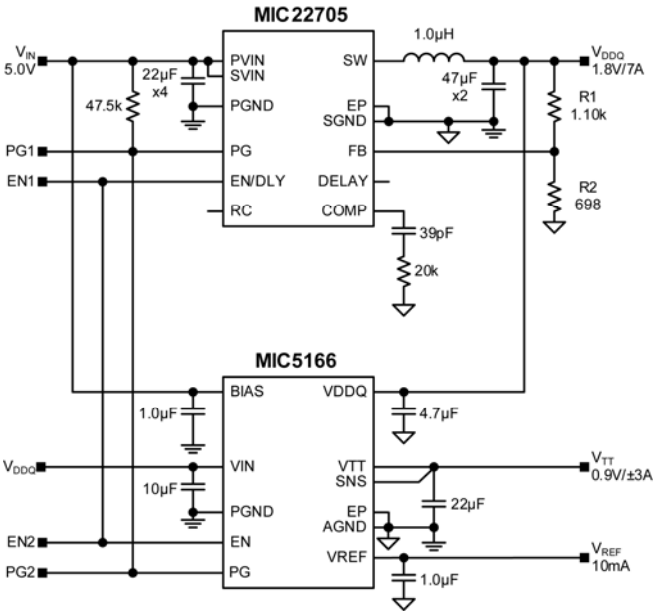
There are two suggested methods for measuring the IC case temperature: a thermocouple or an infrared thermometer. If a thermocouple is used, it must be constructed of 36 gauge wire or higher to minimize the wire heatsinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to make sure that the thermocouple junction is making good contact to the case of the IC. This thermocouple from Omega (5SC-TT-K-36-36) is adequate for most applications.

To avoid this messy thermocouple grease or glue, an infrared thermometer is recommended. Most infrared thermometers’ spot size is too large for an accurate reading on small form factor ICs. However, an IR thermometer from Optris has a 1mm spot size, which makes it ideal for the 3mm x 3mm MLF® package.

Sequencing

The following diagrams illustrate methods for connecting MIC5166's to achieve sequencing requirements:





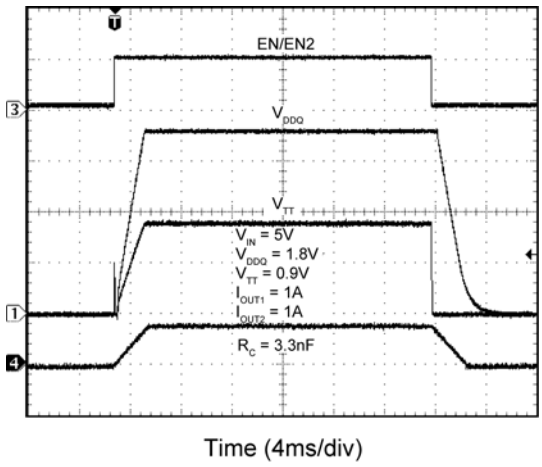


Figure 6. Turn-On Sequence with Soft-Start (RC = 3.3nF)

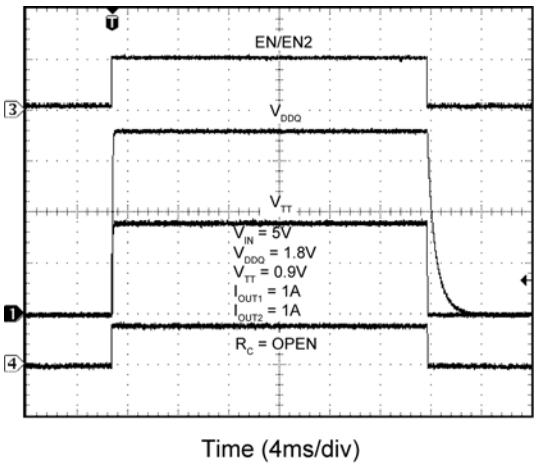


Figure 7. Turn-On Sequence with No Soft-Start (RC = Open)

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC5166 converter.

IC

- The 10µF ceramic capacitor, which is connected to the VIN pin, must be located right at the IC. The VDDQ pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDDQ and AGND pins.
- The signal ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use wide traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

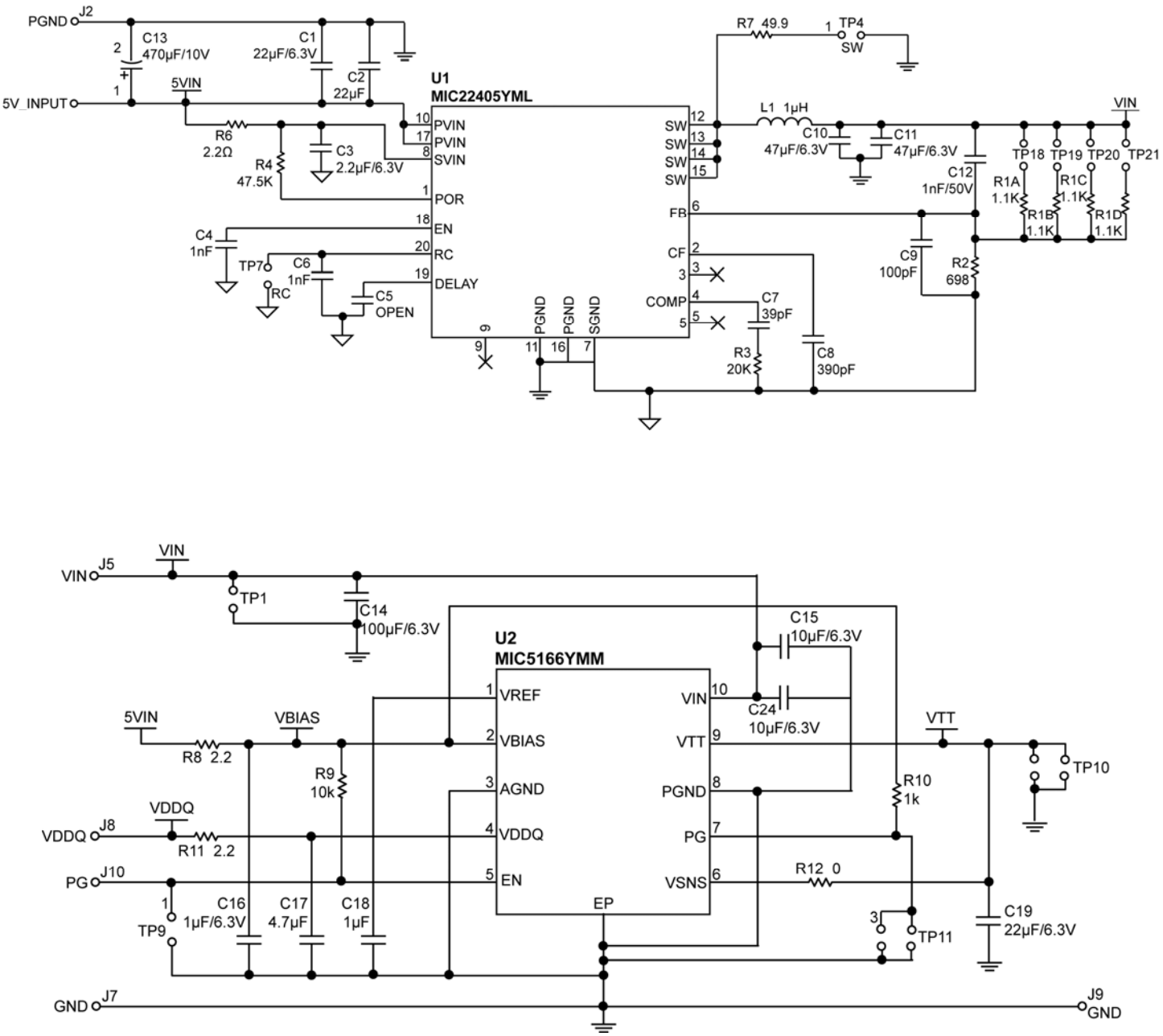
Input Capacitor

- A 10µF X5R or X7R dielectric ceramic capacitor is recommended on each of the VIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the VIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

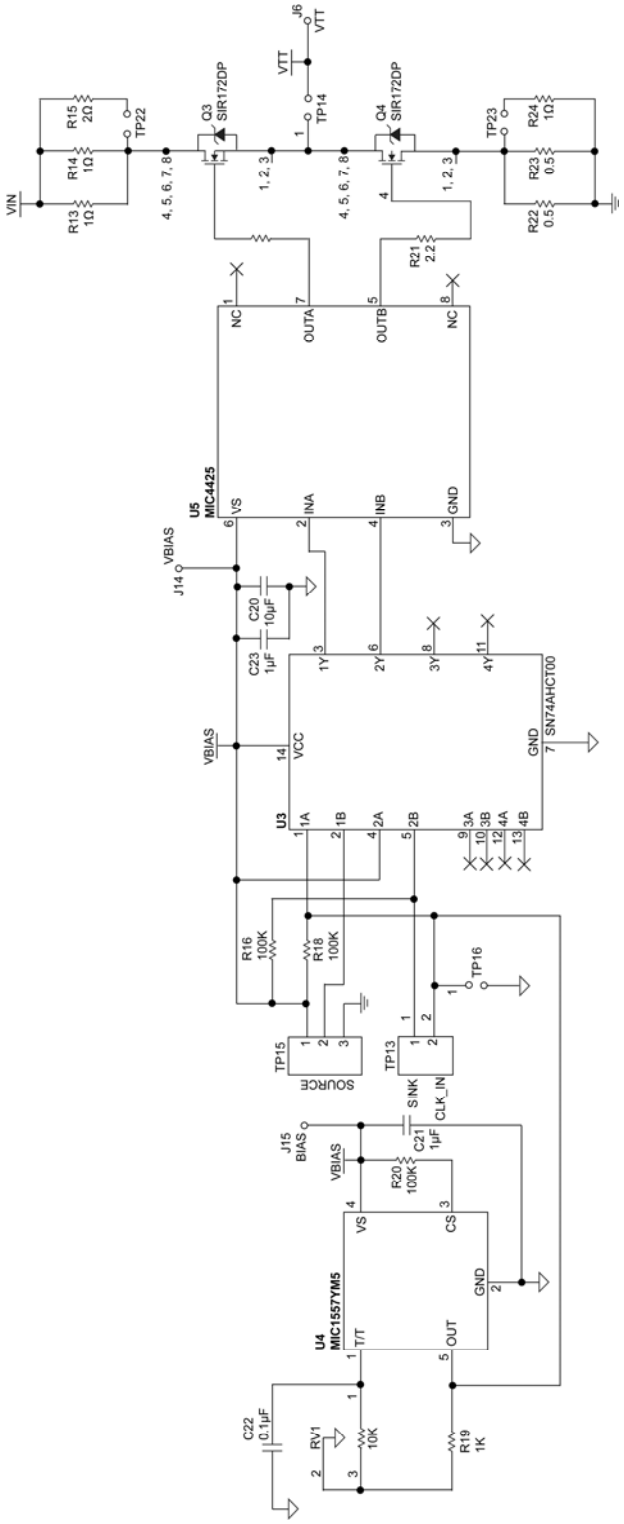
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to AGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Evaluation Board Schematics



Evaluation Board Schematics (Continued)



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C19	08056D226MAT	AVX[3]	22µF, 6.3V, ceramic capacitor, X5R, 0805	3
	C2012X5R0J226K	TDK[2]		
	GRM21BR60J226ME39L	Murata[1]		
C3	08056D225KAT2A	AVX[3]	2.2µF, 6.3V, ceramic capacitor, X5R, 0805	1
	C2012X5R0J225K	TDK[2]		
	GRM21BR60J225KA01L	Murata[1]		
C4, C6, C12	06035C102KAT	AVX[3]	1nF, 50V, ceramic capacitor, X7R, 0603	3
	C1608X7R1H102K	TDK[2]		
	GRM188R71H102KA01D	Murata[1]		
C7	06035A390JAT2A	AVX[3]	39pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK[2]		
	GRM1885C1H390JA01D	Murata[1]		
C8	06035A391JAT2A	AVX[3]	390pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H391J	TDK[2]		
	GRM188R71H391KA01D	Murata[1]		
C9	06035A101JAT2A	AVX[3]	100pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H101J	TDK[2]		
	GRM1885C1H101JA01D	Murata[1]		
C10, C11	12066D476MAT2A	AVX[3]	47µF, 6.3V, ceramic capacitor, X5R,1206	2
	C3216X5R0J476M	TDK[2]		
	GRM31CR60J476ME19L	Murata[1]		
C14	12106D107MAT2A	AVX[3]	100µF, 6.3V, ceramic capacitor, X5R, 1210	1
	C3225X5R0J107M	TDK[2]		
	GRM32ER60J107ME20L	Murata[1]		
C15, C20, C24	06036D106MAT	AVX[3]	10µF, 6.3V, ceramic capacitor, X5R, 0603	3
	FP3-1R0-R	TDK[2]		
	GRM188R60J106ME47D	Murata[1]		
C16, C18, C21, C23	06036D105KAT2A	AVX[3]	1µF, 6.3V, ceramic capacitor, X5R, 0603	4
	C1608X5R0J105K	TDK[2]		
	GRM188R60J105KA01D	Murata[1]		
C17	06036D475KAT2A	AVX[3]	4.7µF, 6.3V, ceramic capacitor, X5R, 0603	1
	C1608X5R0J475M	TDK[2]		
	C1608X5R0J475M	Murata[1]		

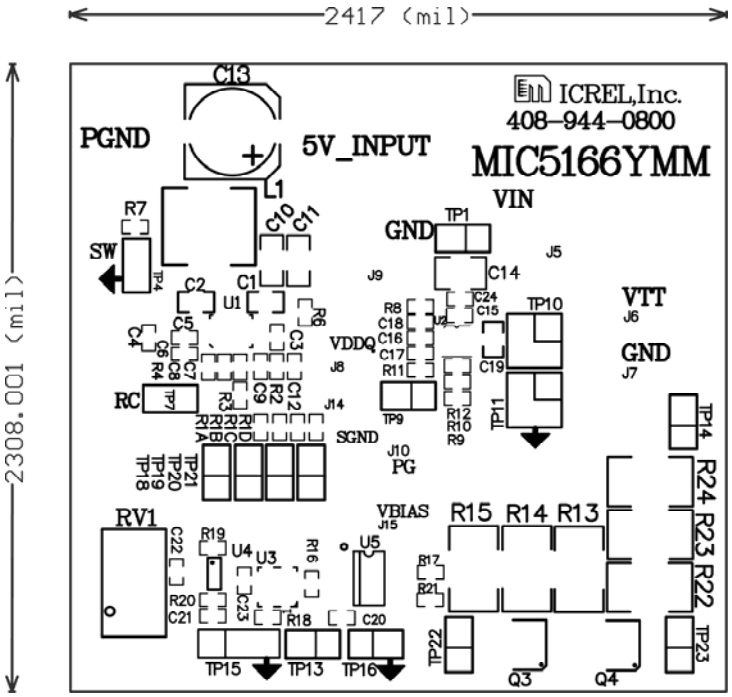
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
C5			N.U. 0603 ceramic capacitor	1
C22	06035C104KAT2A	AVX[3]	0.1µF, 50V, ceramic capacitor, X7R, 0603	1
	C1608X7R1H104K	TDK[2]		
	GRM188R71H104KA93D	Murata[1]		
C13	EEU-FC1A471	Panasonic[4]	470µF/10V, Elect., 20%, 8x11.5, Radial	1
L1	FP3-1R0-R	Cooper[5]	1µH,6.26A Inductor	1
Q3, Q4	NDS8425	Fairchild[7]	MOSFET, N-CH 20V 7.4A 8-SOIC	2
R1A	CRCW0603300RFKEA	Vishay Dale[6]	300Ω, resistor, 1%, 0603	1
R1B	CRCW06031101FKEA	Vishay Dale[6]	510Ω, resistor, 1%, 0603	
R1C	CRCW0603806RFKEA	Vishay Dale[6]	806Ω, resistor, 1%, 0603	
R1D	CRCW06031K10FKEA	Vishay Dale[6]	1.1K, resistor, 1%, 0603	
R2	CRCW0603698RFKEA	Vishay Dale[6]	698Ω, resistor, 1%, 0603	1
R3	CRCW06032002FKEA	Vishay Dale[6]	20K, resistor, 1%, 0603	1
R4	CRCW06034752FKEA	Vishay Dale[6]	47.5K, resistor, 1%, 0603	1
R6, R8, R11, R17, R21	CRCW06032R20RFKEA	Vishay Dale[6]	2.2Ω, resistor, 1%, 0603	5
R7	CRCW060349R9RFKEA	Vishay Dale[6]	49.9Ω, resistor, 1%, 0603	1
R9	CRCW06031002FKEA	Vishay Dale[6]	10K, resistor, 1%, 0603	1
R10, R19	CRCW06031K00FKEA	Vishay Dale[6]	1K, resistor, 1%, 0603	2
R12	CRCW0603000RFKEA	Vishay Dale[6]	0Ω, resistor, 1%, 0603	1
R13, R14, R24	CRCW25121R00FKEGHP	Vishay Dale[6]	1Ω, resistor, 1.5W, 1%, 2512	3
R15	CRCW25122R00JNEG	Vishay Dale[6]	2Ω, resistor, 1.5W, 1%, 2512	1
R16, R18, R20	CRCW06031003FKEA	Vishay Dale[6]	100K, resistor, 1%, 0603	3
R22, R23	LR2512-R50FW	Vishay Dale[6]	0.5Ω, resistor, 1.5W, 1%, 2512	2
RV1	PV36W103C01B00	Murata[1]	Pot, 10KΩ, 0.5W, 9.6x5xx10	1
U1	**MIC22405YML**	**Micrel[9]**	**4A, Synchronous Buck Regulator**	**1**
U2	**MIC5166YMM**	**Micrel[9]**	**3A High-Speed Low V_{IN} DDR Terminator**	**1**
U3	SN74AHCT00RGYR	TI[8]	Quad, 2IN Pos-NAND Gate, 14-pin, QFN	1
U4	**MIC1557YM5**	**Micrel[9]**	**5MHz RC Timer Oscillator**	**1**
U5	**MIC4425**	**Micrel[9]**	**3A Dual Inverting and Non-Inverting MOSFET Driver**	**1**

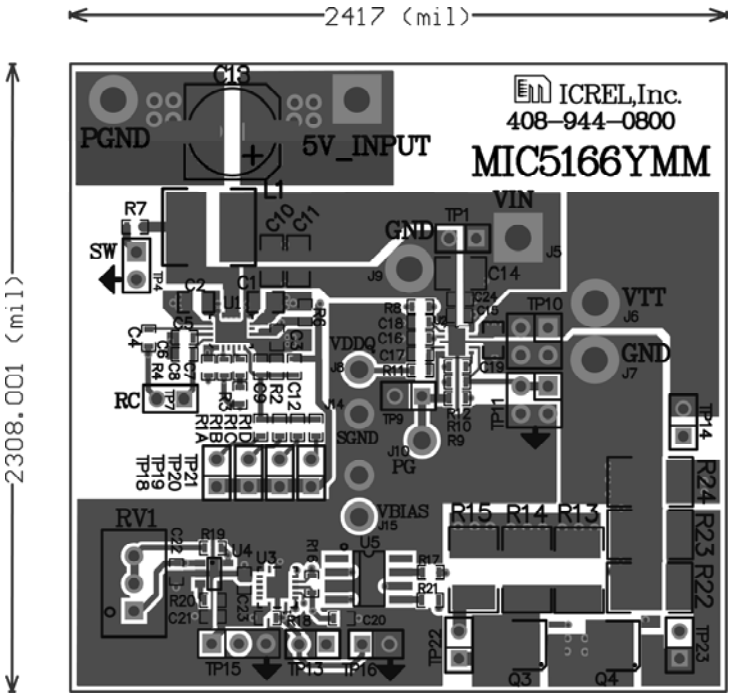
Notes:

1. Murata Tel: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com.
4. Panasonic: www.panasonic.com.
5. Cooper: www.cooper.com
6. Vishay Dale: www.vishay.com.
7. Fairchild: www.fairchildsemi.com.
8. TI: www.ti.com
9. **Micrel, Inc.:** www.micrel.com.

PCB Layout Recommendations

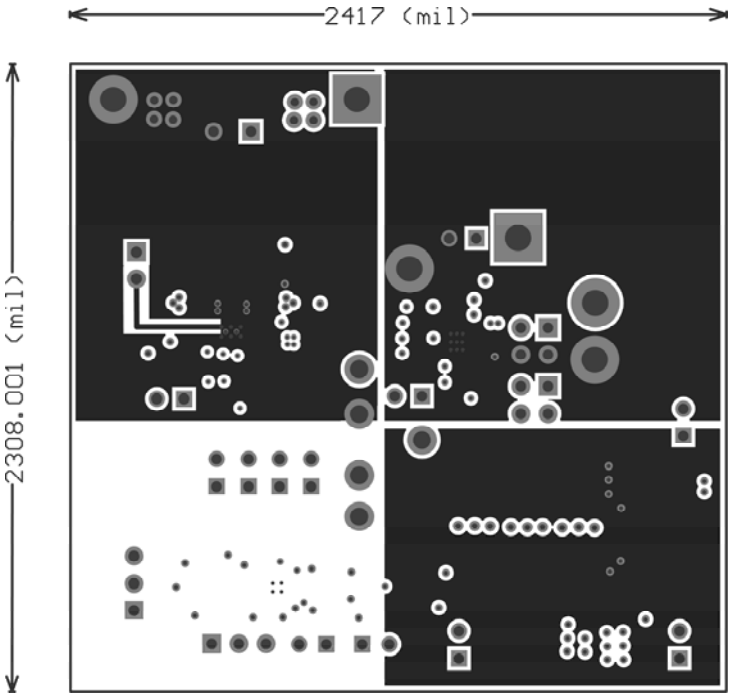


Top Silk

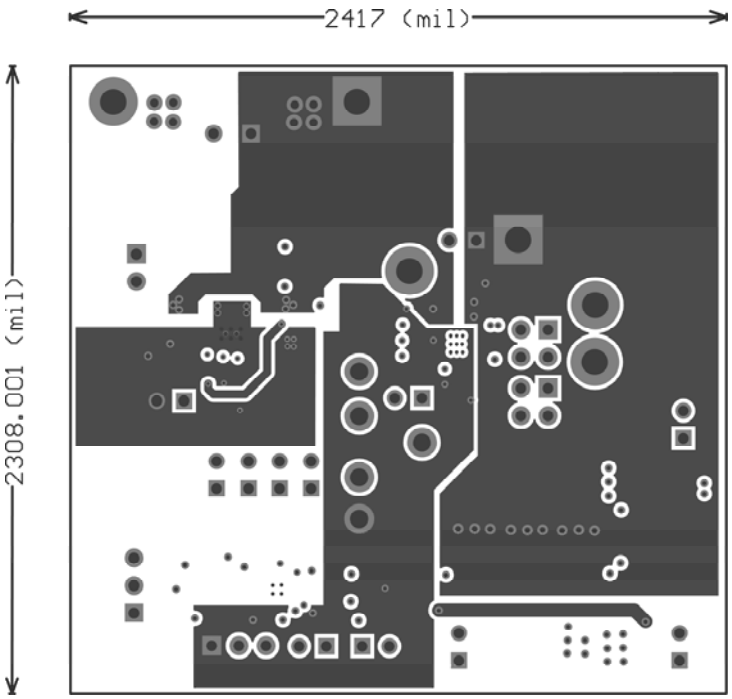


Copper Layer 1

PCB Layout Recommendations (Continued)

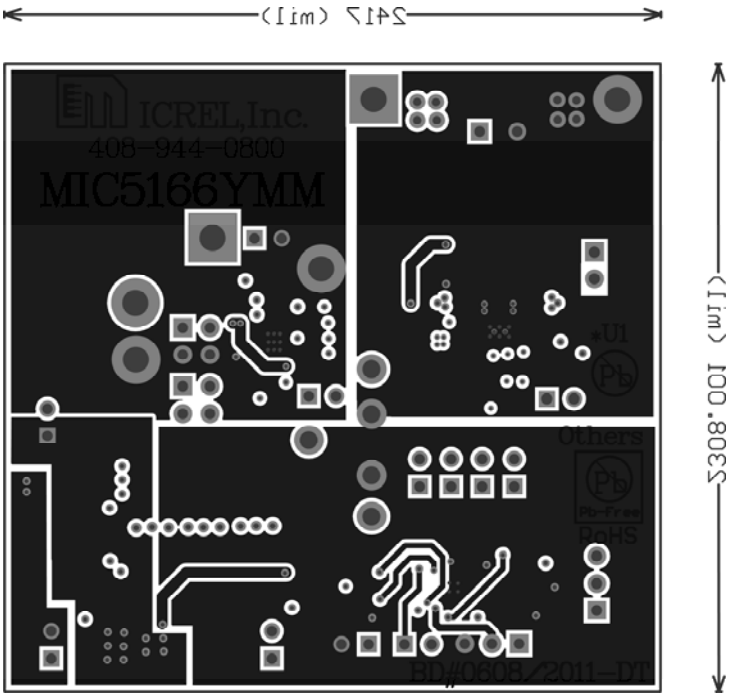


Copper Layer 2

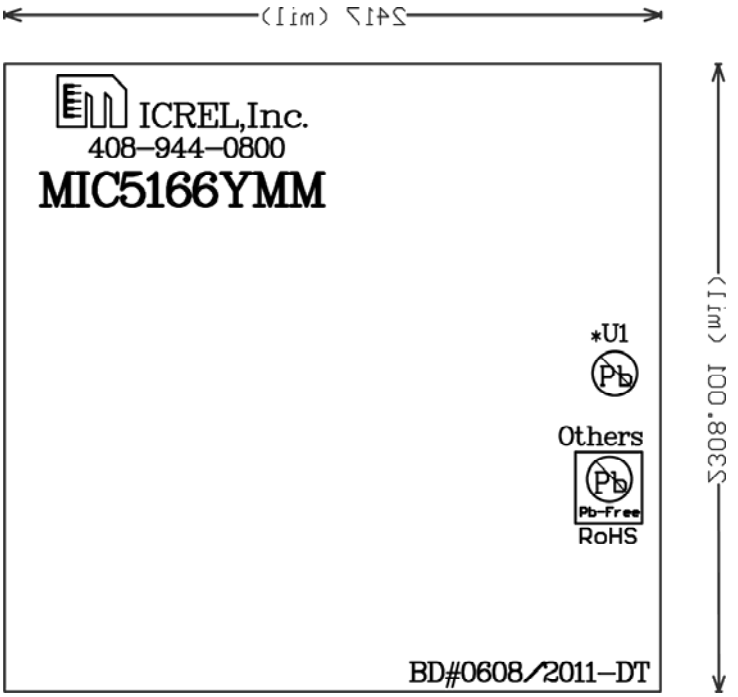


Copper Layer 3

PCB Layout Recommendations (Continued)

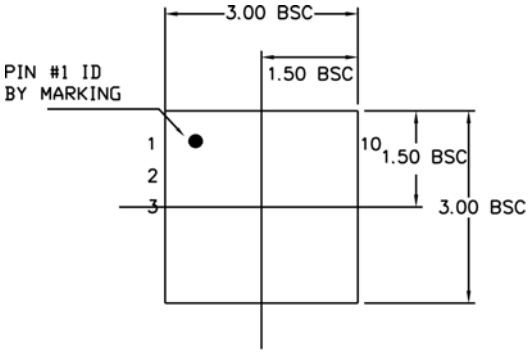


Copper Layer 4

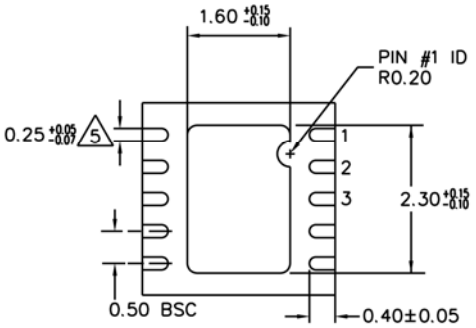


Bottom Silk

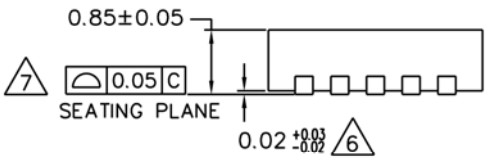
Package Information



TOP VIEW



BOTTOM VIEW



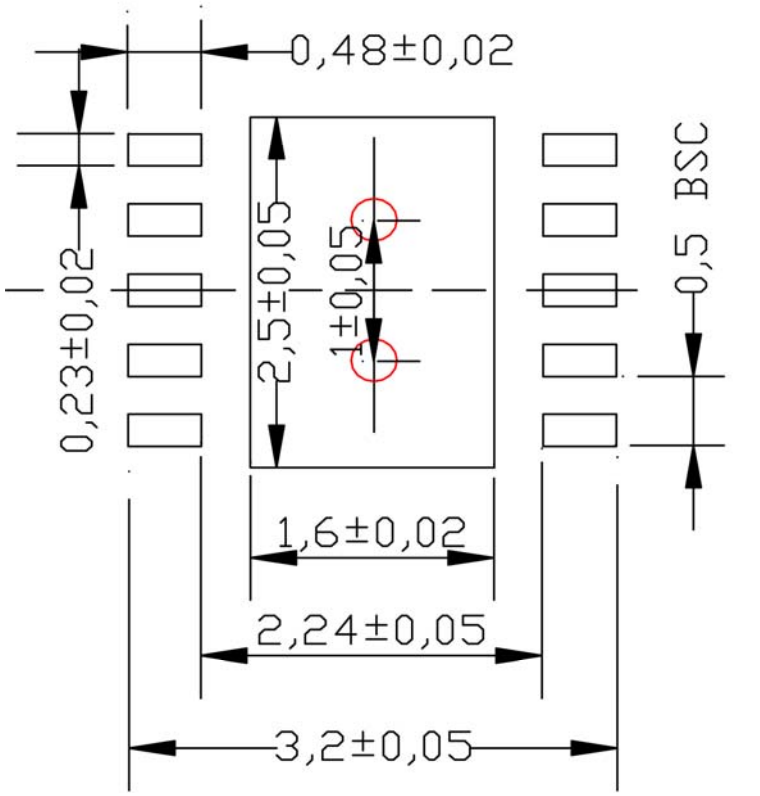
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

10-Pin 3mm × 3mm MLF® (ML)

Recommended Landing Pattern

LP # MLF33D-10LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



Red circle indicates Thermal Via. Size should be .300mm – .350mm in diameter and it should be connected to GND plane for maximum thermal performance.

10-Pin 3mm × 3mm MLF® Land Pattern

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com