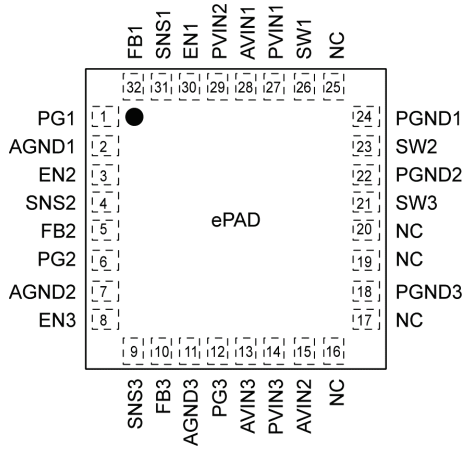
Ordering Information

Part Number	Marking	Nominal Output Voltage	Junction Temperature Range[1]	Package[2, 3]	Lead Finish
MIC23450-AAAYML	AAA	ADJ/ADJ/ADJ	–40C to +125°C	32-Pin 5mm × 5mm QFN	Pb-Free

Notes:

1. Other options available. Contact Micrel for details.
2. QFN is a Green, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.
3. QFN • = Pin 1 identifier.

Pin Configuration



32-Pin 5mm × 5mm QFN (ML) – Adjustable
Top View

Pin Description

Pin Number	Pin Name	Pin Function
26, 23, 21	SW1, 2, 3	Switch (Output). Internal power MOSFET output switches for Output 1/2/3.
30, 3, 8	EN1, 2, 3	Enable (Input). Logic high enables operation of regulator 1/2/3. Logic low will shut down the device. Do not leave floating.
31, 4, 9	SNS1, 2, 3	Sense. Connect to $V_{OUT1,2,3}$ as close to output capacitor as possible to sense output voltage.
32, 5, 10	FB1, 2, 3	Feedback. Connect a resistor Divider from output 1/2/3 to ground to set the output voltage.
1, 6, 12	PG1, 2, 3	Power Good. Open Drain output for the power good indicator for output 1/2/3. Place a resistor between this pin and a voltage source to detect a power good condition.
2, 7, 11	AGND1, 2, 3	Analog Ground. Connect to quiet ground point away from high-current paths, e.g., C_{OUT} for best operation. Must be connected externally to PGND.
27, 29, 14	PVIN1, 2, 3	Power Input Voltage. Connect a capacitor to PGND to localize loop currents and decouple switching noise.
28, 15, 13	AVIN1, 2, 3	Analog Input Voltage. Connect a capacitor to AGND to decouple noise.
24, 22, 18	PGND1, 2, 3	Power Ground.
16, 17, 19, 20, 25	NC	No Connect.
ePAD	ePad	Connect to ground plane to ensure good thermal properties.

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Absolute Maximum Ratings[1]

Supply Voltage (PV_{IN}, AV_{IN}) ..... –0.3 to 6V
Sense (V_{SNS1}, V_{SNS2}, V_{SNS3}) ..... –0.3 to 6V
Power Good (PG1, PG2, PG3) ..... –0.3 to 6V
Output Switch Voltage (V_{SW1}, V_{SW2}, V_{SW3}) ..... –0.3V to 6V
Enable Input Voltage (V_{EN1}, V_{EN2}, V_{EN3}) ..... –0.3V to V_{IN}
Storage Temperature Range ..... –65°C to +150°C
ESD Rating[3] ..... ESD Sensitive

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.7V to +5.5V
Enable Input Voltage (V_{EN1}, V_{EN2}, V_{EN3}) ..... 0V to V_{IN}
Output Voltage Range (V_{SNS1}, V_{SNS2}, V_{SNS3}) ... +1V to +3.3V
Junction Voltage Range (T_J) ..... –40°C ≤ T_J ≤ +125°C
Thermal Resistance
32-Pin 5mm × 5mm QFN (θ_{JA}) ..... +30°C/W
32-Pin 5mm × 5mm QFN (θ_{JC}) ..... +10°C/W

Electrical Characteristics[4]

T_A = +25°C; V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6V; L1 = L2 = L3 = 1µH; C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7µF, unless otherwise specified.
Bold values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		**2.7**		**5.5**	V
Undervoltage Lockout Threshold	Turn-On	**2.45**	2.55	**2.65**	V
Undervoltage Lockout Hysteresis			75		mV
Quiescent Current	I_{OUT} = 0mA, SNS > 1.2 × V_{OUTNOM}		69	**120**	µA
Per Channel Shutdown Current	V_{EN1}, V_{EN2}, V_{EN3} = 0V; V_{IN} = 5.5V		0.01	**5**	µA
Output Voltage Accuracy	V_{IN} = 3.6V if $V_{OUT(NOM)}$ < 2.5V, I_{LOAD} = 20mA	**–2.5**		**+2.5**	%
	V_{IN} = 4.5V if $V_{OUT(NOM)}$ ≥ 2.5V, I_{LOAD} = 20mA				
Feedback Voltage (V_{FB1}, V_{FB2}, V_{FB3})		**.604**	0.62	**.635**	V
Peak Current Limit	I_{OUT1}, I_{OUT2}, I_{OUT3} SNS1, SNS2, SNS3 = 0.9 × V_{OUTNOM}	**2**	4.5		A
Foldback Current Limit			1.8		A
Output Voltage Line Regulation (V_{OUT1}, V_{OUT2}, V_{OUT3})	V_{IN} = 3.6V to 5.5V if $V_{OUTNOM1, 2, 3}$ < 2.5V, I_{LOAD} = 20mA		0.3		%/V
	V_{IN} = 4.5V to 5.5V if $V_{OUTNOM1, 2, 3}$ ≥ 2.5V, I_{LOAD} = 20mA				
Output Voltage Load Regulation (V_{OUT1}, V_{OUT2}, V_{OUT3})	DCM: 20mA < I_{LOAD} < 130mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V		0.2		%
	DCM: 20mA < I_{LOAD} < 130mA, V_{IN} = 5.0V if V_{OUTNOM} > 2.5V		0.4		
	CCM: 200mA < I_{LOAD} < 500mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V		0.6		
	CCM: 200mA < I_{LOAD} < 1A, V_{IN} = 5.0V if V_{OUTNOM} > 2.5V		0.3		
PWM Switch ON-Resistance (R_{SW1}, R_{SW2}, R_{SW3})	I_{SW1}, I_{SW2}, I_{SW3} = +100mA (PMOS)		0.2		Ω
	I_{SW1}, I_{SW2}, I_{SW3} = –100mA (NMOS)				

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

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Electrical Characteristics[4] (Continued)

T_A = +25°C; V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6V; L1 = L2 = L3 = 1µH; C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7µF, unless otherwise specified.
Bold values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Maximum Frequency	I_{OUT1}, I_{OUT2}, I_{OUT3} = 120mA		3		MHz
Soft-Start Time	V_{OUT1}, V_{OUT2}, V_{OUT3} = 90%		115		µs
Power Good Threshold	% of V_{NOM}	83	90	96	%
Power Good Hysteresis			10		%
Power Good Pull Down	V_{SNS} = 90% V_{NOM}, I_{PG} = 1mA			200	mV
Enable Threshold	Turn-On	**0.5**	0.8	**1.2**	V
Enable Input Current			0.1	**1**	µA
Overtemperature Shutdown			160		°C
Overtemperature Shutdown Hysteresis			20		°C

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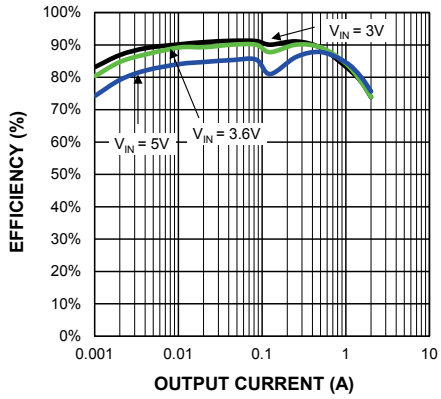
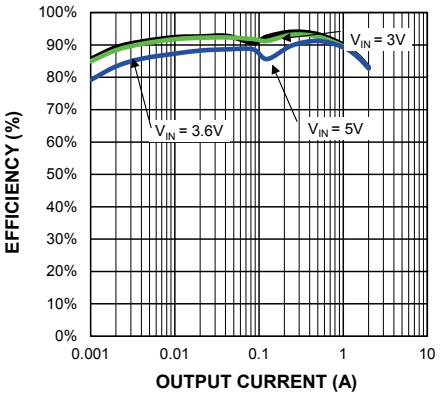
Typical Characteristics

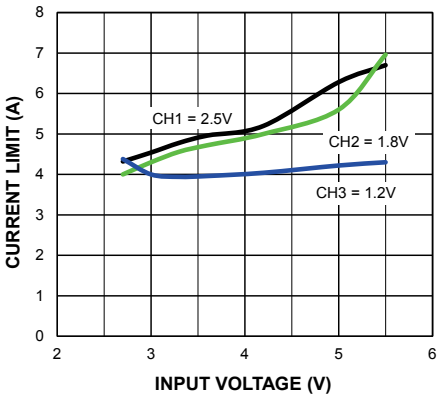
Efficiency vs. Output Current
V_{OUT} = 1.8V



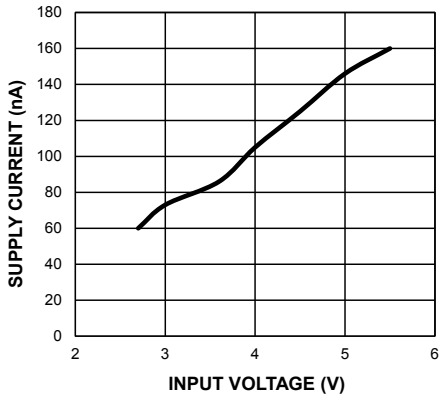
Efficiency vs. Output Current
V_{OUT} = 2.5V



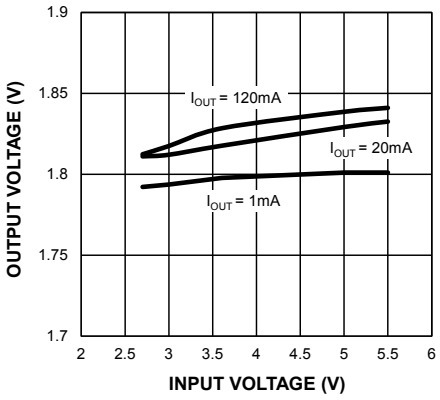
Current Limit
vs. Input Voltage



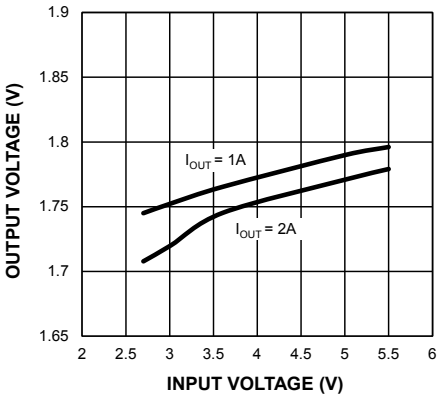
Shutdown Current
vs. Input Voltage



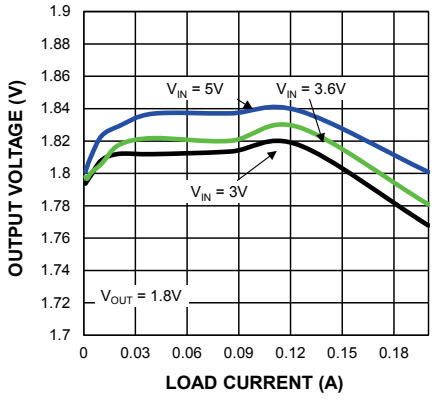
Line Regulation
(Low Loads)



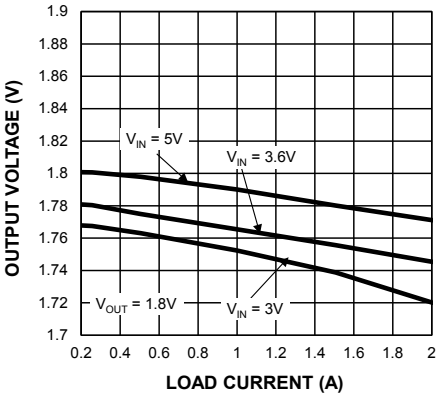
Line Regulation
(High Loads)



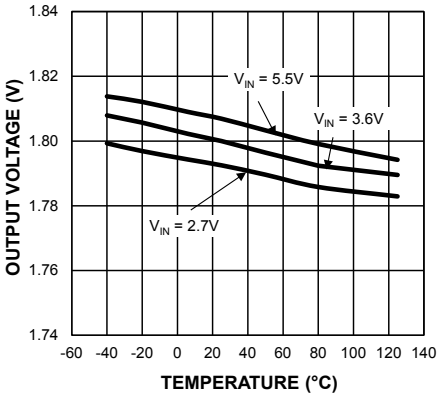
Output Voltage
vs. Output Current (HLL)



Output Voltage
vs. Output Current (CCM)



Output Voltage
vs. Temperature



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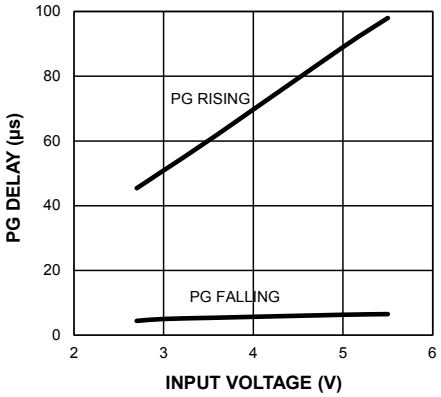
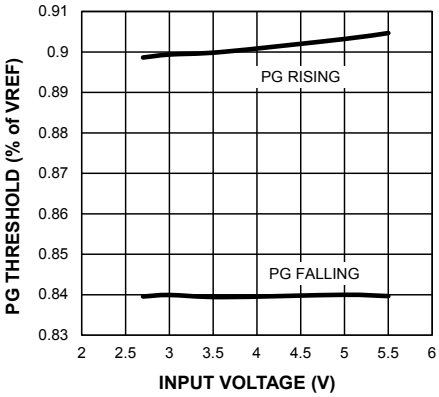
Typical Characteristics (Continued)

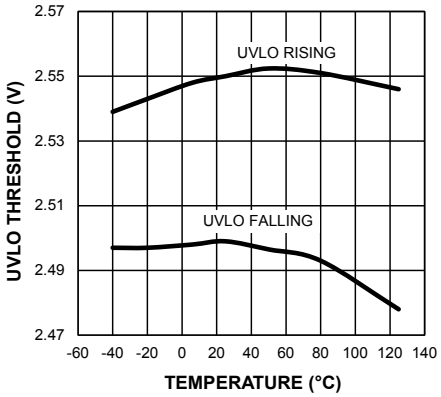
PG Delay Time vs. Input Voltage



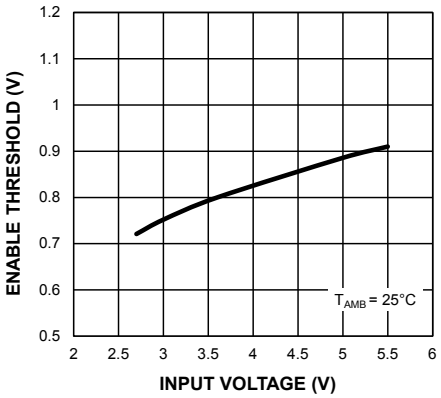
PG Thresholds vs. Input Voltage



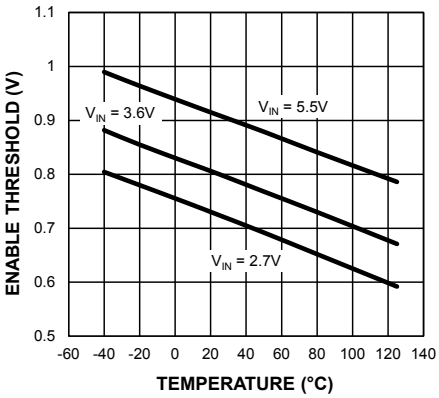
UVLO Threshold vs. Temperature



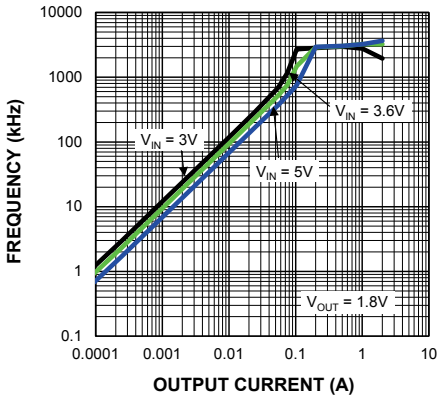
Enable Threshold vs. Input Voltage



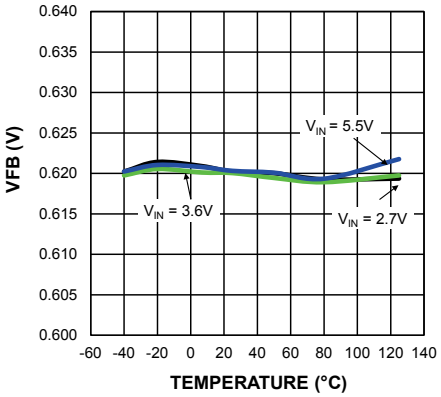
Enable Threshold vs. Temperature



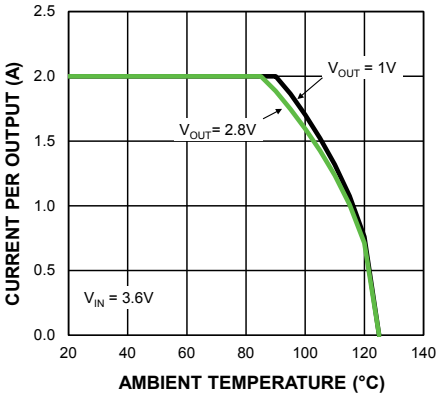
Switching Frequency vs. Load Current



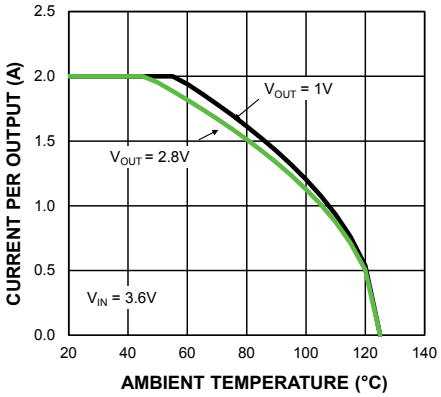
VFB vs. Temperature



Maximum Output Current per O/P vs. Temperature (1 O/P)



Maximum Output Current per O/P vs. Temperature (2 O/Ps)



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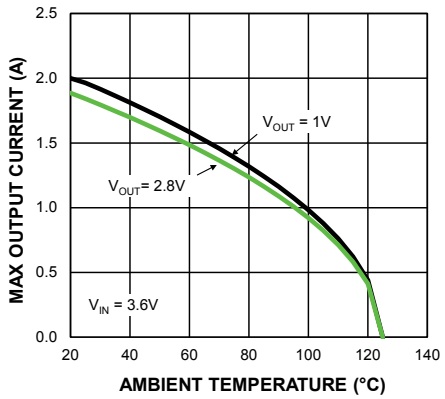
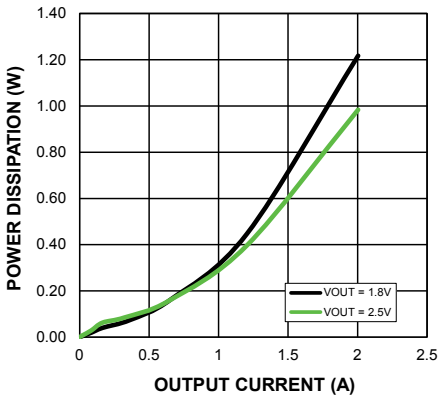
Typical Characteristics (Continued)

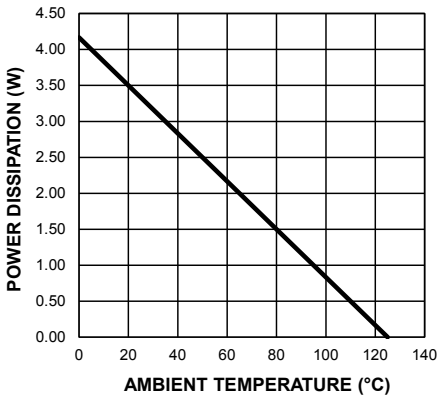
Maximum Output Current per O/P vs. Temperature (3 O/Ps)



Power Dissipation vs. Load Current (per Channel)



Maximum Package Dissipation vs. Ambient Temperature



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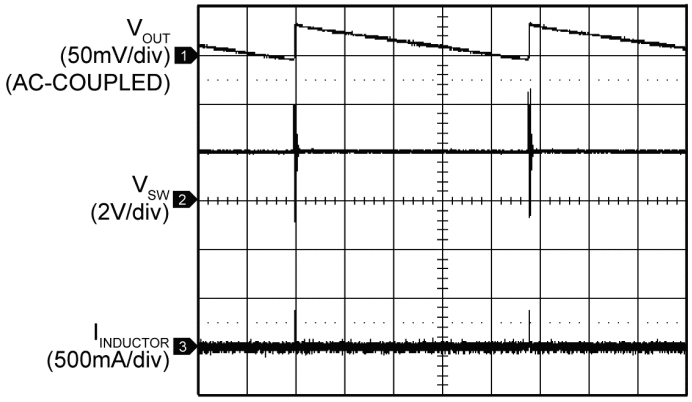
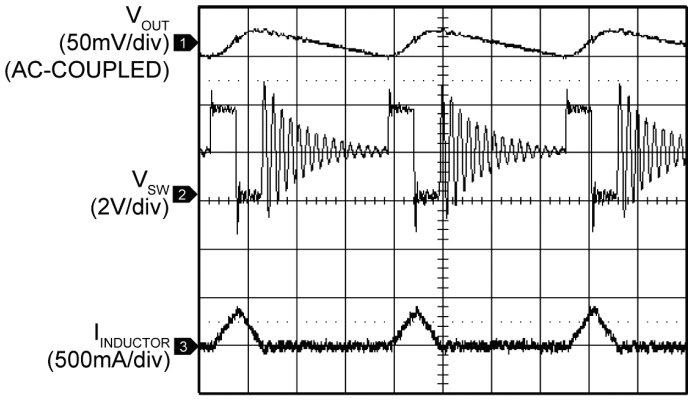
Functional Characteristics

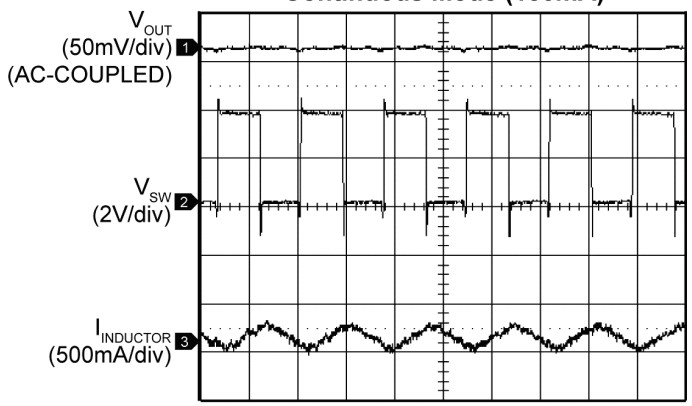
Switching Waveform
Discontinuous Mode (1mA)



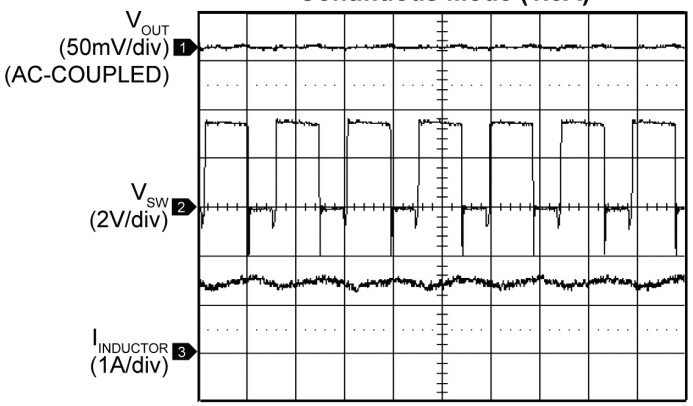
Switching Waveform
Discontinuous Mode (50mA)



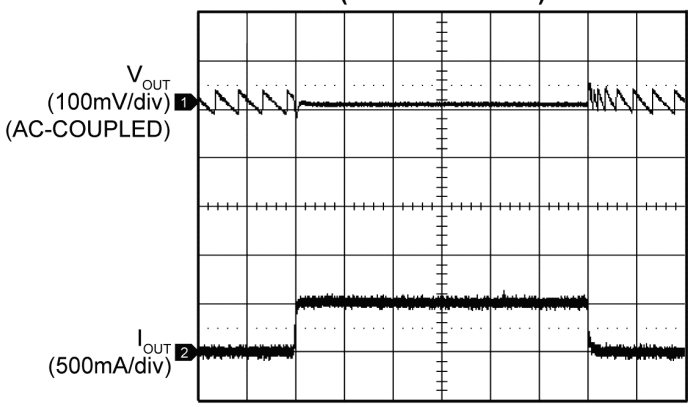
Switching Waveform
Continuous Mode (150mA)



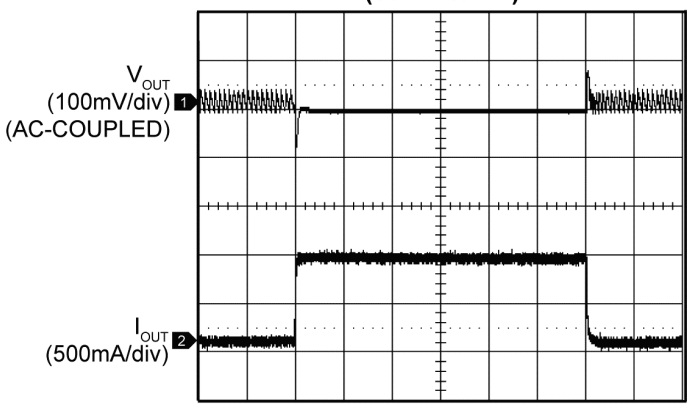
Switching Waveform
Continuous Mode (1.5A)



Load Transient
(10mA to 500mA)



Load Transient
(50mA to 1A)



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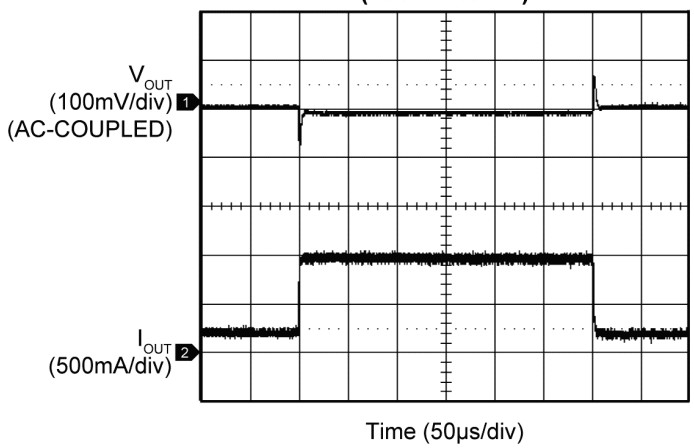
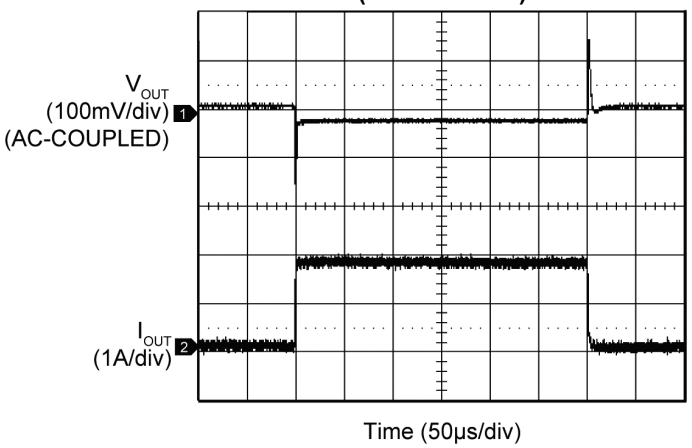
Functional Characteristics (Continued)

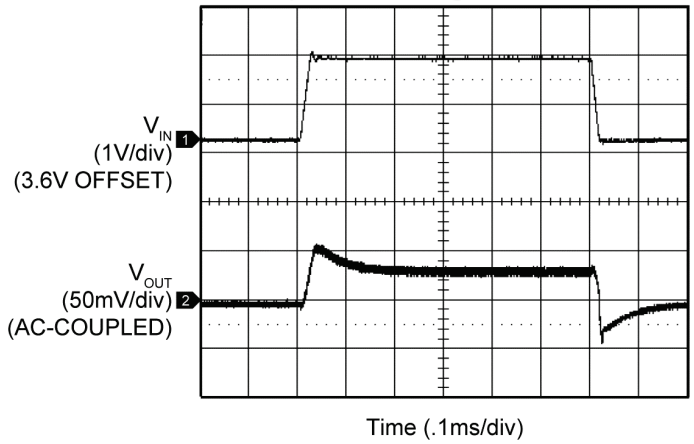
Load Transient (200mA to 1A)



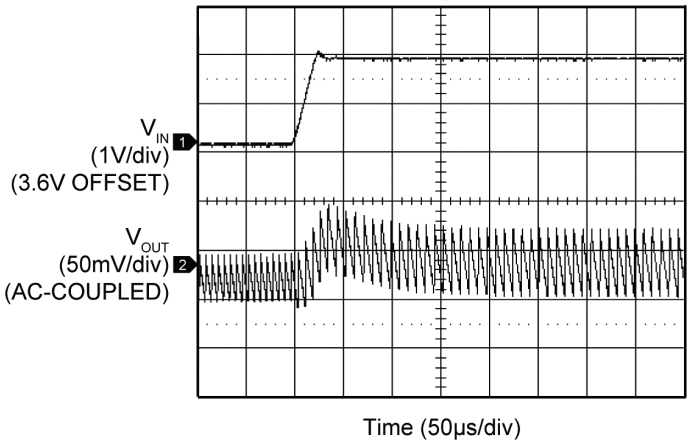
Load Transient (200mA to 2A)



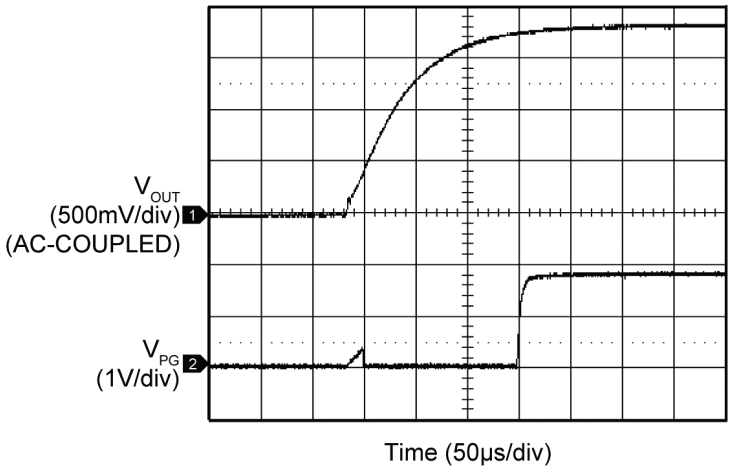
Line Transient (3.6V to 5.5V @ 1.5A Load)



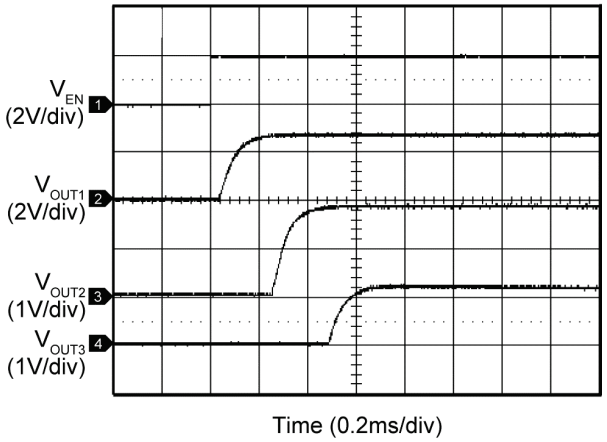
Line Transient (3.6V to 5.5V @ 20mA Load)



Start-Up and PG Waveform



Start-Up and PG Waveform – Sequenced (EN = EN1, PG1 = EN2, PG2 = EN3)



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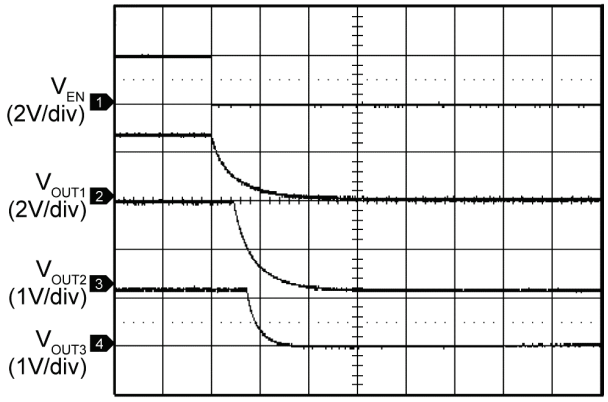
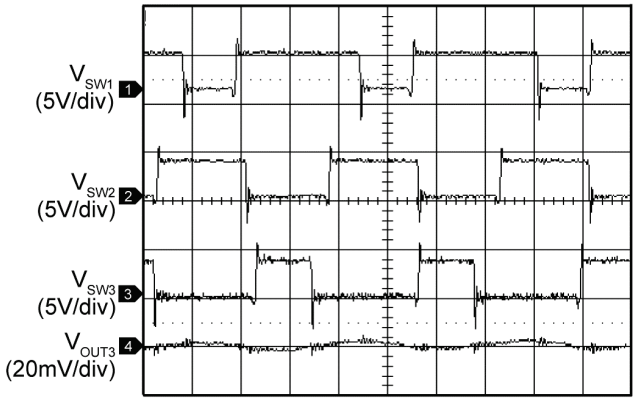
Functional Characteristics (Continued)

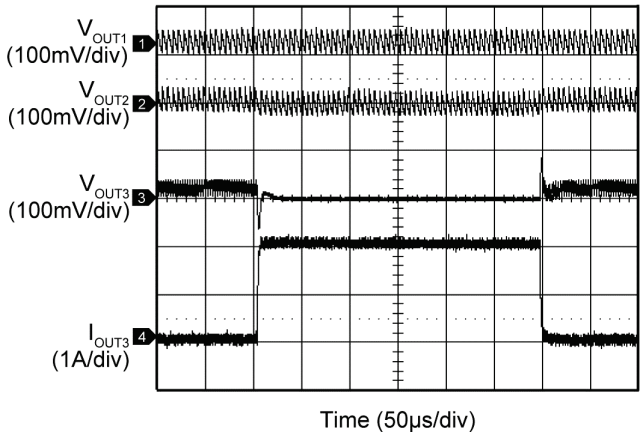
Shut-Down and PG Waveform – Sequenced
(EN = EN1, PG1 = EN2, PG2 = EN3)



Switching Waveform
(All Channels in Continuous Mode)



Transient Cross Regulation
(I_{OUT3} = 50mA to 2A, I_{OUT1}, I_{OUT2} = 20mA)



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Functional Diagram

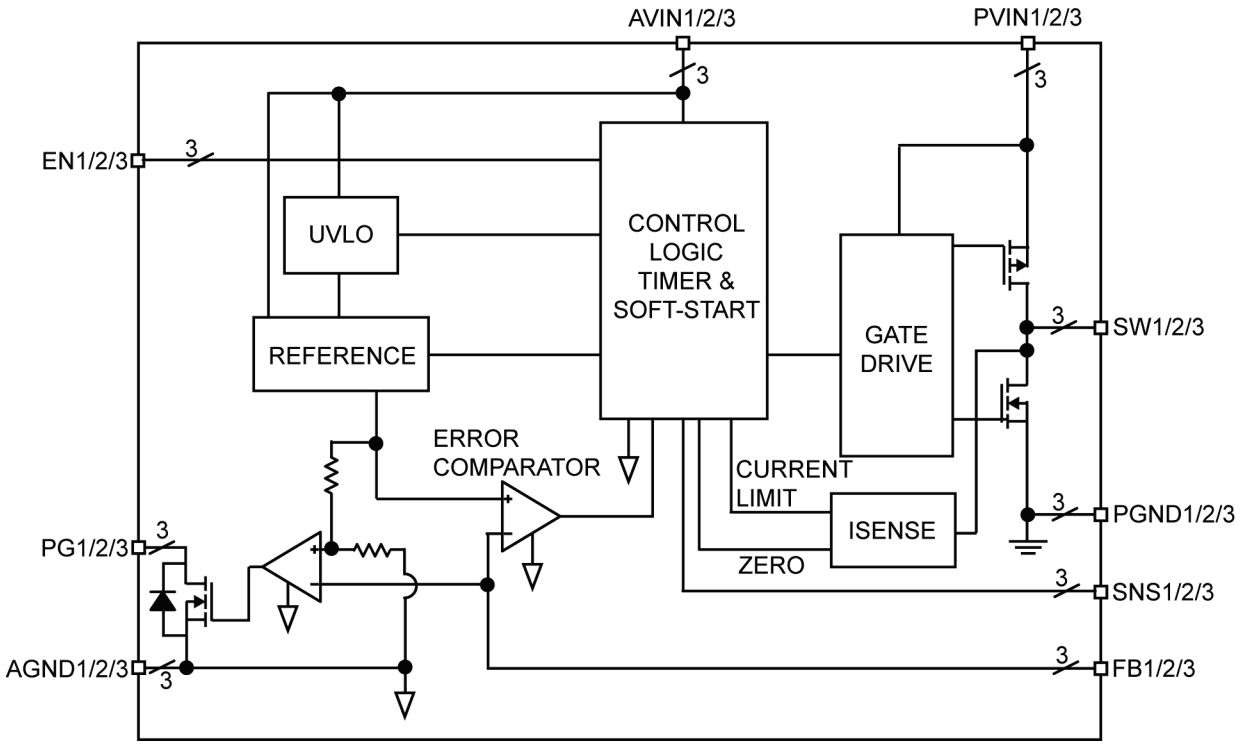

Figure 1. Simplified MIC23450 Adjustable Functional Block Diagram

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Functional Description

PVIN

The input supply (PVIN) provides power to the internal MOSFETs for the switch mode regulator. The VIN operating range is 2.7V to 5.5V so an input capacitor, with a minimum voltage rating of 6.3V, is recommended. Due to the high di/dt switching speeds, a minimum 2.2µF or 4.7µF recommended bypass capacitor placed close to PVIN and the power ground (PGND) pin is required. Refer to the layout recommendations for details.

AVIN

The input supply (AVIN) provides power to the internal control circuitry. As the high di/dt switching speeds on PVIN cause small voltage spikes, an RC filter comprising 50Ω and a minimum 100nF decoupling capacitor placed close to the AVIN and signal ground (AGND) pin is required.

EN

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.01µA. MIC23450 features internal soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. Do not leave the EN pin floating.

SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to the layout recommendations for more details.

AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the layout recommendations for more details.

PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as short and wide as possible and separate from the analog ground (AGND) loop as applicable. Refer to the layout recommendations for more details.

PG

The power good (PG) pin is an open drain output which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5kΩ should be connected from PG to V_{OUT}.

FB

The feedback (FB) pin is the control input for programming the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.62V reference within the regulation loop.

The output voltage can be programmed between 1V and 3.3V using Equation 1:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 1}$$

Where: R1 is the top, V_{OUT} connected resistor, R2 is the bottom, AGND connected resistor.

Table 1 illustrates example feedback resistor values.

V_{OUT}	R1	R2
1.2V	274k	294k
1.5V	316k	221k
1.8V	301k	158k
2.5V	324k	107k
3.3V	309k	71.5k

Table 1. Feedback Resistor Values

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Application Information

The MIC23450 is a triple high performance DC-to-DC step down regulator offering a small solution size. Supporting 3 outputs with currents up to 2A inside a 5mm x 5mm QFN package, the IC requires only five external components per channel while meeting today's miniature portable electronic device needs. Using the HyperLight Load® switching scheme, the MIC23450 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

Input Capacitor

A 2.2µF ceramic capacitor or greater should be placed close to the PVIN pin for each channel and it's corresponding PGND pin for bypassing. For example, Murata GRM188R60J475ME19D, size 0603, 4.7µF ceramic capacitor is ideal, based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The MIC23450 is designed for use with a 2.2µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the Murata GRM188R60J475ME84D, size 0603, 4.7µF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23450 is designed for use with a 0.47µH to 2.2µH inductor. For faster transient response, a 0.47µH inductor will yield the best result. On the other hand, a 2.2µH inductor will yield lower output voltage ripple. For the best compromise of these, generally, a 1µH is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as shown in Equation 2:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \qquad \text{Eq. 2}$$

As shown in Equation 2, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

The transition between high loads (CCM) to HyperLight Load (HLL) mode is determined by the inductor ripple current and the load current as illustrated in Figure 2.

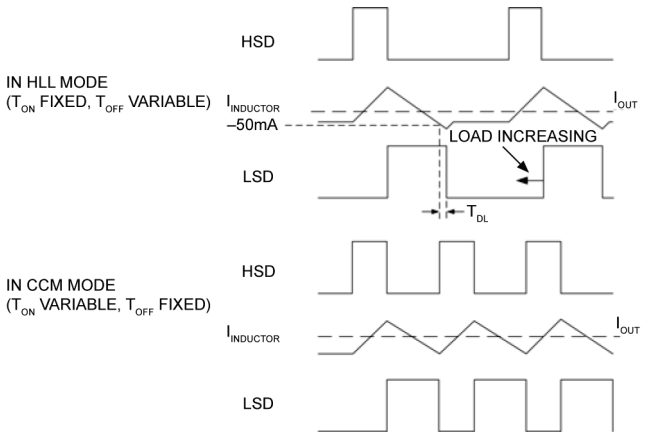

Figure 2. Transition between CCM Mode and HLL Mode

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The diagram shows the signals for high side switch drive (HSD) for T_{ON} control, the Inductor current and the low side switch drive (LSD) for T_{OFF} control.

In HLL mode, the inductor is charged with a fixed T_{ON} pulse on the high side switch (HSD). After this, the LSD is switched on and current falls at a rate V_{OUT}/L. The controller remains in HLL mode while the inductor falling current is detected to cross approximately -50mA. When the LSD (or T_{OFF}) time reaches its minimum and the inductor falling current is no longer able to reach this -50mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Once in CCM mode, the T_{OFF} time will not vary. Therefore, it is important to note that if L is large enough, the HLL transition level will not be triggered.

That inductor is:

$$L_{MAX} = \frac{V_{OUT} \times 135ns}{2 \times 50mA} \qquad \text{Eq. 3}$$

Compensation

The MIC23450 is designed to be stable with a 0.47µH to 2.2µH inductor with a 4.7µF ceramic (X5R) output capacitor.

Duty Cycle

The typical maximum duty cycle of the MIC23450 is 80%.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency } \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100 \qquad \text{Eq. 4}$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET R_{DSON} multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 4MHz frequency and the switching transitions make up the switching losses.

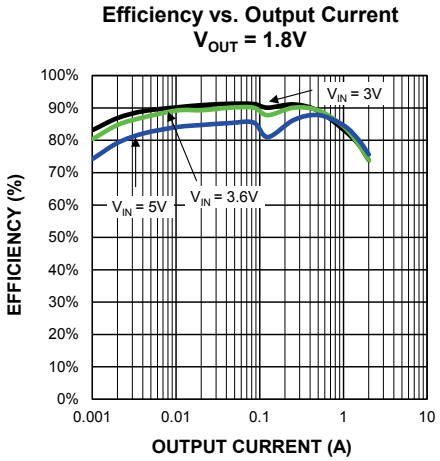

Figure 3. Efficiency under Load

The figure above shows an efficiency curve. From no load to 100mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23450 is able to maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$P_{DCR} = I_{OUT}^2 \text{ x DCR} \qquad \text{Eq. 5}$$

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From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{DCR}}\right)\right] \times 100$$

Eq. 6

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Thermal Considerations

As most applications will not require 2A continuous current from all outputs at all times, it is useful to know what the thermal limits will be for various loading profiles.

The allowable overall package dissipation is limited by the intrinsic thermal resistance of the package ($R\theta_{(J-C)}$) and the area of copper used to spread heat from the package case to the ambient surrounding temperature ($R\theta_{(C-A)}$). The composite of these two thermal resistances is $R\theta_{(J-A)}$, which represents the package thermal resistance with at least 1 square inch of copper ground plane. From this figure, which for the MIC23450 is 30°C/W, we can calculate maximum internal power dissipation as shown in Equation 7:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMB}}{R\theta_{(J-A)}}$$

Eq. 7

where:

T_{JMAX} = Maximum junction temp (125°C)

T_{AMB} = Ambient temperature

$R\theta_{(J-A)}$ = 30°C/W

As can be expected, the allowable dissipation tends towards zero as the ambient temperature increases towards the maximum operating junction temperature.

The graph of PD_{MAX} vs. Ambient temperature could be drawn quite simply using this equation. However, a more useful measure is the maximum output current per regulator vs. ambient temperature. For this, we must first create an 'exchange rate' between power dissipation per regulator (P_{DISS}) and its output current (I_{OUT}).

An accurate measure of this function can utilize the efficiency curve, as illustrated in Equation 8:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

$$P_{LOSS} = \frac{P_{OUT}(1-\eta)}{\eta}$$

Eq. 8

where:

η = Efficiency

$P_{OUT} = I_{OUT}.V_{OUT}$

To arrive at the internal package dissipation P_{DISS}, one would need to remove the inductor loss P_{DCR} which is not dissipated within the package. This however, does not give a worst case figure, since efficiency is typically measured on a nominal part at nominal temperatures. The I_{OUT} to P_{DISS} function we use therefore is a synthesized P_{DISS} which accounts for worst case values at maximum operating temperature, as shown in Equation 9:

$$P_{DISS} = I_{OUT}^2 \left(R_{DSON_P} \times \frac{V_{OUT}}{V_{IN}} + R_{DSON_N} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right)$$

Eq. 9

where:

R_{DSON_P} = Maximum R_{DSON} of the high side, P-Channel switch at T_{JMAX}

R_{DSON_N} = Maximum R_{DSON} of the low side, N-Channel switch at T_{JMAX}

V_{OUT} = Output Voltage,

V_{IN} = Input Voltage

Since ripple current and switching losses are small with respect to resistive losses at maximum output current, they can be considered negligible for the purpose of this method, but could be included if required.

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Now we have a function describing P_{DISS} in terms of I_{OUT}, we can substitute P_{DISS} with Equation 7 to form the function of maximum output current I_{OUTMAX} vs. ambient temperature T_{AMB} (Equation 10):

$$I_{OUTMAX} = \sqrt{\frac{\frac{T_{JMAX} - T_{AMB}}{R\theta_{(J-A)}}}{R_{DSON_P} \times \frac{V_{OUT}}{V_{IN}} + R_{DSON_N} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}} \quad \text{Eq. 10}$$

The curves shown in the characteristic curves section are plots of this function adjusted to account for 1, 2 or 3 regulators running simultaneously.

HyperLight Load Mode

Each regulator in the MIC23450 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23450 works in pulse-frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23450 during light load currents by only switching when it is needed. As the load current increases, the MIC23450 goes into continuous conduction mode (CCM) and switches at a frequency centered at 3MHz. The equation to calculate the load when the MIC23450 goes into continuous conduction mode may be approximated in Equation 11:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f}\right) \quad \text{Eq. 11}$$

As shown in Equation 11, the load at which the MIC23450 transitions from HyperLight Load mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 4, as the Output Current increases, the switching frequency also increases until the MIC23450 goes from HyperLight Load mode to PWM mode at approximately 120mA. The MIC23450 will switch at a relatively constant frequency around 3MHz once the output current is over 120mA.

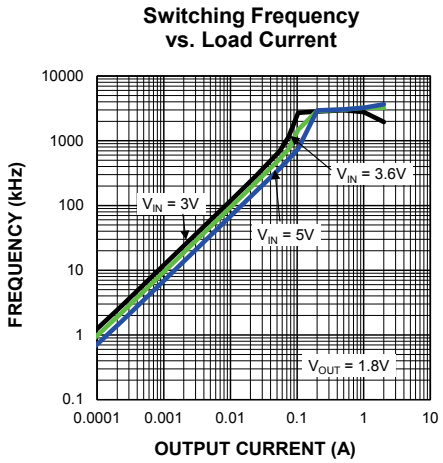

Figure 4. SW Frequency vs. Output Current

Multiple Sources

The MIC23450 provides all the pins necessary to operate the 3 regulators from independent sources. This can be useful in partitioning power within a multi rail system. For example, it is possible that within a system, two supplies are available; 3.3V and 5V. The MIC23450 can be connected to use the 3.3V supply to provide two, low voltage outputs (e.g. 1.2V and 1.8V) and use the 5V rail to provide a higher output (e.g. 2.5V), resulting in the power blocks shown in Figure 5.

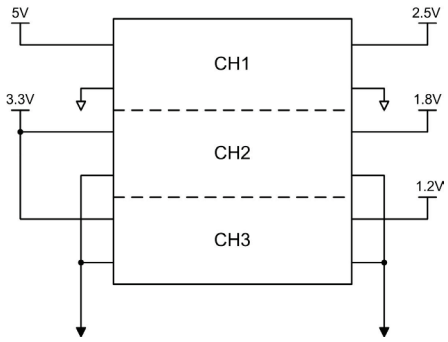

Figure 5. Multi-Source Power Block Diagram

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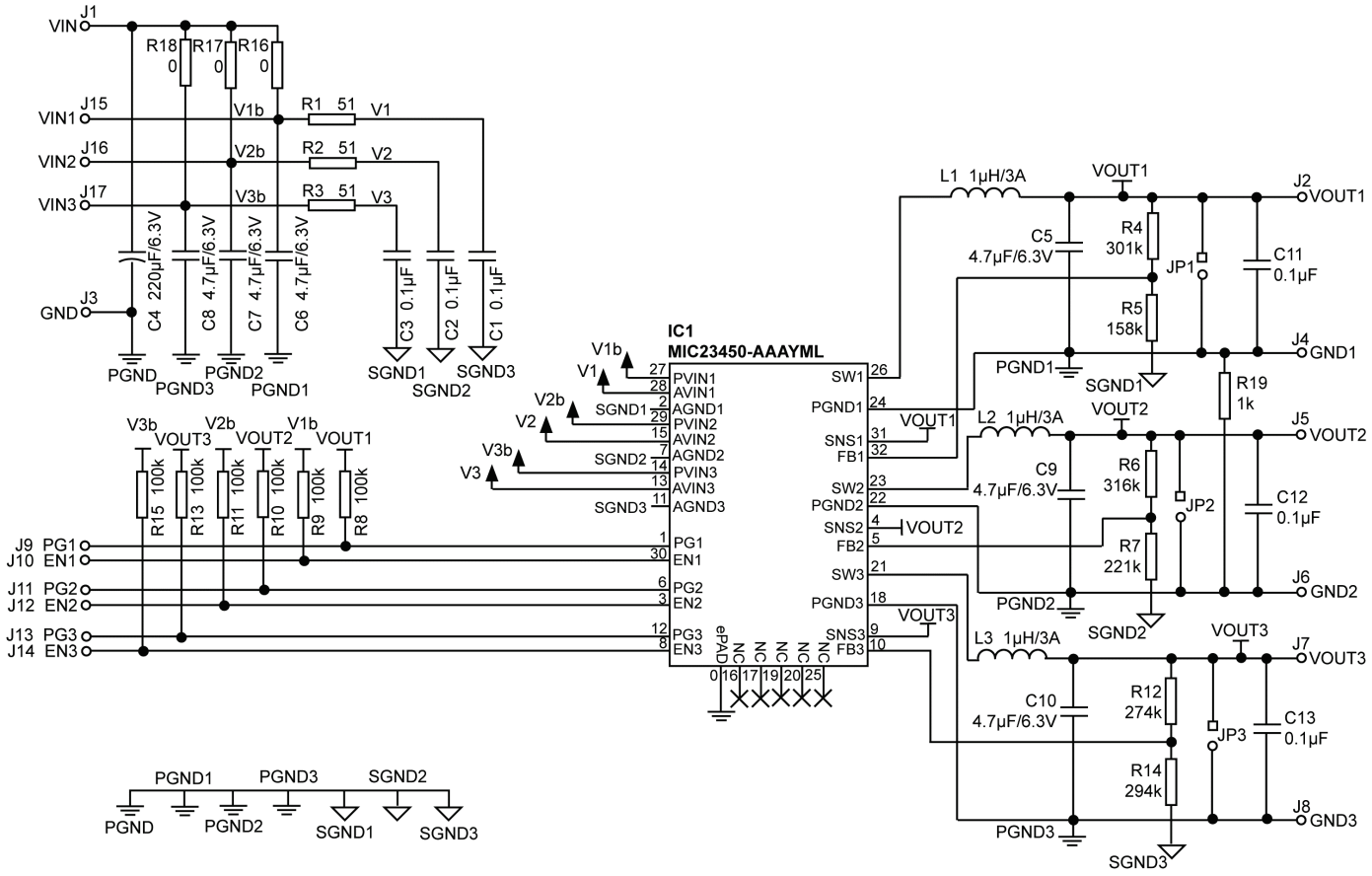
Typical Application Circuit



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C11, C12, C13	C1608X5R1E104K	TDK(1)	Ceramic Capacitor, 0.1µF, 6.3V, X5R, Size 0603	6
	GRM188R60J104KD	Murata(2)		
C4	EEUFR1A221	Panasonic(3)	Electrolytic Capacitor, 220µF, 10V, Size 6.3mm	1
C6, C7, C8, C5, C9, C10	C1608X5R0J475K	TDK	Ceramic Capacitor, 4.7µF, 6.3V, X5R, Size 0603	6
	GRM188R60J475KE19D	Murata		
R1, R2, R3	CRCW040251R0FKEA	Vishay(4)	Resistor, 51Ω, Size 0402	3
R4	CRCW04023013FKEA	Vishay	Resistor, 301kΩ , Size 0402	1

Notes:

1. TDK: www.tdk.com.
2. Murata Tel: www.murata.com.
3. Panasonic: www.panasonic.com.
4. Vishay Tel: www.vishay.com.

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Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R5	CRCW04021583FKEA	Vishay	Resistor, 158kΩ, Size 0402	1
R6	CRCW04023163FKEA	Vishay	Resistor, 316kΩ, Size 0402	1
R7	CRCW04022213FKEA	Vishay	Resistor, 221kΩ, Size 0402	1
R12	CRCW04022743FKEA	Vishay	Resistor, 274kΩ, Size 0402	1
R14	CRCW04022943FKEA	Vishay	Resistor, 294kΩ, Size 0402	1
R8, R9, R10, R11, R13, R15	CRCW04021003FKEA	Vishay	Resistor, 100kΩ, Size 0402	6
R16, R17, R18	CRCW08050000FKEA	Vishay	Resistor, 0Ω, Size 0805	3
L1, L2, L3	VLS3012ST-1R0N1R9	TDK	1µH, 2A, 60mΩ, L3.0mm x W3.0mm x H1.0mm	3
	LQH44PN1R0NJ0	Murata	1µH, 2.8A, 50mΩ, L4.0mm x W4.0mm x H1.2mm	
U1	**MIC23450-AAAYML**	**Micrel, Inc[5]**	**3MHz PWM 2A Buck Regulator with HyperLight Load**	**1**

Note:

5. **Micrel, Inc.: www.micrel.com.**

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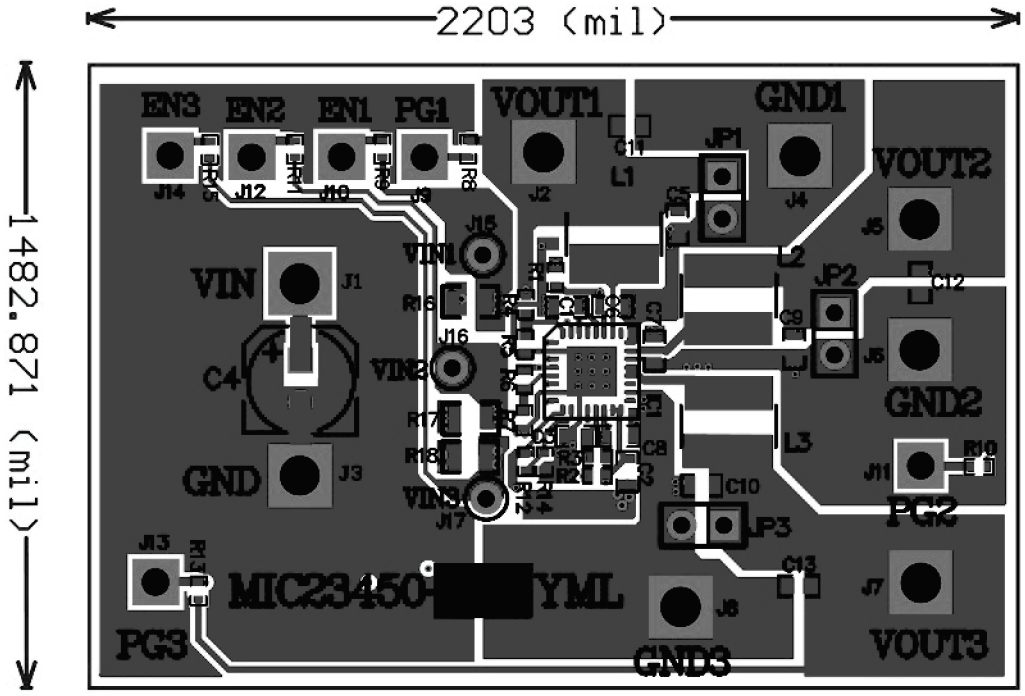
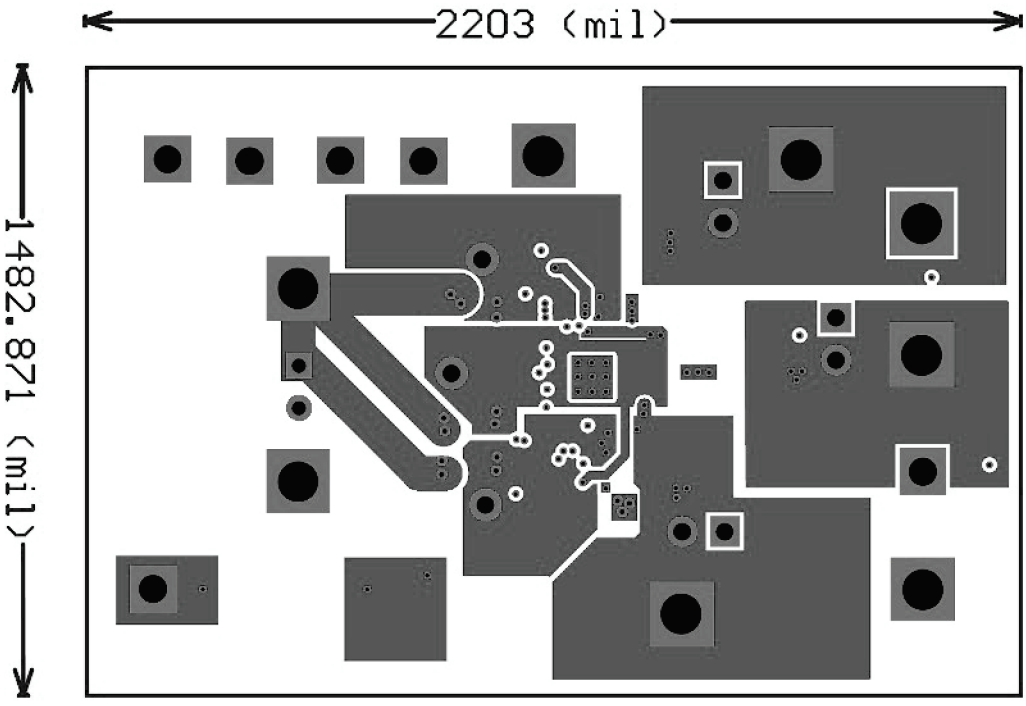
PCB Layout Recommendations



Top Layer



Mid-Layer 1

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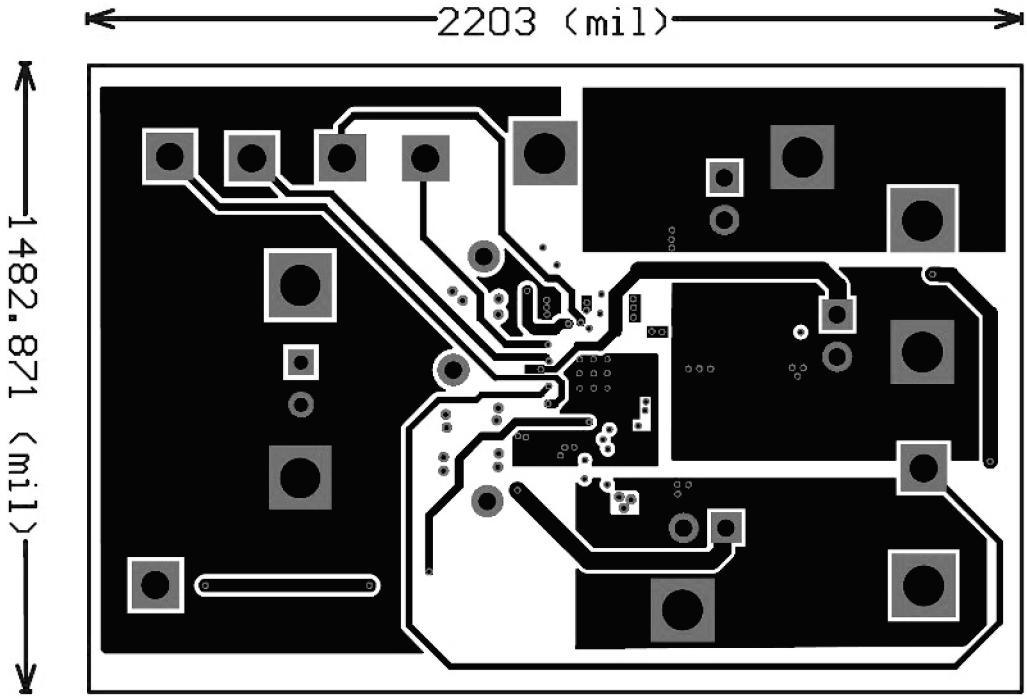
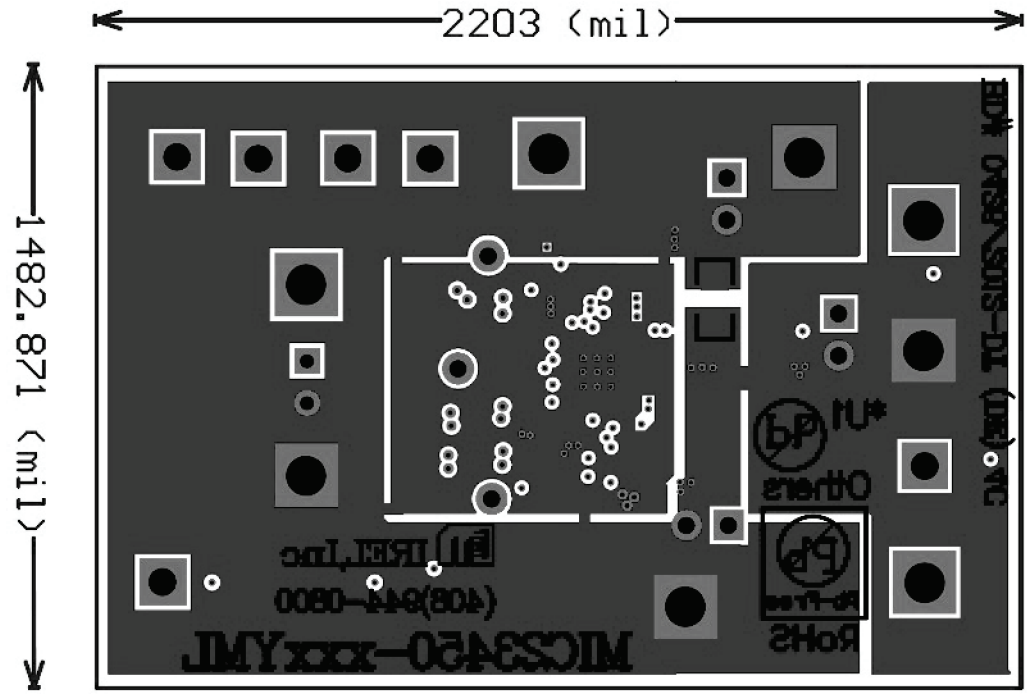


Mid-Layer 2



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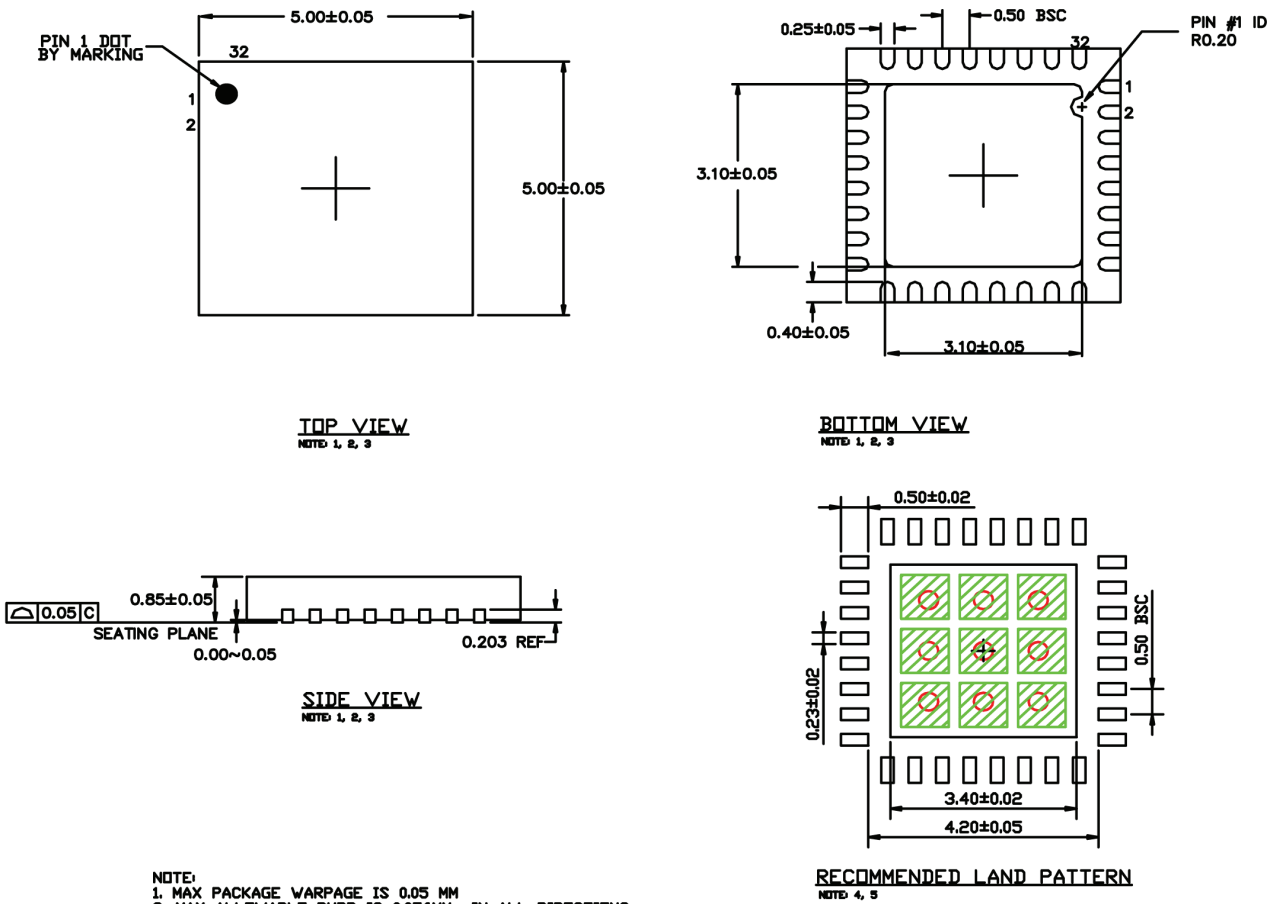
Package Information[1]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.

32-Pin 5mm × 5mm QFN

Note:

1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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