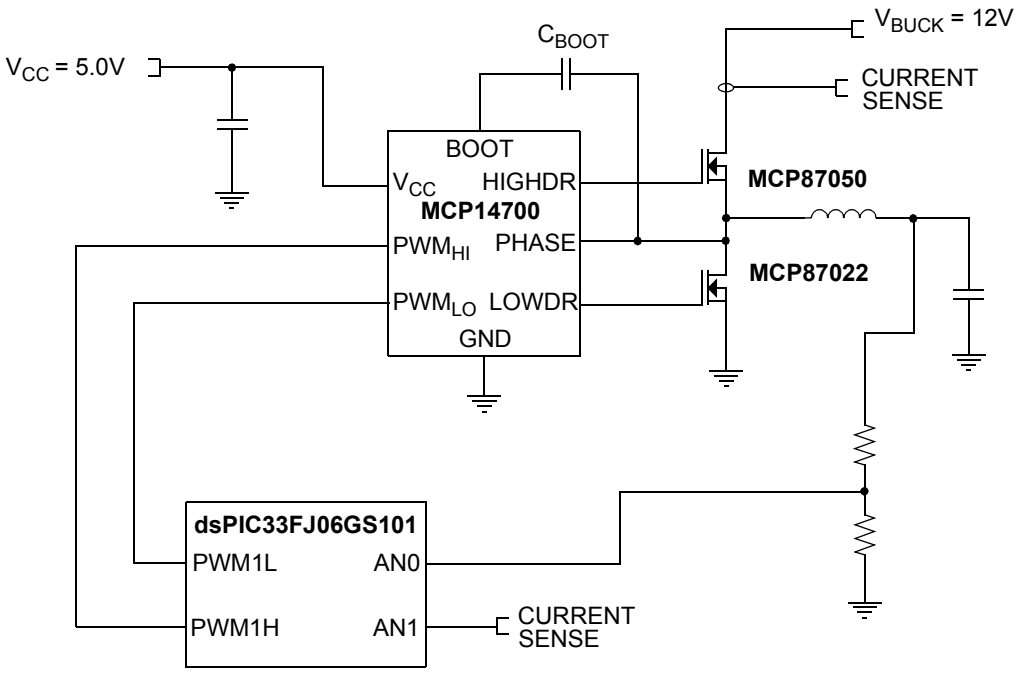
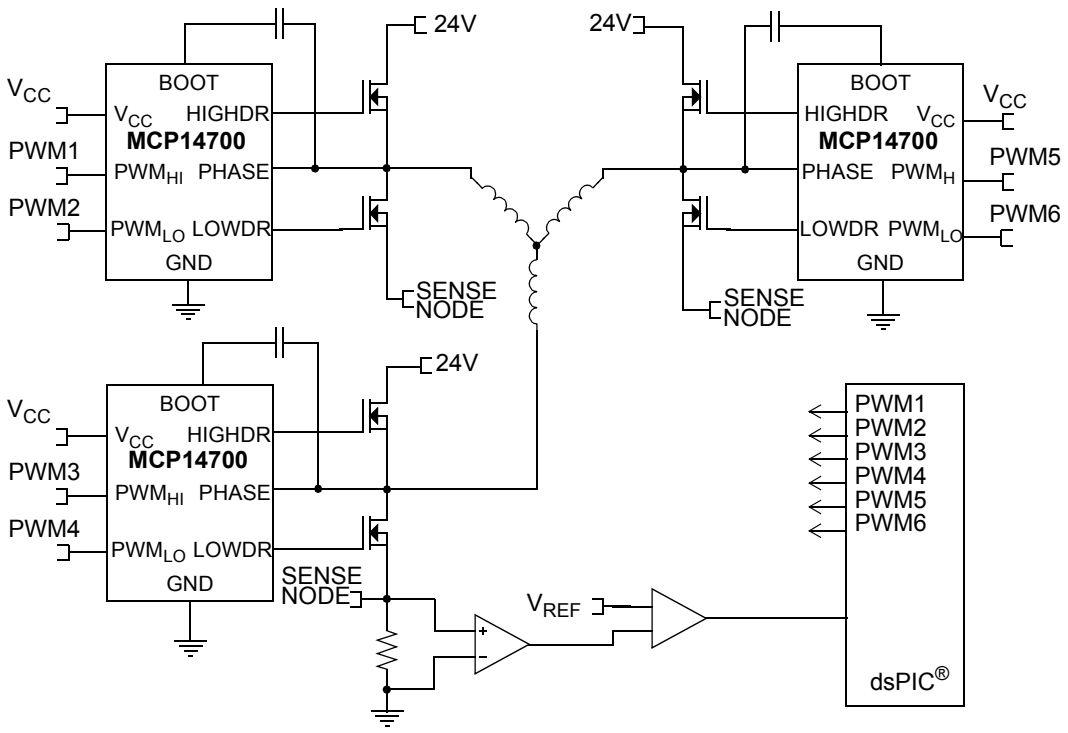
Typical Application Schematic

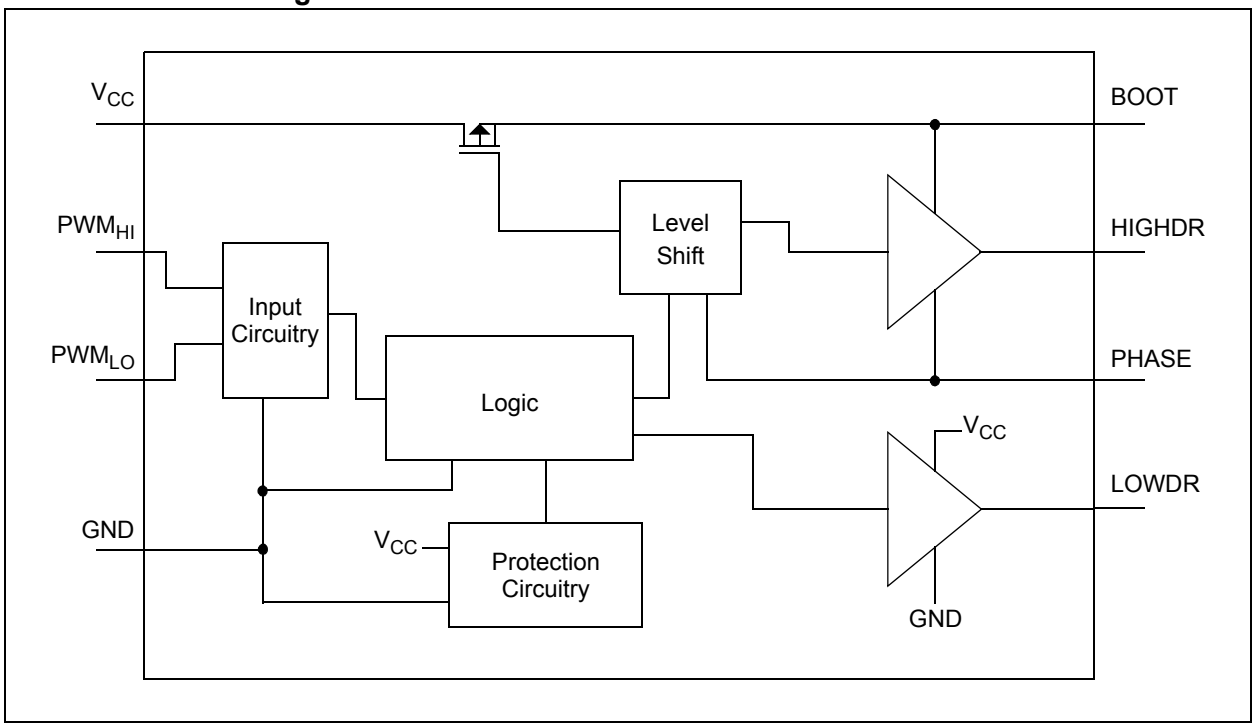
Synchronous Buck Application



3-Phase BLDC Motor Control Application



Functional Block Diagram



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{CC} ..... -0.3V to +7.0V
V_{BOOT} ..... -0.3V to +36.0V
V_{PHASE} ..... V_{BOOT} - 7V to V_{BOOT} + 0.3V
V_{PWM} ..... -0.3V to V_{CC} + 0.3V
V_{HIGHDR} ..... V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{LOWDR} ..... -0.3V to V_{CC} + 0.3V
ESD Protection on all Pins ..... 2 kV (HBM)
..... 400V (MM)

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{CC} = 5.0V, T_J = -40°C to +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{CC} Supply Requirements						
V_{CC} Operating Range	V_{CC}	4.5	5.0	5.5	V	
Bias Supply Voltage	I_{VCC}	—	45	—	µA	PWM_{HI} and PWM_{LO} pin floating
UVLO (Rising V_{CC})	V_{UVLO}	—	3.50	4.00	V	
UVLO Hysteresis	V_{HYS}	—	500	—	mV	
PWM Input Requirements						
PWM Input Current	I_{PWM}	—	7.0	10	µA	V_{PWM} = 3.0V
PWM Input Current	I_{PWM}	—	1.0	—	nA	V_{PWM} = 0V
PWM_{LO} and PWM_{HI} Rising Threshold	PWM_{HI_TH}	1.40	1.60	1.80	V	V_{CC} = 5.0V
PWM_{LO} and PWM_{HI} Falling Threshold	PWM_{LO_TH}	1.10	1.20	1.30	V	V_{CC} = 5.0V
PWM Input Hysteresis	PWM_{HYS}	—	400	—	mV	V_{CC} = 5.0V
Output Requirements						
High Output Voltage (HIGHDR and LOWDR)	V_{OH}	V_{CC} - 0.025	—	—	V	V_{CC} = 5.0V
Low Output Voltage (HIGHDR and LOWDR)	V_{OL}	—	—	0.025	V	V_{CC} = 5.0V
High Drive Source Resistance	R_{HI_SRC}	—	1.0	2.5	Ω	500 mA source current, **Note 1**
High Drive Sink Resistance	R_{HI_SINK}	—	1.0	2.5	Ω	500 mA sink current, **Note 1**
High Drive Source Current	I_{HI_SRC}	—	2.0	—	A	**Note 1**
High Drive Sink Current	I_{HI_SINK}	—	2.0	—	A	**Note 1**
Low Drive Source Resistance	R_{LO_SRC}	—	1.0	2.5	Ω	500 mA source current, **Note 1**
Low Drive Sink Resistance	R_{LO_SINK}	—	0.5	1.0	Ω	500 mA sink current, **Note 1**
Low Drive Source Current	I_{LO_SRC}	—	2.0	—	A	**Note 1**
Low Drive Sink Current	I_{LO_SINK}	—	3.5	—	A	**Note 1**

Note 1: Parameter ensured by characterization, not production tested.
2: See Figure 4-1 and Figure 4-2 for parameter definition.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{CC} = 5.0V, T_J = -40°C to +125°C						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Switching Times						
HIGHDR Rise Time	t_{RH}	—	10	—	ns	C_L = 3.3 nF, **Note 1**, **Note 2**
LOWDR Rise Time	t_{RL}	—	10	—	ns	C_L = 3.3 nF, **Note 1**, **Note 2**
HIGHDR Fall Time	t_{FH}	—	10	—	ns	C_L = 3.3 nF, **Note 1**, **Note 2**
LOWDR Fall Time	t_{FL}	—	6.0	—	ns	C_L = 3.3 nF, **Note 1**, **Note 2**
HIGHDR Turn-off Propagation Delay	t_{PDLH}	20	27	36	ns	No Load, **Note 1**, **Note 2**
LOWDR Turn-off Propagation Delay	t_{PDLL}	10	17	25	ns	No Load, **Note 1**, **Note 2**
HIGHDR Turn-on Propagation Delay	t_{PDHH}	20	27	36	ns	No Load, **Note 1**, **Note 2**
LOWDR Turn-on Propagation Delay	t_{PDHL}	10	17	25	ns	No Load, **Note 1**, **Note 2**
Protection Requirements						
Thermal Shutdown	T_{SHDN}	—	147	—	°C	**Note 1**
Thermal Shutdown Hysteresis	T_{SHDN_HYS}	—	20	—	°C	**Note 1**

Note 1: Parameter ensured by characterization, not production tested.

2: See Figure 4-1 and Figure 4-2 for parameter definition.

TEMPERATURE CHARACTERISTICS

Unless otherwise noted, all parameters apply with V_{CC} = 5.0V						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_A	-65	—	+150	°C	
Specified Temperature Range	T_A	-40	—	+125	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-3x3 DFN	θ_{JA}	—	64	—	°C/W	Typical four-layer board with vias to ground plane
	θ_{JC}	—	12	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
	θ_{JC}	—	42	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with V_{CC} = 5.0V.

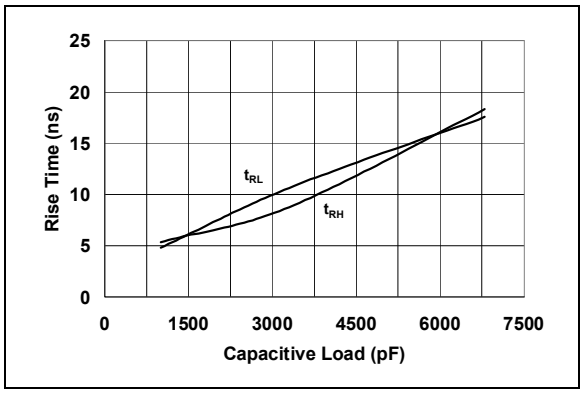


FIGURE 2-1: *Rise Time vs. Capacitive Load.*

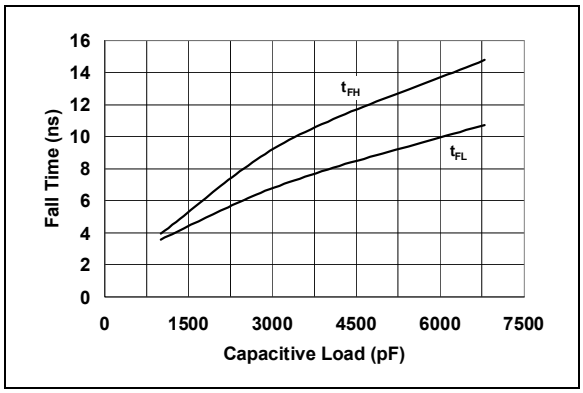


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

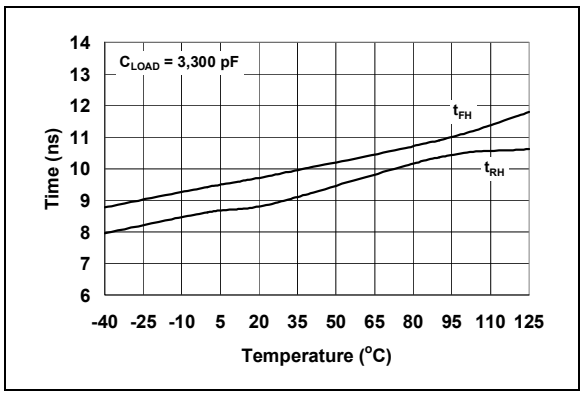


FIGURE 2-2: *HIGHDR Rise and Fall Time vs. Temperature.*

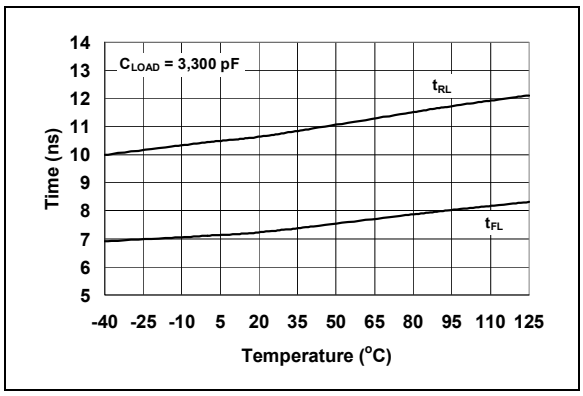


FIGURE 2-5: *LOWDR Rise and Fall Time vs. Temperature.*

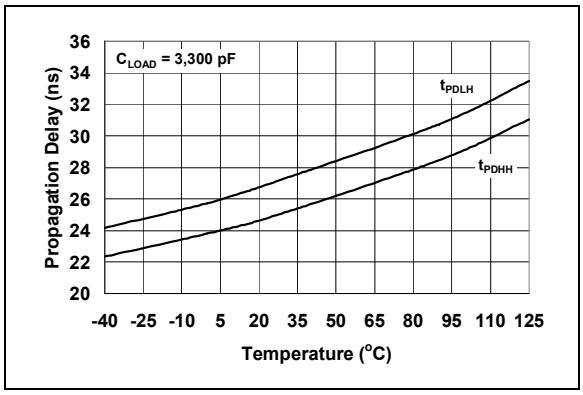


FIGURE 2-3: *HIGHDR Propagation Delay vs. Temperature.*

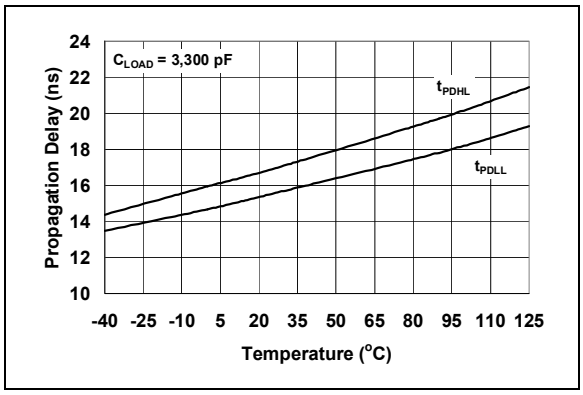


FIGURE 2-6: *LOWDR Propagation Delay vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with V_{CC} = 5.0V.

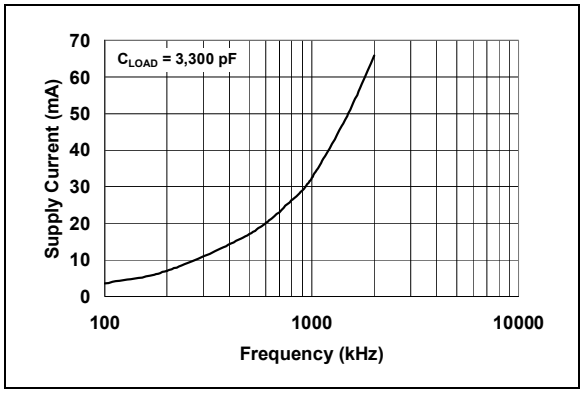


FIGURE 2-7: *Supply Current vs. Frequency.*

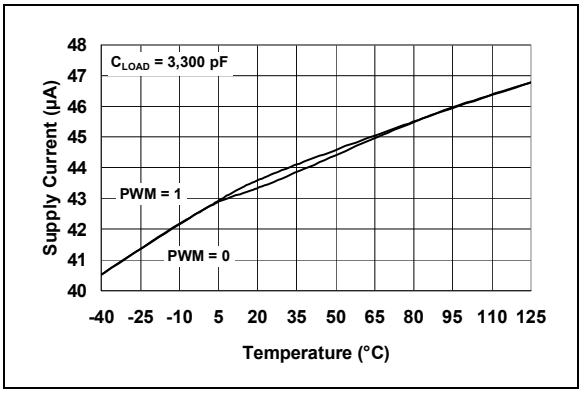


FIGURE 2-8: *Supply Current vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP14700		Symbol	Description
3x3 DFN	SOIC		
1	1	PHASE	Switch Node
2	2	PWM_{HI}	High-Side PWM Control Input Signal
3	3	PWM_{LO}	Low-Side PWM Control Input Signal
4	4	GND	Ground
5	5	LOWDR	Low-side Gate Drive
6	6	V_{CC}	Supply Input Voltage
7	7	BOOT	Floating Bootstrap Supply
8	8	HIGHDR	High-Side Gate Drive
9	—	EP	Exposed Metal Pad

3.1 Switch Node (PHASE)

The PHASE pin provides a return path for the high-side gate driver. The source of the high-side and the drain of the low-side power MOSFETs are connected to this pin.

3.2 High-Side PWM Control Input Signal (PWM_{HI})

The PWM input signal to control the high-side power MOSFET is applied to the PWM_{HI} pin. A logic high on the PWM_{HI} pin causes the HIGHDR pin to also transition high.

3.3 Low-Side PWM Control Input Signal (PWM_{LO})

The PWM input signal to control the low-side power MOSFET is applied to the PWM_{LO} pin. A logic high on the PWM_{LO} pin causes the LOWDR pin to also transition high.

3.4 Ground (GND)

The GND pin provides ground for the MCP14700 circuitry. It should have a low-impedance connection to the bias supply source return. High peak currents will flow out the GND pin when the low-side power MOSFET is being turned off.

3.5 Low-side Gate Drive (LOWDR)

The LOWDR pin provides the gate drive signal to control the low-side power MOSFET. The gate of the low-side power MOSFET is connected to this pin.

3.6 Supply Input Voltage (V_{CC})

The V_{CC} pin provides bias to the MCP14700 device. A bypass capacitor is to be placed between this pin and the GND pin. This capacitor should be placed as close to the MCP14700 as possible.

3.7 Floating Bootstrap Supply (BOOT)

The BOOT pin is the floating bootstrap supply pin for the high-side gate drive. A capacitor is connected between this pin and the PHASE pin to provide the necessary charge to turn on the high-side power MOSFET.

3.8 High-Side Gate Drive (HIGHDR)

The HIGHDR pin provides the gate drive signal to control the high-side power MOSFET. The gate of the high-side power MOSFET is connected to this pin.

3.9 Exposed Metal Pad (EP)

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

NOTES:

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP14700 is a synchronous MOSFET driver with dual independent PWM inputs capable of controlling both a ground referenced and floating N-Channel MOSFET. The PWM input threshold levels are truly 3.0V logic tolerant and have 400 mV of typical hystereses making the MCP14700 ideal for use with low-voltage controllers.

The MCP14700 is capable of suppling 2A (typical) peak current to the floating high-side MOSFET that is connected to the HIGHDR. With the exception of a capacitor, all of the circuitry needed to drive this high-side N-channel MOSFET is internal to the MCP14700. A blocking device is placed between the V_{CC} and BOOT pins that allows the bootstrap capacitor to be charged to V_{CC} when the low-side power MOSFET is conducting. Refer to the application section, **Section 5.1 "Bootstrap Capacitor Select"**, for information on determining the proper size of the bootstrap capacitor. The HIGHDR is also capable of sinking 2A (typical) peak current.

The LOWDR is capable of sourcing 2A (typical) peak current and sinking 3.5A (typical) peak current. This helps ensure that the low-side MOSFET stays turned off during the high dv/dt of the PHASE node.

4.2 PWM Inputs

A logic high on either PWM pin causes the corresponding output drive signal to be high. See Figure 4-1 and Figure 4-2 for a graphical representation of the MCP14700 operation. Internally the PWM pins are pulled to ground to ensure there is no drive signal to the external MOSFETs if the pins are left floating. For reliable operation, it is recommended that the rising and falling slew rate of the PWM signal be faster than 1V/50 ns.

When designing with the MCP14700 in applications where cross conduction of the external MOSFETs is not desired, care must be taken to ensure the PWM inputs have the proper timing. There is no internal cross conduction protection in the MCP14700.

4.3 Under Voltage Lockout (UVLO)

The UVLO feature of the MCP14700 does not allow the HIGHDR or LOWDR output to function when the input voltage, V_{CC}, is below the UVLO threshold regardless of the state of the PWM_{HI} and PWM_{LO} pins.

Once V_{CC} reaches the UVLO threshold, the HIGHDR and LOWDR outputs will respond to the state of the PWM_{HI} or PWM_{LO} pins. There is a 500 mV hystereses on the UVLO threshold.

4.4 Overtemperature Protection

The MCP14700 is protected from an overtemperature condition by an internal thermal shutdown feature. When the internal temperature of the MCP14700 reaches 147°C typically, the HIGHDR and LOWDR outputs will transition to a low state regardless of the state of the PWM_{HI} or PWM_{LO} pins. Once the internal temperature is reduced by 20°C typically, the MCP14700 will automatically respond to the states of the PWM_{HI} and PWM_{LO} pins.

4.5 Timing Diagram

The PWM signal applied to the MCP14700 is supplied by a controller IC. The timing diagram in Figure 4-1 graphically depicts the PWM signal and the output signals of the MCP14700.

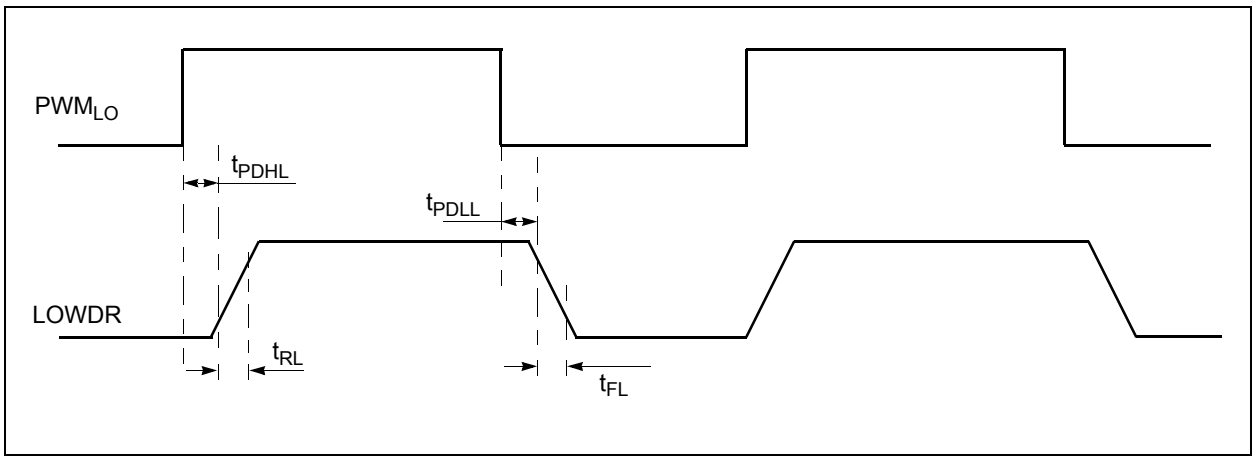


FIGURE 4-1: *MCP14700 LOWDR Timing Diagram.*

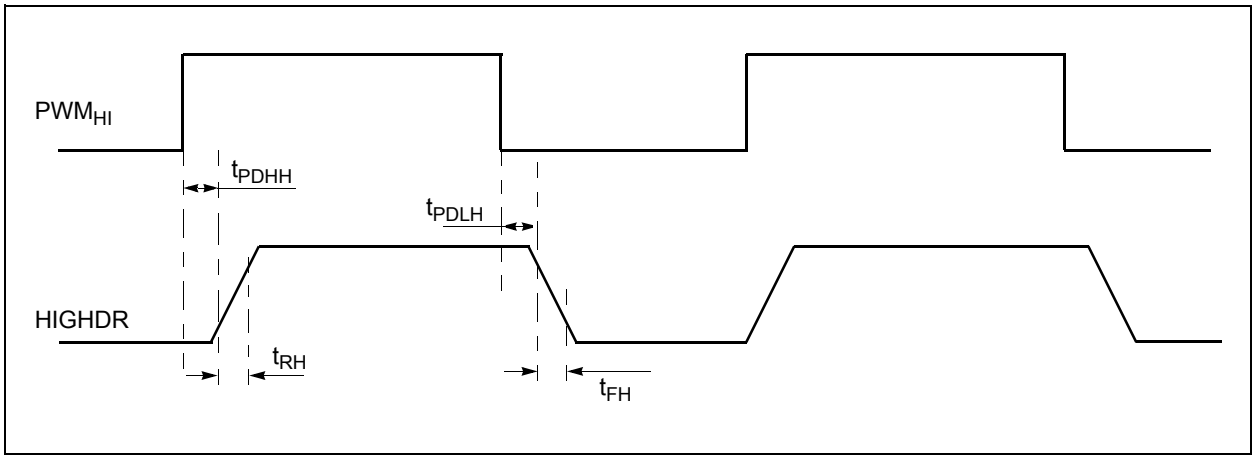


FIGURE 4-2: *MCP14700 HIGHDR Timing Diagram.*

5.0 APPLICATION INFORMATION

5.1 Bootstrap Capacitor Select

The selection of the bootstrap capacitor is based upon the total gate charge of the high-side power MOSFET and the allowable droop in gate drive voltage while the high-side power MOSFET is conducting.

EQUATION 5-1:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{DROOP}}$$

Where:

C_{BOOT}	=	Bootstrap capacitor value
Q_{GATE}	=	Total gate charge of the high-side MOSFET
ΔV_{DROO}	=	Allowable gate drive voltage droop

For example:

Q_{GATE} = 30 nC

ΔV_{DROOP} = 200 mV

$C_{BOOT} \geq$ 0.15 uF

A low ESR ceramic capacitor is recommend with a maximum voltage rating that exceeds the maximum input voltage, V_{CC}, plus the maximum supply voltage, V_{SUPPLY}. It is also recommended that the capacitance of C_{BOOT} does not exceed 1.2 uF.

5.2 Decoupling Capacitor

Proper decoupling of the MCP14700 is highly recommended to help ensure reliable operation. This decoupling capacitor should be placed as close to the MCP14700 as possible. The large currents required to quickly charge the capacitive loads are provided by this capacitor. A low ESR ceramic capacitor is recommended.

5.3 Power Dissipation

The power dissipated in the MCP14700 consists of the power loss associated with the quiescent power and the gate charge power.

The quiescent power loss can be calculated by the following equation and is typically negligible compared to the gate drive power loss.

EQUATION 5-2:

$$P_Q = I_{VCC} \times V_{CC}$$

Where:

P_Q	=	Quiescent power loss
I_{VCC}	=	No Load Bias Current
V_{CC}	=	Bias Voltage

The main power loss occurs from the gate charge power loss. This power loss can be defined in terms of both the high-side and low-side power MOSFETs.

EQUATION 5-3:

$$P_{GATE} = P_{HIGHDR} + P_{LOWDR}$$
$$P_{HIGHDR} = V_{CC} \times Q_{HIGH} \times F_{SW}$$
$$P_{LOWDR} = V_{CC} \times Q_{LOW} \times F_{SW}$$

Where:

P_{GATE}	=	Total Gate Charge Power Loss
P_{HIGHDR}	=	High-Side Gate Charge Power Loss
P_{LOWDR}	=	Low-Side Gate Charge Power Loss
V_{CC}	=	Bias Supply Voltage
Q_{HIGH}	=	High-Side MOSFET Total Gate Charge
Q_{LOW}	=	Low-Side MOSFET Total GAte Charge
F_{SW}	=	Switching Frequency

5.4 PCB Layout

Proper PCB layout is important in a high current, fast switching circuit to provide proper device operation. Improper component placement may cause errant switching, excessive voltage ringing, or circuit latch-up.

There are two important states of the MCP14700 outputs, high and low. Figure 5-1 depicts the current flow paths when the outputs of the MCP14700 are high and the power MOSFETs are turned on. The charge needed to turn on the low-side power MOSFET comes from the decoupling capacitor C_{VCC}. The current flows from this capacitor through the internal LOWDR circuitry, into the gate of the low-side power MOSFET, out the source, into the ground plane, and back to C_{VCC}. To reduce any excess voltage ringing or spiking, the inductance and area of this current loop must be minimized.

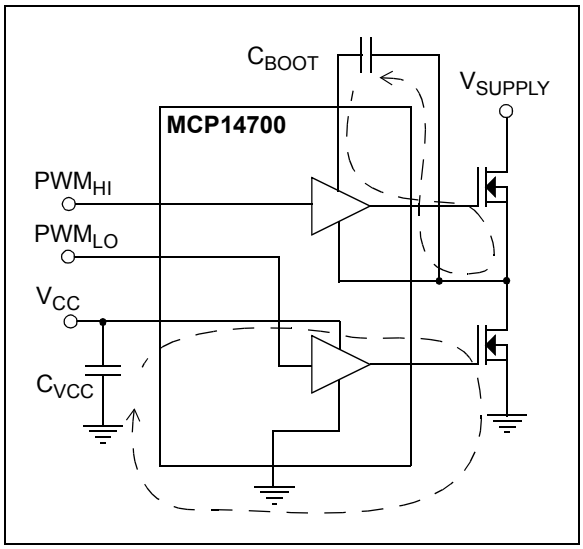


FIGURE 5-1: *Turn On Current Paths.*

The charge needed to turn on the high-side power MOSFET comes from the bootstrap capacitor C_{BOOT}. Current flows from C_{BOOT} through the internal HIGHDR circuitry, into the gate of the high-side power MOSFET, out the source and back to C_{BOOT}. The printed circuit board traces that construct this current loop need to have a small area and low inductance. To control the inductance, short and wide traces must be used.

Figure 5-2 depicts the current flow paths when the outputs of the MCP14700 are low and the power MOSFETs are turned off. These current paths should also have low inductance and a small loop area to minimize the voltage ringing and spiking.

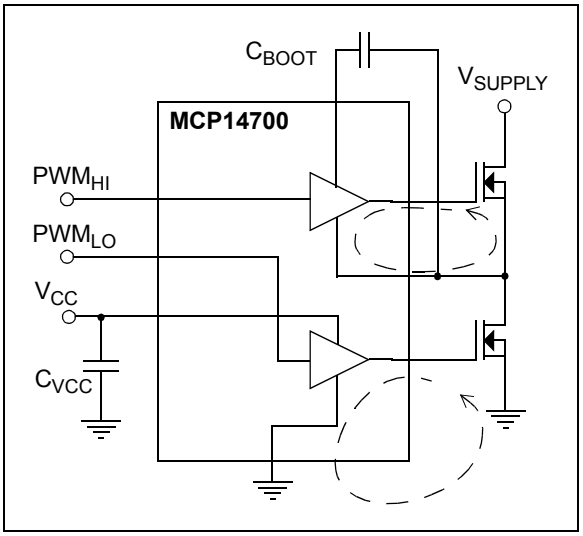


FIGURE 5-2: *Turn Off Current Paths.*

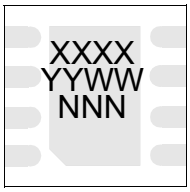
The following recommendations should be followed for optimal circuit performance:

- The components that construct the high current paths previously mentioned should be placed close the MCP14700 device. The traces used to construct these current loops should be wide and short to keep the inductance and impedance low.
- A ground plane should be used to keep both the parasitic inductance and impedance minimized. The MCP14700 device is capable of sourcing and sinking high peaks current and any extra parasitic inductance or impedance will result in non-optimal performance.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

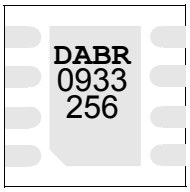
8-Lead DFN (3x3)



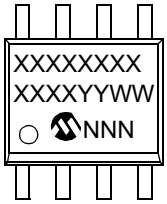
Device	Code
MCP14700	DABR

Note: Applies to 8-Lead 3x3 DFN

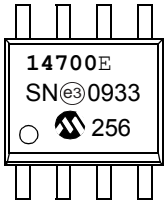
Example:



8-Lead SOIC (150 mil)



Example:

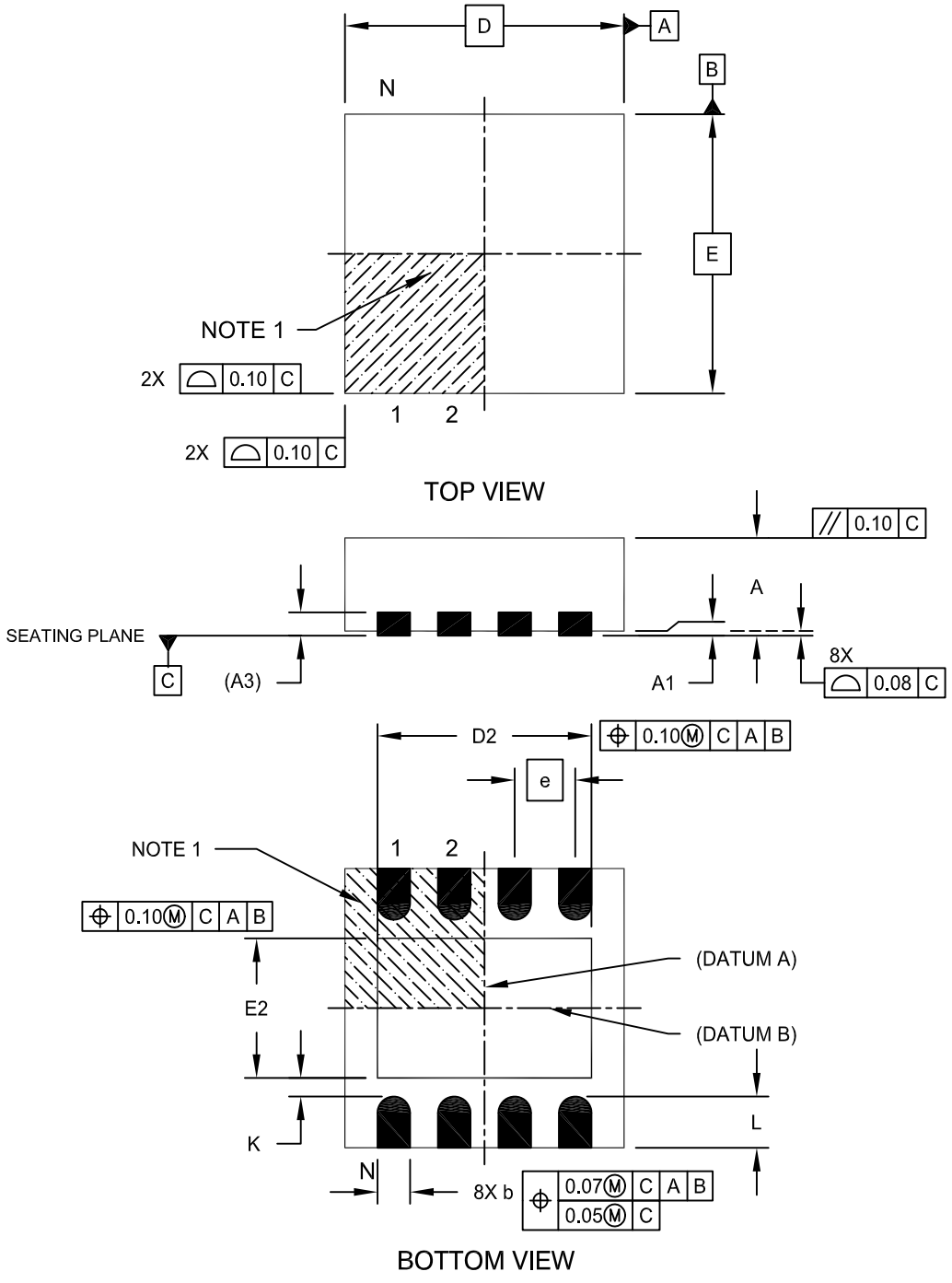


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

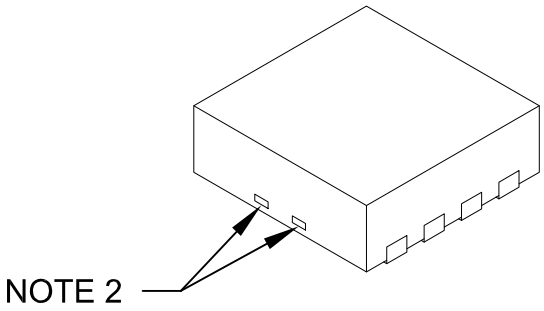
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

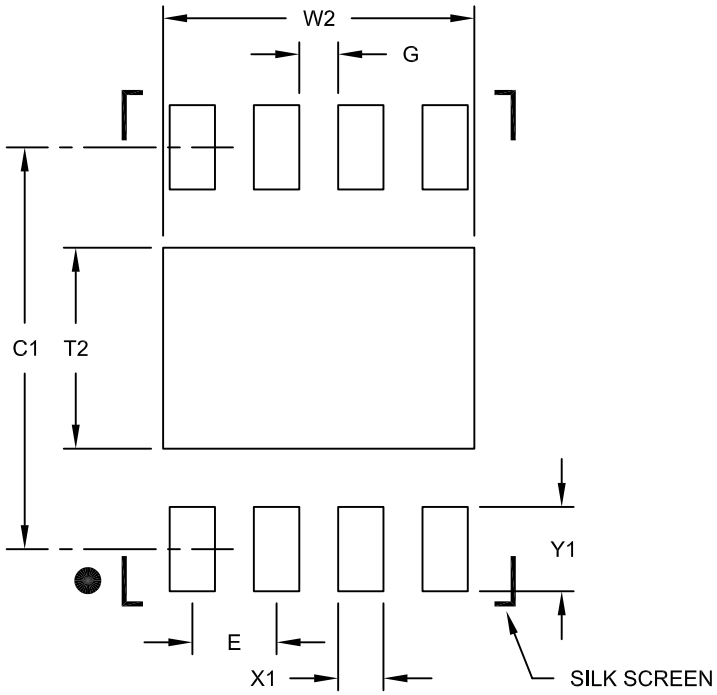
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

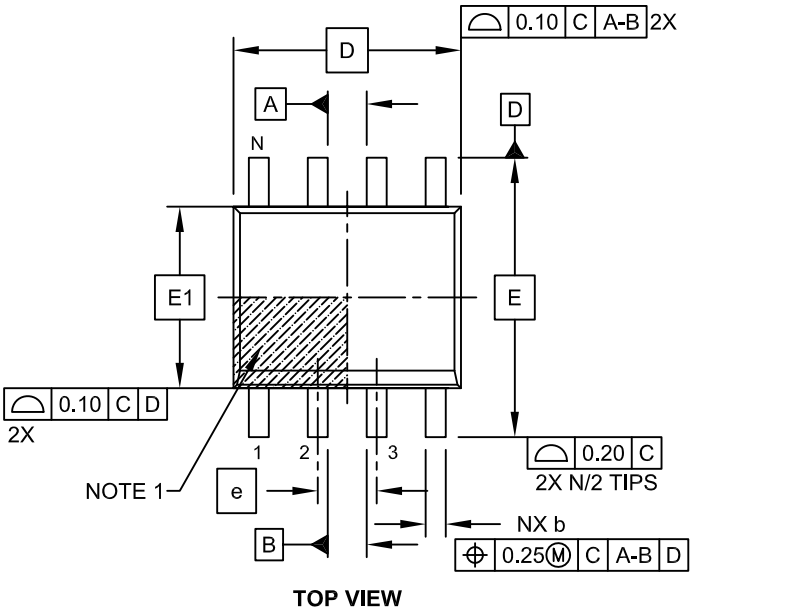
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

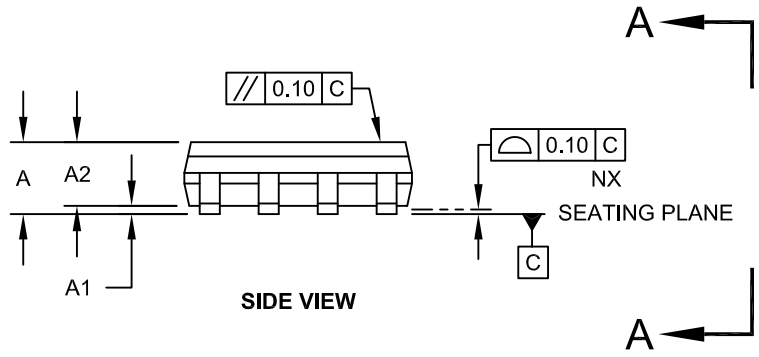
Microchip Technology Drawing No. C04-2062B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

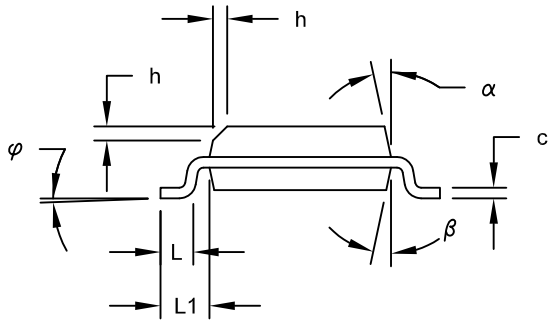
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

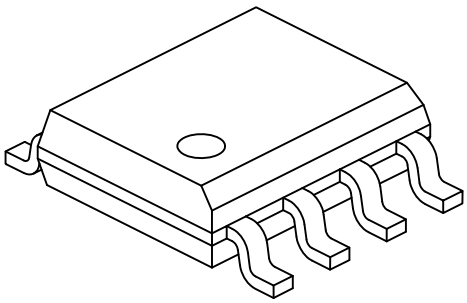


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

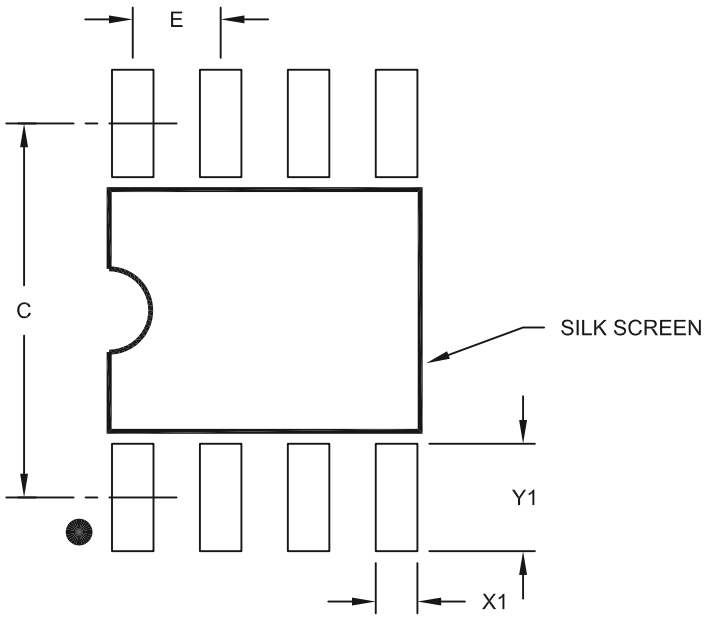
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (January 2013)

The following is the list of modifications:

1. Updated the Features: list on page 1.
2. Updated the Typical Application Schematic.

Revision A (September 2009)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP14700:	Dual Input Synchronous MOSFET Driver
	MCP14700T:	Dual Input Synchronous MOSFET Driver - Tape and Reel (DFN and SOIC)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MF =	Plastic Dual Flat, No Lead (3x3 DFN), 8-lead
	SN =	Plastic Small Outline, (3.90 mm), 8-lead

Examples:

a) MCP14700-E/MF: Extended Temperature, 8LD DFN package.

b) MCP14700T-E/MF: Tape and Reel, Extended Temperature, 8LD DFN package.

a) MCP14700-E/SN: Extended Temperature, 8LD SOIC package.

b) MCP14700T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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