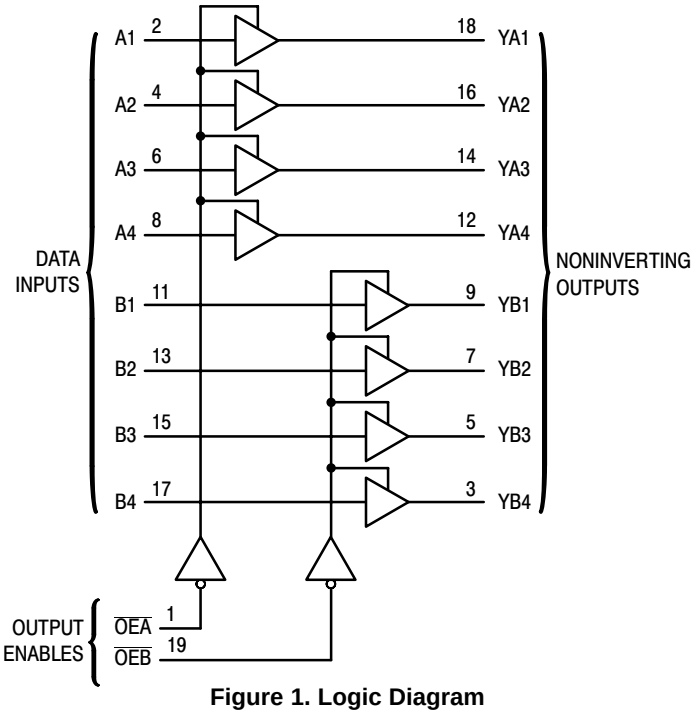


Figure 1. Logic Diagram

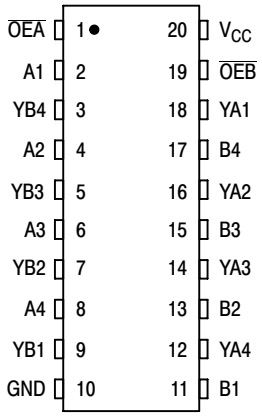


Figure 2. Pin Assignment

FUNCTION TABLE

Inputs		Outputs
$\overline{OEA}$, $\overline{OEB}$	A, B	YA, YB
L L H	L L H H X Z	

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +7.0	V
V_{in}	DC Input Voltage		–0.5 to +7.0	V
V_{out}	DC Output Voltage	Output in 3−State High or Low State	–0.5 to +7.0 –0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		±20	mA
I_{out}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		–65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
†Derating − SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage	Output in 3−State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		−40	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 5.0 V ± 0.5 V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 40 to 85°C		T_A = 85 to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	Maximum Low−Level Input Voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	Minimum High−Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5		4.4		4.4		V
		I_{OH} = −8 mA	4.5	3.94			3.80		3.66		
V_{OL}	Maximum Low−Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5		0.0	0.1		0.1		0.1	V
		I_{OL} = 8 mA	4.5			0.36		0.44		0.52	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			±0.25		±2.5		2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} =3.4 V Other Input: V_{CC} or GND	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -40$ to $85°C$ Min	$T_A = -40$ to $85°C$ Max	$T_A = 85$ to $125°C$ Min	$T_A = 85$ to $125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay A to YA or B to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $C_L = 50$ pF		5.4 5.9	7.4 8.4	1.0 1.0	8.5 9.5	11.0 1.0	9.5 10.5	ns
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OEA}$ to YA or $\overline{OEB}$ to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 15$ pF $R_L = 1$ kΩ $C_L = 50$ pF		7.7 8.2	10.4 11.4	1.0 1.0	12.0 13.0	1.0 1.0	13.5 14.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OEA}$ to YA or $\overline{OEB}$ to YB	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF $R_L = 1$ kΩ		8.8	11.4	1.0	13.0	1.0	14.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5$ V $C_L = 50$ pF (Note 1)			1.0		1.0		1.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Typical @ 25°C, $V_{CC} = 5.0$ V Min	Typ	Max	Unit
C_{PD}	Power Dissipation Capacitance (Note 2)		18		pF
C_{in}	Maximum Input Capacitance		4	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)		9		pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.1	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.9	−1.1	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT244ADWR2	SOIC−20WB	1000 / Tape & Reel
MC74VHCT244ADWRG	SOIC−20WB (Pb−Free)	1000 / Tape & Reel
MC74VHCT244ADT	TSSOP−20*	75 Units / Rail
MC74VHCT244ADTG	TSSOP−20*	75 Units / Rail
MC74VHCT244ADTR2	TSSOP−20*	2500 / Tape & Reel
MC74VHCT244ADTRG	TSSOP−20*	2500 / Tape & Reel
MC74VHCT244AMEL	SOEIAJ−20	2000 / Tape & Reel
MC74VHCT244AMELG	SOEIAJ−20 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

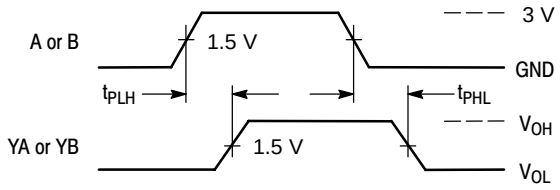


Figure 3. Switching Waveform

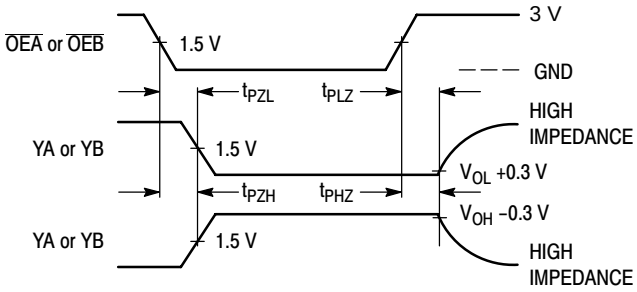
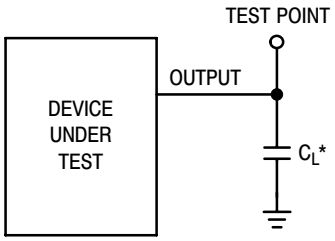
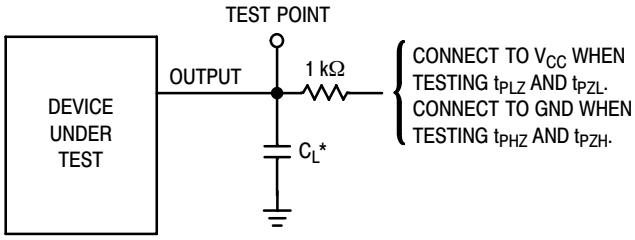


Figure 4. Switching Waveform



*Includes all probe and jig capacitance

Figure 5. Test Circuit

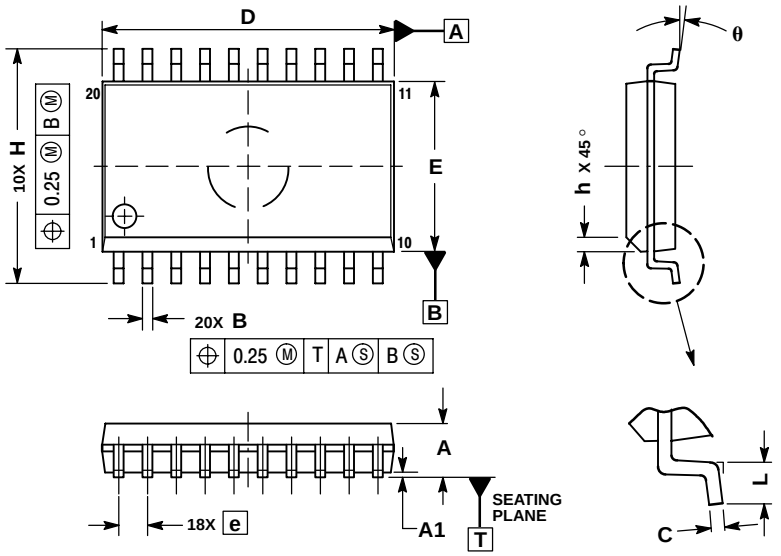


*Includes all probe and jig capacitance

Figure 6. Test Circuit

PACKAGE DIMENSIONS

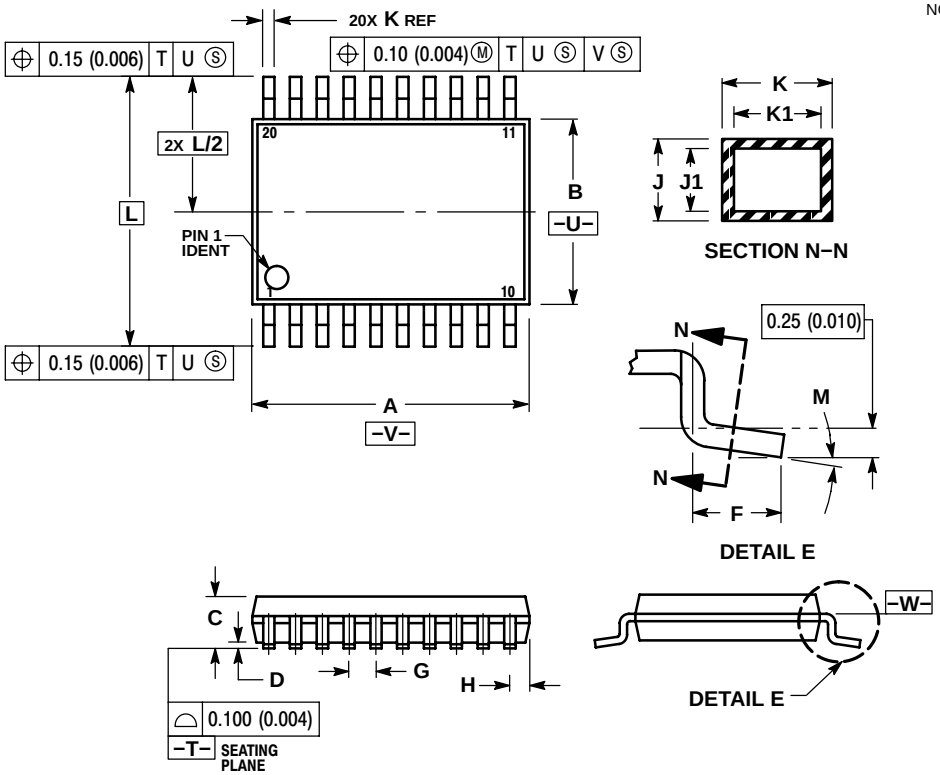
SOIC−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

TSSOP−20
D5 SUFFIX
CASE 948E−02
ISSUE B



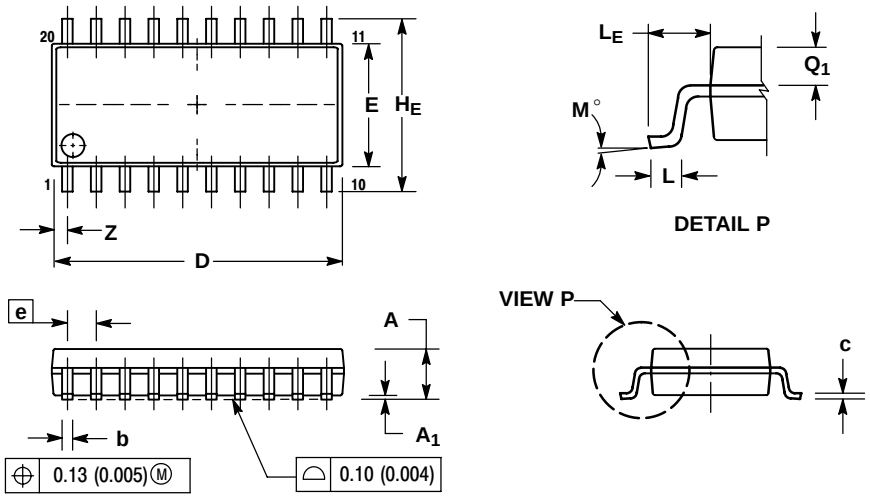
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHCT244A

PACKAGE DIMENSIONS

SOEIAJ−20
M SUFFIX
CASE 967−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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