DEVICE VARIATIONS

Table 1. MC35XS3500 Device Variations

Part Number	Package	Temp.	Comment
MC35XS3500HFK	24 PQFN	-40 to 125 °C	Initial release
MC35XS3500DHFK			D version is more robust against V_{BAT} interrupt

INTERNAL BLOCK DIAGRAM

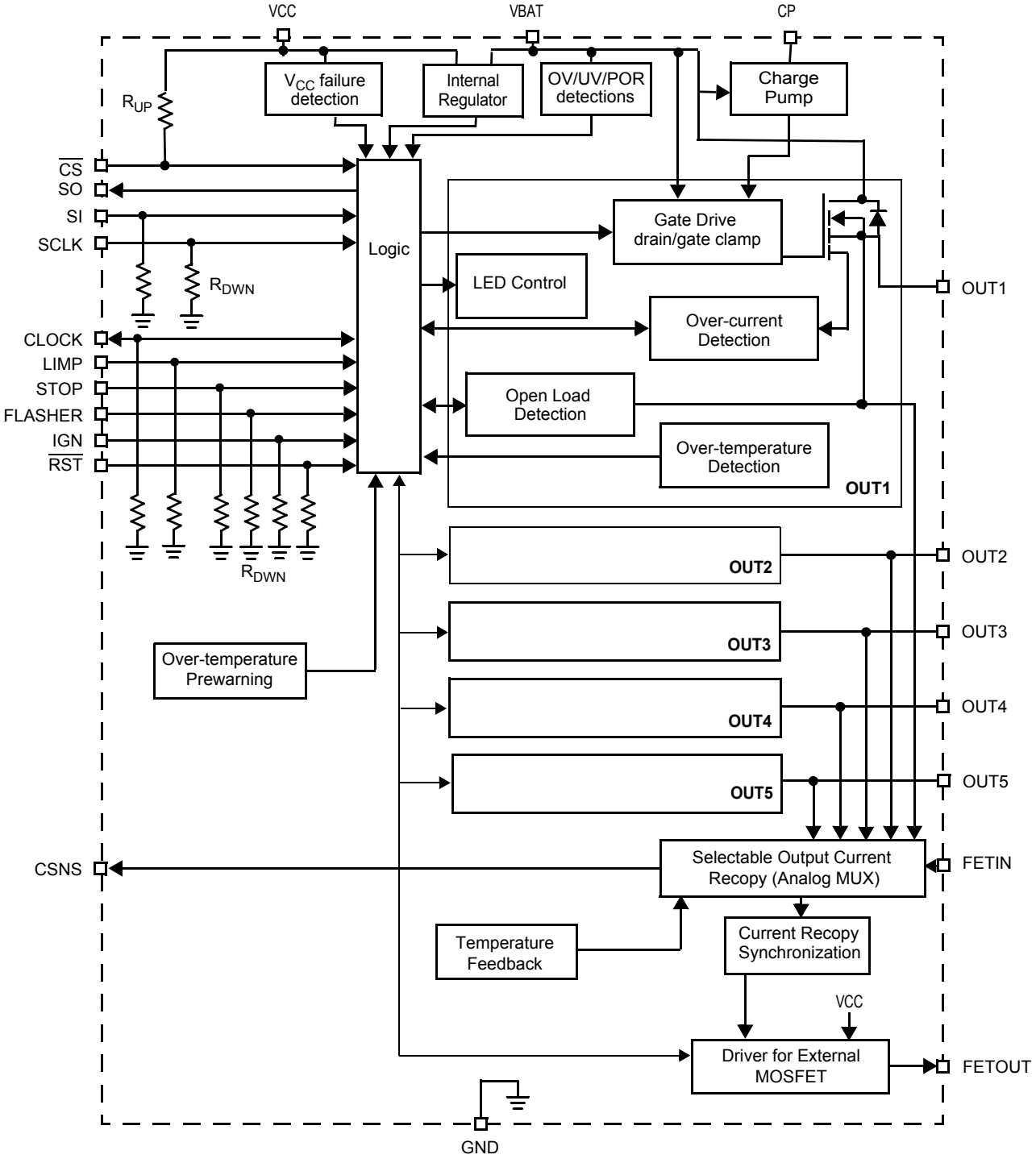


Figure 2. 35XS3500 Simplified Internal Block Diagram

PIN CONNECTIONS

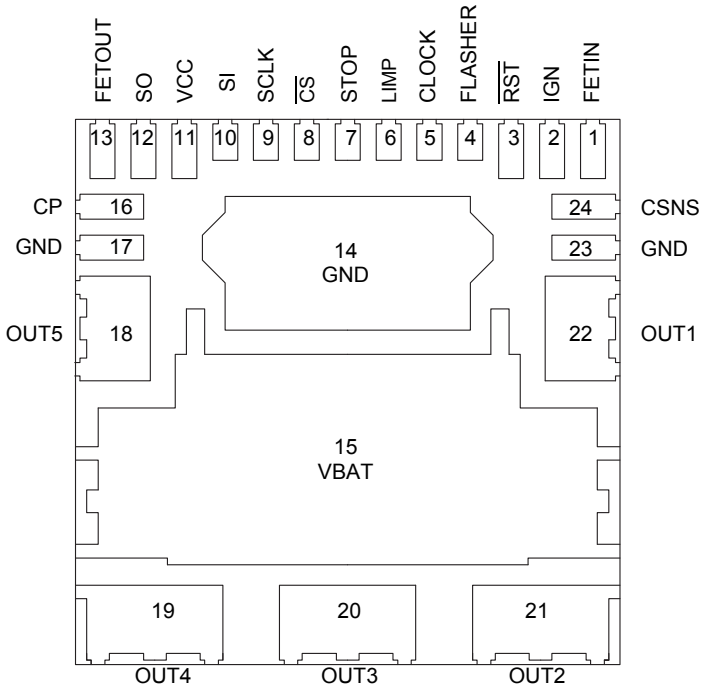


Figure 3. 35XS3500 Pin Connections (Transparent Package Top View)

Table 2. 35XS3500 Pin Definitions

Functional descriptions these pins can be found in the Functional Description section beginning on page 20.

Pin	Pin Name	Pin Function	Formal Name	Definition
1	FETIN	Input	External FET Input	This pin is the current sense recopy of the external MOSFET.
2	IGN	Input	Ignition Input (Active High)	This input wakes the device. It also controls outputs 1 and 2 in case of Fail mode activation. This pin has a passive internal pull-down.
3	$\overline{\text{RST}}$	Input	Reset	This input wakes the device. It is also used to initialize the device configuration and fault registers through the SPI. This pin has a passive internal pull-down.
4	FLASHER	Input	Flasher Input (Active High)	This input wakes the device. This pin has a passive internal pull-down.
5	CLOCK	Input	Clock Input	This pin state depends on $\overline{\text{RST}}$ logic level. As long as $\overline{\text{RST}}$ input pin is set to logic [0], this pin is pulled up in order to report wake event. Otherwise, the PWM frequency and timing are generated from this digital clock input by the PWM module. This pin has a passive internal pull-down.
6	LIMP	Input	Limp Home Input (Active High)	The Fail mode can be activated by this digital input. This pin has an active internal pull-down current source.
7	STOP	Input	Stop Light Input (Active High)	This input wakes the device. This pin has a passive internal pull-down.
8	$\overline{\text{CS}}$	Input	Chip Select (Active Low)	When this signal is high, SPI signals are ignored. Asserting this pin low starts a SPI transaction. The transaction is signaled as completed when this signal returns high. This pin has a passive internal pull-up resistance.
9	SCLK	Input	SPI Clock Input	This input pin is connected to the master microcontroller providing the required bit shift clock for SPI communication. This pin has a passive internal pull-down resistance.

Table 2. 35XS3500 Pin Definitions (continued)

Functional descriptions these pins can be found in the Functional Description section beginning on page 20.

Pin	Pin Name	Pin Function	Formal Name	Definition
10	SI	Input	Master-Out Slave-In	This data input is sampled on the positive edge of the SCLK. This pin has a passive internal pull-down resistance.
11	VCC	Input	Logic Supply	SPI Logic power supply.
12	SO	Output	Master-In Slave-Out	SPI data sent to the MCU by this pin. This data output changes on the negative edge of SCLK, and when $\overline{CS}$ is high. This pin is high-impedance.
13	FETOUT	Output	External FET Gate	This pin controls an external SMART MOSFET by logic level. This output called OUT6. If OUT6 is not used in the application, this output pin is set to logic high when the current sense output becomes valid when CSNS sync SPI bit is set to logic [1].
14, 17, 23	GND	Ground	Ground	This pin is the ground for the logic and analog circuitry of the device.(1)
15	VBAT	Input	Battery Input	Power supply pin.
16	CP	Output	Charge Pump	This pin is the connection for an external tank capacitor (for internal use only).
18 19 20 21 22	OUT5 OUT4 OUT3 OUT2 OUT1	Output Output Output Output Output	Output 5 Output 4 Output 3 Output 2 Output 1	Protected 35 mΩ high side power output to the load.
24	CSNS	Output	Current Sense Output	This pin is used to output a current proportional to OUT1:OUT5, FETin current, and it is used externally to generate a ground-referenced voltage for the microcontroller to monitor output current. Moreover, this pin can report a voltage proportional to the temperature on the GND flag. OUT1:OUT5, FETin current sensing and Temperature feedback choice is SPI programmable.

Notes

1. The pins 14, 17, and 23 must be shorted on the board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Over-voltage Test Range Maximum Operation Voltage Load Dump (400 ms) at 25 °C	V_{BAT}	 28 40	V
Reverse Polarity Voltage Range 2.0 Min at 25 °C	V_{BAT}	 -18	V
VCC Supply Voltage	V_{CC}	-0.3 to 5.5	V
Output Voltage Positive Negative (ground disconnected)	V_{OUT}	 40 -16	V
Digital Input Current in Clamping Mode (SI, SCLK, $\overline{CS}$, IGN, FLASHER, STOP, LIMP)	I_{IN}	±1.0	mA
FETIN Input Current	I_{FETIN}	+10 -1.0	mA
SO and FETOUT Output Voltage	V_{SO}	-0.3 to V_{CC}+0.3	V
Outputs clamp energy using single pulse method (L = 2.0 mH; R = 0 Ω; VBAT = 14 V at 150 °C initial)	E	30	mJ
ESD Voltage[2] Human Body Model (HBM) OUT[1:5], VPWR, and GND Charge Device Model (CDM) Corner Pins (1,13,19,21) All Other Pins (2-12, 14-18, 20, 22-24)	V_{ESD}	 ±2000 ±8000 ±750 ±500	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Peak Package Reflow Temperature During Reflow[3], [4]	T_{PPRT}	Note 4	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal Resistance, Junction to Case[5]	$R_{\theta JC}$	1.0	°C/W

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.
3. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
5. Typical value is guaranteed per design.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (VBAT, VCC)					
Battery Supply Voltage Range	V_{BAT}				V
Full Performance and Short-circuit		7.0	–	20	
Extended Voltage Range[6]		6.0	–	28	
Battery Supply Under-voltage (UV flag is set ON)	V_{BATUV}	5.0	5.5	6.0	V
Battery Voltage Clamp (OV flag is set ON)	$V_{BATCLAMP\_OV}$	27.5	30	32.5	V
Battery Voltage Clamp	$V_{BATCLAMP}$	40	–	48	V
Battery Supply Power on Reset[9]					V
If V_{BAT} < 5.5 V, V_{BAT} = V_{CC}	$V_{BATPOR1}$	2.0	–	3.0	
If V_{BAT} < 5.5 V, V_{BAT} = 0	$V_{BATPOR2}$	2.0	–	4.0	
VBAT Supply Current at 25 °C and V_{BAT} =12 V and V_{CC} = 5.0 V					
Sleep State Current, Outputs Open	$I_{BATSLEEP1}$	–	0.5	5.0	µA
Sleep State Current, Outputs Grounded	$I_{BATSLEEP2}$	–	0.5	5.0	µA
Normal Mode, IGN = 5.0 V, $\overline{RST}$ = 5.0 V, Outputs Open	I_{BAT}	–	10	20	mA
Digital Voltage Range, Full Performance	V_{CC}	3.0	–	5.5	V
Digital Supply Under-voltage (V_{CC} Failure)	V_{CCUV}	2.2	2.5	2.8	V
Sleep Current Consumption on V_{CC} at 25 °C and V_{BAT} = 12 V	$I_{CCSLEEP}$				µA
Output OFF		–	0.2	5.0	
Supply Current Consumption on V_{CC} and V_{BAT} = 12 V	I_{CC}				mA
No SPI		–	–	2.6	
3.0 MHz SPI Communication		–	–	5.0	
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, STOP)					
Input High Logic Level[7]	V_{IH}	2.0	–	–	V
Input Low Logic Level[7]	V_{IL}	–	–	0.8	V
Ignition Threshold Level (IGN, FLASHER, STOP and $\overline{RST}$)	V_{IGNTH}	1.0		2.2	V
Input Clamp Voltage (IGN, FLASHER, LIMP, STOP, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_POS}				V
I = 1.0 mA		7.5	–	13	
Input Forward Voltage (IGN, FLASHER, LIMP, STOP, $\overline{CS}$, SCLK, SI, $\overline{RST}$)	V_{CL_NEG}				V
I = 1.0 mA		-2.0	–	-0.3	
Input Passive Pull-up Resistance on $\overline{CS}$ pin[8]	R_{UP}	100	200	400	kΩ
Input Passive Pull-down Resistance on SI, SCLK, FLASHER, IGN, FOG, CLOCK, LIMP and $\overline{RST}$ pins[8]	R_{DWN}	100	200	500	kΩ
SO High-state Output Voltage	V_{SOH}				V_{CC}
I_{OH} = 1.0 mA		0.8	0.95	–	
CLOCK Output Voltage reporting wake-up event (I_{CLOCK}=1.0 mA)	V_{CLOCKH}	0.8	0.95	–	V_{CC}

Notes

6. In extended mode, the functionality is guaranteed but not the electrical parameters.
7. Valid for $\overline{RST}$, SI, SCLK, CLOCK, FLASHER, STOP, and LIMP pins.
8. Valid for the following input voltage range: VCC = -0.3 to +0.3 V.
9. Please refer to Loss of VBAT section for more details.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, $\overline{RST}$, LIMP, STOP) (CONTINUED)					
SO Low-state Output Voltage I_{OL} = -1.6 mA	V_{SOL}	– 	0.2 	0.4 	V
SO Tri-state Leakage Current $\overline{CS}$ ≥ 0.7 V_{CC}	I_{SOLEAK}	-1.0 	0.0 	1.0 	µA
CSNS Tri-state Leakage Current VCC = 5.5 V, CSNS = 4.5 V VCC = 5.0 V, CSNS = 5.5 V VCC = 5.0 V, CSNS = 3.0 V	$I_{CSNSLEAK}$	 -5.0 -10 -1.0	 0.0 0.0 0.0	 1.0 1.0 1.0	µA
Current Sense Output Clamp Voltage I_{CSNS} < 10.0 mA	V_{CSNS}	5.0 	6.0 	7.0 	V
OUTPUT (OUT 1:5)					
Output Leakage Current in OFF state Sleep mode, Outputs Grounded Normal mode, Outputs Grounded	$I_{OUTLEAK}$	 – –	 0 20	 2.0 25	µA
Output Negative Clamp Voltage I_{OUT} = -500 mA, Outputs OFF	V_{OUT}	 -22	 –	 -16	V
Current Sense Output Precision[10] Full-Scale Range (FSR) for LED Control bit = 0 0.75 FSR 0.50 FSR 0.25 FSR 0.10 FSR Full-Scale Range (FSR) for LED Control bit = 1 0.187 FSR = 0.75 FSR_{LED} 0.125 FSR = 0.50 FSR_{LED} 0.062 FSR = 0.25 FSR_{LED} 0.025 FSR = 0.10 FSR_{LED}	$\delta I_{CS}/I_{CS}$	 -14 -15 -17 -22 -13 -13 -20 -30	 - - - - - - - -	 14 15 17 22 13 13 20 30	%
Current Sense Output Precision Over-temperature Range [-40;125 °C], V_{BAT} Range [10 V-16 V] and FSR Range [25%-100%], calculated with one calibration point (Taken at 25 °C, VBAT = 13.5 V and 50% FSR)[12]		-6.0	-	6.0	%
Current Sense Output Precision with one calibration point (50% FSR_{LED}, V_{BAT} = 13.5 at 25 °C[12]		-6.0	–	6.0	%
Temperature Drift of Current Sense Output[11] V_{BAT} = 13.5 V, I_{OUT} = 2.8 A reference taken at T_A = 25 °C	$\Delta I_{CS}/\Delta T$	 –	 ±280	 ±400	ppm/ °C

Notes

10. 10 V < V_{BAT} < 16 V. ($\delta I_{CS}/I_{CS}$ = (measured I_{CS}- targeted I_{CS})/ targeted I_{CS} with targeted I_{CS} = 5.0 mA
11. Based on statistical data. Not production tested. $\Delta I_{CS}/\Delta T$ = [(measured at I_{CS} at T_1 - measured at I_{CS} at T_2) measured at I_{CS} at room]/ (T_1 - T_2)
12. Based on statistical analysis covering 99.74% of parts.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT (OUT 1:5) (CONTINUED)					
Minimum Output Current Reported in CSNS for OUT[1-5][13] 10 V ≤ VBAT ≤ 16 V	$I_{35MIN(CSNS)}$	65	–	–	mA
Minimum Output Current Reported in CSNS for OUT[1-5] in LED Mode[13] 10 V ≤ VBAT ≤ 16 V	$I_{35MIN(CSNS)\ LED}$	40	–	–	mA
Over-temperature Shutdown	T_{OTS}	155	175	195	°C
Thermal Prewarning[14]	$T_{OTSWARN}$	110	125	140	°C
Output Voltage Threshold	V_{OUT_TH}	0.475	0.5	0.525	V_{BAT}
TAIL LIGHT (OUT1)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[14]	$R_{DS(ON)}$	–	–	59.5	mΩ
Reverse Output ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[15]	$R_{SD(ON)}$	–	–	70	mΩ
TAIL LIGHT (OUT1)					
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[16]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[17] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	4.0	10	20	mA
Current Sense Full-scale Range[18]	$I_{CS\ FSR}$	–	6.0	–	A

Notes
13. Output current value computed after leakage current removal (open load condition)
14. Parameter guaranteed by design; however it is not production tested.
15. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
16. OLLED1, bit D0 in SI data is set to [0]
17. OLLED1, bit D0 in SI data is set to [1]
18. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TAIL LIGHT (OUT1) (CONTINUED)					
Current Sense Full-scale Range [19] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range [19]	$R_{SC1(OUT1)}$	350	–	–	mΩ
LICENSE LIGHT (OUT2)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -13.5 V, T_A = 25 °C)[20]	$R_{DS(ON)}$	–	–	59.5	mΩ
Reverse Output ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 12 V, T_A = 150 °C)[21]	$R_{SD(ON)}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[22]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[23] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 4.0	 10	 20	mA
Current Sense Full-Scale Range[24]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-Scale Range[20] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe short-circuit impedance range[20]	$R_{SC1(OUT2)}$	350	–	–	mΩ

Notes
19. Output current value computed after leakage current removal (open load condition)
20. Parameter guaranteed by design; however, it is not production tested.
21. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
22. OLLED2, bit D0 in SI data is set to [0]
23. OLLED2, bit D0 in SI data is set to [1]
24. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TAIL LIGHT (OUT3)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)[25]	$R_{DS(ON)150}$	–	–	59.5	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)[26]	$R_{SD(ON)25}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over Current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State[27]	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED[28] V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 4.0	 10	 20	mA
Current Sense Full-scale Range[29]	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range[25] depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe short-circuit impedance range[25]	$R_{SC1(OUT3)}$	350	–	–	mΩ

Notes
25. Parameter guaranteed by design; however, it is not production tested.
26. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
27. OLLED3, bit D2 in SI data is set to [0]
28. OLLED3, bit D2 in SI data is set to [1]
29. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STOP LIGHT (OUT4)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)(30)	$R_{DS(ON)150}$	–	–	59.5	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)(31)	$R_{DS(ON)25}$	–	–	70	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State(32)	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED(33) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 4.0	 10	 20	mA
Current Sense Full-scale Range(34)	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range(30) depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range(30)	$R_{SC1(OUT4)}$	350			mΩ

Notes
30. Parameter guaranteed by design; however, it is not production tested.
31. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
32. OLLED3, bit D2 in SI data is set to [0]
33. OLLED3, bit D2 in SI data is set to [1]
34. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FLASHER (OUT5)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25 °C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150 °C)(35)	$R_{DS(ON)150}$	–	–	59.5	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, V_{BAT} = -12 V, T_A = 25 °C)(36)	$R_{SD(ON)25}$	–	–	70	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} =1.5 A, T_A = 25 °C) for LED Control = 1 V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25\_LED}$	 – –	 – –	 70 110	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 1.5 A, V_{BAT} = 13.5 V, T_A = 150 °C) for LED Control = 1	$R_{DS(ON)150\_LED}$	–	–	119	mΩ
High Over-current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40 °C V_{BAT} = 16 V, T_A = 25 °C V_{BAT} = 16 V, T_A = 125 °C	I_{OCHI1}	28.0 30.2 29.4 28.3	35.0 36.0 35.0 33.8	43.5 41.8 40.6 39.3	A
High Over-current Shutdown Threshold 2	I_{OCHI2}	12.3	15.4	18.5	A
Low Over-current Shutdown Threshold	I_{OCLO}	5.7	7.2	8.9	A
Open Load Current Threshold in ON State(37)	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED(38) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 4.0	 10	 20	mA
Current Sense Full-scale Range(39)	$I_{CS\ FSR}$	–	6.0	–	A
Current Sense Full-scale Range(35) depending on LED Control = 1	$I_{CS\ FSR\_LED}$	–	1.6	–	A
Severe Short-circuit Impedance Range(35)	$R_{SC1(OUT5)}$	350	–	–	mΩ

Notes

35. Parameter guaranteed by design; however, it is not production tested.
36. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
37. OLLED3, bit D2 in SI data is set to [0]
38. OLLED3, bit D2 in SI data is set to [1]
39. For a typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is not guaranteed.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 3.0 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPARE (FETOUT, FETIN)					
FETOUT Output High Level at I = 1.0 mA	$V_{H\ MAX}$	0.8	–	–	V_{CC}
FETOUT Output Low Level at I = 1.0 mA	$V_{H\ MIN}$	–	0.2	0.4	V
FETIN Input Full Scale Range Current	I_{FETIN}	–	5.0	–	mA
FETIN Input Clamp Voltage	V_{CLIN}	5.3	–	7.0	V
Drop Voltage between FETIN and CSNS for MUX[2:0] = 110 I_{FETIN} = 5 mA, 5.5 V > CSNS > 0.0 V	V_{DRIN}	0.0	–	0.4	V
FETIN Leakage Current when external current switch sense is enabled 4.5 V > V_{FETIN} > 0 V, 5.5 V > VCC > 4.5 V, CSNS open 3.0 V > V_{FETIN} > 0 V, 4.5 V > VCC > 0, CSNS open	$I_{FETINLEAK}$	 -1.0 -1.0	 – –	 5.0 1.0	µA
TEMPERATURE OF GND FLAG					
Analog Temperature Feedback at T_A = 25 °C with 5.0 kΩ > R_{CSNS} > 500 Ω	V_{T_FEED}	920	1025	1140	mV
Analog Temperature Feedback Derating with 5.0 kΩ > R_{CSNS} > 500 Ω[40]	V_{DT_FEED}	10.9	11.3	11.7	mV/ °C
Analog Temperature Feedback Precision[40]	V_{DT_ACC}	-15	–	15	°C
Analog Temperature Feedback Precision with calibration point at 25 °C[40]	$V_{DT\_ACC\_CAL}$	-5.0	–	5.0	°C

Notes

40. Parameter guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS TIMING (OUT1:5)					
Current Sense Valid Time on resistive load only(41) SR bit = 0 SR bit = 1	$t_{CSNS(VAL)}$	 – –	 90 45	 150 75	µs
Current Sense Synchronization Time on FETOUT SR bit = 0 SR bit = 1	$t_{CSNS(SYNC)}$	 – –	 130 70	 185 110	µs
Current Sense Settling Time on resistive load only(41)	$t_{CSNS(SET)}$	–	10	30	µs
Driver Output Positive Slew Rate (30% to 70% at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	SR_R	 0.10 0.20	 0.25 0.40	 0.56 0.80	V/µs
Driver Output Negative Slew Rate (70% to 30% at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	SR_F	 0.10 0.20	 0.25 0.40	 0.56 0.80	V/µs
Driver Output Matching Slew Rate (SR_R/SR_F)(70% to 30% at V_{BAT} = 14 V at 25 °C)	ΔSR	0.8	1.0	1.2	
Driver Output Turn-ON Delay (SPI ON Command [No PWM, $\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	t_{DLYON}	 50 25	 – –	 120 65	µs
Driver Output Turn-OFF Delay (SPI OFF command [$\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} at V_{BAT} = 14 V) SR bit = 0, I_{OUT} = 2.8 A SR bit = 1, I_{OUT} = 0.7 A	t_{DLYOFF}	 50 25	 – –	 120 65	µs
Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) at Output = 50% V_{BAT} with V_{BAT} = 14 V, f_{PWM} = 240 Hz, δ_{PWM} = 50%, at 25 °C SR bit = 0, I_{OUT} = 2.8 A for OUT1/2/3/4/5 SR bit = 1, I_{OUT} = 0.7 A for OUT1/2/3/4/5	Δt_{RF}	 -40 -23	 – –	 20 7.0	µs

Notes
41. Not production tested.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PWM MODULE					
Nominal PWM Frequency Range(44)	f_{PWM}	30	–	400	Hz
Clock Input Frequency Range	f_{CLK}	7.68	–	51.2	kHz
Output PWM Duty Cycle maximum range for 11 V<V_{BAT}<18 V(42), (44)	PWM_MAX	4.0	–	96	%
Output PWM Duty Cycle linear range for 11 V<V_{BAT}<18 V(43), (44)	PWM_LIN	5.5	–	96	%
Output PWM Duty Cycle range for full diagnostic for 11 V<VBAT<18 V(45) 200 Hz Output PWM frequency 400 Hz Output PWM frequency	PWM_DIAG	 5.5 11	 – –	 96 90	%
WATCHDOG TIMING					
Watchdog Timeout (SPI Failure)	t_{WDTO}	50	75	100	ms
I/O PLAUSIBILITY CHECK TIMING					
Fault Shutdown Delay Time (from Over-temperature or OCHI1 or OHCI2 or OCLO Fault Detection to Output = 50% V_{BAT} without round shaping feature for turn off)	t_{SD}	–	7.0	30	µs
Under-voltage Deglitch Time(46)	t_{UV}	0.8	1.25	2.0	µs
High Over-current Threshold Time 1	t_1	7.0	10	13.5	ms
High Over-current Threshold Time 2	t_2	52.5	75	97.5	ms
Autorestart Period	$t_{AUTORST}$	52.5	75	97.5	ms
Autorestart Over-current Shutdown Delay Time	t_{OCSH_AUTO}	3.5	5.0	6.5	ms
Limp Home Input pin Deglicher Time	t_{LIMP}	7.0	10.0	13.0	ms
Cyclic Open Load Detection Timing with LED(47)	t_{OLLED}	105	150	195	ms
Flasher Toggle Timeout	$t_{FLASHER}$	1.4	2.3	3.0	s
Ignition Toggle Timeout	$t_{IGNITION}$	1.4	2.3	3.0	s
Stop Toggle Timeout	t_{STOP}	1.4	2.3	3.0	s
Clock Input Low Frequency Detection Range	$f_{LCLK\ DET}$	1.0	2.0	4.0	kHz
Clock Input High Frequency Detection Range	$f_{HCLK\ DET}$	100	200	400	kHz

Notes

42. The PWM ratio is measured at V_{OUT} = 50% of V_{BAT} in nominal range of frequency. It is possible to put the device fully on (PWM duty cycle = 100%) and fully off (PWN duty cycle = 0%). Between 4%-96%, $OCLO_{1,2}$, OCLO and open load are available in ON state. See Input Timing Switching Characteristics on page 18.
43. Linear range is defined by output duty cycle to SPI duty cycle configuration +/- LSB. For values outside the linear duty cycle range, a calibration curve is available.
44. Not production tested.
45. Full diagnostic corresponds to the availability of the following features: output current sensing, output status and openload detection. Not production tested.
46. This time is measured from the $V_{BAT(UV)}$ level to the fault reporting. Parameter guaranteed in testmode.
47. OLLEDn bit (where “n” corresponds to respective outputs 1 through 5) in SI data is set to logic [1]. Refer to Table 9. Serial Input Address and Configuration Bit Map.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 20 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time)(48)	$t_{\overline{CS}}$	–	–	1.0	us
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)(48)	t_{LEAD}	–	–	500	ns
Required High State Duration of SCLK (Required Setup Time)(48)	t_{WSCLKH}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time)(48)	t_{WSCLKI}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)(48)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time)(49)	t_{SISU}	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time)(49)	t_{SIHOLD}	–	25	83	ns
SO Rise Time C_L = 80 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 80 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time(50)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time(50)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance(51)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance(52)	$t_{SO(DIS)}$	–	65	145	ns

Notes

48. Maximum setup time required for the 35XS3500 is the minimum guaranteed time needed from the microcontroller.
49. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
50. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
51. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
52. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

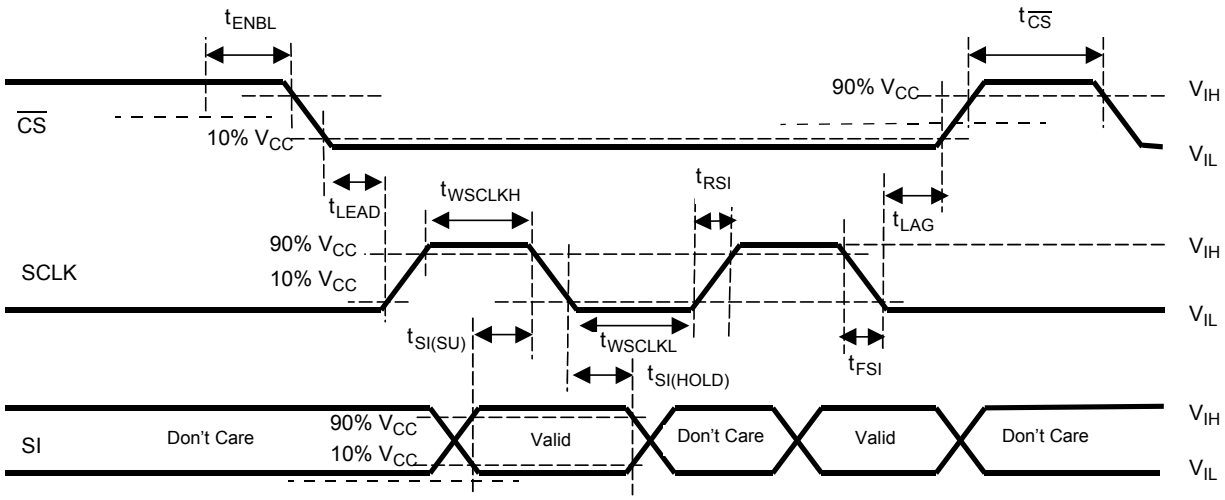


Figure 4. Input Timing Switching Characteristics

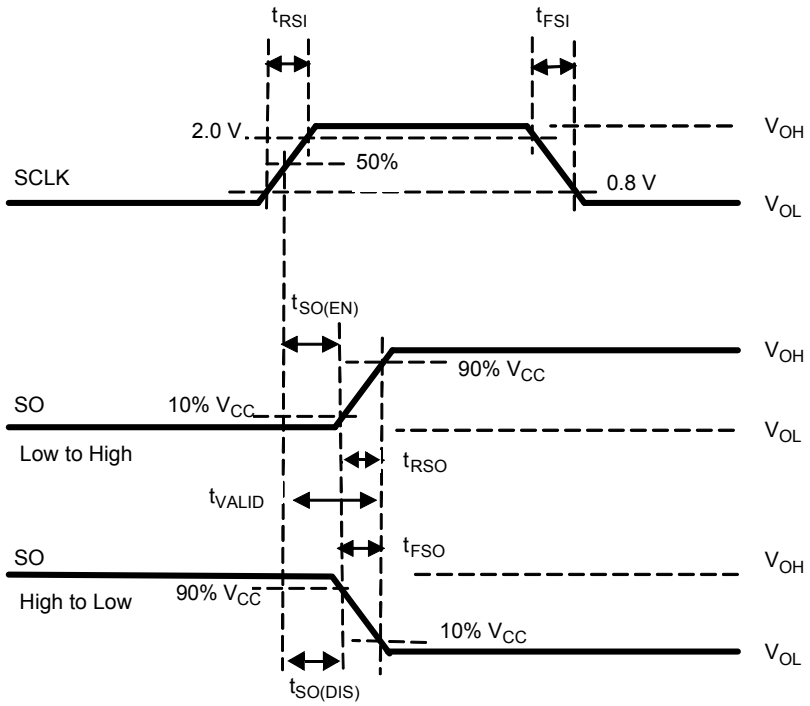


Figure 5. SCLK Waveform and Valid SO Data Delay Time

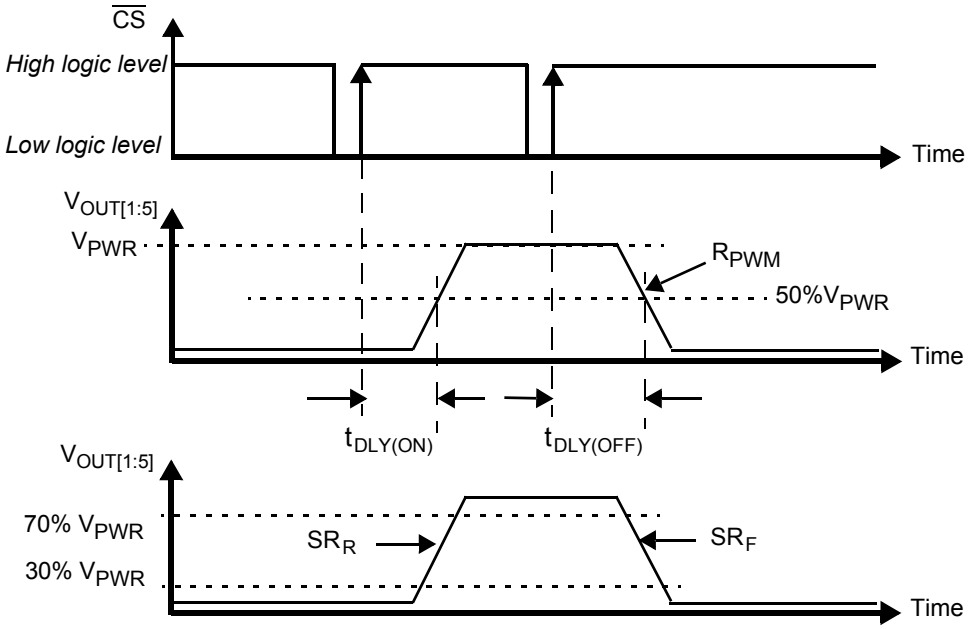


Figure 6. Output Slew Rate and Time Delays

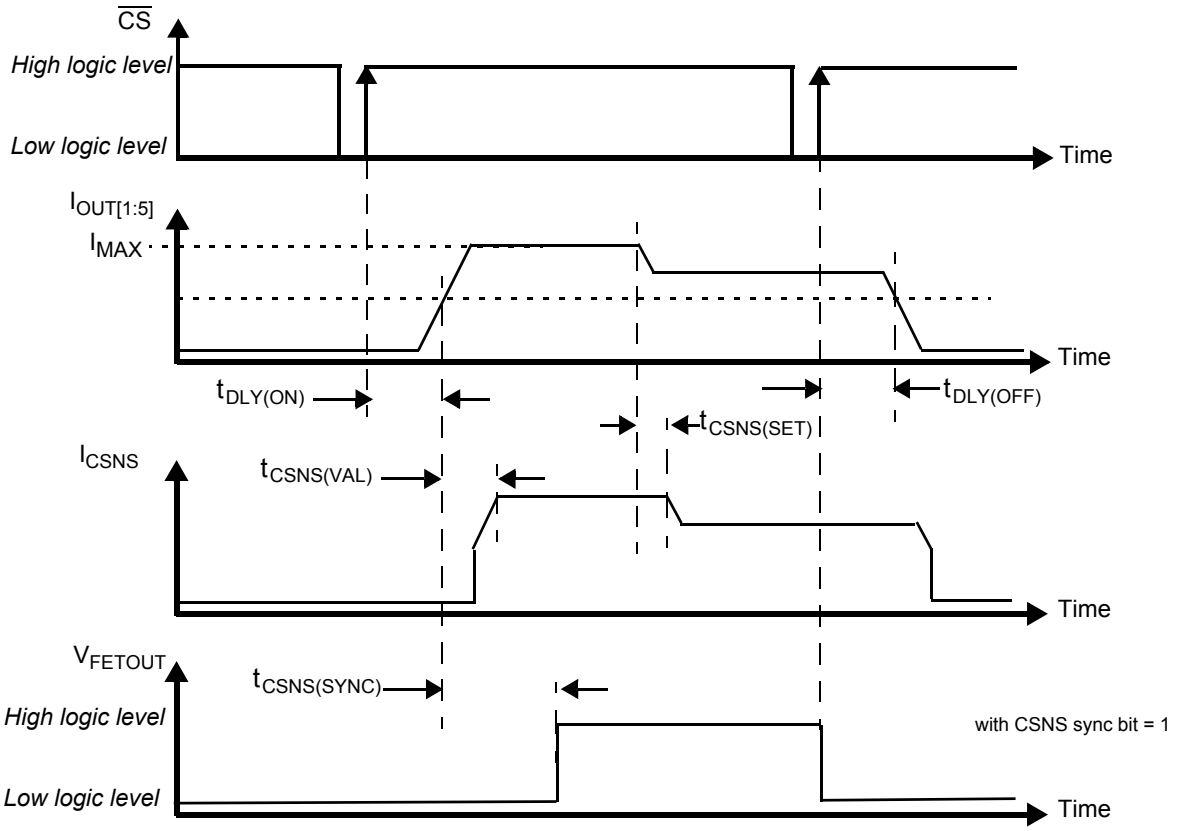


Figure 7. Current Sensing Time Delays

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 35XS3500 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (five 35 mΩ) can control the high sides of five separate resistive loads (bulbs). Programming, control, and diagnostics are accomplished using a 16-bit SPI interface.

FUNCTIONAL PIN DESCRIPTION

Supply Voltage (VBAT)

The VBAT pin of the 35XS3500 is the power supply of the device. In addition to its supply function, this tab contributes to the thermal behavior of the device by conducting the heat from the switching MOSFETs to the printed circuit board.

Supply Voltage (VCC)

This is an external voltage input pin used to supply the SPI digital portion of the circuit and the gate driver of the external SMART MOSFET.

Ground (GND)

This pin is the ground of the device.

Clock Input (CLOCK) and PWM Module

When the part is in Normal Mode ($\overline{RST}$=1), the PWM frequency and timing are generated from the rising edge of clock input by the PWM module. The clock input frequency is the selectable factor 2^7 = 128 or 2^8 = 256 of the PWM frequency per output, depending PR bit value.

The OUT1:6 can be controlled in the range of 4% to 96% with a resolution of 7 bits of duty cycle (bits D[6:0]).

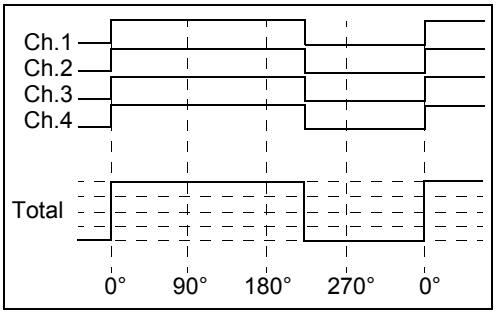
The following table describes the PWM resolution.

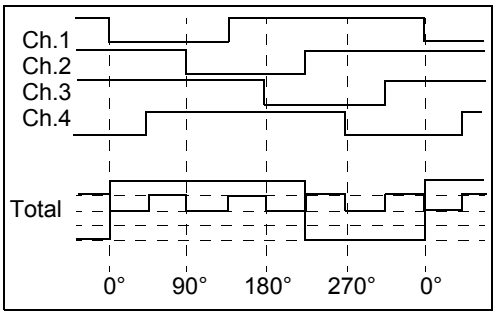
On/Off (Bit D7)	Duty cycle (7 bits resolution)	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	1111111	fully ON

Table 6. PWM Resolution

The timing includes four programmable PWM switching phases (0°, 90°, 180°, and 270°) to improve overall EMC behavior of the light module.

The amplitude of the input current is divided by four while the frequency is four times the original one. The two following pictures illustrate the behavior.





The synchronization of the switching phases between different corner light IC is provided by a SPI command in combination with the $\overline{CS}$ input. The bit in the SPI is called PWM sync (initialization register).

In Normal mode, No PWM feature (100% duty cycle) is provided in the following instances:

- with the following SPI configuration: D7:D0=FF.
- In case of clock input signal failure (out of f_{PWM}), the outputs state depends on the D7 bit value (D7=1+ON) in Normal mode.

In Fail mode. The outputs state depends on the IGN, STOP and Flasher pins.

If $\overline{RST}$=0, this pin reports the wake-up event for wake=1 when VBAT and VCC are in operational voltage range.

Limp Home (LIMP)

The Limp Home mode of the component can be activated by this digital input port. The signal is “high active”, meaning the Fail mode can be activated by a logic high signal at the input.

Ignition Input (IGN)

The Ignition input wakes the device. It also controls the Fail Home mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

Flasher Input (FLASHER)

The Flasher input wakes the device. It also controls the Fail mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

Reset Input ($\overline{\text{RST}}$)

This input wakes the device when the $\overline{\text{RST}}$ pin is at logic [1]. It is also used to initialize the device configuration and the SPI fault registers when the signal is low. All SI/SO registers described in Table 9 and Table are reset. The fault management is not affected by $\overline{\text{RST}}$ (see Figure 2).

Current Sense Output (CSNS)

The current sense output pin is an analog current output or a voltage proportional to the temperature on the GND flag. The routing to the common resistor is SPI programmable.

This current sense monitoring may be synchronized in case of the OUT6 is not used. So, the current sense monitoring can be synchronized with a rising edge on the FETOUT pin ($t_{CSNS(SYNC)}$) if CSNS sync SPI bit is set to logic [1]. Connection of the FETOUT pin to a MCU input pin allows the MCU to sample the CSNS pin during a valid time-slot. Since this falling edge is generated at the end of this timeslot, upon a switch-off command, this feature may be used to implement maximum current control.

Charge Pump (CP)

An external capacitor is connected between this pin and the VBAT pin. It is used as a tank for the internal charge pump. Its typical value is 100 nF ±20%, 25 V maximum.

FETOUT Output (FETOUT)

This output pin is used to control an external MOSFET (OUT6).

The high level of the FETOUT Output is VCC if V_{BAT} and V_{CC} are available in case of FETOUT is controlled ON.

FETOUT is not protected in case of a short-circuit or under-voltage on V_{BAT}.

In case of a reverse battery, OUT6 is OFF.

FETIN Input (FETIN)

This input pin gives the current recopy of the external MOSFET. It can be routed on the CSNS output by a SPI command.

SPI Protocol Description

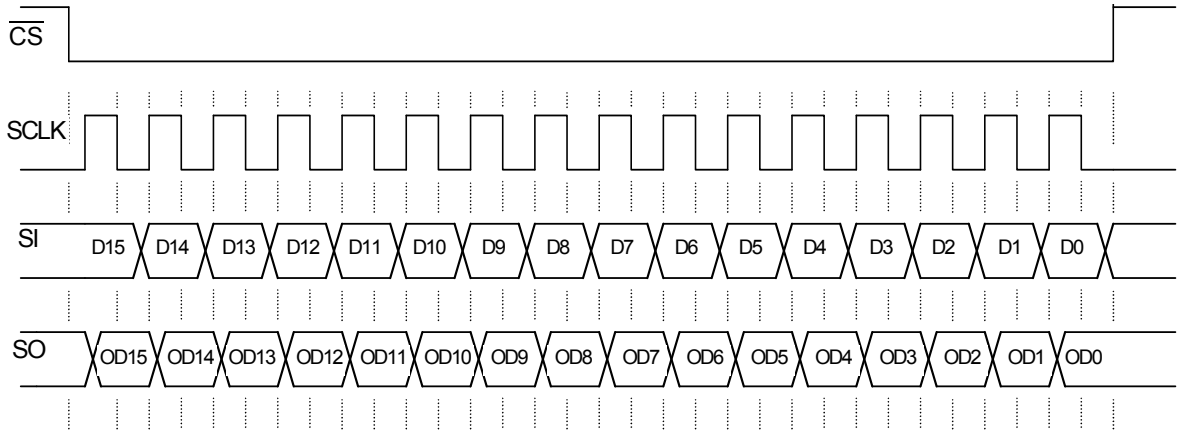
The SPI interface has a full-duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{\text{CS}}$).

The SI/SO pins of the 35XS3500 device follow a first-in, first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels supplied by V_{CC}.

The SPI lines perform the following functions:

Serial Clock (SCLK)

The SCLK pin clocks the internal shift registers of the 35XS3500 device. The SI pin accepts data into the input shift register on the falling edge of the SCLK signal, while the SO pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic low state whenever $\overline{\text{CS}}$ makes any transition. For this reason, it is recommended that the SCLK pin be in a logic [0] whenever the device is not accessed ($\overline{\text{CS}}$ logic [1] state). SCLK has a passive pull-down, R_{DWN}. When $\overline{\text{CS}}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 8).



Notes
1. D15:D0 relate to the most recent ordered entry of data into the device.
2. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 8. Single 16-Bit Word SPI Communication

Serial Input (SI)

The SI pin is a serial interface command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 to D0. SI has a passive pull-down, R_{DOWN}.

Serial Output (SO)

The SO data pin is a tri-state output from the shift register. The SO pin remains in a high-impedance state until the $\overline{CS}$ pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin enables communication with the master device. When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the master device. The 35XS3500 device latches in data from the Input Shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has a passive pull-up, R_{UP}.

STOP Input (STOP)

The STOP input wakes the device. It also controls the Fail mode activation. The signal is “high active“, meaning the component is active in case of a logic high at the input.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

Sleep Mode

The Sleep mode is the default mode of the 35XS3500. This is the state of the device after first applying battery voltage (V_{BAT}) and prior to any I/O transitions. This is also the state of the device when IGN, $\overline{RST}$, FLASHER, and STOP are logic [0]. In the Sleep mode, the output and all internal circuitry are OFF to minimize current draw. In addition, all SPI-configurable features of the device are reset. The 35XS3500 will transit to two modes (Normal and Fail) depending on wake and fail signals (see Table 18).

The transition to the other modes is according to the following signals:

- Wake = IGN or IGN_ON or FLASHER or FLASHER_ON or STOP or STOP_ON or $\overline{RST}$
- Fail = VCC fail or SPI fail or External limp

Normal Mode

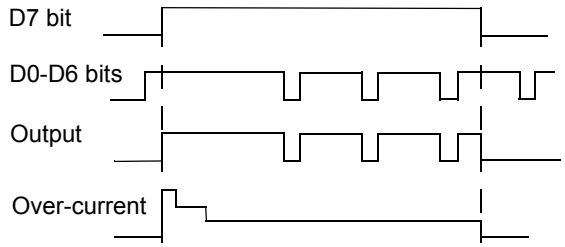
The 35XS3500 is in Normal mode when:

- Wake = 1
- Fail = 0

In Normal operating mode the power outputs are under full control of the SPI as follows:

- The outputs 1 to 6, including multiphase timing, and selectable slew-rate, are controlled by the programmable PWM module.
- The output 4 is activated directly by the STOP external pin in case the STOP_en bit is set to a logic [1].
- The outputs 1 to 5 are switched OFF in case of under-voltage on VBAT.
- The outputs 1 to 5 are protected by the selectable over-current double window and over-temperature shutdown circuit.
- The digital diagnosis feature transfers status of the smart outputs via the SPI.
- The analog current sense output (current recopy feature) can be rerouted by the SPI.
- The outputs can be configured to control LED loads: $R_{DS(ON)}$ is increased by a factor of 2 and the current recopy ratio is scaled by a factor of 4.
- The SPI reports NM=1 in this mode.

The following figure describes the PWM, outputs and over-current behavior in Normal mode.



Fail Mode

The 35XS3500 is in Fail mode when:

- Wake = 1
- Fail = 1

In Fail mode:

- The outputs are under control of the external pins (see Table 6).
- The outputs are fully protected in case of overload, over-temperature and under-voltage (on B_{VAT} or on V_{CC}).
- The SPI reports continuously the content of address 11, disregard to previous requested output data word.
- Neither digital diagnosis feature (SPI) nor analog current sense are available.
- In case of overload (OCHI2 or OCLO) conditions or under-voltage on VBAT, the outputs are under control of the autorestart feature.
- In case of a serious overload condition (OCHI1 or OT) the corresponding output is latched OFF until a new wake-up event (wake = 0 then 1)

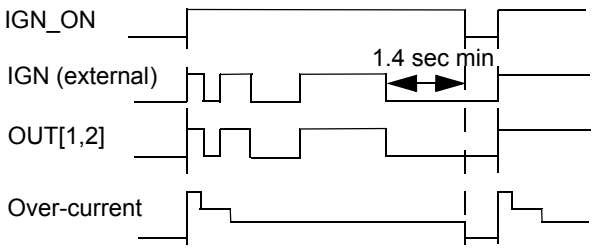


Table 7. Limp Home Output State

Output 1 Tail Light	Output 2 License Light	Output 3 Rear Drive Light	Output 4 Stop Light	Output 5 Flasher	External Switch Rear Fog Light
IGN Pin	OFF	OFF	STOP Pin	FLASHER Pin	OFF

Autorestart Strategy

The autorestart circuitry is used to supervise the outputs and reactivate high side switches in case of overload or under-voltage failure conditions, and provide a high availability of the outputs.

This autorestart is available in Fail mode when no supervising intelligence of the microcontroller is available. Autorestart is activated in case of an overload condition (OCHI2 or OCLO) or under-voltage condition on VBAT (Table 9, Over-current window in case of Autorestart).

The autorestart switches ON the outputs. During the ON state of the switch OCHI1, the window is enabled for tochi_Auto, then after the output is protected by OCLO.

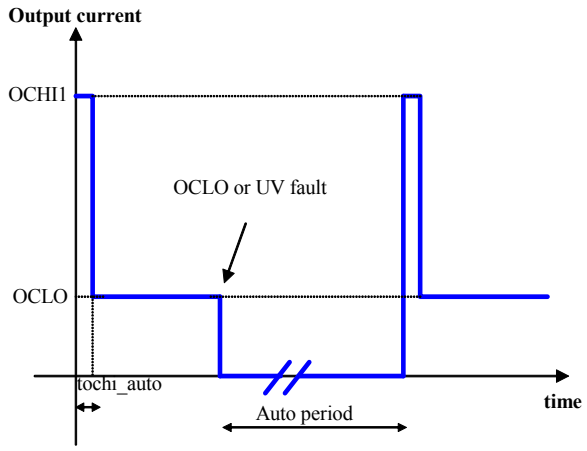


Figure 9. Over-current window in case of Autorestart

In case of OCHI1 or OT, the switch is latched OFF until wake up (wake=0, then 1).

In case of OCLO or under-voltage, the output switch is OFF. After the autorestart period (75 ms) is turned ON again.

In case an under-voltage occurred in Fail mode, it will be latched and delatched after the auto restart period ($t_{AUTORST}$).

The Autorestart is not limited in time.

Transition Fail to Normal Mode

To leave the Fail mode, the fail condition must be removed (fail=0). The microcontroller has to toggle the SPI D10 bit (0 to 1) to reset to the watchdog bit; the other bits are not considered. The previous latched faults are reset by the transition into Normal mode.

Transition Normal to Fail Mode

To leave the Normal mode, a fail condition must occur (fail=1). The previous latched faults are reset by the transition into Fail mode.

If the SI is shorted to VCC, the device transmits to Fail Safe mode until the WD bit toggles through the SPI (from [0] to [1]).

All settings are according to predefined values (all bits set to logic [0]).

START-UP SEQUENCE

The 35XS3500 enters into Normal mode after start-up if the following sequence is provided:

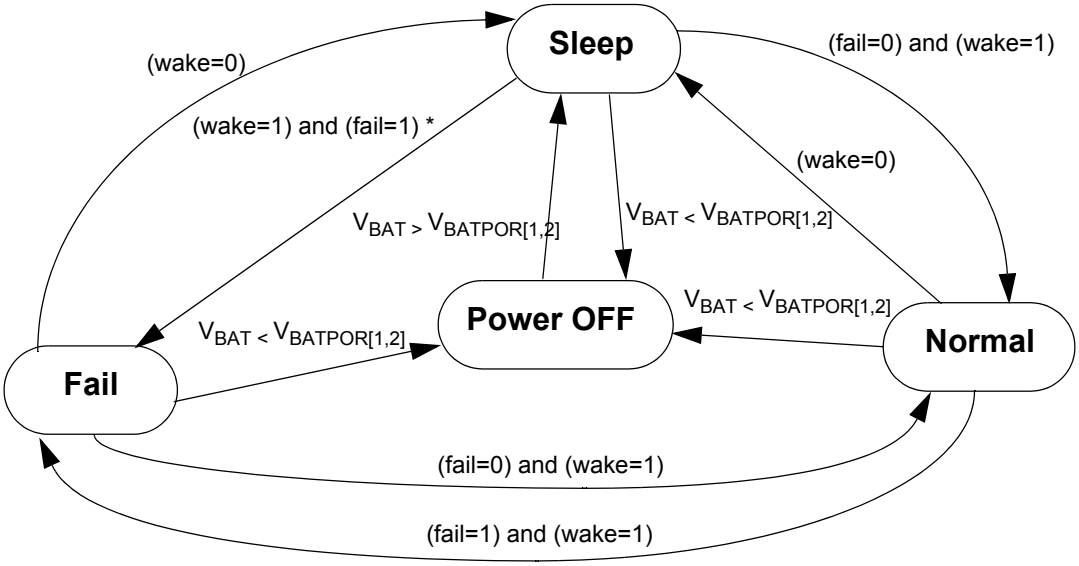
- V_{BAT} and V_{CC} power supplies must be above their under-voltage thresholds (Sleep mode).
- Generate a wake-up event (wake=1) from 0 to 1 on $\overline{RST}$. The device switches to Normal mode.
- Apply the PWM clock after a maximum of 200 µs (min. 50 µs).
- Send a SPI command to the device status register to clear the clock fail flag and enable the PWM module to start.

If the correct startup sequence is not provided, the PWM function is not guaranteed.

Figure 10 describes the wake-up block diagram.

POWER OFF MODE

The 35XS3500 is in Power OFF mode when the battery voltage is below $V_{BATPOR[1,2]}$ thresholds. For more details, please refer to Loss of VBAT paragraph.



Notes:
* only available in case of V_{CC} fail condition
wake=($\overline{RST}$=1) OR (IGN_ON=1) OR (Flasher_ON=1) OR (Stop_ON=1)
fail=(V_{CC}_fail=1) OR (SPI_fail=1) OR (ext_limp=1)

Figure 10. Operating Modes State Machine

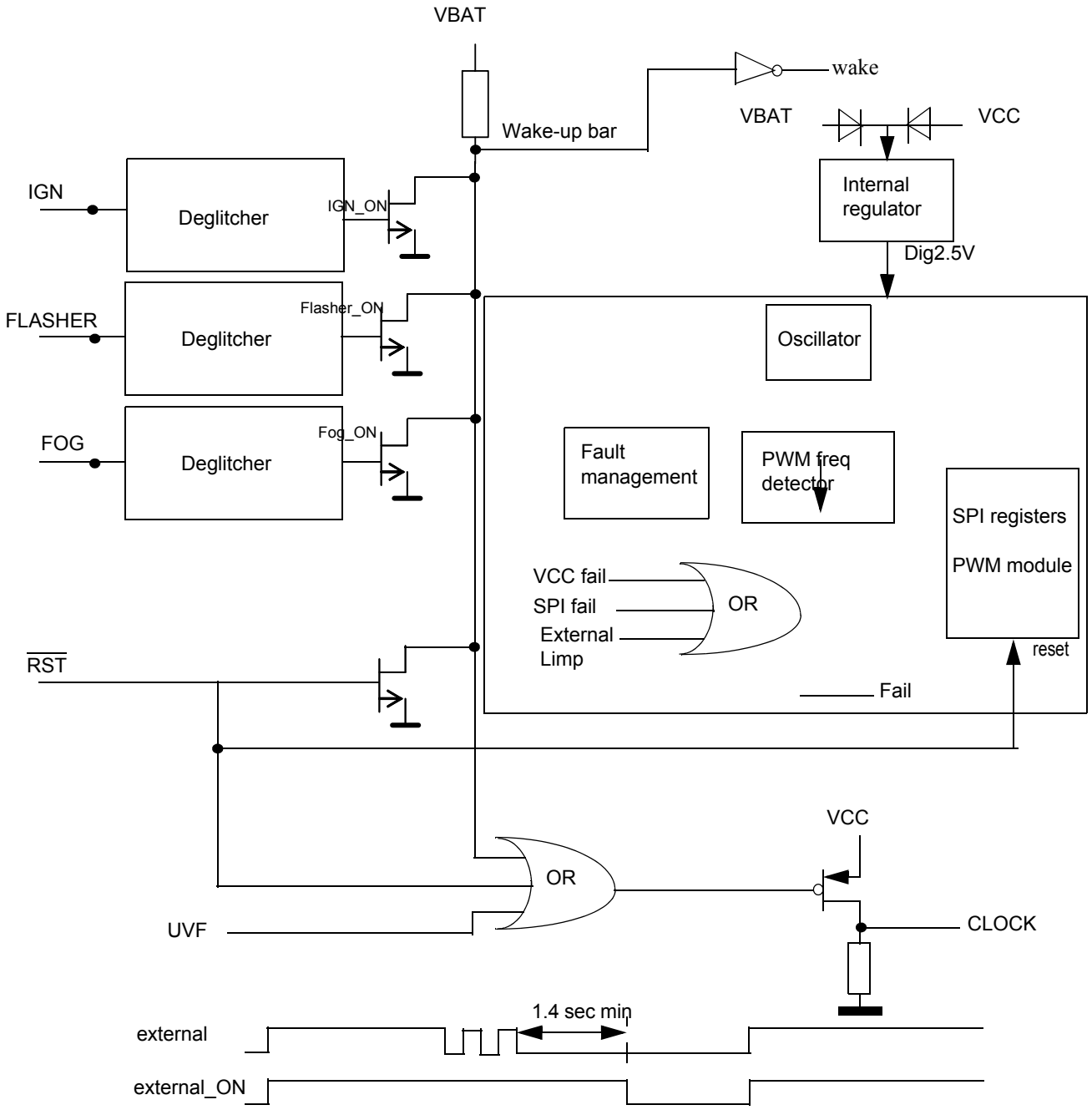


Figure 11. Wake-up Block Diagram

LOGIC COMMANDS AND REGISTERS

Serial Input Communication

SPI communication compliant to 3.3 and 5.0 V is accomplished using 16-bit messages. A message is transmitted by the master starting with the MSB, D15, and ending with the LSB, D0. Each incoming command message on the SI pin can be interpreted using the bit assignment described in Table 8. The 5 bits D15:D11, called register address bits, are used to select the command register. Bit D10 is the watchdog bit. The remaining 10 bits, D9:D0, are used to configure and control the output and its protection features. Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

All SPI registers are reset (all bits equal 0) in case of $\overline{\text{RST}}$ equals 0 or fail mode (Fail=1).

Table 8. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15:D11	Register address bits.
	D10	Watchdog in: toggled to satisfy watchdog requirements.
LSB	D9:D0	Used to configure inputs, outputs, device protection features, and SO status content.

Device Register Addressing

The register addresses (D15:D11) and the impact of the serial input registers on device operation are described in this section. Table 9 summarizes the content of the SI registers.

Table 9. Serial Input Address and Configuration Bit Map

SI Register	SI Address					SI Data										
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialization	0	0	0	0	0	WD	0	0	STOPen	PWM sync	0	MUX2	MUX1	MUX0	SOA1	SOA0
Config OL	0	0	0	0	1	WD	LED Control5	LED Control4	LED Control3	LED Control 2	LED Control 1	OLLED5	OLLED4	OLLED3	OLLED2	OLLED1
Config Prescaler	0	0	0	1	0	WD	0	PR1	PR2	PR3	0	0	0	PR4	PR5	PR6
Config SR	0	0	0	1	0	WD	1	SR1	SR2	SR3	0	0	0	SR4	SR5	0
Config CSNS	0	0	0	1	1	WD	CSNS sync	0	0	0	0	NO_OC HI5	NO_OC HI4	NO_OC HI3	NO_OC HI2	NO_OC HI1
Control OUT1	0	1	0	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT2	0	1	0	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT3	0	1	0	1	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT4	0	1	1	0	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT5	0	1	1	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control External Switch	0	1	1	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0

Table 9. Serial Input Address and Configuration Bit Map

RESET	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Note: testmode address used only by FSL is D[15:11]=01111 with $\overline{RST}$ voltage higher than 8.0 V typ.

ADDRESS 00000—Initialization

The Initialization register is used to read the various statuses, choose one of the six outputs current recopy, enable the STOP pin, and synchronize the switching phases between different corner light devices. The register bits D1 and D0 determine the content of the 16 bits of SO data. (Refer to the section entitled Serial Output Communication (Device Status Return Data)) Bits D9:D2 are described in Table .

The watchdog timeout is specified by the t_{WDTO} parameter. As long as the WD bit (D10) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally. If an internal watchdog timeout occurs before the WD bit is toggled, the device will revert to Fail mode. All registers are cleared. To exit the Fail mode, send valid SPI communication with WD bit = 1.

Table 10. Initialization Register

SI Address					SI Data										
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	WD	0	0	STOPen	PWM sync	0	MUX2	MUX1	MUX0	SOA1	SOA0

x = Don't care
D6 (PWM sync) = 0, No synchronization
D6 (PWM sync) = 1, Synchronization on CSB positive edge
D7 (STOPen) = 0, STOP pin does not control the output 4.
D7 (STOPen) = 1, STOP pin controls the output 4.

D4, D3, D2 (MUX2, MUX1, MUX0) = 000, No current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 001, OUT1 current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 010,current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 011, OUT3 current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 100, OUT4 current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 101, OUT5 current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 110, External Switch current sense
D4, D3, D2 (MUX2, MUX1, MUX0) = 111, Temperature analog feedback

ADDRESS 00001—Configuration OL

The Configuration OL register is used to enable the open load detection for LEDs in Normal mode (OLLEDn in Table 9) and to active the LED Control.

When bit D0 is set to logic [1], the open load detection circuit for LED is activated for output 1. When bit D0 is set to logic [0], open load detection circuit for standard bulbs is activated for output 1.

When bit D5 is set to logic [1], the LED Control is activated for output 1.

ADDRESS 00010—CONFIGURATION PRESCALER AND SR

Two configuration registers are available at this address. The Configuration Prescaler when D9 bit is set to logic [0] and Configuration SR when D9 bit is set to logic [1].

The Configuration Prescaler register is used to enable the PWM clock prescaler per output. When the corresponding PR bit is set to logic [1], the clock prescaler (reference clock divided by 2) is activated for the dedicated output.

The SR Prescaler register is used to increase the output slew-rate by a factor of 2. When the corresponding SR bit is set to logic [1], the output switching time is divided by 2 for the dedicated output.

ADDRESS 00011—CONFIGURATION CSNS

The Configuration Current Sense register is used todisable the high over-current shutdown phase (OCHI1 and OCHI2 dynamic levels) in order to activate immediately the current sense analog feedback.

When bit D9 is set to logic [1], the current sense synchronization signal is reported on FETOUT output pin.

When the corresponding NO_OCHI bit is set to logic [1], the output is only protected with OCLO level. And the current sense is immediately available if it is selected through SPI, as described in Figures 13. The NO_OCHI bit per output is automatically reset at each corresponding ON off bit transition from logic [1] to [0] and in case of over-temperature or over-current fault. All NO_OCHI bits are also reset in case of under-voltage fault detection.

ADDRESS 01001—Control OUT1

Bits D9 and D8 control the switching phases as shown in Table 11.

Table 11. Switching Phases

D9:D8	PWM Phase
00	0°
01	90°
10	180°
11	270°

Bit D7 at logic [1] turns ON OUT1. OUT1 is turned OFF with bit D7 at logic [0]. This register allows the master to control the duty cycle and the switching phases of OUT1. The duty cycle resolution is given by bits D6:D0.

D7 = 0, D6:D0 = XX output OFF.

D7 = 1, D6:D0 = 00 output ON during 1/128.

D7 = 1, D6:D0 = 1 A output ON during 27/128 on PWM period.

D7 = 1, D6:D0 = 7 F output continuous ON (no PWM).

ADDRESS 01010—Control OUT2

Same description as OUT1.

ADDRESS 011111—Control OUT3

Same description as OUT1.

ADDRESS 01100—Control OUT4

Same description as OUT1.

ADDRESS 01101—Control OUT5

Same description as OUT1.

ADDRESS 01110—Control External Switch

Same description as OUT1.

ADDRESS 01111 —Test Mode

This register is reserved for test and is not available with the SPI during normal operation.

Serial Output Communication (Device Status Return Data)

When the $\overline{CS}$ pin is pulled low, the output register is loaded. Meanwhile, the data clocks out the MSB first as the new message data is clocked into the SI pin. The first 16 bits of data clocking out of the SO, and following a $\overline{CS}$ transition, is dependant upon the previously written SPI word (SOA1 and SOA0 defined in the last SPI initialization word).

Any bits clocked out of the SO pin after the first 16 will be representative of the initial message bits clocked into the SI pin, since the $\overline{CS}$ pin first transitioned to a logic [0]. This feature is useful for daisy chaining devices.

A valid message length is determined following a $\overline{CS}$ transition of logic [0] to logic [1]. If the message length is valid, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the Initialization-selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V, resulting in an under-voltage shutdown of the outputs, may result in incorrect data loaded into the SPI register, except the UVF fault reporting (OD13).

Serial Output Bit Assignment

The contents of bits OD15:OD0 depend on bits D1:D0 from the most recent initialization command SOA[1:0] (refer to Table 12), as explained in the paragraphs that follow.

The register bits are reset by a read operation and also if the fault is removed.

Table 12 summarizes the SO register content. Bit OD10 reflects Normal mode (NM).

Table 12. Serial Output Bit Map Description

Status/ Mode	Previous SI Data		SO Data															
	SOA1	SOA0	OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
Output Status	0	0	0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1
Overload Status	0	1	0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1
Device Status	1	0	1	0	UVF	OTW	OTS	NM	0	OV	STOP_ON	IGN_ON	FLASHER_ON	RC	STOP pin	FLASHER pin	IGN pin	CLOCK fail
Output Status	1	1	1	1	UVF	OTW	OTS	NM	0	0	X	X	X	OUT5	OUT4	OUT3	OUT2	OUT1
Reset	X	X	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Previous Address SOA[1:0]=00

If the previous two LSBs are 00, bits OD15:OD0 reflect the output status (Table 13).

Table 13. Output Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OL5, OL4, OL3, OL2, OL1) = Open Load Flag at Outputs 5 through 1, respectively.

OD8, OD6, OD4, OD2, OD0 (OVL5, OVL4, OVL3, OVL2, OVL1) = Overload Flag for Outputs 5 through 1, respectively.This corresponds to over-temperature or OCHI or OCLO faults.

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OVL=OCHI1+OCHI2+OCLO

Previous Address SOA[1:0]=01

If the previous two LSBs are 01, bits OD15:OD0 reflect reflect the temperature status (Table 14).

Table 14. Overload Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OC5, OC4, OC3, OC2, OC1) = High Over-current Shutdown Flag for Outputs 5 through 1, respectively

OD8, OD6, OD4, OD2, OD0 (OTS5, OTS4, OTS3, OTS2, OTS1) = Over-temperature Flag for Outputs 5 through 1, respectively

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OC=OCHI1+OCHI2

Previous Address SOA[1:0]=10

If the previous two LSBs are 01, bits OD15:OD0 reflect the status of the 35XS3500 (Table 15).

Table 15. Device Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
1	0	UVF	OTW	OTS	NM	0	OV	STOP_ ON	IGN_ON	FLASH ER_ON	RC	STOP pin	FLASH ER pin	IGN pin	CLOCK fail

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD8 (Over-voltage) = Over-voltage Flag on V_{BAT} in real time

OD7 = Indicates the state of internal STOP_ON signal, as described in Figures 11

OD6 = Indicates the state of internal IGN_ON signal

OD5 = Indicates the state of internal FLASHER_ON signal

OD4 (RC) = Logic [0] indicates a Front Corner Light Switch. Logic [1] indicates a Rear Corner Light Switch

OD3 (STOP pin) = Indicates the STOP pin state in real time

OD2 (FLASHER pin) = Indicates the FLASHER pin state in real time

OD1 (IGN pin) = Indicates the IGN pin state in real time

OD0 (CLOCK fail) = Logic [1], which indicates a clock failure

Previous Address SOA[1:0]=11

If the previous two LSBs are 11, bits OD15:OD0 reflect the status of the 35XS3500 (Table 15).

Table 16. Output Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
1	1	UVF	OTW	OTS	NM	0	0	X	X	X	OUT5	OUT4	OUT3	OUT2	OUT1

OD13 (UVF) = Under-voltage Flag on V_{BAT}

OD12 (OTW) = Over-temperature Prewarning Flag

OD11 (OTS) = Over-temperature Flag for all outputs

OD10 (NM) = Normal mode

OD4 (OUT5) = Logic [0] indicates the OUT5 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT5 voltage is higher than V_{OUT_TH}

OD3 (OUT4) = Logic [0] indicates the OUT4 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT4 voltage is higher than V_{OUT_TH}

OD2 (OUT3) = Logic [0] indicates the OUT3 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT3 voltage is higher than V_{OUT_TH}

OD1 (OUT2) = Logic [0] indicates the OUT2 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT2 voltage is higher than V_{OUT_TH}

OD0 (OUT1) = Logic [0] indicates the OUT5 voltage is lower than V_{OUT_TH}. Logic [1] indicates the OUT1 voltage is higher than V_{OUT_TH}

Protection and Diagnosis

Output Protection Features

The 35XS3500 provides the following protection features:

- Protection against transients on V_{BAT} supply line (per ISO 7637)
- Active clamp, including protection against negative transients on output line
- Over-temperature
- Severe and resistive over-current
- Open Load during ON state

These protections are provided for each output (OUT1:5).

Over-temperature detection

The 35XS3500 provides over-temperature shutdown for each output (OUT1:OUT5). It can occur when the output pin is in the ON or OFF state. An over-temperature fault condition results in turning OFF the corresponding output. The fault is latched and reported via the SPI. To delatch the fault and be able to turn the outputs ON again, the failure condition must be removed (T< 175 °C typically) and:

- if the device was in Normal mode, the output corresponding register (bit D7) must be rewritten. Application of the complete OCHI window (OCHI1+OCHI2 during t2) depends on toggling or not toggling D7 bit.
- if the device was in Fail mode, the corresponding output is locked until device restart: wake up from Sleep mode or $V_{BATPOR1}$.

The SPI fault report (OTS bit) is removed after a read operation.

Over-current detections

The 35XS3500 provides intelligent over-current shutdown (see Figure 12) in order to protect the internal power transistors and the harness in the event of overload (fuse characteristic).

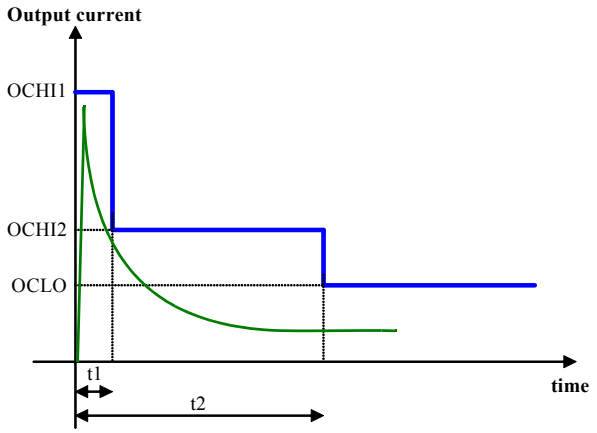


Figure 12. Double Over-current Window in Normal Mode

OCHI (I_{OCHI1} and then I_{OCHI2}) is only activated after toggling the D7 bit in Normal mode. During the output switching, the severe short-circuit condition provided on the module connector is reported as an OCHI fault. In Fail mode, the control of OCHI window is provided by the toggles: IGN_ON, Flasher_ON. The current thresholds (I_{OCHI1}, I_{OCHI2} and I_{OCLO}) and the time (t_1 and t_2) are fixed numbers for each driver. After t_2, the OCLO current threshold is set to protect in steady state. t_1 and t_2 times are compared to “on” state duration (t_{ON}) of the output. In case of the output is controlled in PWM mode during the inrush period, the t_{ON} corresponds to the sum of each “on” state duration in order to expand dynamically the transient over-current profile.

In case of an overload (OCHI1 or OCHI2 or OCLO detection), the corresponding output is disabled immediately. The fault is latched and the status is reported via the SPI. To delatch the fault, the failure condition must be removed and:

For OCHI1:

- if the device was in Normal mode: the output corresponding register (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail mode, the failure is locked until restart of the device: wake-up from Sleep mode or $V_{BATPOR1}$.

For OCHI2 and OCLO:

- if the device was in Normal mode: the output corresponding register (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail mode, autorestart is activated. The device autorestart feature provides a fixed duty cycle and fixed period with OCHI1 window. autorestart feature resets OCHI2 or OCLO fault after corresponding Autorestart period.

The SPI fault reports are removed after a read operation:

- OC bit=(OCHI1) or (OCHI2) fault
- OVL bit=(OCHI1) or (OCHI2) or (OCLO) fault

Over-voltage detection and active clamp

The 35XS3500 provides an active gate clamp circuit, in order to limit the maximum drain to source voltage.

In case of overload on an output, the corresponding switch (OUT[1 to 5]) is turned off which leads to a high voltage at VBAT, with an inductive V_{BAT} line. The maximum VBAT voltage is limited at $V_{BATCLAMP}$ by active clamp circuitry through the load. In case of open load condition, the positive transient pulses (ISO 7637 pulse 2 and inductive battery line) shall be handled by the application.

Figures 13 and 14 describe the faults management in Normal mode and Fail mode.

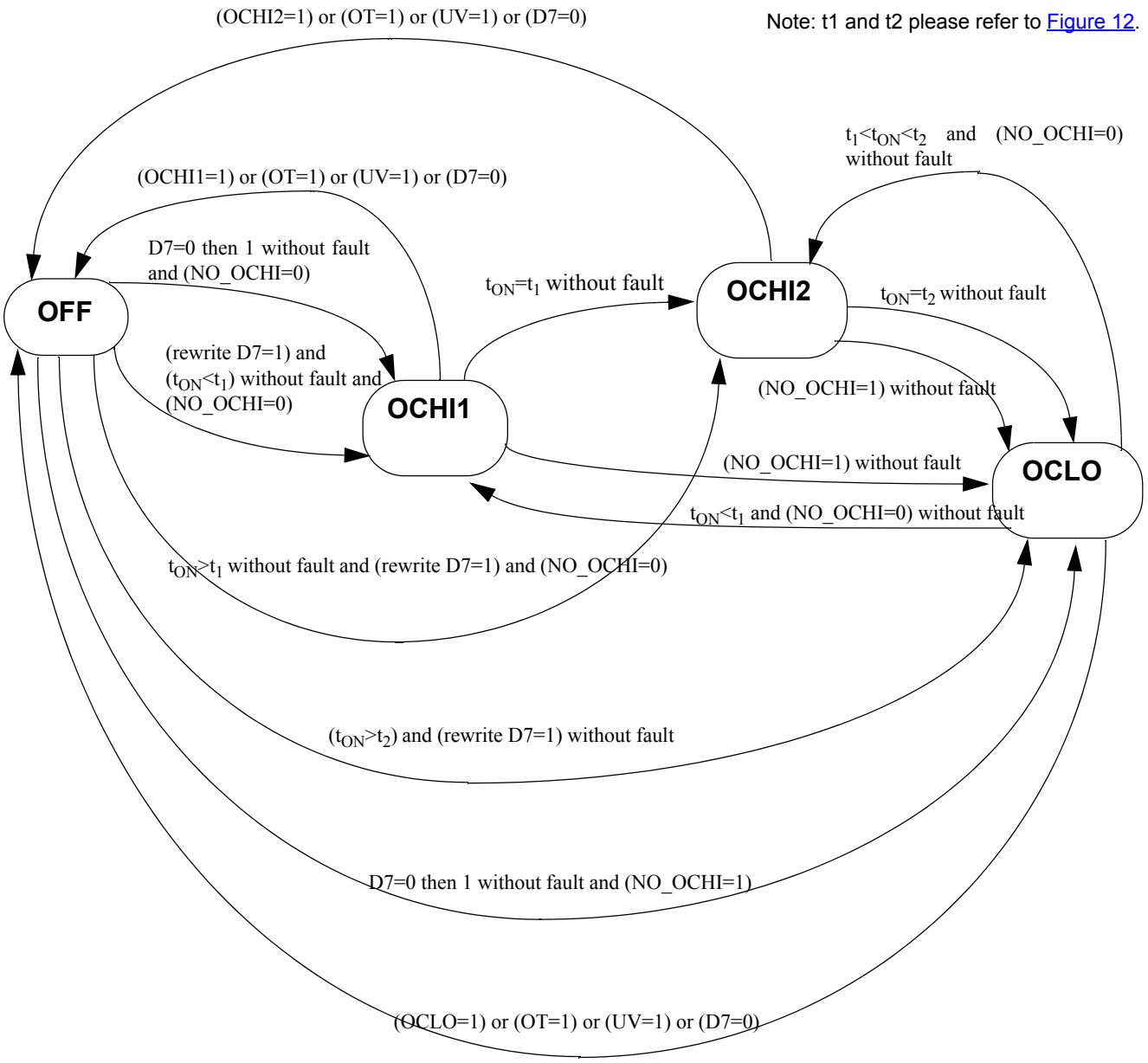
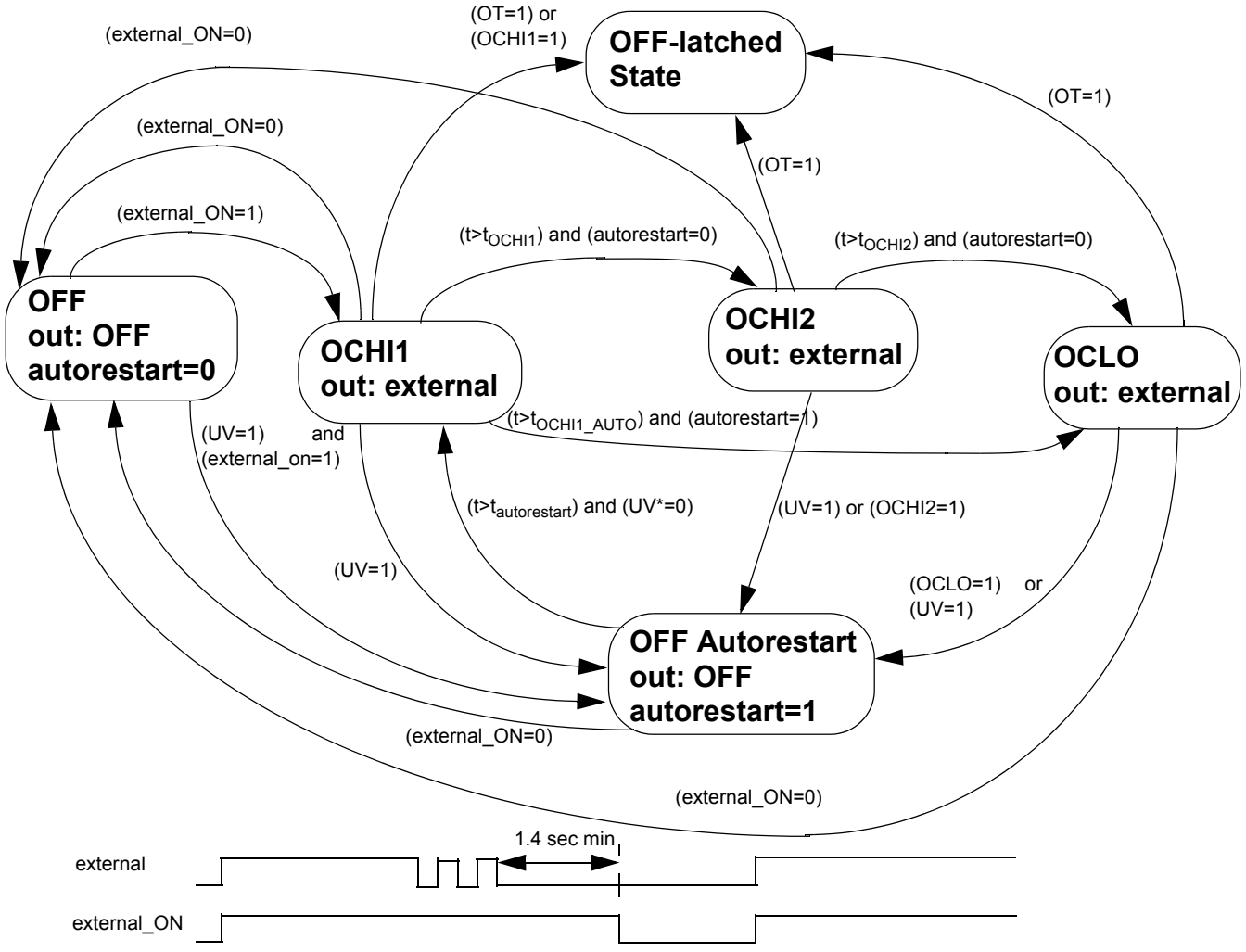


Figure 13. Faults Management in Normal Mode (for OUT[1:5] only)



external: IGN, Flasher, Stop
external_ON: IGN_ON, Flasher_ON, Stop_ON
Note: * See Autorestart strategy chapter.

Figure 14. Faults Management in Fail Mode (for OUT[1:5] only)

DIAGNOSIS

Open Load

The 35XS3500 provides open load detection for each output (OUT1:OUT5) when the output pin is in the ON state. Open load detection levels can be chosen by the SPI to detect a standard bulb or LEDs (OLLED bit). Open load for LEDs only is detected during each regular switch-off state or periodically each t_{OLLED} (fully-on, D[6:0] = 7F). To detect OLLED in fully on state, the output must be on at least t_{OLLED}. When an open load has been detected, the output stays ON.

To delatch the diagnosis, the condition should be removed and a SPI read operation is needed (OL bit). In case of a Power on Reset on VBAT, the fault will be reset.

Current Sense

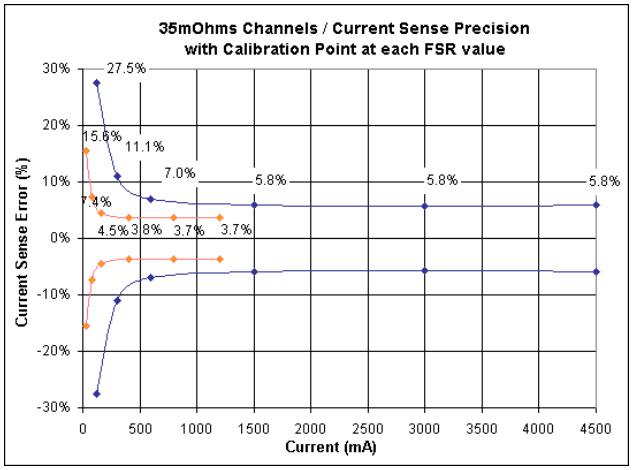
The 35XS3500 diagnosis for load current (OUT1:6) is done using the current sense (CSNS) pin connected to an external resistor. The CSNS resistance value is defined in function to VCC voltage value. It is recommended to use resistor 500 Ω < R_{CSNS} < 5.0 kΩ. Typical value is 1.0 kΩ for 5.0 V application. The routing of the current sense sources is SPI programmable (MUX[2,0] bits).

The current recopy feature for OUT1:5 is disabled during a high over-current shutdown phase (t_2) and is only enabled during low over-current shutdown thresholds. The current recopy output delivers current only during ON time of the output switch without overshoot (aperiodic settling).

The current recopy is not active in Fail mode.

With a calibration strategy, the output current sensing precision can be improved significantly. One calibration point at 25 °C for 50% of FSR allows removing part to part contribution. So, the calibrated part precision goes down to +/-6.0% over [20% - 75%] output current FSR, over voltage range (10 to 16 V) and temperature range (-40 to 125 °C).

With dedicated calibration points, the current recopy allows diagnosing lamp damage in paralleling operations, like as flasher topology. The Figure 15 summaries test results covering 99.74% of parts (device ageing not included) for Standard lamps and LEDs.



Orange = LED mode
Blue = lamp mode (default mode)

Figure 15. Current Sense Precision with Calibration Strategy

Board Temperature Feedback

The 35XS3500 provides a voltage proportional to the temperature on the GND flag. This analog feedback is available in CSNS output pin for MUX[2,0] bits set to “111”, as described in Figure 16.

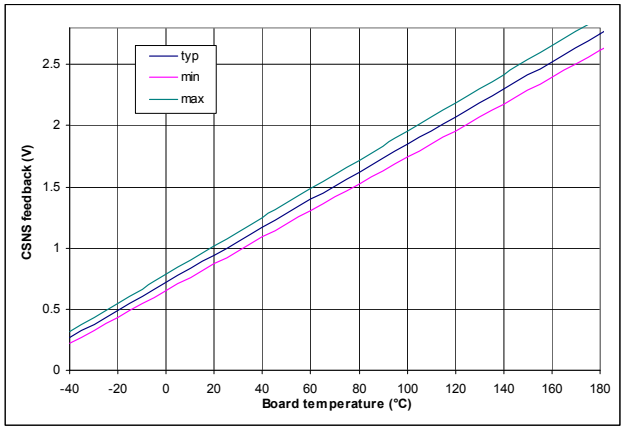


Figure 16. Analog Temperature Precision

The board temperature feedback is not active in Fail mode.

With a calibration strategy, the temperature monitoring precision can be improved. So, one calibration point at 25 °C allows removing part to part contribution, as presented in Figure 17.

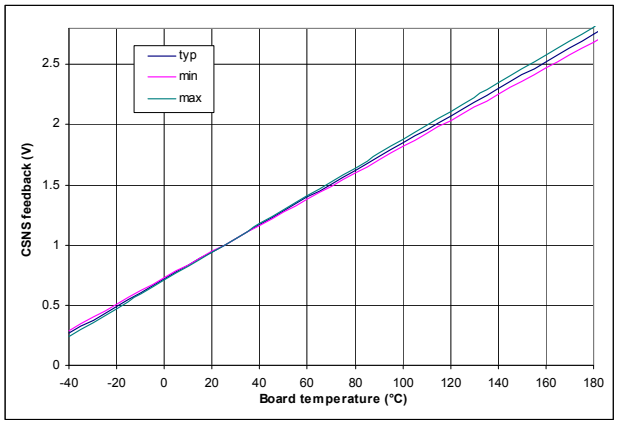


Figure 17. Analog Temperature Precision with Calibration Strategy

Output Status

The 35XS3500 provides the state of OUT1:OUT5 outputs in real time through SPI. The OUT bit is set to logic [1] when the corresponding output voltage is closed to half of battery. This bit allows synchronizing current sense and diagnosing short-circuit between OUT and VBAT pins.

Temperature Prewarning

The 35XS3500 provides a temperature prewarning reported via the SPI (OTW bit) in Normal mode. The information is latched. To delatch, a read SPI command is needed. In case of a Power on Reset, the fault will be reset.

External Pin Status

The 35XS3500 provides the status of the FLASHER, IGN, STOP, and CLOCK pins via the SPI in real time and in Normal mode.

Failure Handling Strategy

A highly sophisticated failure handling strategy enables light functionality even in case of failures inside the component or the light module. Components are protected against:

- Reverse Polarity
- Loss of Supply Lines
- Fatal Mistreatment of Logic I/O Pins

Reverse Polarity Protection on V_{BAT}

In case of a permanently reverse polarity operation, the output transistors are turned ON (R_{SD}) to prevent thermal overloads and no protections are available.

An external diode on VCC is necessary in order to not to destroy the 35XS3500 in cases of reverse polarity.

In case of negative transients on the VBAT line (per ISO 7637), the VCC line is still operating, while the VBAT line is negative. Without loads on OUT1:5 terminal, an external clamp between V_{BAT} and GND is mandatory to avoid exceeding maximum rating. The maximum external clamp voltage shall be between the reverse battery condition and -20 V.

Therefore, the device is protected against latch-up with or without load on OUT outputs.

Loss of Supply Lines

The 35XS3500 is protected against the loss of any supply line. The detection of the supply line failure is provided inside the device itself.

Loss of V_{BAT}

During an under-voltage of V_{BAT} ($V_{BATPOR1}$<V_{BAT}<V_{BATUV}) and with an active device (wake=1), the outputs [1-5] are switched off immediately. No current path exists from V_{BAT} to V_{CC}. The external MOSFET (OUT6) can be controlled by the SPI if V_{CC} remains and is above to V_{CCUV}. The fault is reported to the UVF bit (OD13). To delatch the fault, the under-voltage condition should be removed and:

- the bit D7 must be rewritten to a logic [1] in Normal mode. Application of the OCHI window depends on toggling or not toggling the D7 bit. When the fault is delatched, the 35XS3500 returns to the configuration it was just before the failure.
- if the device was in Fail mode, the fault will be delatched periodically by the Autorestart feature.

In case of V_{BAT}<$V_{BATPOR1}$ (Power OFF state), the behavior depends on V_{CC}:

- all latched faults are reset if V_{CC} < V_{CCUV},
- all latched faults are maintained under V_{CC} in nominal conditions. In case V_{BAT} is disconnected, OUT[1:5] outputs are OFF. OUT6 output state depends on the previous SPI configuration. The SPI configuration, reporting (if V_{BAT} was previously in the nominal voltage range for at least 35 µsec), and daisy-chain features are provided for $\overline{RST}$ is set to logic [1]. The SPI pull-up and pull-down current resistors are available. This fault condition can be diagnosed with UVF fault in OD13 reporting bit. The previous device configuration is maintained. No current is conducted from V_{CC} to V_{BAT}.

Loss of V_{CC} (Digital Logic Supply Line)

During loss a of V_{CC} (V_{CC} < V_{CCUV}) and with wake=1, the 35XS3500 is switched automatically into Fail mode (no deglich time). The external SMART MOSFET is OFF. All SPI registers are reset and must be reprogrammed when V_{CC} goes above V_{CCUV}. The device will transit in OFF mode if VBAT < $V_{BATPOR2}$.

LOSS OF V_{CC} AND V_{BAT}

If the external V_{BAT} and V_{CC} supplies are disconnected (or not within specification: (V_{CC} and V_{BAT}) < $V_{BATPOR1}$), all SPI register contents are reset with default values corresponding to all SPI bits are set to logic [0] and all latched faults are also reset.

Loss of Ground (GND)

During a loss of ground, the 35XS3500 cannot operate the loads (the outputs (1:5) are switched OFF), but is not destroyed by the operating condition. Current limit resistors in the digital input lines protect the digital supply against excessive current (1.0 kohm typical). The state of the external smart power switch controlled by FETOUT is not guaranteed, and the state of the external smart MOS is defined with an external termination resistor.

Fatal Mistreatment of Logic I/O Pins

The digital I/Os are protected against fatal mistreatment by a signal plausibility check according to Table 17.

Table 17. Logic I/O Plausibility Check

Input/Output	Signal Check Strategy
LIMP	Debounce for 10 ms
(PWM) CLOCK	Frequency range (bandpass filter)
SPI (MOSI, SCLK, $\overline{CS}$)	WD, D10 bit internal toggle

In case the LIMP input is set to a logic [1] for a delay longer than 10 ms typical, the 35XS3500 is switched into Fail mode. In case of a (PWM) Clock failure, no PWM feature is provided, and the bit D7 defines the outputs state. In case of a SPI failure, the 35XS3500 is switched into Fail mode (Figure 18)

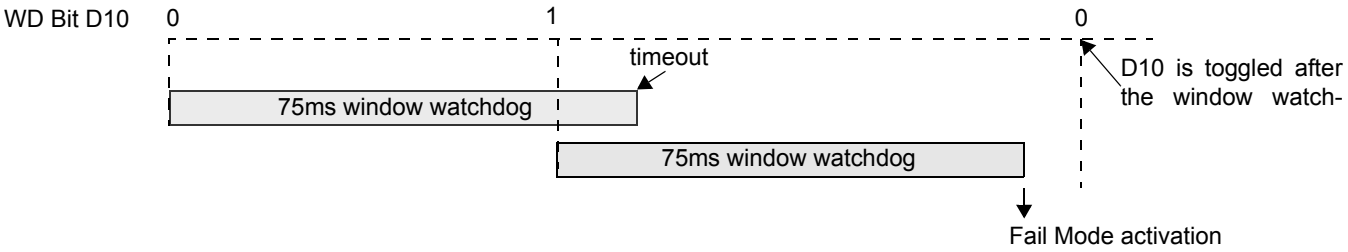


Figure 18. Watchdog Window

TYPICAL APPLICATIONS

Figure 19 shows full vehicle light functionality, including fog lights, battery redundancy concept, light substitution mode, and Limp Home mode.

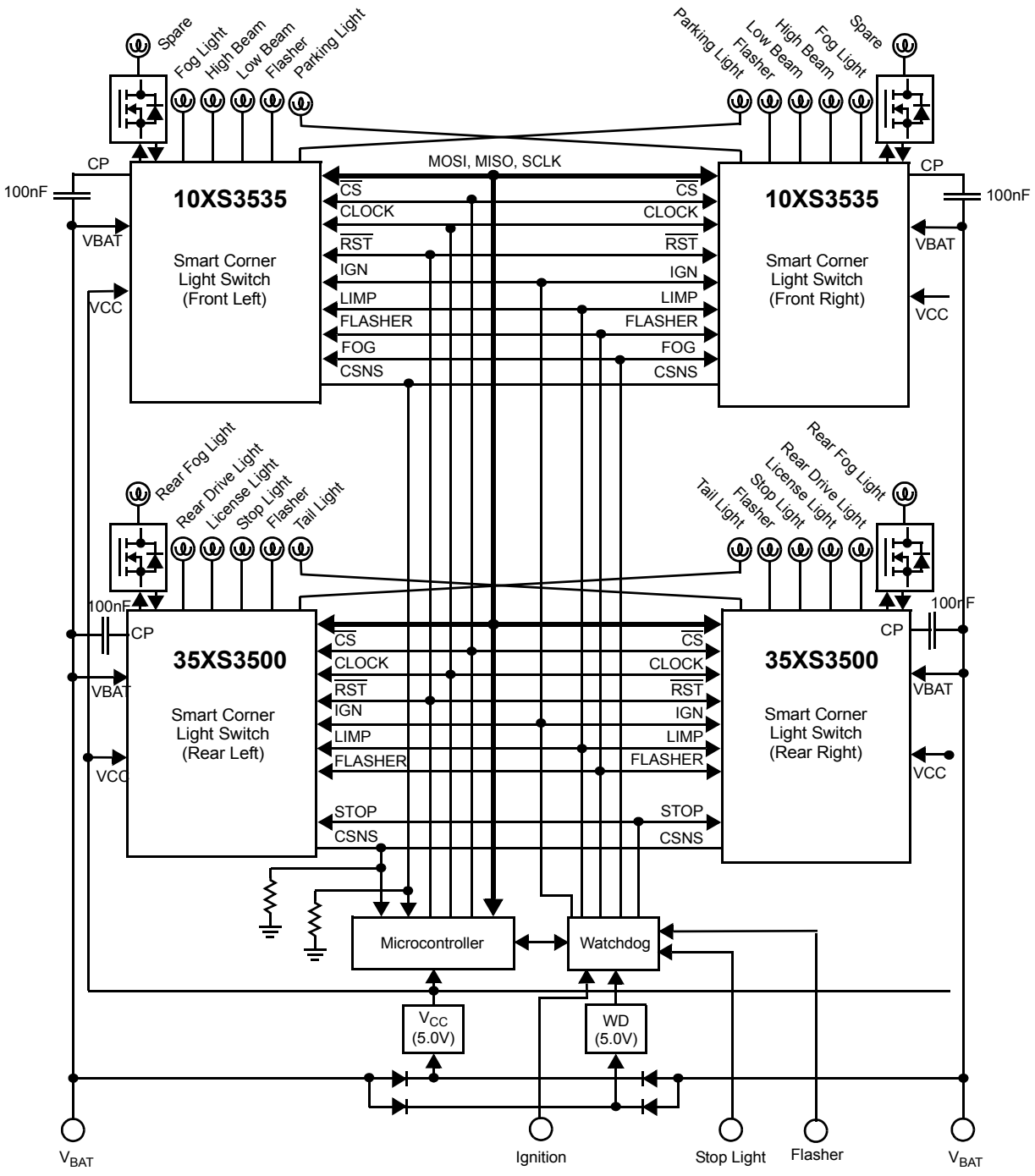


Figure 19. Typical Application

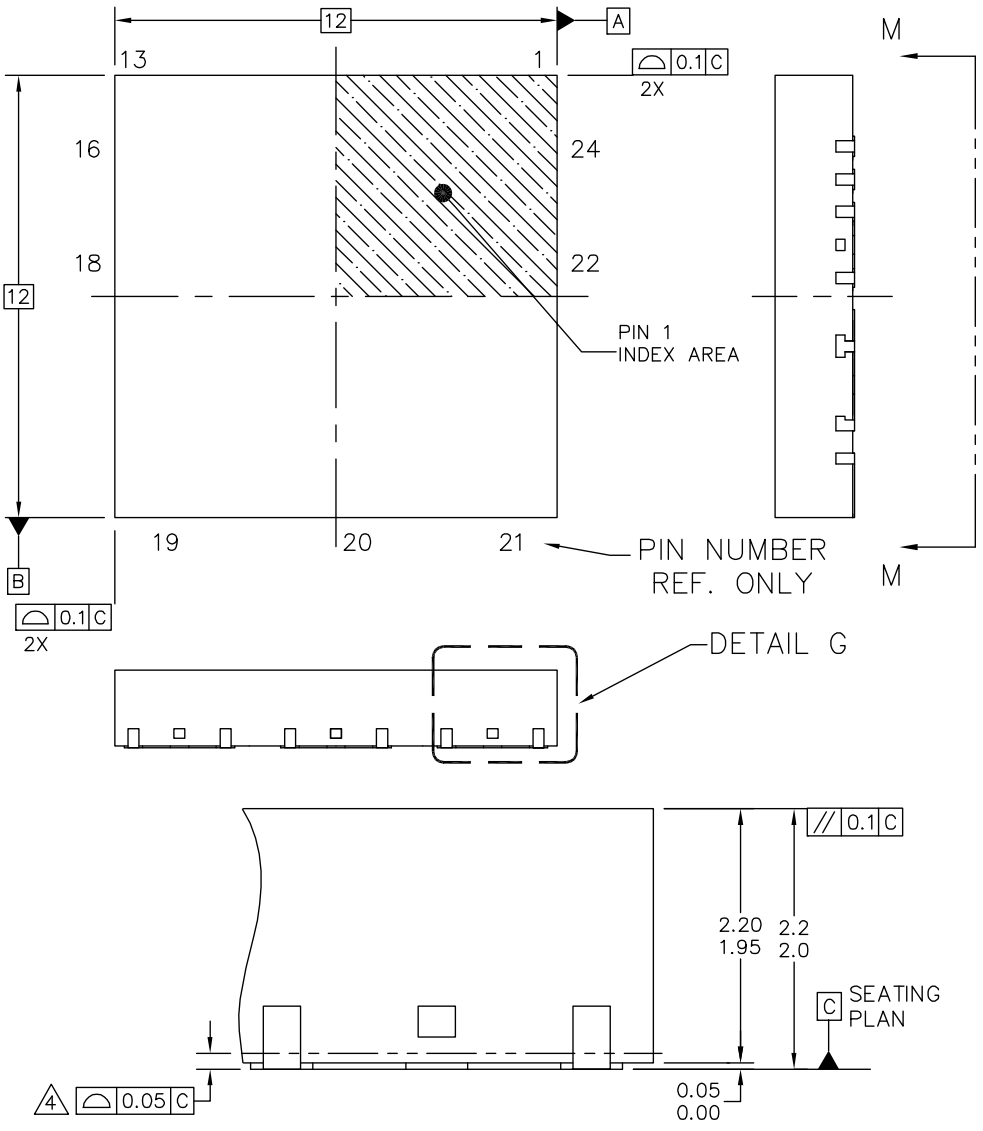
EMC & EMI PERFORMANCES

The 35XS3500 will be compliant to CISPR25 Class5 in Standby mode with 22 nF decoupling capacitor on OUT[1:5].

PACKAGING

PACKAGING DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98ART10511D listed below. Dimension shown are provided for reference ONLY.



DETAIL G

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TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PQFN),24 TERMINAL, 0.9 PITCH(12X12X2.1),CORNERLIGHT FRONT	DOCUMENT NO: 98ART10511D	REV: O
	CASE NUMBER: 1951-01	14 MAR 2007
	STANDARD: NON-JEDEC	

FK SUFFIX
24-PIN PQFN
98ART10511D
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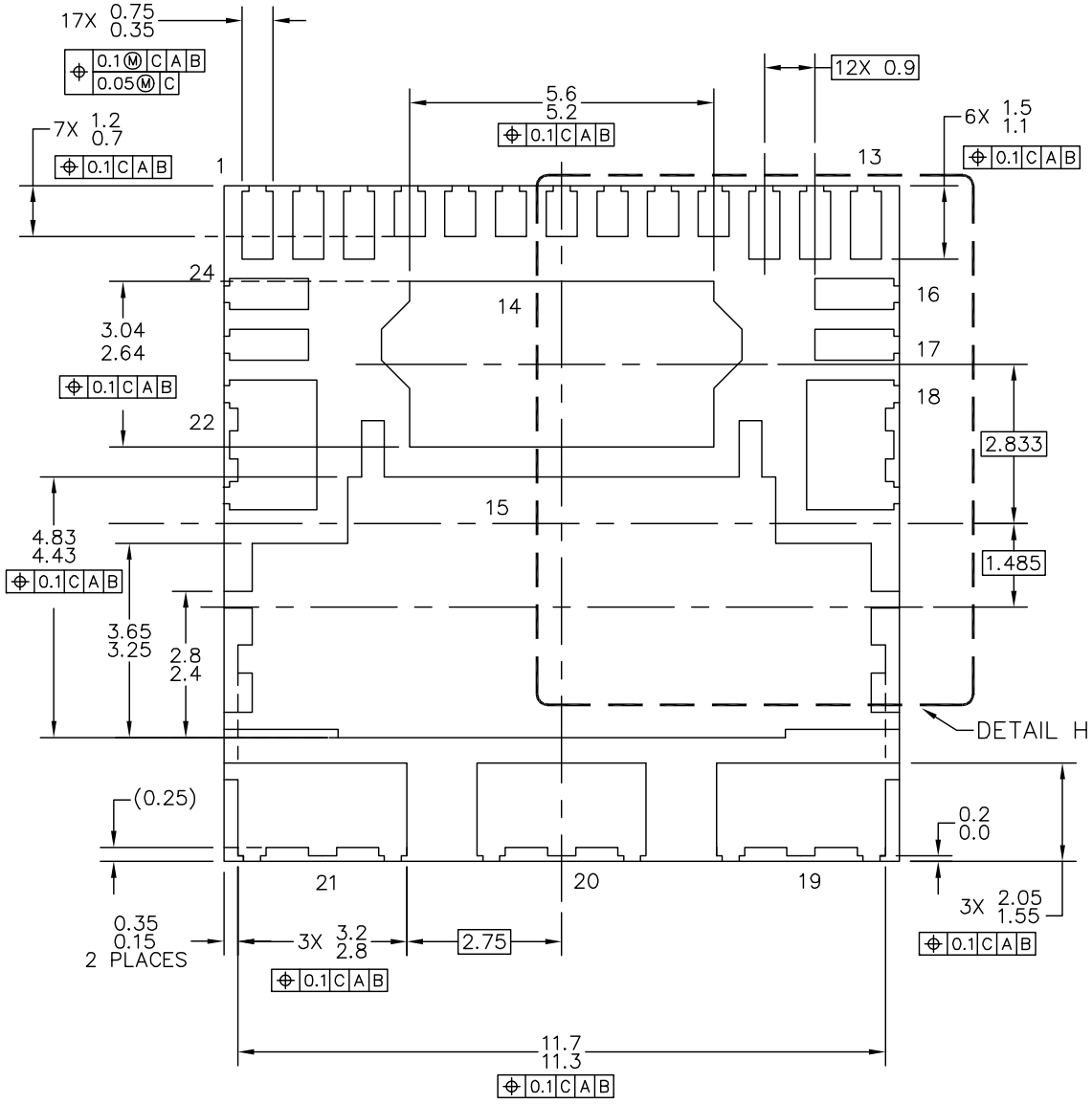

VIEW M–M

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	CASE NUMBER: 1951–01	14 MAR 2007
	STANDARD: NON–JEDEC	

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24-PIN PQFN
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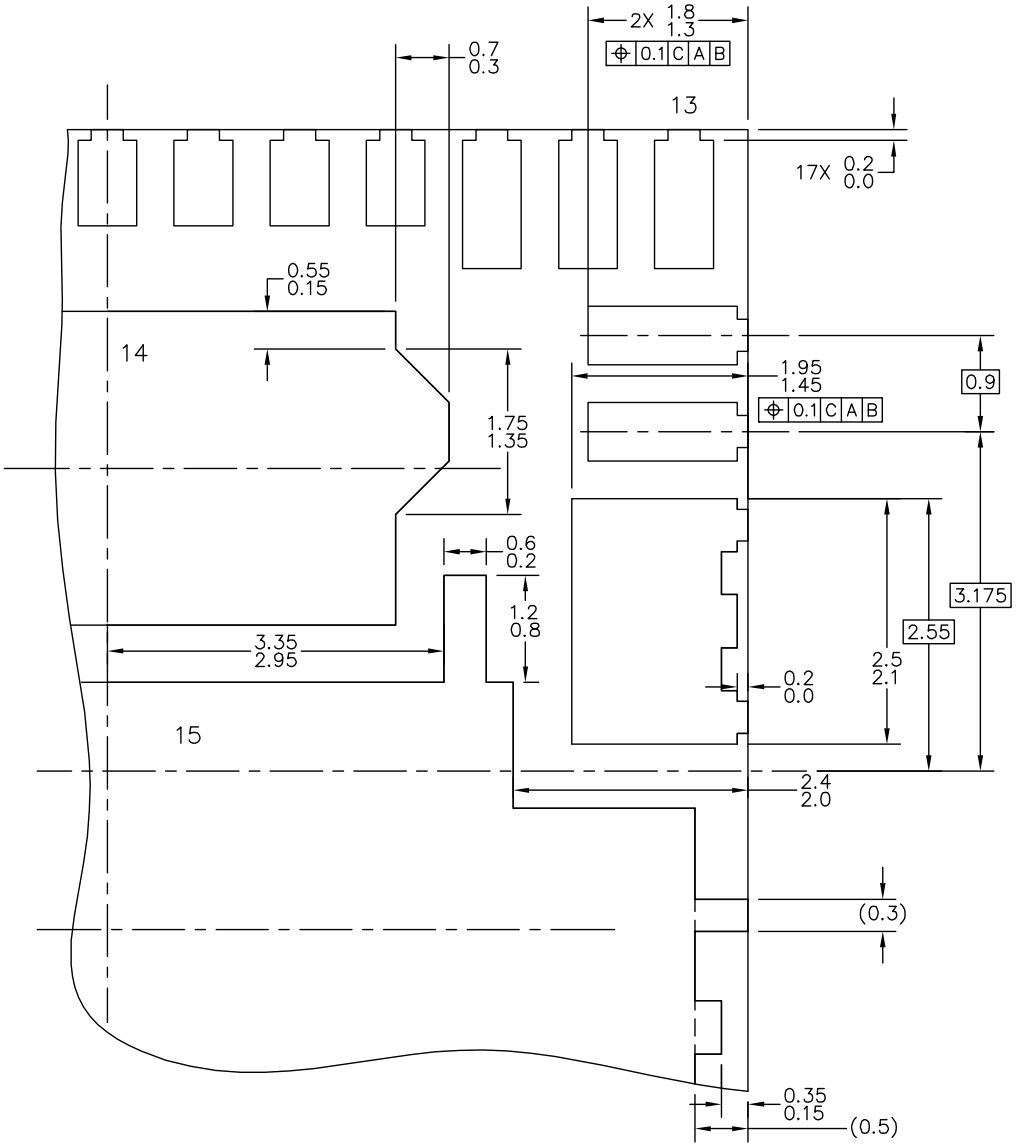

DETAIL H

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	CASE NUMBER: 1951-01	14 MAR 2007
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP IS GUARANTEED TO BE 0.25MM.

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	CASE NUMBER: 1951–01	14 MAR 2007
	STANDARD: NON–JEDEC	

FK SUFFIX
24-PIN PQFN
98ART10511D
ISSUE 0

REVISION HISTORY

Revision	Date	Description of Changes
1.0	5/2010	• Initial Release
2.0	7/20101	• Changed PN to MC35XS3500PNA • Changed classification to Advance Information
3.0	9/2010	• Added Minimum Output Current Reported in CSNS for OUT[1-5](13) to Table 3. • Added Minimum Output Current Reported in CSNS for OUT[1-5] in LED Mode(13) to Table 3. • Added Note: Output current value computed after leakage current removal (open load condition) to Table 3.
4.0	5/2011	• Added Under-voltage Deglitch Time parameter.
5.0	4/2012	• Added Orderable Part Number PC35XS3500HFK • Corrected errors in Table 12 and Table 15
6.0	6/2012	• Removed MC35XS3500PNA • Updated PC35XS3500HFK to MC35XS3500HFK • Added (4) • Updated Under-voltage Deglitch Time t_{UV} parameter in Table 5, Dynamic Electrical Characteristics on page 15 • Updated Freescale form and style
7.0	12/2012	• Added "if V_{BAT} was previously in the nominal voltage range for at least 35 µsec" to Loss of V_{BAT} Section. • Added MC35XS3500DHFK to the ordering information.
8.0	8/2013	• Changed CSNS condition for CSNS Tri-state Leakage Current • Changed Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) at Output = 50% V_{BAT} with V_{BAT} = 14 V, $_{fPWM}$ = 240 Hz, δ_{PWM} = 50%, at 25 °C • Corrected conditions for FETIN Leakage Current when external current switch sense is enabled

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