ABSOLUTE MAXIMUM RATINGS

Referenced to GND
V_{CC1}, V_{CC2}, EN .....-0.3V to +6.0V
SETV, SETD .....-0.3V to the higher of (V_{CC1} + 0.3V) and (V_{CC2} + 0.3V)
GATE .....-0.3V to +12.0V
Input Current/Output Current (all pins) 20mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC1} or V_{CC2} > +2.125V to +5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC1}, V_{CC2}	(Note 2)	0.9		5.5	V
V_{CC1}, V_{CC2} Supply Current	I_{CC}	V_{CC1} = V_{CC2} = +3.3V		60	120	µA
V_{CC1}, V_{CC2} Disable Mode Current		V_{CC1} = V_{CC2} = +3.3V, EN = GND		20		µA
V_{CC1}, V_{CC2} Slew Rate (Note 3)		MAX6819	6			V/s
		MAX6820 (Note 4)	1.2 / t_{DELAY}			
Undervoltage Lockout (UVLO)	V_{UVLO}		1.875	2.0	2.125	V
SETV Threshold	V_{TH}	V_{SETV} rising, enables GATE	0.602	0.618	0.634	V
SETV Input Current		(Note 3)		10	100	nA
SETV Threshold Hysteresis		V_{SETV} falling, disables GATE		-1		%
SETV to GATE Delay	t_{DELAY}	V_{SETV} > V_{TH}, V_{EN} ≥ 2V (MAX6819)	140	200	280	ms
SETD Ramp Current (MAX6820)	I_{SETD}	V_{CC1} or V_{CC2} > +2.125V	400	500	600	nA
SETD Voltage (MAX6820)	V_{SETD}	V_{CC1} or V_{CC2} > +2.125V	1.210	1.242	1.273	V
SETD Threshold Hysteresis (MAX6820)		V_{SETD} falling		-62		mV
GATE Turn-On Time	t_{ON}	C_{GATE} = 1500pF, V_{CC2} = +3.3V, V_{GATE} = +7.8V	0.5	1.5	10	ms
GATE Turn-Off Time	t_{OFF}	C_{GATE} = 1500pF, V_{CC2} = +3.3V, V_{GATE} = +0.5V		30		µs
GATE Voltage	V_{GATE}	With respect to V_{CC2} (Note 2) R_{GATE} > 50MΩ to V_{CC2}	4.5	5.5	6.0	V
		With respect to V_{CC2} (Note 2) R_{GATE} > 5MΩ to V_{CC2}	4.0		6.0	
EN Input Voltage	V_{IL}	V_{CC1} or V_{CC2} > +2.125V to + 5.5V			0.4	V
	V_{IH}		2.0			

Note 1: 100% production tested at T_A = +25°C. Specifications over temperature limit are guaranteed by design.
Note 2: Either V_{CC1} or V_{CC2} must be > 2.125V. The other supply can go to 0.
Note 3: Guaranteed by design, not production tested.
Note 4: t_{DELAY} (s) = 2.48 × 10^6 × C_{SET}

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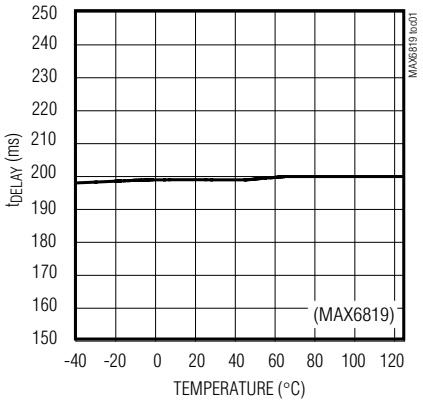
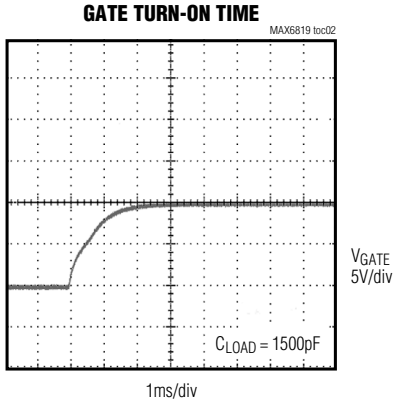
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

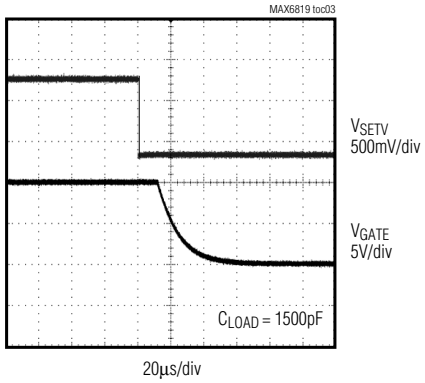
t_{DELAY} vs. TEMPERATURE



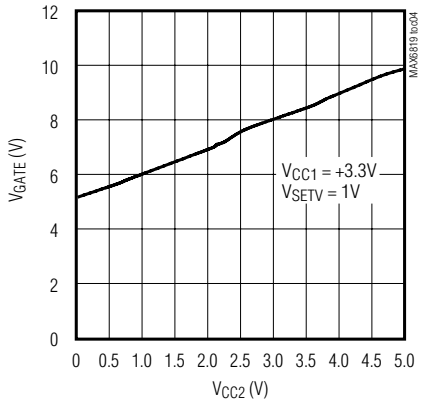
GATE TURN-ON TIME



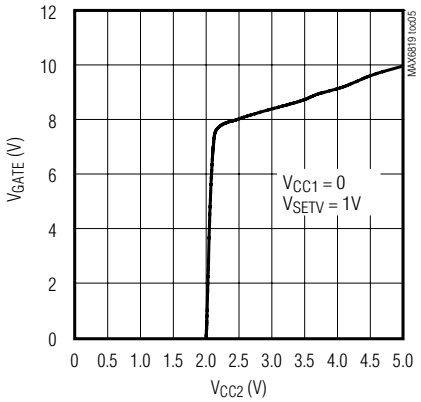
GATE TURN-OFF TIME



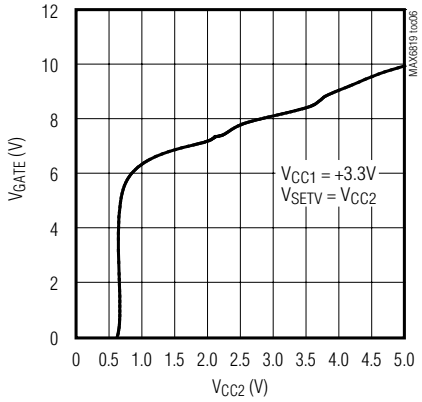
V_{CC2} vs. GATE VOLTAGE



V_{CC2} vs. GATE VOLTAGE



V_{CC2} vs. GATE VOLTAGE



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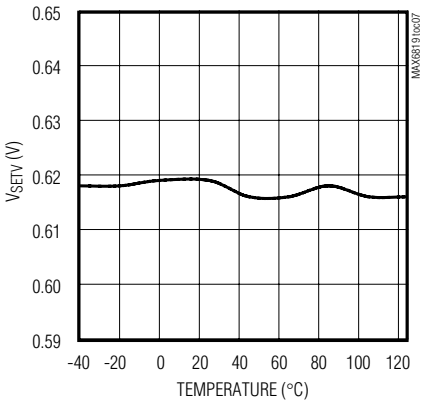
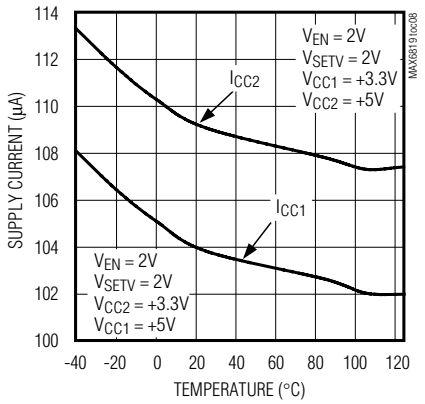
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

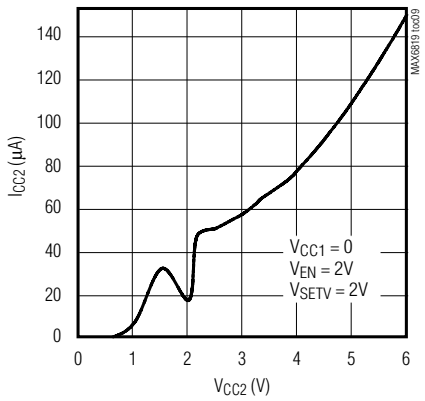
V_{SETV} vs. TEMPERATURE



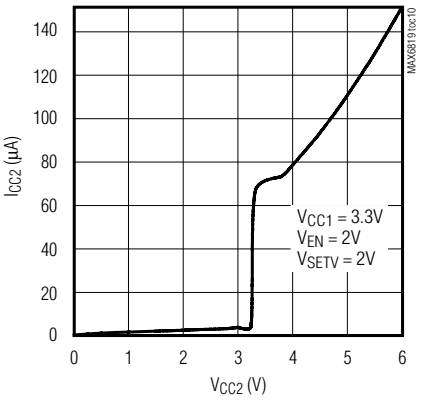
SUPPLY CURRENT vs. TEMPERATURE



I_{CC2} vs. V_{CC2}



I_{CC2} vs. V_{CC2}



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Pin Description

PIN		NAME	FUNCTION
MAX6819	MAX6820		
1	1	V_{CC1}	Supply Voltage 1. Either V_{CC1} or V_{CC2} must be greater than the UVLO to enable external MOSFET drive.
2	2	GND	Ground
3	3	SETV	Sequence Threshold Set. Connect to an external resistor-divider network to set the V_{CC1} threshold that enables GATE turn-on. The internal reference is 0.618V.
4	—	EN	Active-High Enable. GATE drive is enabled t_{DELAY} after EN is driven high. GATE drive is immediately disabled when EN is driven low. Connect to the higher of V_{CC1} and V_{CC2} if not used.
—	4	SETD	GATE Delay Set Input. Connect an external capacitor from SETD to GND to adjust the delay from SETV > V_{TH} to GATE turn-on. t_{DELAY} (s) = 2.484 x 10^6 x C_{SET} (F).
5	5	GATE	GATE Drive Output. GATE drives an external n-channel MOSFET to connect V_{CC2} to the load. GATE drive enables t_{DELAY} after SETV exceeds V_{TH} and ENABLE is driven high. GATE drive is immediately disabled when SETV drops below V_{TH} or ENABLE is driven low. When enabled, an internal charge pump drives GATE to V_{CC2} + 5.5V to fully enhance the external n-channel MOSFET.
6	6	V_{CC2}	Supply Voltage 2. Either V_{CC1} or V_{CC2} must be greater than the UVLO to enable external MOSFET drive.

Detailed Description

Many dual-supply processors or multivoltage boards require one power supply to rise to the proper operating voltage before another supply is applied. Improper sequencing can lead to chip latchup, incorrect device initiation, or long-term reliability degradation. If the various supply voltages are not locally generated (coming from a main system bus, an externally purchased silver box, or a nonsequenced power management chip), power-on and power-off sequencing can be difficult to control or predict. Supply loading can affect turn-on/turn-off times from board to board.

The MAX6819/MAX6820 provide proper local voltage sequencing in multisupply systems. The sequencers use an external n-channel MOSFET to switch the secondary supply to the load only when the primary supply is above a desired operating voltage threshold. The n-channel MOSFET operates in a default off mode when the primary supply is below the desired threshold or if neither supply exceeds the sequencer's UVLO level.

When the primary supply voltage is above the set threshold, the external MOSFET is driven on. An internal charge pump fully enhances the external MOSFET by providing a gate-to-source voltage (V_{GS}) of +5.5V (typ). The charge pump fully enhances the MOSFET to yield a low drain-to-source impedance ($R_{DS(ON)}$) for reduced switch voltage drop. The MOSFET is never driven on unless the sequencer can provide a minimum V_{GS} enhancement, ensuring that the switch MOSFET never operates in its higher impedance linear range.

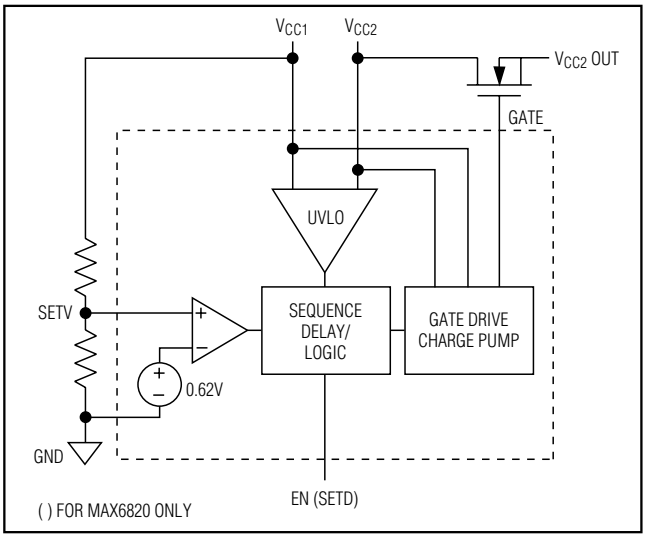

Figure 1. Functional Diagram

Either supply may act as the primary source, regardless of the voltage level, provided that V_{CC1} or V_{CC2} is greater than 2.125V (Figure 1 and Figure 2).

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SOT23 Power-Supply Sequencers

Applications Information

Adjusting t_{DELAY}

The MAX6820 features a capacitor adjustable sequence delay. The adjustable delay provides power sequencing for a wide range of devices with different power-supply delay requirements. Connect a capacitor (C_{SET}) between SETD and GND to adjust the delay time (Figure 2). Calculate the sequence delay time as follows:

$$t_{DELAY}\ (s) = 2.48 \times 10^6 \times C_{SET}$$

Setting Threshold Voltage at SETV

The threshold voltage is the minimum V_{CC1} voltage at which V_{CC2} turn-on is acceptable. To monitor voltages higher than the threshold voltage, connect external resistors as a voltage-divider to SETV, and calculate the minimum V_{CC} turn-on voltage as follows:

$$R1 = R2\ ((V_{TRIP} / V_{TH}) - 1)$$

where V_{TRIP} is the minimum turn-on voltage at V_{CC1} and V_{TH} = 0.618V (Figure 2).

Since SETV input current is 10nA (typ), high value resistors can be used.

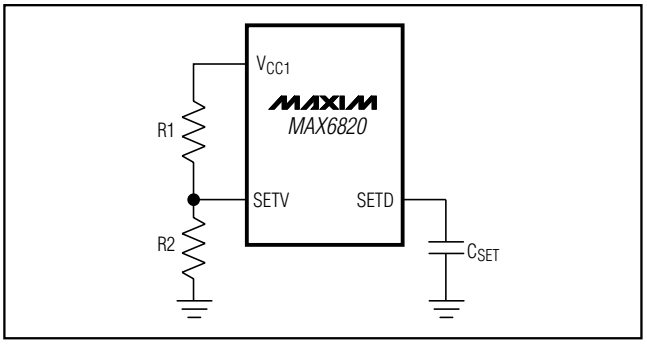

Figure 2. t_{DELAY} (MAX6820 ONLY) and V_{TH} Adjust

Selecting the Pass MOSFET

The external pass MOSFET is connected in series with the sequenced power-supply source. Since the load current and the MOSFET drain-to-source impedance (R_{DS}) determine the voltage drop, the on characteristics of the MOSFET affect the load supply accuracy. The MAX6819/MAX6820 fully enhance the external MOSFET out of its linear range to ensure the lowest drain-to-source on impedance. For highest supply accuracy/lowest voltage drop, select a MOSFET with an appropriate drain-to-source on impedance for a gate-to-source bias of 4.5V to 6.0V.

Gate Drive Characteristics

The MAX6819/MAX6820 internal charge pump drives the n-channel MOSFET with a gate-to-source voltage (V_{GS}) of 5.5V, ensuring low MOSFET on-resistance $R_{DS(ON)}$. The charge pump drives the high-impedance capacitive load of a MOSFET gate input.

Loading the GATE output resistively adds load current and reduces gate drive capability. The internal charge pump does not require external capacitors.

The external pass MOSFET is disabled, and charge pump circuitry is turned off when neither V_{CC1} nor V_{CC2} are above the 1.875V UVLO or EN is low.

Logic Driven Supply Sequencing

The MAX6819 offers a logic-compatible enable input (EN) that allows digital devices to control sequencing. When the TTL/CMOS-compatible EN input is logic-low, the GATE output is low. When the EN input is logic-high (and SETV is above the monitor threshold), the GATE output is enabled after an internally fixed 200ms delay. For a logic-controlled sequencer when voltage monitoring is not desired, connect SETV to V_{CC1} or V_{CC2} > 0.62V (Figure 3).

Sequencing Three or More Supplies

Cascade multiple MAX6819/MAX6820 to sequence more than two supplies. Daisy-chaining devices allows one sequencer to monitor the passed voltage of an upstream sequencer through the SETV comparator inputs. EN allows any sequencer to be shut down independent of the SETV levels. Figure 4 shows an example of a three-supply system in which the first supply must come up before the second supply and the third supply must yield for both supplies.

Negative-Going Voltage Transient Immunity

The MAX6819/MAX6820 power-supply voltage sequencers are relatively immune to short-duration (pulse width), negative-going voltage transients (Figure 5). However, the amplitude of the transient is inversely proportional to its pulse width.

Chip Information

TRANSISTOR COUNT: 638

PROCESS: BiCMOS

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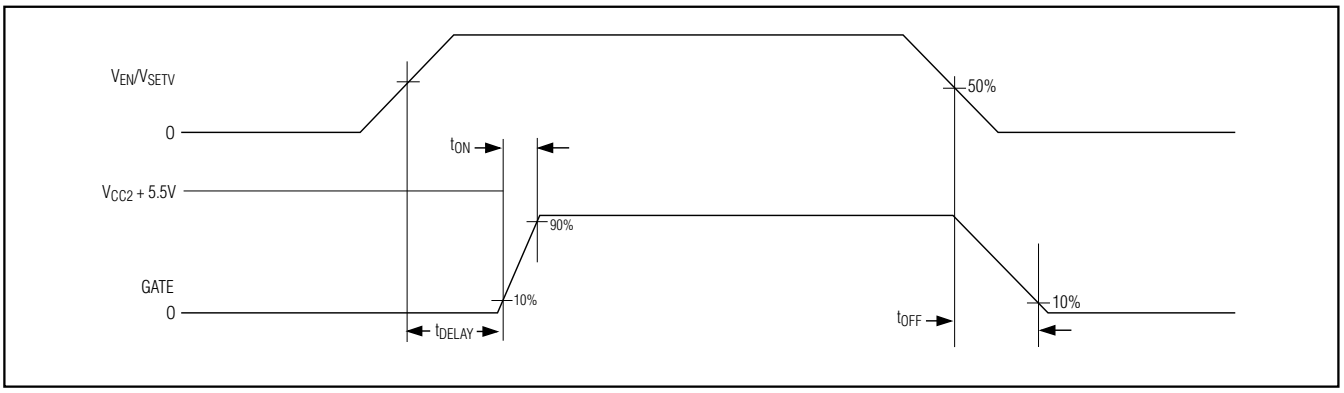

Figure 3. Timing Diagram

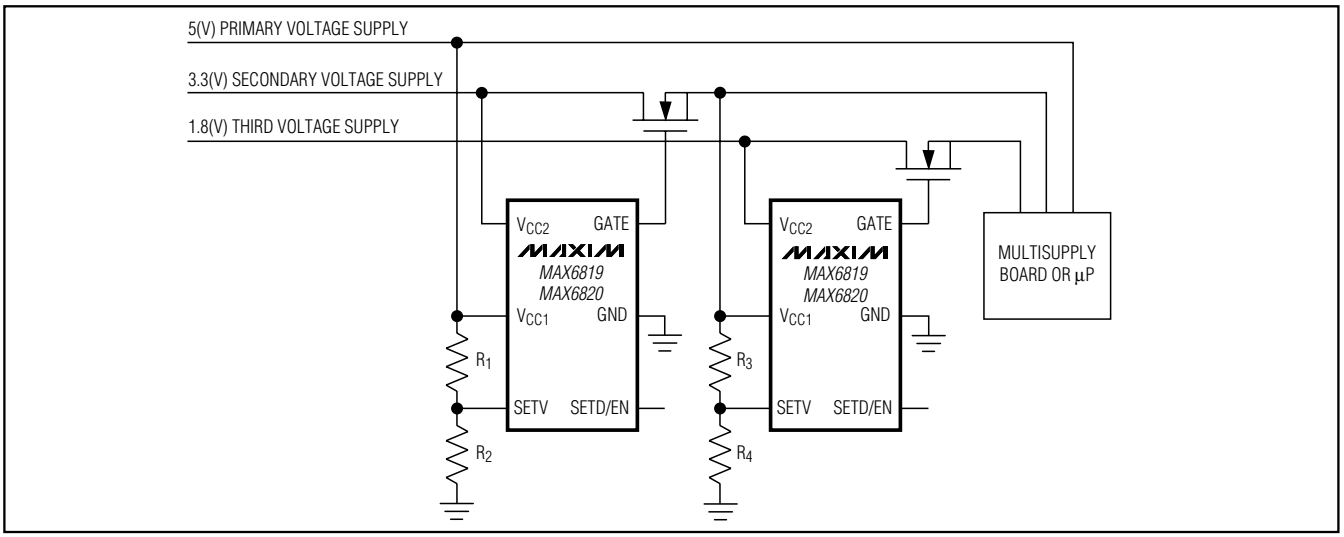

Figure 4. Sequencing Three Power Supplies

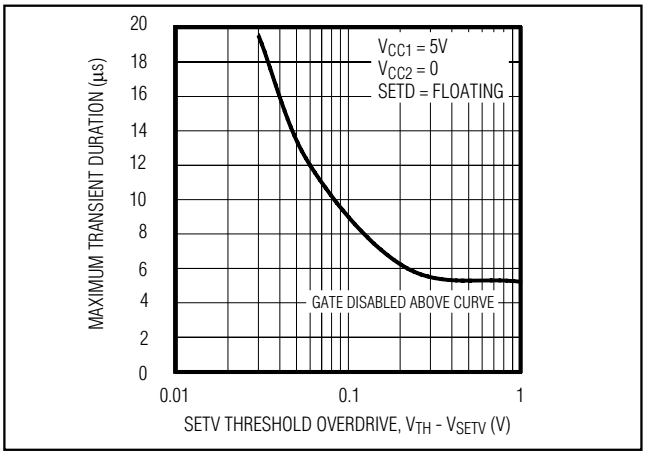

Figure 5. Maximum Transient Duration vs. SETV Threshold in Overdrive

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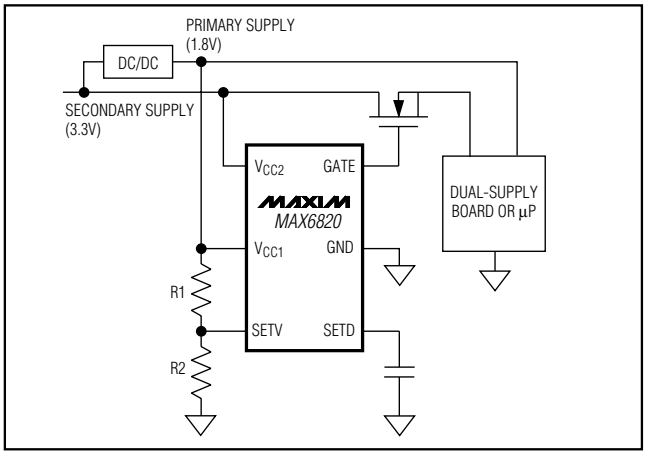
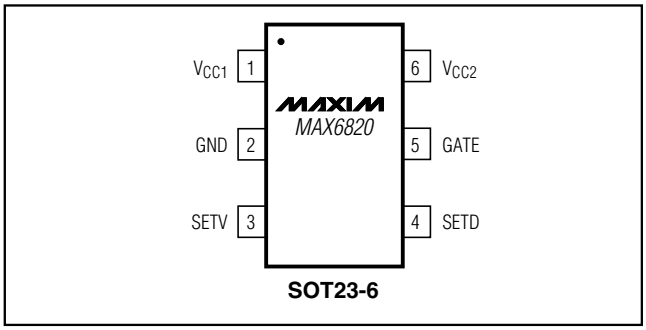
SOT23 Power-Supply Sequencers

Typical Operating Circuits (continued)



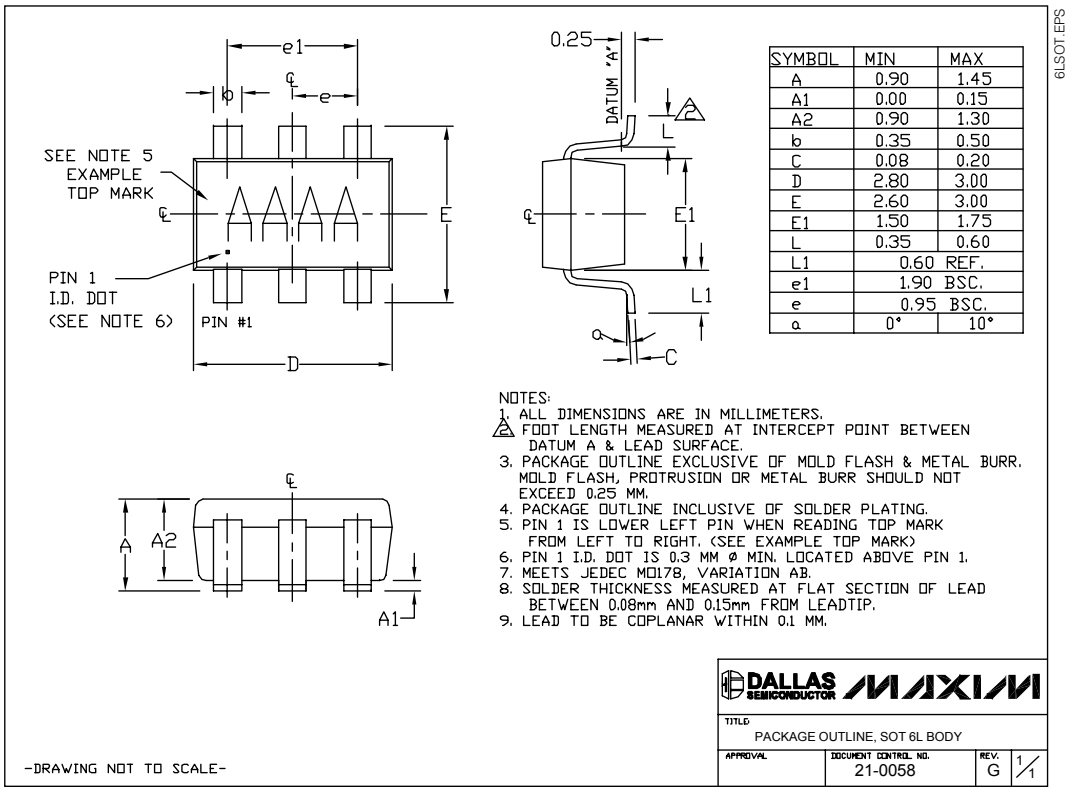
Pin Configurations (continued)



SOT23-6

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



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