Component List (continued)

DESIGNATION	QTY	DESCRIPTION
CLK, OUT	2	0.92in SMA PC edge-mount connectors Rosenberger 32K243-40ML5
GND	4	Black test points
H1, H2	2	Vertical 2 x 60 surface-mount high-speed socket connectors Samtec QSH-060-01-L-D-A
J1	1	8- pin (2 x 4) header
JU1, JU2, JU6–JU9	6	2-pin headers
JU3, JU5	2	4-pin headers
JU4	1	3-pin header
L1, L2, L3, L6	4	Chip-bead cores (1812) Panasonic EXC-CL4532U1
L4, L5	2	390nH wire-wound chip inductors (2520) Coilcraft 1008CS-391XJLB
R1, R12, R20, R22, R23	0	Not installed, resistors (0603)
R2, R11, R16, R19, R21	5	0Ω ±5% resistors (0603)
R3, R4	2	49.9Ω ±1% resistors (0402)
R5	1	499Ω ±1% resistor (0402)
R6	1	2.0kΩ ±1% resistor (0603)
R7–R10	4	10kΩ ±1% resistors (0603)
R13	1	133kΩ ±1% resistor (0603)
R14	1	80.6kΩ ±1% resistor (0603)
R15	1	100Ω ±1% resistor (0603)
R17, R18	2	27kΩ ±1% resistors (0402)
T1–T5	5	1:1 3000MHz RF transformers Mini-Circuits TC1-1-13M+
U1	1	14-bit, 2.3Gsps DAC (256 CSBGA) Maxim MAX5879EXF+D
U2	1	1.25V precision voltage reference (8 SO) Maxim MAX6161AESA+ or Maxim MAX6161BESA+
U3	1	Dual SPDT analog switch (6 SOT23) Maxim MAX4644EUT+
U4	1	3.3V LVDS clock driver (16 MLF) Micrel SY89876LMG (Top Mark: 876L)
U5, U7	2	500mA LDO regulators (8 TDFN-EP) Maxim MAX8902AATA+ (Top Mark: ABG)
U6	1	1A LDO regulator (16 TSSOP-EP) Maxim MAX1793EUE50+
U8	1	1.8V LDO regulator (16 TSSOP-EP) Maxim MAX1793EUE18+
—	13	Shunts (J1, JU1–JU9)
—	1	PCB: MAX5879 EVALUATION KIT

HSDCEP Assembly Components

QTY	DESCRIPTION
4	4-40 x 0.75in machine screws, pan
2	Nylon round spacers, M3 (OD - 6.35mm, ID = 3.18mm, L = 4.8mm)
2	4-40 hex-nut machine screws
6	Flat washer (ID - 0.12in, OD - 0.312in)
2	4-40 x 1-1/4 in aluminum hex standoffs
2	Nylon flat washers (ID - 0.14in, OD - 0.375in)

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corporation	843-946-0238	www.avx.com
Coilcraft, Inc.	847-639-6400	www.coilcraft.com
Mini-Circuits	718-934-4500	www.minicircuits.com
Panasonic Corp.	800-344-2112	www.panasonic.com
Rosenberger Hochfrequenztechnik GmbH	011-49-8684-18-0	www.rosenberger.de
Samtec, Inc.	800-726-8329	www.samtec.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX5879 when contacting these component suppliers.*

Quick Start

Required Equipment

- MAX5879 EV kit
- One 3.6V, 2A power supply
- Signal generator with low phase noise and low jitter for clock input signal (e.g., Rohde and Schwarz SMF100A)
- Bandpass filters for clock input (optional)
- High-performance spectrum analyzer (e.g., Rohde and Schwarz FSU or Agilent PXA)
- Maxim HSDCEP data source board (optional)

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation. **Caution: Do not turn on the power supplies or signal sources until all connections are completed.**

1) Verify that shunts are configured in the following default positions:

JU1, JU2:	Installed (on-board reference enabled)
JU3 (1-2), JU5 (1-4):	f_{CLK} frequency range = 2150MHz to 2304MHz
JU4 (1-2):	External clock divider disabled
J1 (1-2), J1 (7-8):	Not installed (NRZ mode)
J1 (3-4):	Installed (internal clock divider enabled)
J1 (5-6):	Not installed 2:1 (mux mode)
JU6, JU7, JU8:	Installed (on-board supply regulators connected to the device)
JU9:	Installed (on-board supply regulator connected to external clock divider/buffer)

2) Set the 3.6V DC power supply to 3.6V and disable the power-supply output.
3) Connect the 3.6V DC power supply to the VIN and GND PCB pads.
4) Connect the HSDCEP data source board's J5 and J6 connectors to the EV kit's H1 and H2 connectors, respectively.
5) Connect the spectrum analyzer to the EV kit SMA connector labeled OUT.
6) Connect the clock-signal generator to the EV kit SMA connector labeled CLK.
7) Enable the DC power supply.
8) Enable the clock-signal generator.
9) Enable the HSDCEP data source board using the supplied EV kit firmware. Refer to the HSDCEP User's Guide for instructions on configuring the HSDCEP for operation.
10) Observe the output spectrum on the spectrum analyzer.

Detailed Description of Hardware

The MAX5879 EV kit is a fully assembled and tested PCB that contains all the components necessary to evaluate the performance of the MAX5879 14-bit, 2.3Gsps direct RF synthesis DAC. The EV kit operates with either LVDS or D-HSTL data inputs, a single-ended clock input signal, and a single 3.6V, 2A power supply for simple board operation.

The device is a high-performance, 14-bit, current-steering DAC with an integrated 50Ω differential output termination to the device's AVDD3.3 supply. The device has four 14-bit multiplexed, low-voltage differential signaling (LVDS) input ports, and includes a DCLK output for synchronization with the data source, as well as SYNC and parity input bits. The data interface is configurable to operate in either single-data rate (SDR) or double-data rate (DDR) modes, and either 2:1 or 4:1 input mux mode. The device integrates a delay-locked loop (DLL) to ease the interface required for FPGA or ASIC data sources.

The EV kit features on-board QSH connectors that interface directly to the Maxim HSDCEP data source board. The HSDCEP drives the device's LVDS inputs and controls the DLLOFF multiplexer using an SPDT analog switch (U3). The EV kit contains circuitry that converts the differential 50Ω output to a single-ended 50Ω signal, and circuitry to convert a user-supplied single-ended clock signal to a differential clock. The EV kit includes jumpers that configure the frequency-response mode, the reference voltage, data clock, and DLL/delay settings. The EV kit includes an external buffer/divider clock circuit to ease the interfacing of data sources.

Power Supplies

The EV kit operates from a single 3.6V power supply applied at the VIN and GND PCB pads. VIN provides the power necessary for operating two 3.3V LDO regulators (U6, U7) and two 1.8V LDO regulators (U5, U8) used for on-board regulation of the device's AVDD3.3, VDD1.8, and AVCLK inputs and clock divider (U4) VCC input. The EV kit also provides the option of using external power supplies to power the device inputs or for monitoring the input supply current. See Tables 1–4 for proper shunt settings for the EV kit power-supply inputs.

Table 1. AVDD3.3 Input Power Configuration (JU6)

SHUNT POSITION	AVDD3.3 INPUT SOURCE
Installed*	3.3V LDO (U6) power source for the device's AVDD3.3 input.
Not installed	External supply applied at the AVDD3.3V and GND test points.

**Default position.*

Table 2. VDD1.8 Input Power Configuration (JU7)

SHUNT POSITION	VDD1.8 INPUT SOURCE
Installed*	1.8V LDO (U5) powers the device's VDD1.8 input.
Not installed	External supply applied at the VDD1.8V and GND test points.

**Default position.*

Table 3. AVCLK Input Power Configuration (JU8)

SHUNT POSITION	AVCLK INPUT SOURCE
Installed*	1.8V LDO (U8) output powers the device's AVCLK input.
Not installed	External supply applied at the AVCLK and GND PCB test points.

**Default position.*

Table 4. U4 Input Power Configuration (JU9)

SHUNT POSITION	U4 INPUT SOURCE
Installed*	3.3V LDO (U7) powers clock divider (U4) IC.
Not installed	External supply applied at the ACLKDIV and GND PCB test points.

**Default position.*

Table 5. Reference Voltage Selection (JU1, JU2)

SHUNT POSITIONS		VOLTAGE REFERENCE MODE
JU1	JU2	
Installed*	Installed*	External 1.25V reference (U2) connected to the device's REFIO pin.
Not installed	Not installed	The device's internal 1.2V bandgap reference or user-supplied voltage reference at the REFIO PCB pad (0.5V to 1.8V).

**Default position.*

Clock Signal

The device requires a differential clock input signal with minimal jitter. The EV kit features single-ended-to-differential-conversion circuitry. Supply a single-ended clock signal at the CLK SMA connector. The power applied to the SMA connector should be between 10dBm and 13dBm when measured at the connector. Insertion losses due to the interconnecting cable decrease the power seen at the EV kit input. Account for these losses when setting the signal-generator amplitude.

Reference Voltage Options

The device requires a reference voltage to set the DAC output power. The DAC features a stable on-chip bandgap reference of 1.2V. The internal reference can be overdriven by an external reference to enhance accuracy and drift performance, or for gain control.

The EV kit features multiple reference options. Use the device's internal voltage reference by removing the shunts on jumpers JU1 and JU2. Use an external reference by removing the shunts on JU1 and JU2 and connecting a stable voltage reference at the REFIO PCB pad. Install shunts on JU1 and JU2 to use the EV kit's on-board 1.25V reference, MAX6161 (U2). See Table 5 to configure the shunts on JU1 and JU2 and select the source of the reference voltage.

The DAC full-scale output current is limited to 80mA and is set by the reference voltage and resistor R6. Use the equation below to calculate the DAC full-scale output current:

$$I_{OUT} = 128 \times \left(\frac{V_{REFIO}}{R6} \right) [A]$$

where:

I_{OUT} = DAC full-scale output current,

V_{REFIO} = Voltage present at the REFIO PCB pad in volts (1.2V if using the device's internal reference),

R6 = Value of resistor R6 in ohms (2kΩ default).

The 80mA full-scale output current results in a maximum continuous-wave (CW) output power of 9dBm.

Refer to the *Reference System* section in the MAX5879 IC data sheet for additional information.

Data Interface Operating Modes

The EV kit supports both single data-rate (SDR) and double data-rate (DDR) data interfaces depending on the EV kit various jumper configurations. Header J1 configures the EV kit for mux mode operation, sets the data clock (DCLK) output frequency, and sets the DAC impulse/frequency-response mode.

Mux Mode and DCLK Frequency Configuration

The EV kit can be configured for 2:1 or 4:1 input mux mode operation using header J1. When configured for 2:1 input mux mode, the device accepts data on ports B and C only. When configured for 4:1 input mux mode, except RFZ mode, the device accepts data on all ports. The device only accepts data on ports A and C when configured for RFZ mode.

The device's LVDS-level data clock outputs (DCLKP, DCLKN) synchronize the data source and the DAC during normal operation. The input clock-signal frequency (f_{CLK}) applied at the CLK SMA connector is divided internally to create the internal clock used to latch input data. The DCLK output frequency of (f_{DCLK} frequency) is determined by the mux mode configuration and the state of the DCLKDIV input. SDR mode is enabled when DCLKDIV is low ($f_{CLK}/4$). DDR mode is enabled when DCLKDIV is high.

See Table 6 for proper jumper configuration for setting the input mux mode and DCLK_ output frequency.

Additional circuitry (U4, JU4) is available and provides a separate divide-by-2 scaling down of the DCLK_ frequency to ease the interfacing of various data sources. See the *Data Clock Frequency for HSDCEP Operation* section for additional information.

Refer to the *Data Input s*ection in the MAX5879 IC data sheet for additional information.

DAC Impulse/Frequency-Response Modes

The device features four impulse/frequency-response modes (NRZ, RZ, RFZ, and RF). Refer to the *DAC Impulse/Frequency-Response Modes* section in the MAX5879 IC data sheet for additional information. Shunts placed across header J1, pins 1-2 and pins 7-8 control the active impulse-response mode. See Table 7 for proper jumper settings.

DLLOFF/Delay Frequency Selection (JU5, JU3)

Jumpers JU3 and JU5 are used for enabling/disabling the device's DLL function and selecting the device's DLL operating frequency range. The DLL frequency (f_{DLL}) is also dependent on the mux-mode configuration. See Table 8 for proper jumper configuration of JU3 and JU5. Refer to the *DLL Frequency Selection and 4-Level Input* and *Data Inputs* sections in the MAX5879 IC data sheet for additional information.

Differential Output

The DAC features a differential output with built-in output termination resistors. The EV kit pulls the outputs up to AVDD3.3 through on-board bias inductors L4 and L5 to optimize performance of the device. Balun transformers T4 and T5 convert the differential signal to a single-ended signal. Measure the resulting DAC output at the OUT SMA connector. When generating signals in excess of 1.5GHz, it is recommended that transformer T5 be removed.

Table 6. MUX Mode and DCLK Frequency Setting (J1)

SHUNT POSITION		INPUT MUX MODE	DCLK FREQUENCY
J1(5-6) → MUX	J1 (3-4) → DCLKDIV		
Not installed*	Not installed*	2:1	$f_{DCLK} = f_{CLK}/2$ (SDR)
Not installed	Installed		$f_{DCLK} = f_{CLK}/4$ (DDR)
Installed	Not installed	4:1	$f_{DCLK} = f_{CLK}/4$ (SDR)
Installed	Installed		$f_{DCLK} = f_{CLK}/8$ (DDR)

**Default position.*

Table 7. Frequency-Response Selection (J1)

SHUNT POSITION		OPERATING MODE
J1 (7-8) → RZ	J1 (1-2) → RF	
Not installed	Not installed	NRZ mode*
Installed	Not installed	RZ mode
Not installed	Installed	RF mode
Installed	Installed**	RFZ mode**

**Default position.*

***Only valid when the device is configured in 4:1 input mux mode.*

Table 8. DLLOFF/DELAY (JU5, JU3)

MUX MODE	SHUNT POSITION			MAX5879 f_{CLK} (MHz)	f_{DLL} (MHz)	EV KIT OPERATION
	J1 (5-6)	JU5 (DLLOFF)	JU3 (DELAY)			
2:1	Not installed	1-2	1-2	—	—	DLL disabled (one f_{CLK} period delay added to the DCLKP/DCLKN outputs)
		1-2	1-4	—	—	DLL disabled (no delay added to the DCLKP/DCLKN outputs)
		1-4*	1-2*	2150 to 2300	1075 to 1150	DLL enabled
		1-4	Not installed	1900 to 2150	950 to 1075	
		Not installed	1-4	1650 to 1900	825 to 950	
		Not installed	1-2	1400 to 1650	700 to 825	
		Not installed	Not installed	1250 to 1400	625 to 700	
		1-3	1-4	1100 to 1250	550 to 625	
		1-3	1-2	950 to 1100	475 to 550	
		1-3	Not installed	800 to 950	400 to 475	
4:1	Installed	1-3	1-4	2200 to 2300	550 to 575	
		1-3	1-2	1900 to 2200	475 to 550	
		1-3	Not installed	1600 to 1900	400 to 475	

Note: *Reset the DLL circuitry at power-up and each time the frequency range is changed. Set DLLOFF to high (install a shunt on pins 1-2 of jumper JU5) prior to selecting the range to perform the reset.*

**Default position.*

Using the HSDCEP Data Source Board with the EV Kit

The HSDCEP can be used as a high-speed data source for the EV kit. Test patterns can be generated using a PC and can be uploaded to the HSDCEP for evaluation of the device. An EV kit-specific firmware load is required to configure the HSDCEP. Refer to the *HSDCEP User's Guide* for specific system requirements, software installation instructions, loading configuration file, and data-pattern format.

Digital Logic Inputs

The EV kit's QSH connectors (H1 and H2) are used to connect to the HSDCEP data source board. Connectors H1 and H2 are also used to control the device's LVDS inputs (XORP, XORN), LVDS parity bit inputs (PARP, PARN), and SYNCP and SYNCN inputs. Refer to the *XOR and Parity Inputs* section in the MAX5879 IC data sheet for additional information.

Data Clock Frequency for HSDCEP Operation

The HSDCEP requires the data clock frequency to be $f_{CLK}/4$ or $f_{CLK}/8$. Additional circuitry (U4, JU4) is available and provides a separate divide-by-2 scaling down of the f_{DCLK} frequency to ease the interfacing of various data sources. See Table 6 to determine if the frequency requires additional scaling. Install a shunt on pins 1-2 on jumper JU4 to set the HSDCEP clock frequency to the EV kit current f_{DCLK} frequency setting. Install a shunt on pins 2-3 to set the HSDCEP clock frequency signal to one-half the programmed f_{DCLK} frequency. See Table 9 for proper jumper configuration.

Table 9. HSDCEP Frequency Setting (JU4)

SHUNT POSITION	HSDCEP FREQUENCY
1-2*	$f_{HSDCEP} = f_{DCLK}$
2-3	$f_{HSDCEP} = f_{DCLK}/2$

**Default position.*

Connecting the HSDCEP to the EV Kit

The HSDCEP and EV kit boards can be connected using the hardware supplied with the EV kit. See Figure 1 for details on connecting the boards together. Alternatively, the two boards can be connected with coaxial ribbon cables (Part No. HQCD-060-06.00-STR-TBR-1). Note that it is necessary to use the supplied hardware or cables to get a reliable electrical connection between the two boards.

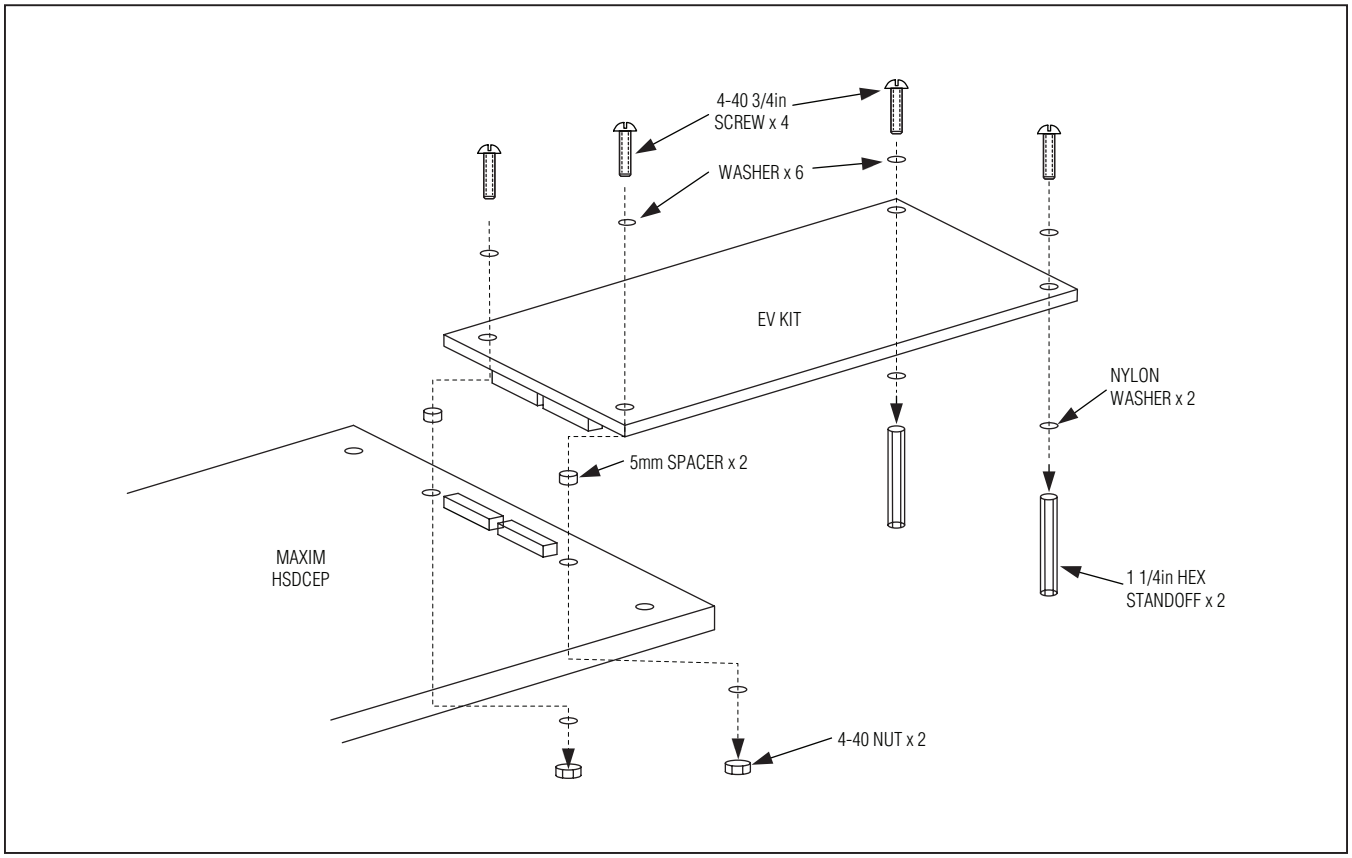


Figure 1. Connection of HSDCEP to MAX5879 EV Kit

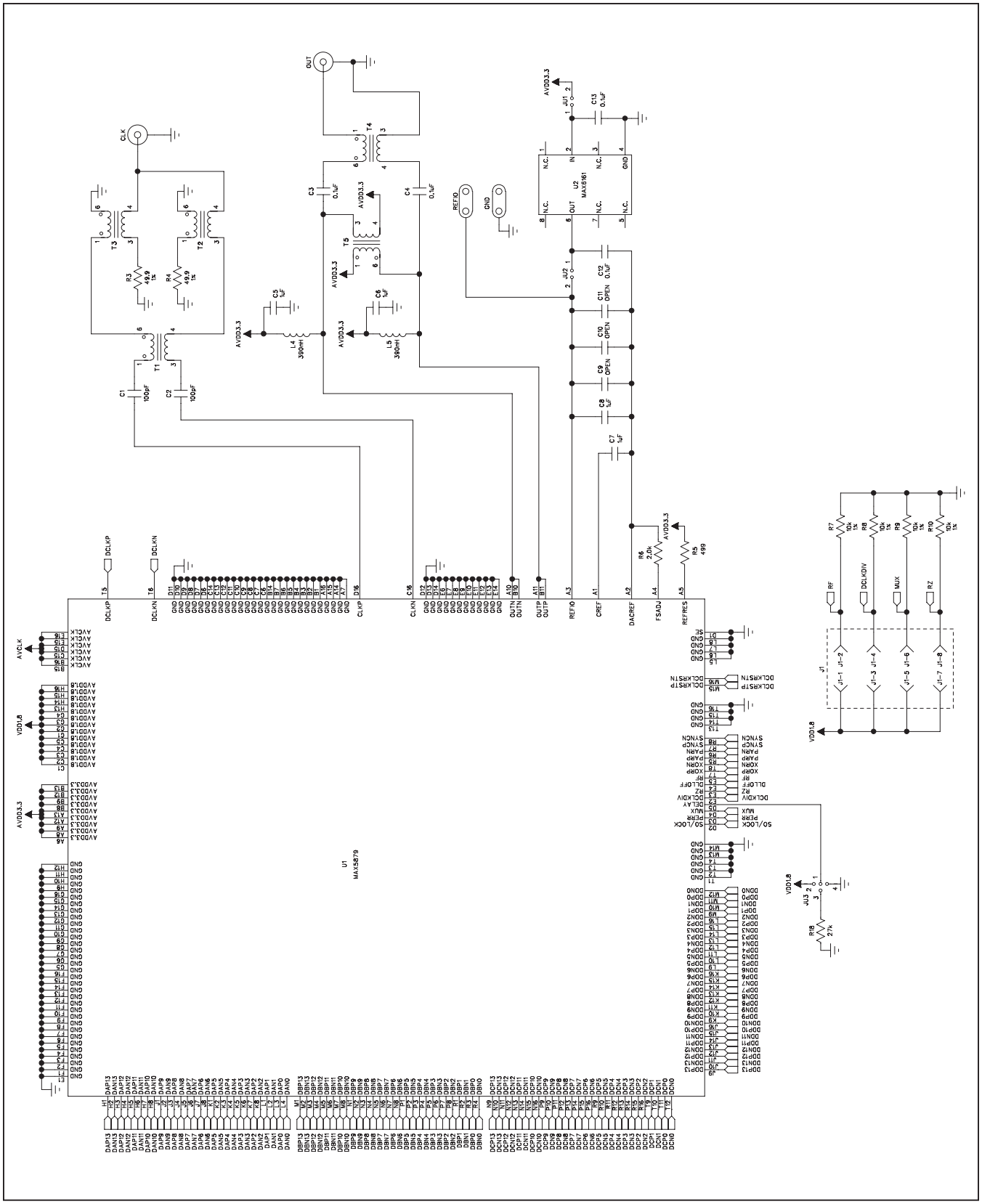


Figure 2a. MAX5879 EV Kit Schematic (Sheet 1 of 3)

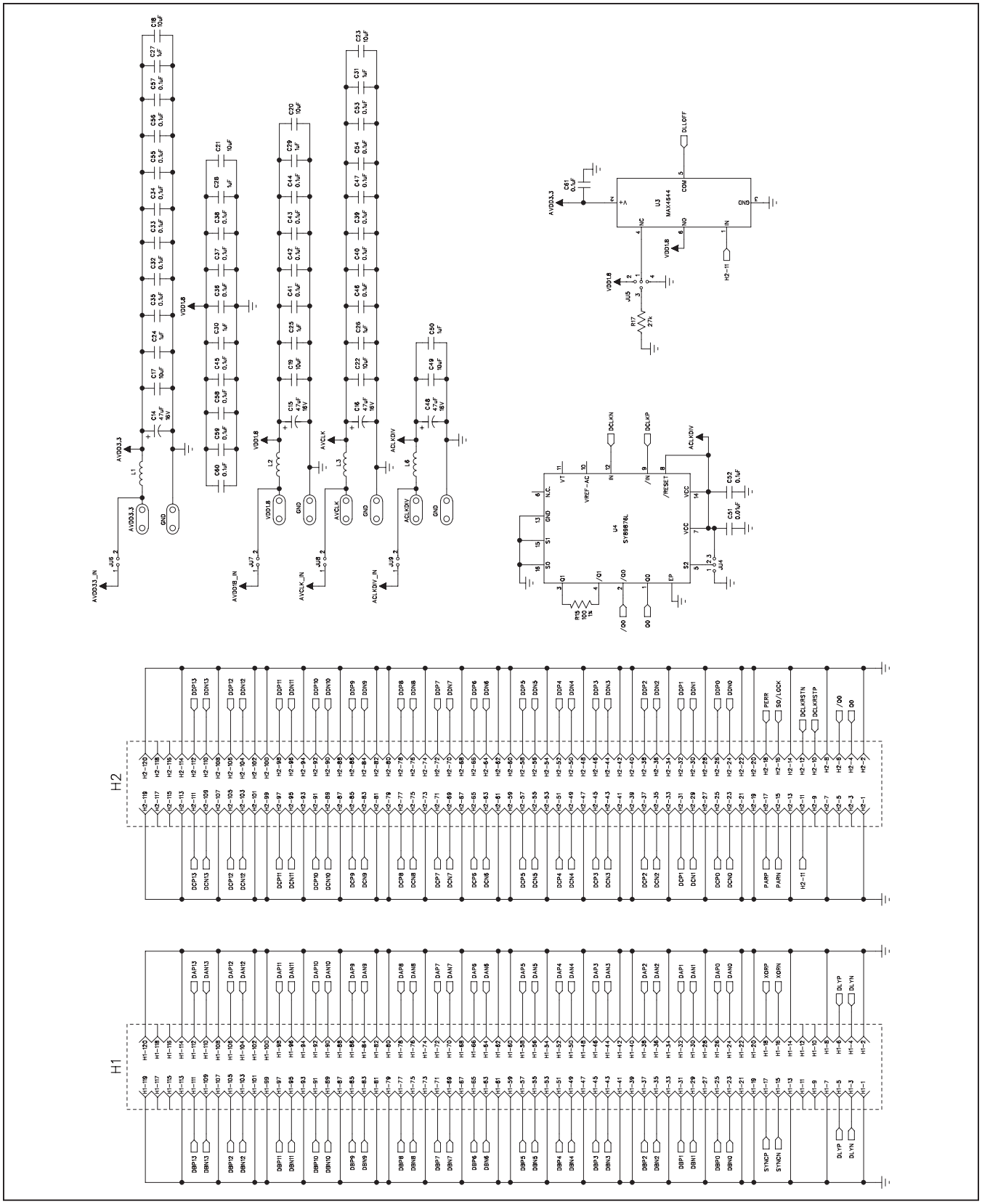
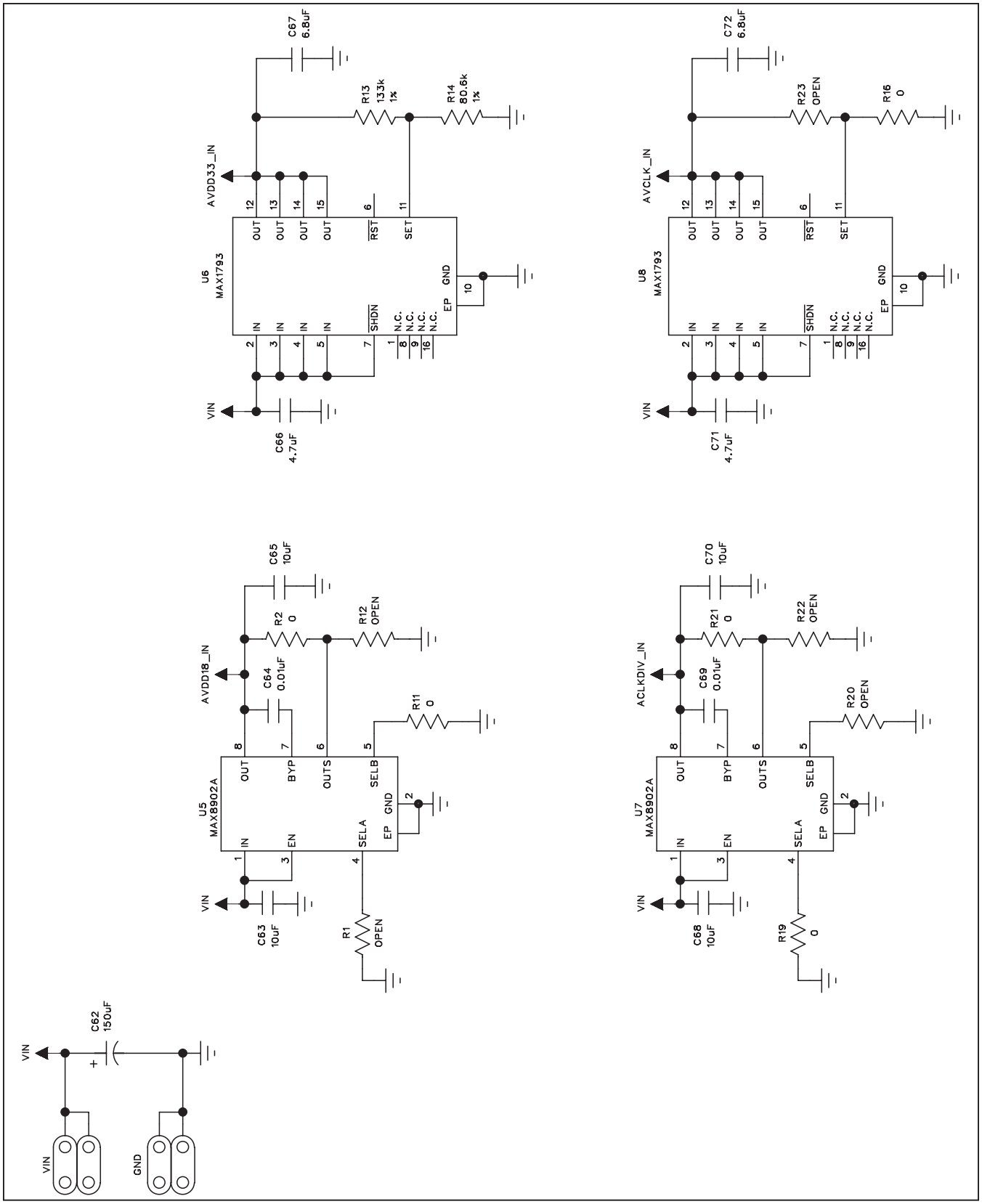


Figure 2b. MAX5879 EV Kit Schematic (Sheet 2 of 3)



Figeure 2c. MAX5879 EV Kit Schematic (Sheet 3 of 3)

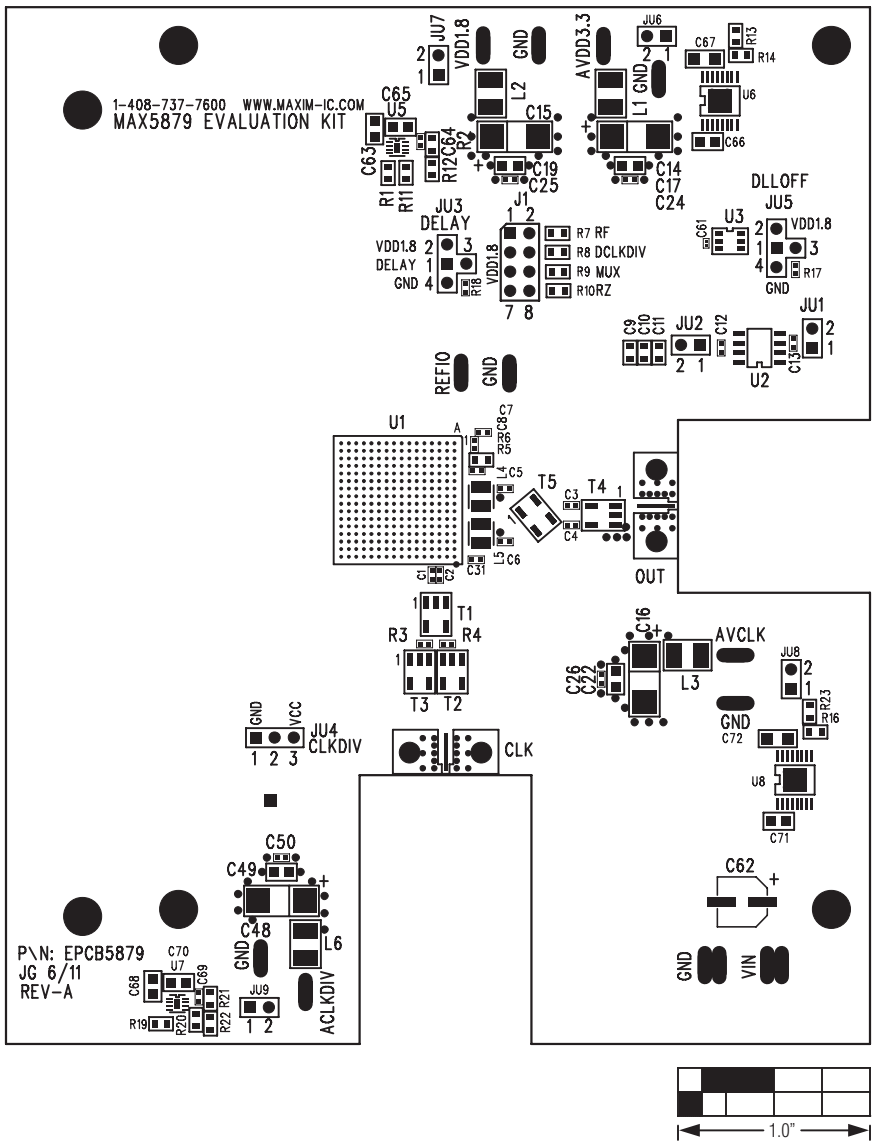


Figure 3. MAX5879 EV Kit Component Placement Guide—Component Side

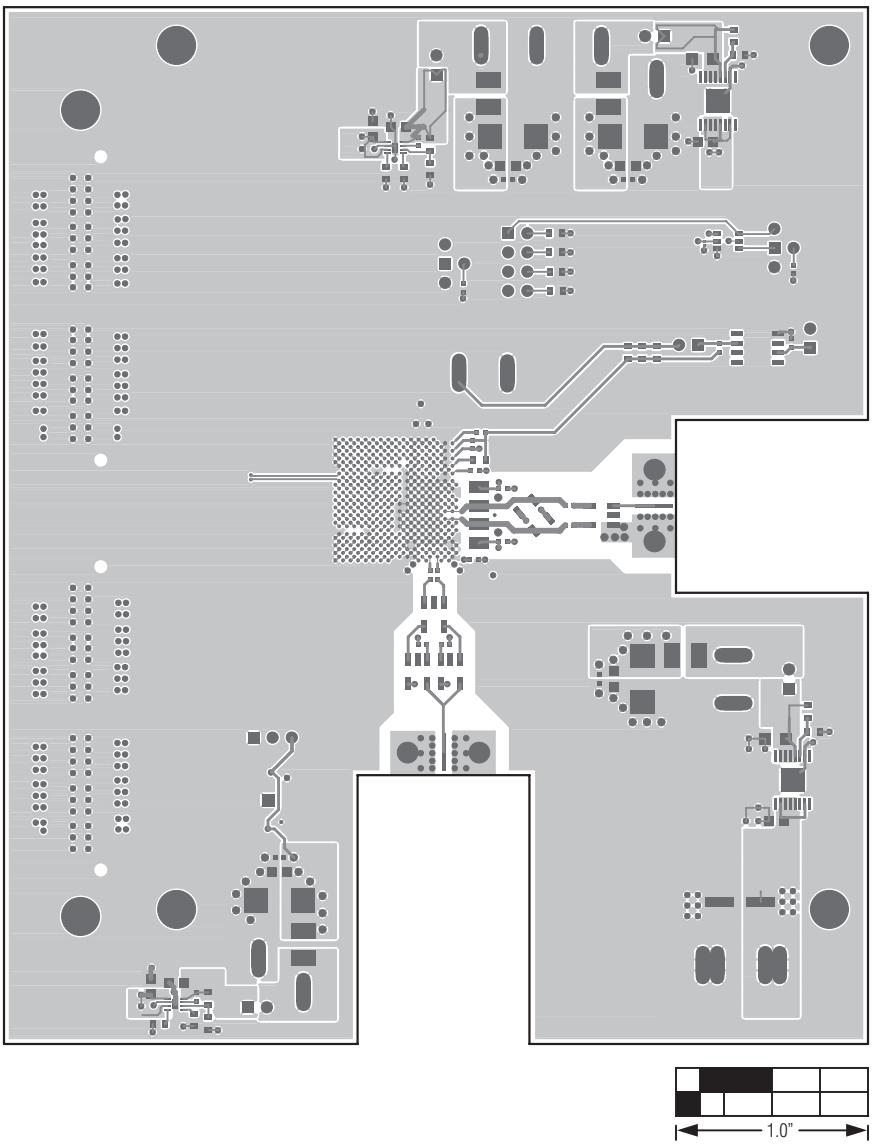


Figure 4. MAX5879 EV Kit PCB Layout—Component Side

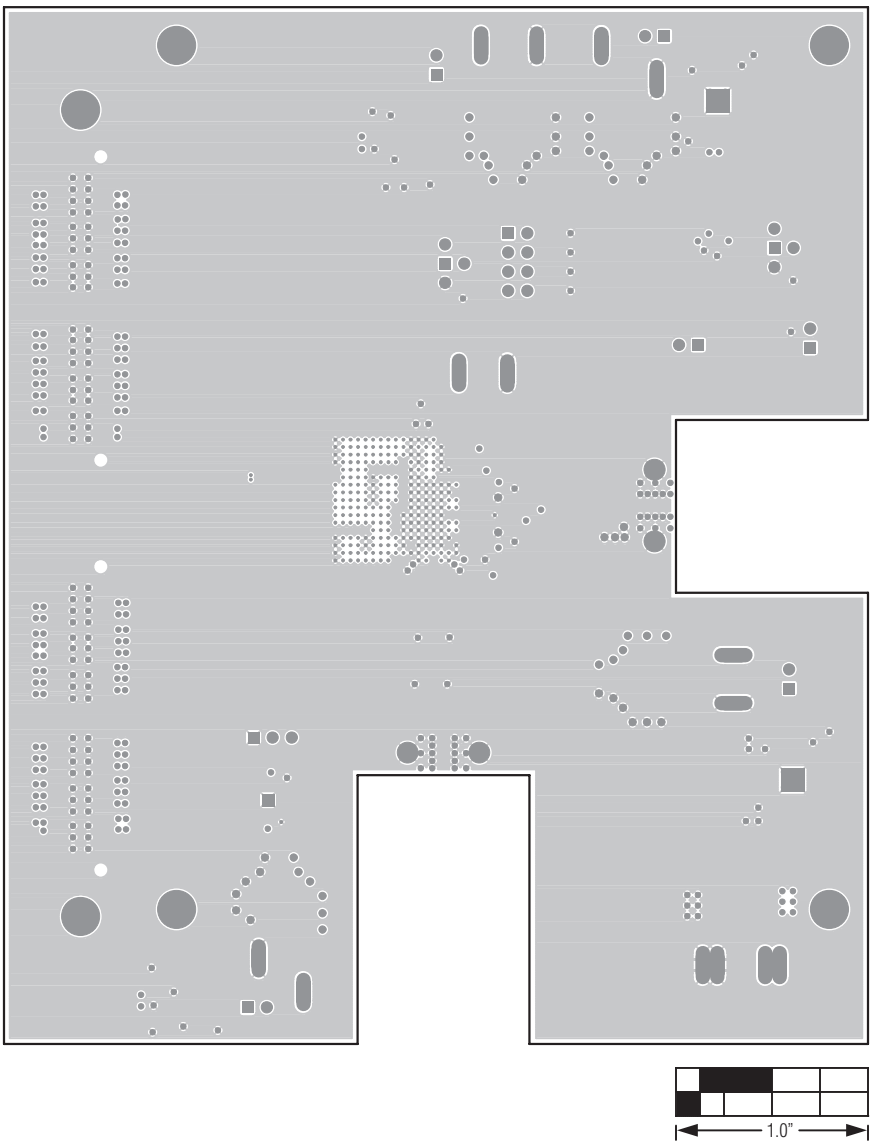


Figure 5. MAX5879 EV Kit PCB Layout (Inner Layer 2)—Ground Plane

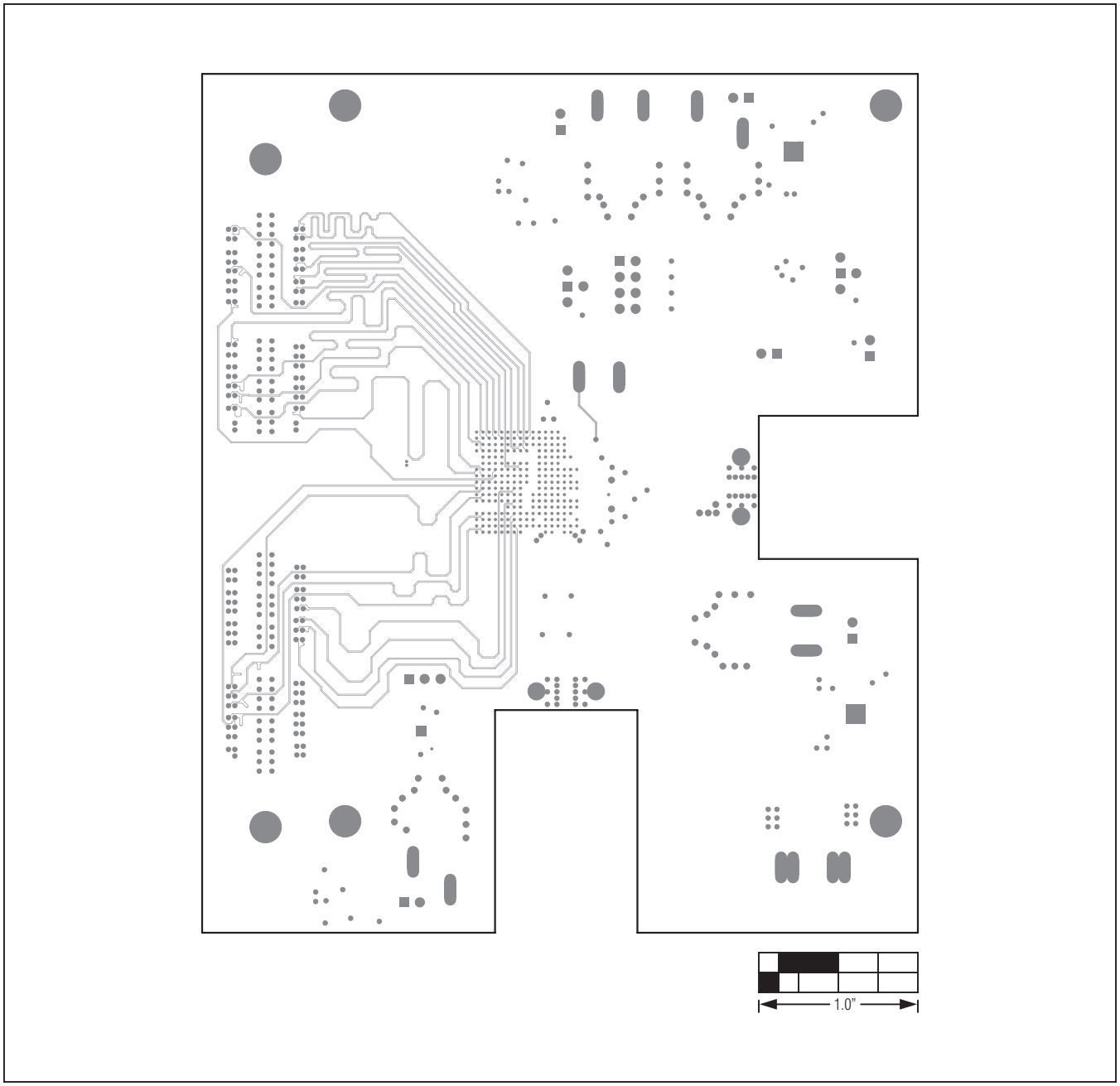


Figure 6. MAX5879 EV Kit PCB Layout (Inner Layer 3)—Signals

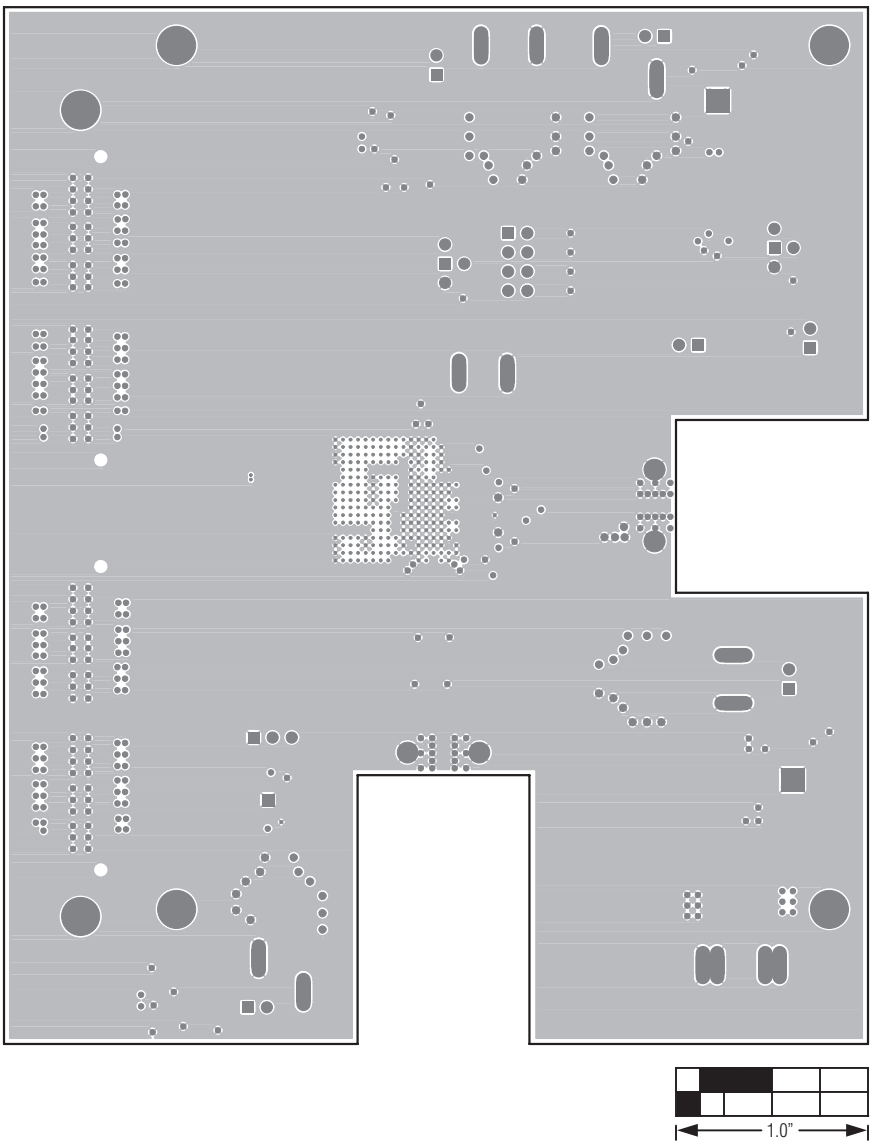


Figure 7. MAX5879 EV Kit PCB Layout (Inner Layer 4)—Ground Plane

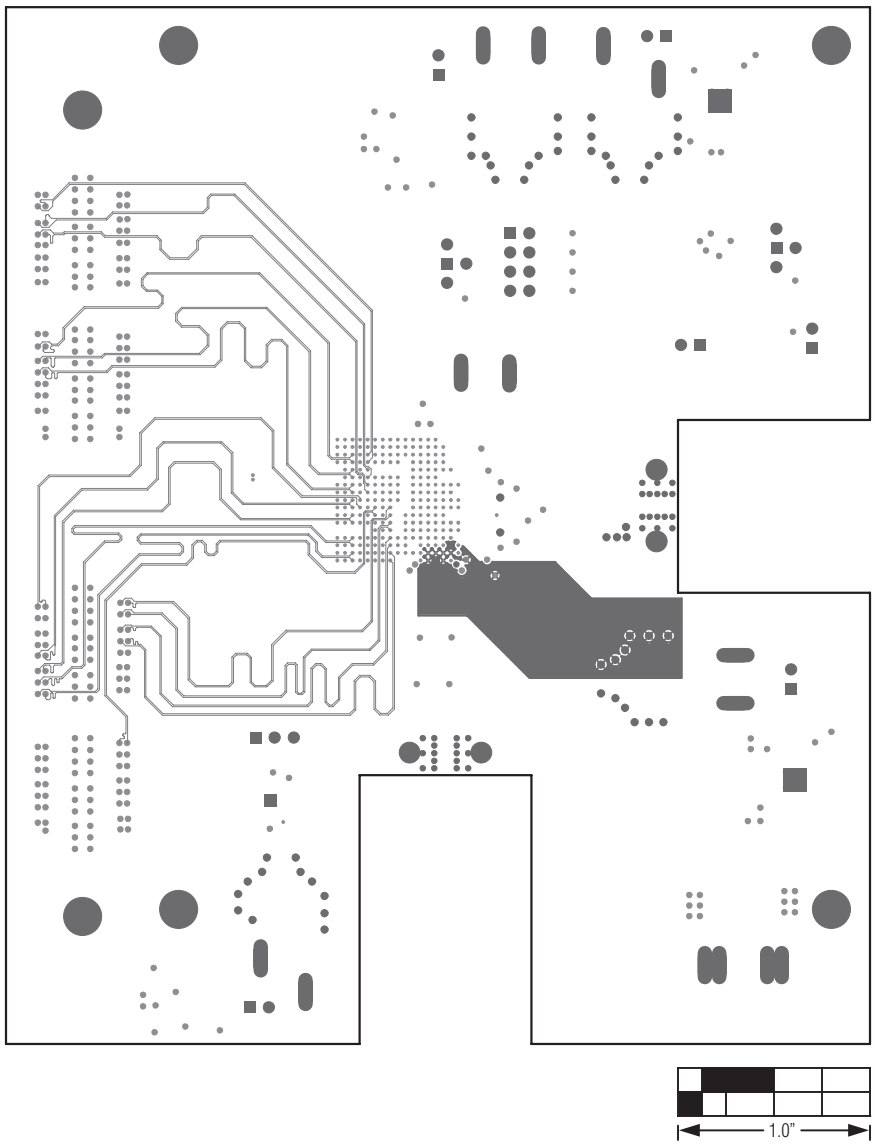


Figure 8. MAX5879 EV Kit PCB Layout (Inner Layer 5)—Signals

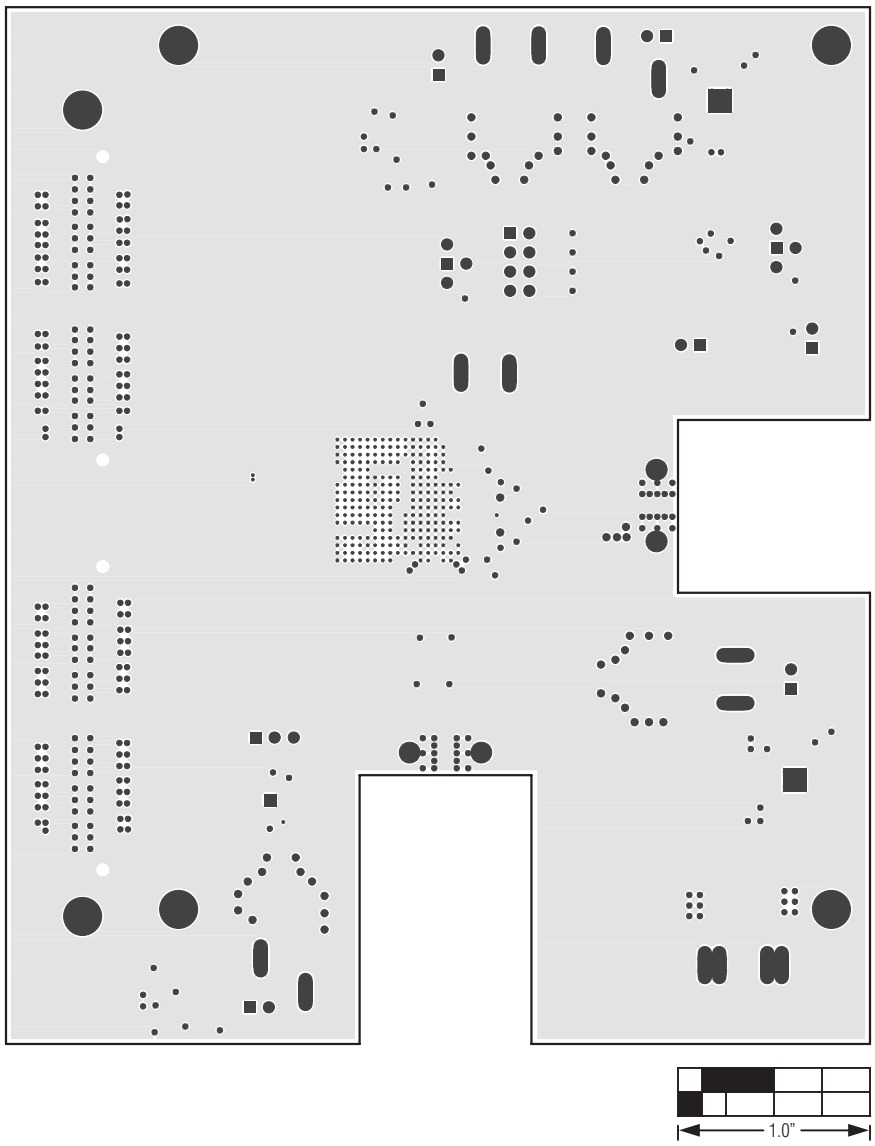


Figure 9. MAX5879 EV Kit PCB Layout (Inner Layer 6)—Ground Plane

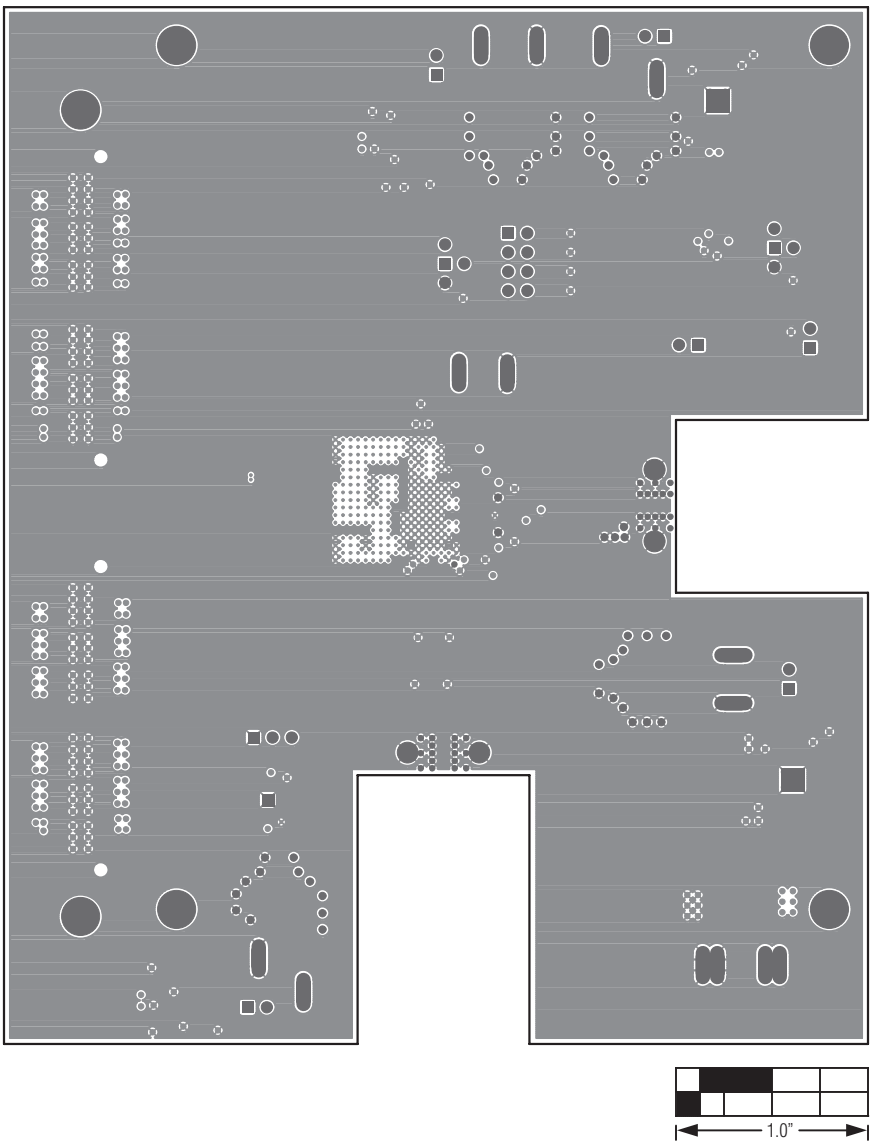


Figure 10. MAX5879 EV Kit PCB Layout (Inner Layer 7)—Ground Plane

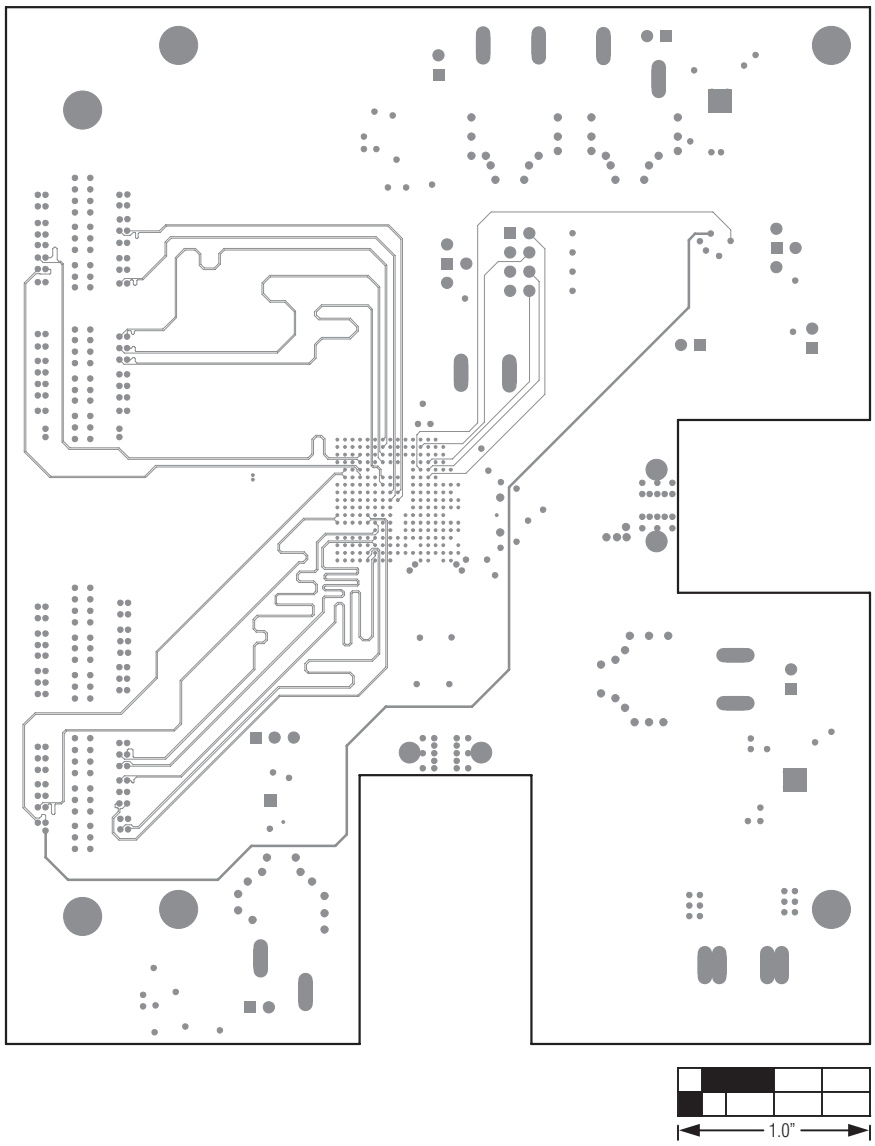


Figure 11. MAX5879 EV Kit PCB Layout (Inner Layer 8)—Signals

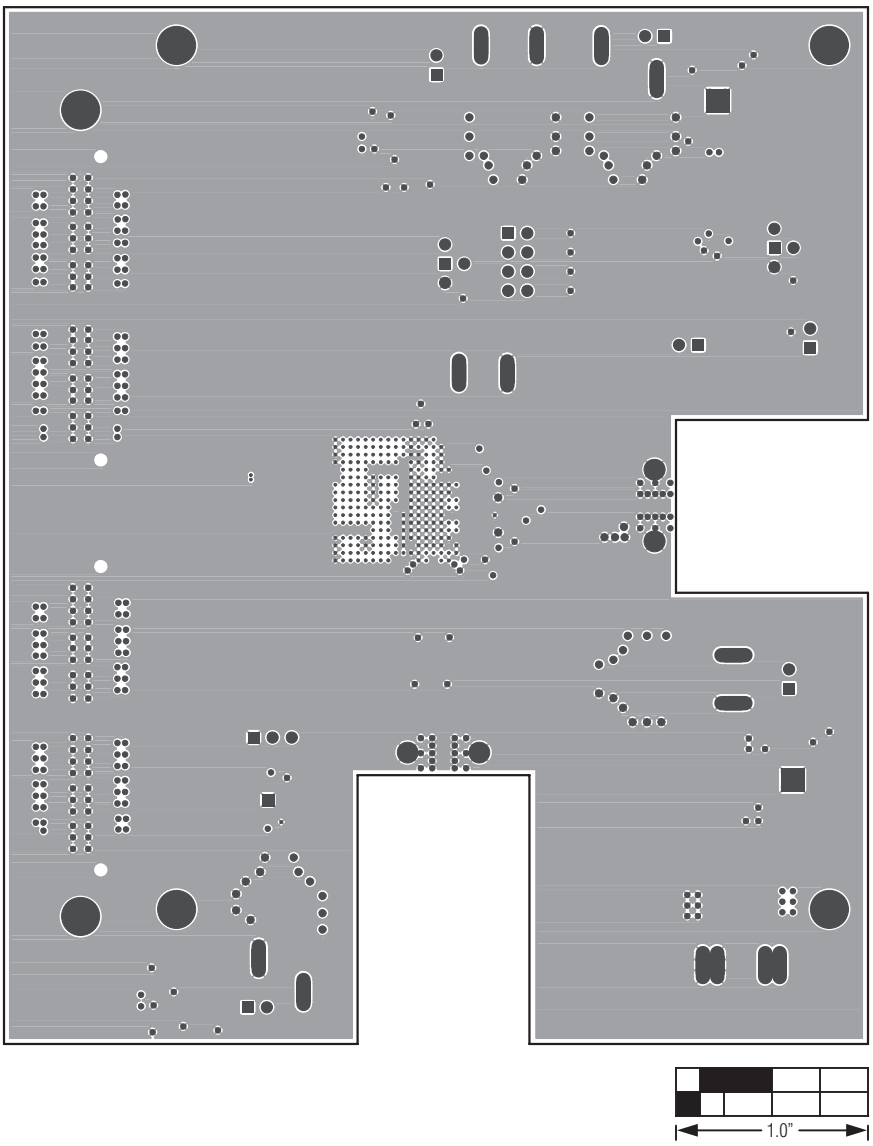


Figure 12. MAX5879 EV Kit PCB Layout (Inner Layer 9)—Ground Plane

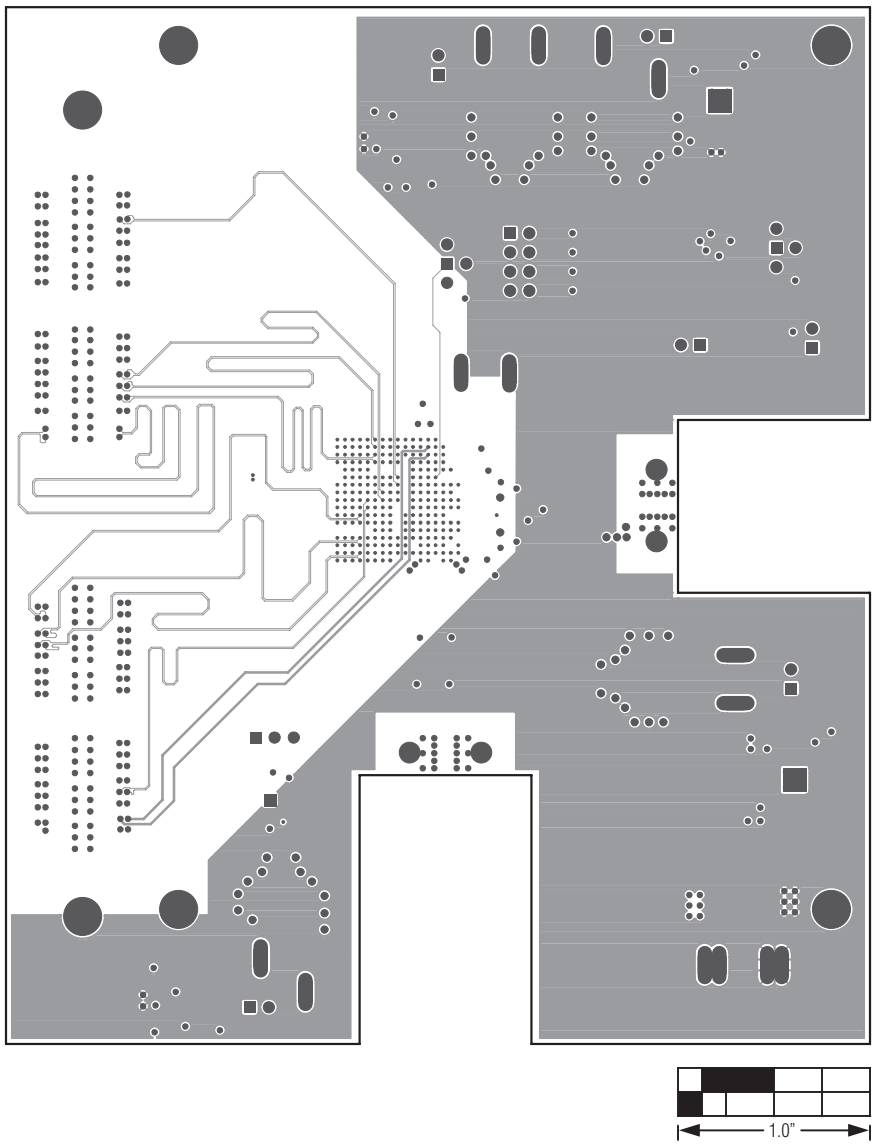


Figure 13. MAX5879 EV Kit PCB Layout (Inner Layer 10)—Signals

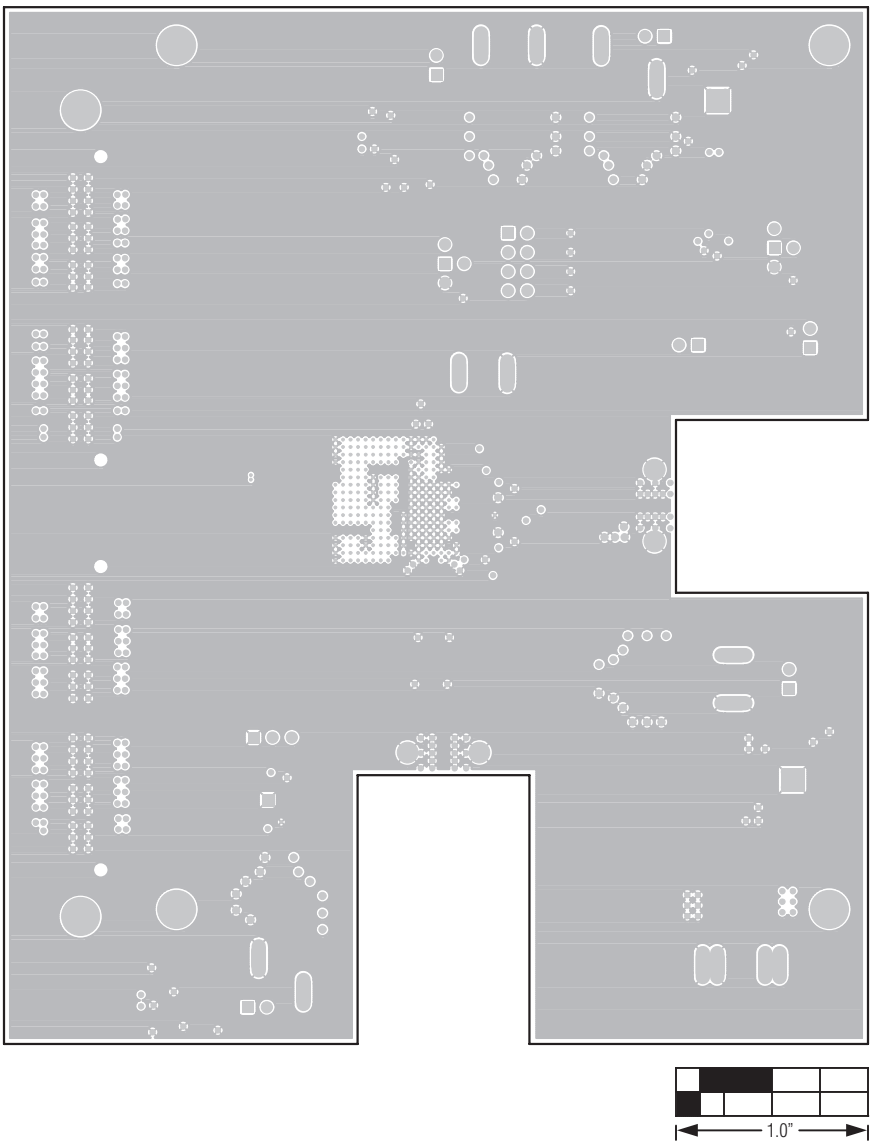


Figure 14. MAX5879 EV Kit PCB Layout (Inner Layer 11)—Ground Plane

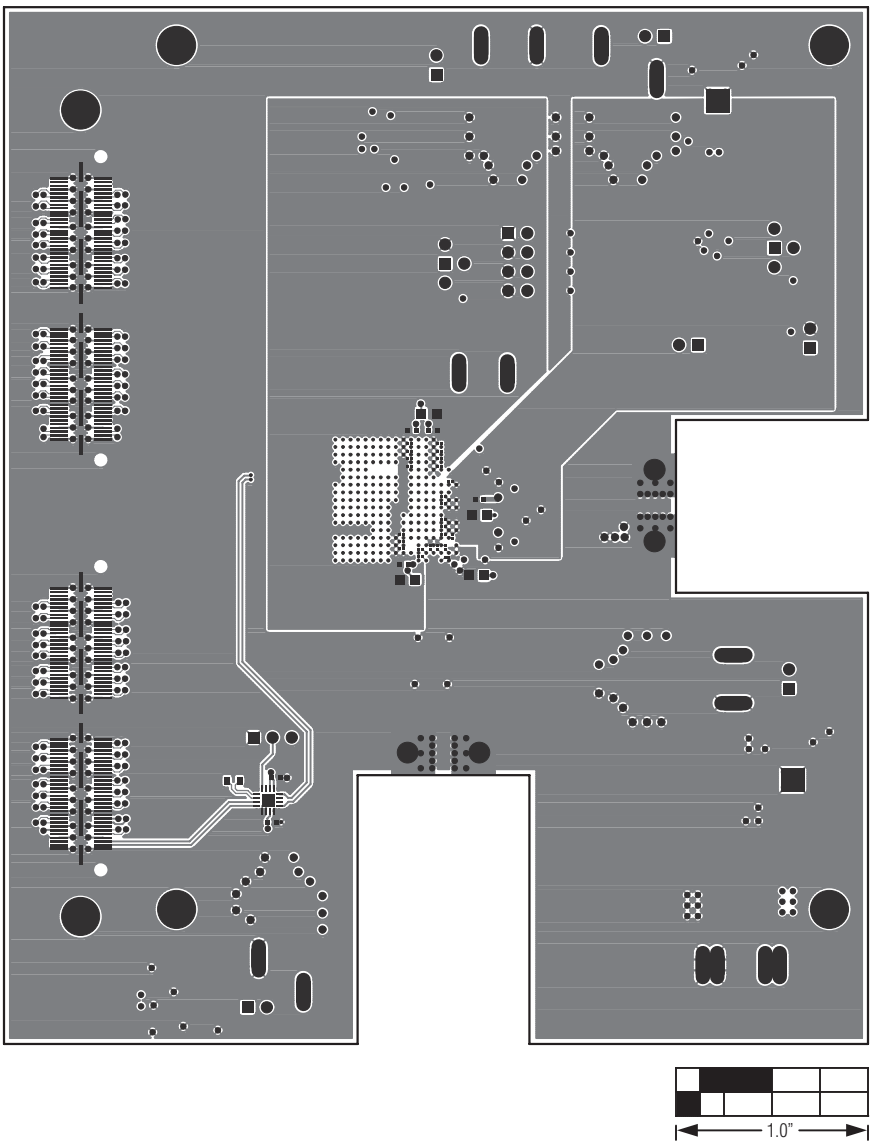


Figure 15. MAX5879 EV Kit PCB Layout—Solder Side

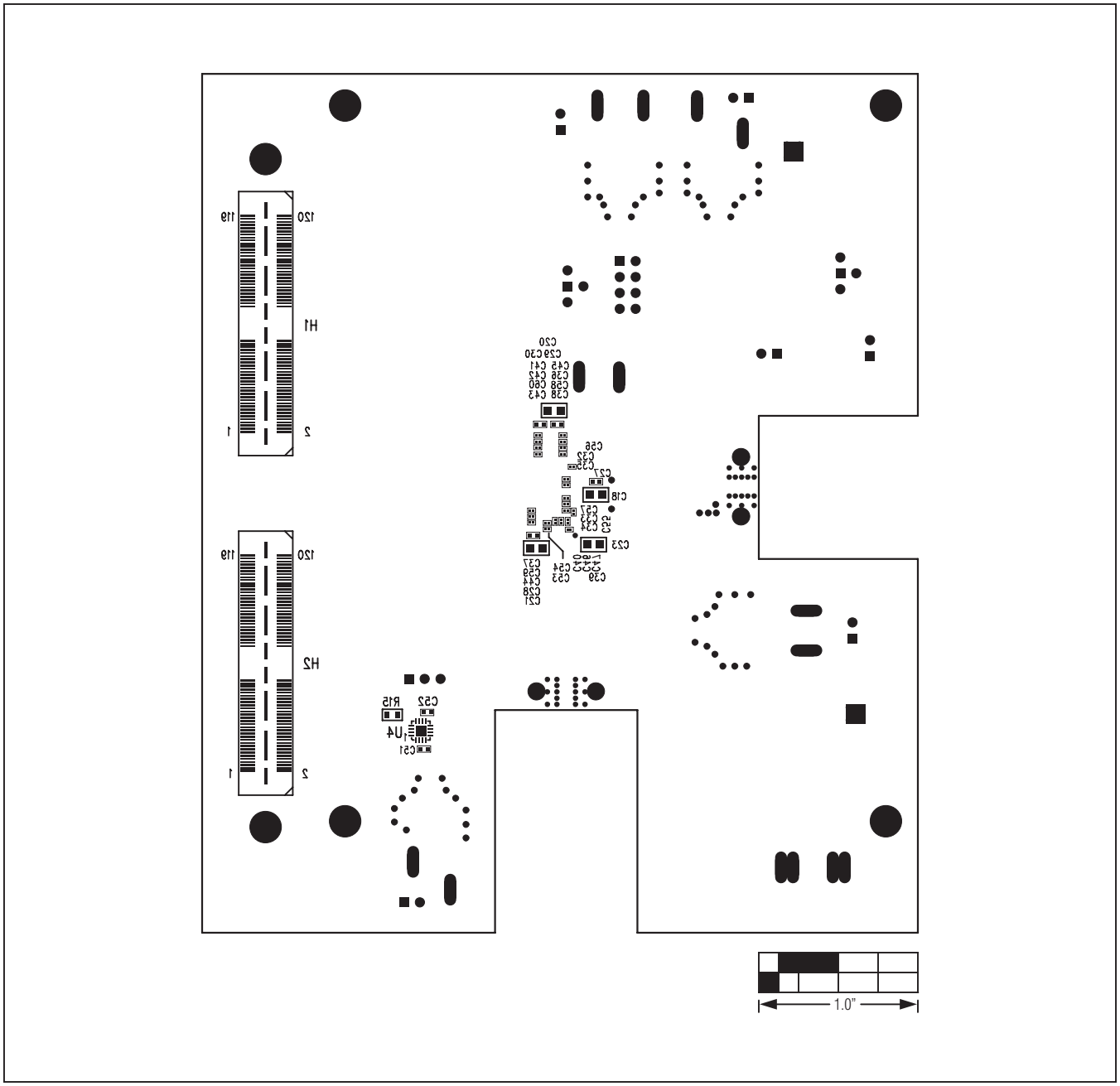


Figure 16. MAX5879 EV Kit Component Placement Guide—Solder Side

Ordering Information

PART	TYPE
MAX5879EVKIT#	EV Kit
HSDCEP	High-Speed Data Converter Evaluation Platform

#Denotes RoHS compliant.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/11	Initial release	—