+2.7V to +5.5V, Low-Power, Dual, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
D_, A0, $\overline{WR}$, SHDN to GND ....-0.3V to +6V
REF to GND ....-0.3V to (V_{DD} + 0.3V)
OUT_ to GND ....-0.3V to V_{DD}
Maximum Current into Any Pin ....±50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 5.7mW/°C above +70°C) 457mW
Operating Temperature Range
MAX5102_EUE ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{REF} = +2.7V to +5.5V, GND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = V_{REF} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution						8	Bits
Integral Nonlinearity (Note 1)	INL	MAX5102A				±1	LSB
		MAX5102B				±2	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex				±20	mV
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 2.7V to 5.5V				10	mV
Zero-Code Temperature Coefficient		Code = 00 hex			±10		µV/°C
Gain Error (Note 2)		Code = F0 hex				±1	%
Gain-Error Temperature Coefficient		Code = F0 hex			±0.001		LSB/°C
Power-Supply Rejection		Code = FF hex	V_{DD} = 2.7V to 3.6V, V_{REF} = 2.5V			1	LSB
			V_{DD} = 4.5V to 5.5V, V_{REF} = 4.096V			1	
REFERENCE INPUT							
Input Voltage Range				0		V_{DD}	V
Input Resistance				320	460	600	kΩ
Input Capacitance					15		pF
DAC OUTPUTS							
Output Voltage Range		R_L = ∞		0		V_{REF}	V
DIGITAL INPUTS							
Input High Voltage	V_{IH}	V_{DD} = 2.7V to 3.6V		2			V
		V_{DD} = 3.6V to 5.5V		3			
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = V_{DD} or GND				±1.0	µA
Input Capacitance	C_{IN}				10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{REF} = +2.7V to +5.5V, GND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = V_{REF} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Output Voltage Slew Rate		From code 00 to code F0 hex		0.6		V/µs
Output Settling Time (Note 3)		To 1/2LSB, from code 00 to code F0 hex		6		µs
Channel-to-Channel Isolation (Note 4)		Code 00 to code FF hex		500		nVs
Digital Feedthrough (Note 5)		Code 00 to code FF hex		0.5		nVs
Digital-to-Analog Glitch Impulse		Code 80 hex to code 7F hex		90		nVs
Signal-to-Noise plus Distortion Ratio	SINAD	REF = 2.5Vp-p at 1kHz, $V_{REF(DC)}$ = 1.5V, V_{DD} = 3V, code FF hex		70		dB
		REF = 2.5Vp-p at 10kHz, $V_{REF(DC)}$ = 1.5V, V_{DD} = 3V, code FF hex		60		
Multiplying Bandwidth		REF = 0.5Vp-p, $V_{REF(DC)}$ = 1.5V, V_{DD} = 3V, -3dB bandwidth		650		kHz
Wideband Amplifier Noise				60		μV_{RMS}
Shutdown Recovery Time	t_{SDR}	To ±1/2LSB of final value of V_{OUT}		13		µs
Time to Shutdown	t_{SDN}	I_{DD} < 5µA		20		µs
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		5.5	V
Supply Current (Note 6)	I_{DD}			190	360	µA
Shutdown Current				0.001	1	µA
DIGITAL TIMING (Figure 1) (Note 7)						
Address to $\overline{WR}$ Setup	t_{AS}		5			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns
Data to $\overline{WR}$ Setup	t_{DS}		25			ns
Data to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{WR}$ Pulse Width	t_{WR}		20			ns

Note 1: Reduced digital code range (code 00 hex to code F0 hex) due to swing limitations when the output amplifier is loaded.
Note 2: Gain error is: [100 ($V_{F0,meas}$ - ZCE - $V_{F0,ideal}$) / V_{REF}]. Where $V_{F0,meas}$ is the DAC output voltage with input code F0 hex, and $V_{F0,ideal}$ is the ideal DAC output voltage with input code F0 hex (i.e., V_{REF} • 240 / 256).
Note 3: Output settling time is measured from the 50% point of the falling edge of $\overline{WR}$ to ±1/2LSB of V_{OUT}'s final value.
Note 4: Channel-to-channel isolation is defined as the glitch energy at a DAC output in response to a full-scale step change on any other DAC output. The measured channel has a fixed code of 80 hex.
Note 5: Digital feedthrough is defined as the glitch energy at any DAC output in response to a full-scale step change on all eight data inputs with $\overline{WR}$ at V_{DD}.
Note 6: R_L = ∞, digital inputs at GND or V_{DD}.
Note 7: Timing measurement reference level is (V_{IH} + V_{IL}) / 2.

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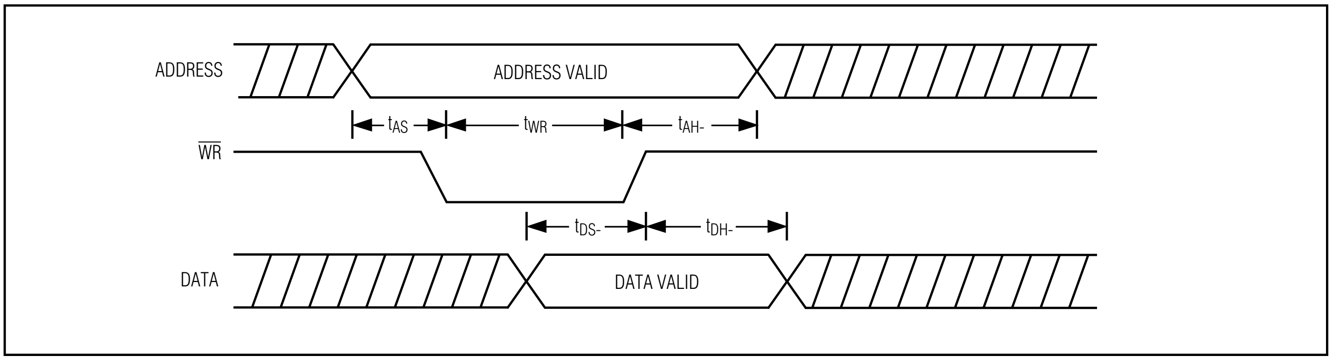
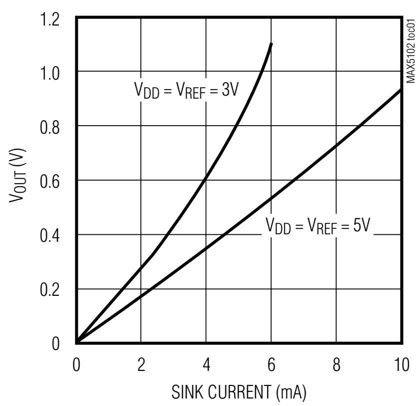


Figure 1. Timing Diagram

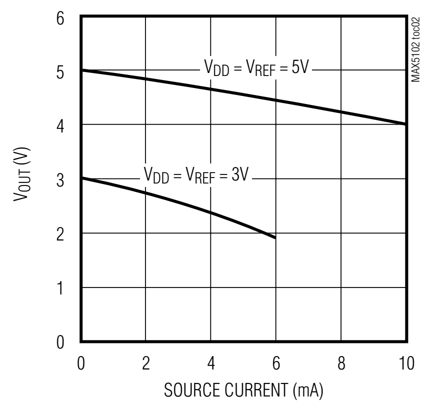
Typical Operating Characteristics

(V_{DD} = V_{REF} = +3V, R_L = 10kΩ, C_L = 100pF, code = FF hex, T_A = +25°C, unless otherwise noted.)

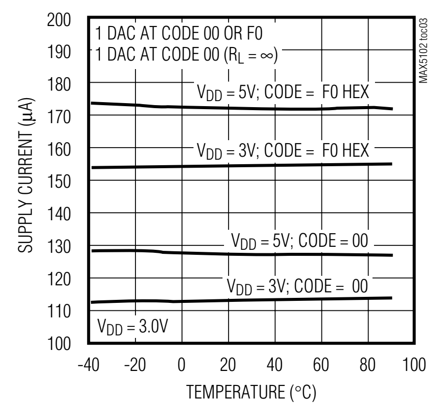
DAC ZERO-CODE OUTPUT VOLTAGE vs. SINK CURRENT



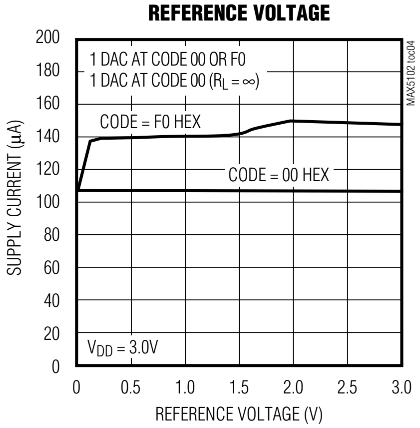
DAC FULL-SCALE OUTPUT VOLTAGE vs. SOURCE CURRENT



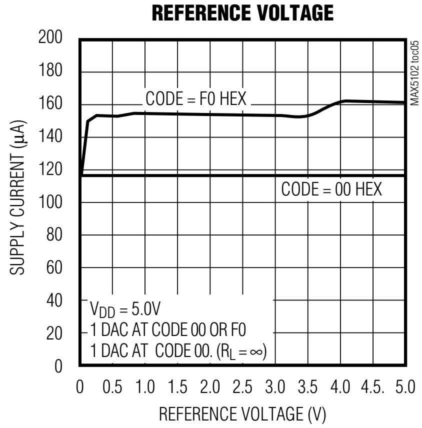
SUPPLY CURRENT vs. TEMPERATURE



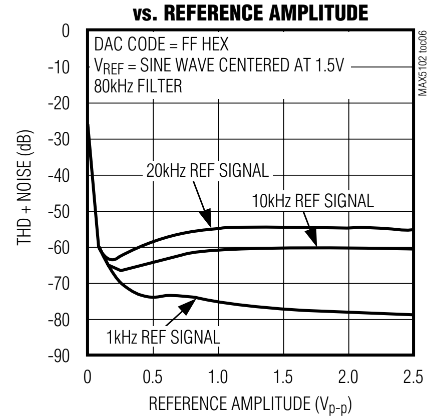
SUPPLY CURRENT vs. REFERENCE VOLTAGE



SUPPLY CURRENT vs. REFERENCE VOLTAGE



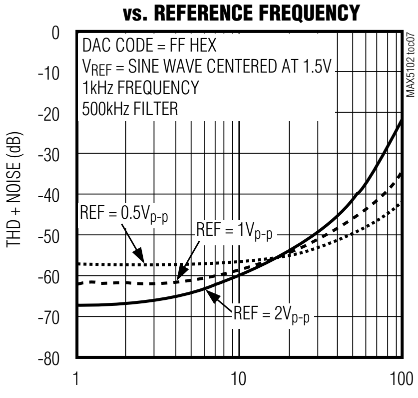
TOTAL HARMONIC DISTORTION PLUS NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



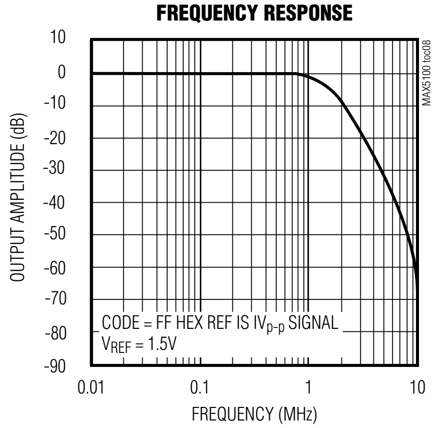
Typical Operating Characteristics (continued)

(V_{DD} = V_{REF} = +3V, R_L = 10kΩ, C_L = 100pF, code = FF hex, T_A = +25°C, unless otherwise noted.)

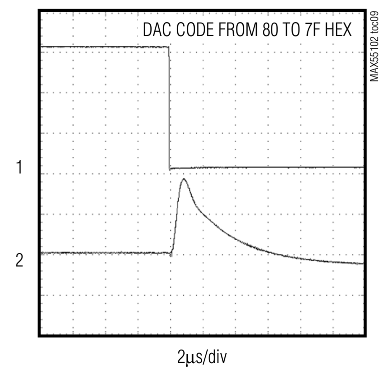
TOTAL HARMONIC DISTORTION PLUS NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



REFERENCE INPUT FREQUENCY RESPONSE

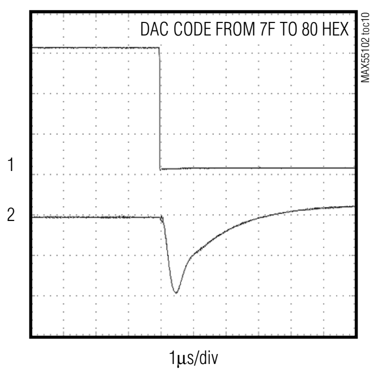


WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



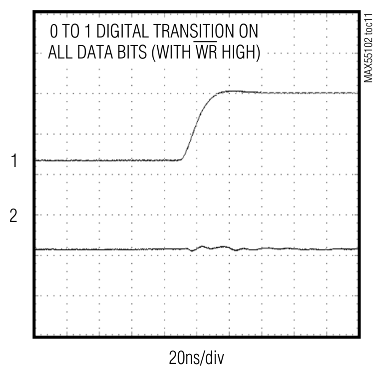
CH1 = $\overline{WR}$, 1V/div, CH2 = V_{OUTA}, 50mV/div, AC-COUPLED

WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



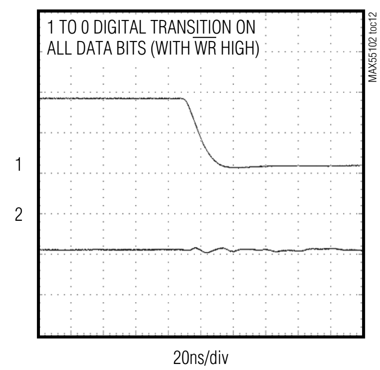
CH1 = $\overline{WR}$, 1V/div, CH2 = V_{OUTA}, 50mV/div, AC-COUPLED

DIGITAL FEEDTHROUGH GLITCH IMPULSE (0 TO 1 DIGITAL TRANSITION)



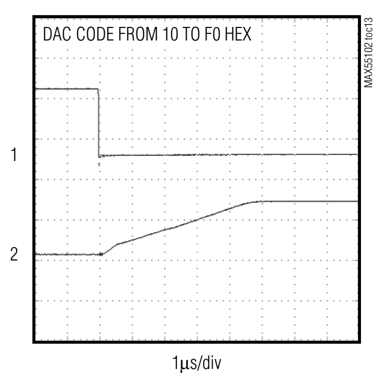
CH1 = D7, 2V/div, CH2 = V_{OUTA}, 1mV/div

DIGITAL FEEDTHROUGH GLITCH IMPULSE (1 TO 0 DIGITAL TRANSITION)



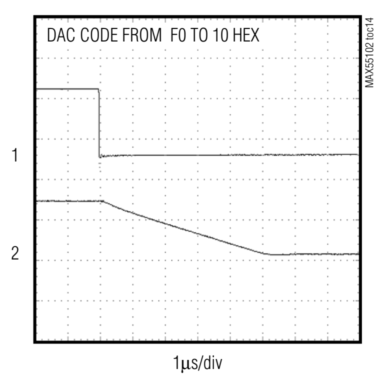
CH1 = D7, 2V/div, CH2 = V_{OUTA}, 1mV/div

POSITIVE SETTLING TIME



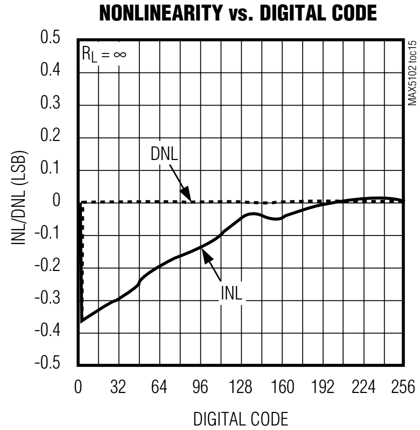
CH1 = $\overline{WR}$ = 2V/div, CH2 = V_{OUTA} = 2V/div

NEGATIVE SETTLING TIME



CH1 = $\overline{WR}$, 2V/div, CH2 = V_{OUTA}, 2V/div

INTEGRAL AND DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to GND using a 0.1µF capacitor.
2	REF	Reference Voltage Input
3	SHDN	Shutdown. Connect SHDN to GND for normal operation.
4	$\overline{WR}$	Write Input (active low). Use $\overline{WR}$ to load data into the DAC input latch selected by A0.
5–12	D7–D0	Data Inputs
13	A0	DAC Address Select Bit
14	GND	Ground
15	OUTB	DAC B Voltage Output
16	OUTA	DAC A Voltage Output

Detailed Description

Digital-to-Analog Section

The MAX5102 uses a matrix decoding architecture for the DACs. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor network converts the 8-bit digital input into an equivalent analog output voltage in proportion to the applied reference voltage input. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output.

These devices can be used in multiplying applications. Their voltages are buffered by rail-to-rail op amps connected in a follower configuration to provide a rail-to-rail output (see *Functional Diagram*).

Low-Power Shutdown Mode

The MAX5102 features a shutdown mode that reduces current consumption to 1nA. A high voltage on the SHDN pin shuts down the DACs and the output amplifiers. In shutdown mode, the output amplifiers enter a high-impedance state. When bringing the device out of shutdown, allow 13µs for the output to stabilize.

Output Buffer Amplifiers

The DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. The typical settling time to ±1/2LSB at the output is 6µs when loaded with 10kΩ in parallel with 100pF.

Reference Input

The MAX5102 provides a code-independent input impedance on the REF input. Input impedance is typically 460kΩ in parallel with 15pF, and the reference input voltage range is 0 to V_{DD}. The reference input accepts positive DC signals, as well as AC signals with peak values between 0 and V_{DD}. The voltage at REF sets the full-scale output voltage for the DAC. The output voltage (V_{OUT}) for any DAC is represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (N_B \cdot V_{REF}) / 256$$

where N_B is the numeric value of the DAC binary input code.

Digital Inputs and Interface Logic

In the MAX5102, address line A0 selects the DAC that receives data from D0–D7, as shown in Table 1. When $\overline{WR}$ is low, the addressed DAC's input latch is transparent. Data is latched when $\overline{WR}$ is high. The DAC outputs (OUTA, OUTB) represent the data held in the two 8-bit

Table 1. MAX5102 Addressing Table (partial list)

$\overline{WR}$	A0	LATCH STATE
H	X	Input data latched
L	L	DAC A input latch transparent
L	H	DAC B input latch transparent

H = High state, L = Low state, X = Don't care input latches. To avoid output glitches in the MAX5102, ensure that data is valid before $\overline{WR}$ goes low. When the device powers up (i.e., V_{DD} ramps up), all latches are internally preset with code 00 hex.

Applications Information

External Reference

The reference source resistance must be considerably less than the reference input resistance. To keep within 1LSB error in an 8-bit system, R_S must be less than $R_{REF}/256$. Hence, maintain a value of $R_S < 1k\Omega$ to ensure 8-bit accuracy. If V_{REF} is DC only, bypass REF to GND with a 0.1µF capacitor. Values greater than this improve noise rejection.

Power Sequencing

The voltage applied to REF should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND can create noise at the analog output. Return GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and GND as possible.

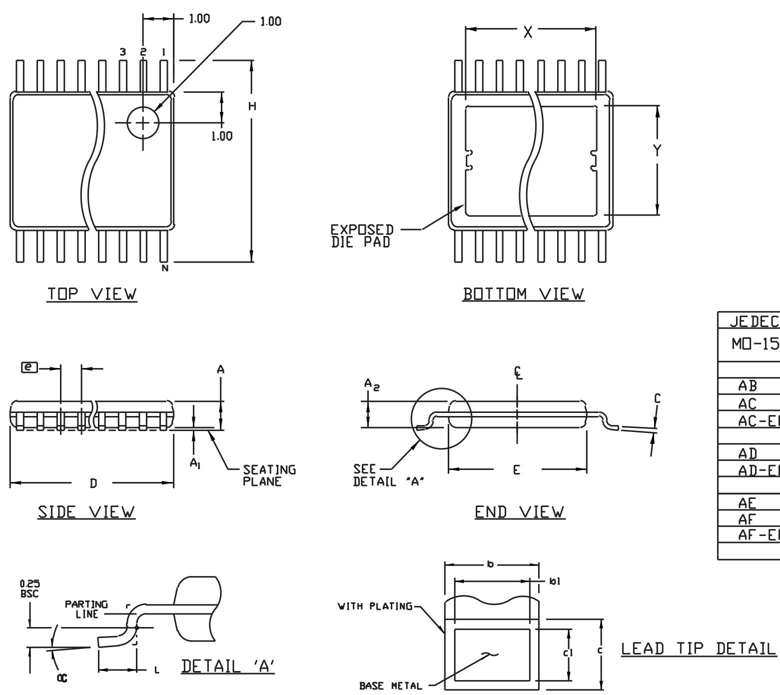
Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Chip Information

TRANSISTOR COUNT: 6848

Package Information

TSSOP.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV C | 1/1