Wide Input Range, Synchronizable, PWM SLIC Power Supply

ABSOLUTE MAXIMUM RATINGS

V_{CC}, SYNC/$\overline{SHDN}$ to GND .....-0.3V to +30V
PGND to GND .....-0.3V to +0.3V
LDO, FREQ, FB, CS to GND.....-0.3V to +6V
EXT, REF to GND.....-0.3V to (V_{LDO} + 0.3V)
LDO Output Current.....-1mA to +20mA
LDO Short Circuit to GND .....<100ms
REF Short Circuit to GND .....Continuous

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = SYNC/$\overline{SHDN}$, V_{CC} = 5V, V_{LDO} = 5V, R_{OSC} = 200kΩ, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Operating Input Voltage Range	V_{CC}			3		28	V
		V_{CC} = V_{LDO}		2.7		5.5	V
FB Input Current	I_{FB}	V_{FB} = -0.05V			1	50	nA
Load Regulation		V_{CS} = 0 to 100mV for 0 to $I_{LOAD(MAX)}$			0.013		%/mV
Line Regulation		Typically 0.0074% per % duty factor on EXT			0.0074		%/%
Current-Limit Threshold	V_{CS}			85	100	115	mV
CS Input Current	I_{CS}	CS = GND				1	µA
Idle Mode Current-Sense Threshold				5	15	25	mV
V_{CC} Supply Current (Note 1)	I_{CC}	V_{FB} = -0.05V, V_{CC} = 3V to 28V			250	400	µA
Shutdown Supply Current		SYNC/$\overline{SHDN}$ = GND, V_{CC} = 28V			3.5	6	µA
REFERENCE AND LDO REGULATOR							
LDO Output Voltage	V_{LDO}	R_{LDO} = 400Ω	5V ≤ V_{CC} ≤ 28V	4.50	5.00	5.50	V
			3V ≤ V_{CC} ≤ 28V	2.65		5.50	
Undervoltage Lockout Threshold	V_{UVLO}	V_{LDO} falling edge, 1% hysteresis (typ)		2.40	2.50	2.60	V
REF to FB Voltage (Note 2)	V_{REF}	R_{REF} = 10kΩ, C_{REF} = 0.22µF		1.225	1.250	1.275	V
REF Load Regulation		I_{REF} = 0 to 400µA			-2	-10	mV
REF Undervoltage Lockout Threshold		Rising edge, 1% hysteresis (typ)		1.0	1.1	1.2	V
OSCILLATOR							
Oscillator Frequency	f_{OSC}	R_{OSC} = 100kΩ ±1%		425	500	575	kHz
		R_{OSC} = 200kΩ ±1%		225	250	275	
		R_{OSC} = 500kΩ ±1%		85	100	115	
Maximum Duty Cycle	D	R_{OSC} = 100kΩ ±1%		86	90	94	%
		R_{OSC} = 200kΩ ±1%		87	90	93	
		R_{OSC} = 500kΩ ±1%		86	90	94	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = SYNC/$\overline{SHDN}$, V_{CC} = 5V, V_{LDO} = 5V, R_{OSC} = 200kΩ, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum EXT Pulse Width				290		ns
Minimum SYNC Input Signal Duty Cycle				20	45	%
Minimum SYNC Input Low Pulse Width				50	200	ns
Maximum SYNC Input Rise/Fall Time				200		ns
SYNC Input Frequency Range	f_{SYNC}		100		500	kHz
SYNC/$\overline{SHDN}$ Falling Edge to Shutdown Delay	t_{SHDN}			50		µs
SYNC/$\overline{SHDN}$ Input High Voltage	V_{IH}		2.0			V
SYNC/$\overline{SHDN}$ Input Low Voltage	V_{IL}				0.45	V
SYNC/$\overline{SHDN}$ Input Current		$V_{SYNC/\overline{SHDN}}$ = 5V		0.5	3.0	µA
		$V_{SYNC/\overline{SHDN}}$ = 28V		1.5	10	
EXT Sink/Source Current	I_{EXT}	EXT forced to 2V		1		A
EXT On-Resistance	$R_{ON(EXT)}$	EXT high or low		2	5	Ω

ELECTRICAL CHARACTERISTICS

(V_{CC} = SYNC/$\overline{SHDN}$, V_{CC} = 5V, V_{LDO} = 5V, R_{OSC} = 200kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Operating Input Voltage Range	V_{CC}			3		28	V
		V_{CC} = V_{LDO}		2.7		5.5	V
FB Input Current	I_{FB}	V_{FB} = -0.05V				50	nA
Current-Limit Threshold	V_{CS}			85		115	mV
CS Input Current	I_{CS}	CS = GND				1	µA
V_{CC} Supply Current (Note 1)	I_{CC}	V_{FB} = -0.05V, V_{CC} = 3V to 28V				400	µA
Shutdown Supply Current		SYNC/$\overline{SHDN}$ = GND, V_{CC} = 28V				6	µA
REFERENCE AND LDO REGULATOR							
LDO Output Voltage	V_{LDO}	R_{LDO} = 400Ω	5V ≤ V_{CC} ≤ 28V	4.50		5.50	V
			3V ≤ V_{CC} ≤ 28V	2.65		5.50	
REF to FB Voltage (Note 2)	V_{REF}	R_{REF} = 10kΩ, C_{REF} = 0.22µF		1.22		1.28	V
REF Load Regulation		I_{REF} = 0 to 400µA				-10	mV
REF Undervoltage Lockout Threshold		Rising edge, 1% hysteresis (typ)		1.0		1.2	V
OSCILLATOR							
Oscillator Frequency	f_{OSC}	R_{OSC} = 100kΩ ±1%		425		575	kHz
		R_{OSC} = 200kΩ ±1%		222		278	
		R_{OSC} = 500kΩ ±1%		85		115	

Wide Input Range, Synchronizable, PWM SLIC Power Supply

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = SYNC/$\overline{SHDN}$, V_{CC} = 5V, V_{LDO} = 5V, R_{OSC} = 200kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	D	R_{OSC} = 100kΩ ±1%	86		94	%
		R_{OSC} = 200kΩ ±1%	87		93	
		R_{OSC} = 500kΩ ±1%	86		94	
Minimum SYNC Input Signal Duty Cycle					45	%
Minimum SYNC Input Low Pulse Width					200	ns
SYNC Input Frequency Range	f_{SYNC}		100		500	kHz
SYNC/$\overline{SHDN}$ Input High Voltage	V_{IH}		2.0			V
SYNC/$\overline{SHDN}$ Input Low Voltage	V_{IL}				0.45	V
SYNC/$\overline{SHDN}$ Input Current		$V_{SYNC/\overline{SHDN}}$ = 5V			3.0	µA
		$V_{SYNC/\overline{SHDN}}$ = 28V			10	
EXT On-Resistance	$R_{ON(EXT)}$	EXT high or low			5	Ω

Note 1: This is the V_{CC} current consumed when active, but not switching, so the gate-drive current is not included.

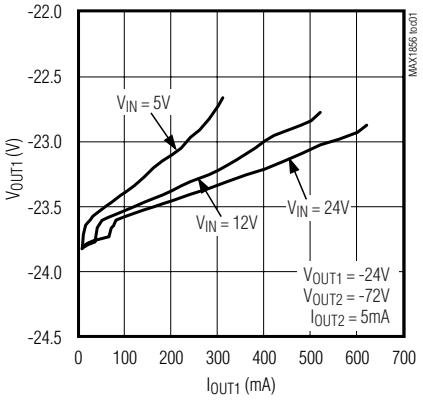
Note 2: The reference output voltage (V_{REF}) is measured with respect to FB. The difference between REF and FB is guaranteed to be within these limits to ensure output voltage accuracy.

Note 3: Specifications to -40°C are guaranteed by design, not production tested.

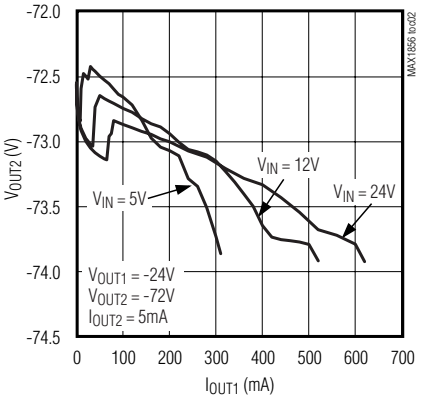
Typical Operating Characteristics

(Circuit of Figure 1, V_{CC} = $V_{SYNC/\overline{SHDN}}$ = 12V, V_{OUT1} = -24V, V_{OUT2} = -72V, R_{OSC} = 200kΩ, unless otherwise noted.)

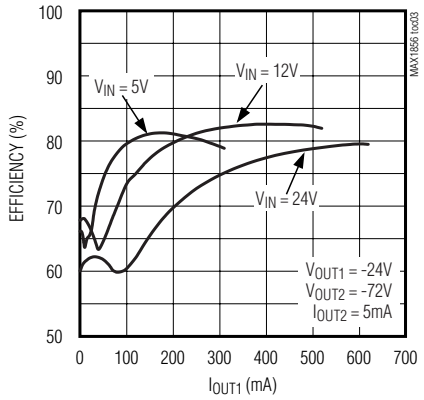
-24V OUTPUT VOLTAGE vs. LOAD CURRENT



-72V CROSS-REGULATION VOLTAGE vs. LOAD CURRENT



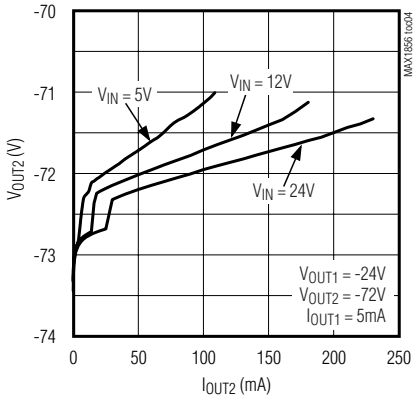
EFFICIENCY vs. LOAD CURRENT (-24V OUTPUT)



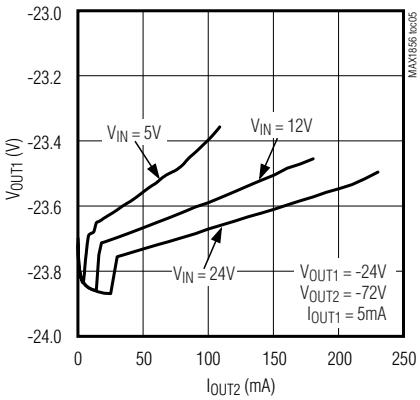
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{CC} = $V_{SYNC/\overline{SHDN}}$ = 12V, V_{OUT1} = -24V, V_{OUT2} = -72V, R_{OSC} = 200kΩ, unless otherwise noted.)

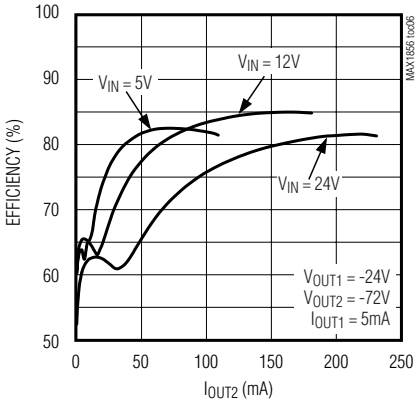
-72V OUTPUT VOLTAGE vs. LOAD CURRENT



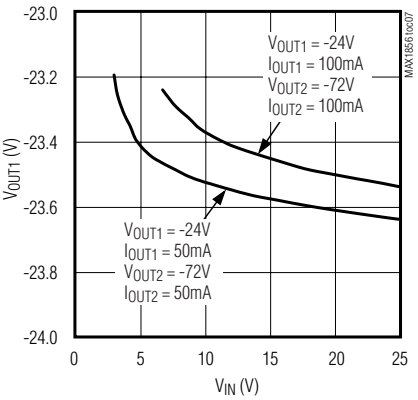
-24V CROSS-REGULATION VOLTAGE vs. LOAD CURRENT



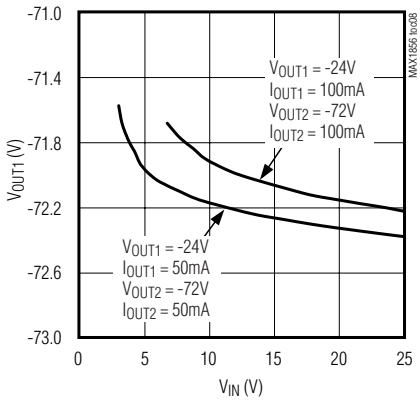
EFFICIENCY vs. LOAD CURRENT (-72V OUTPUT)



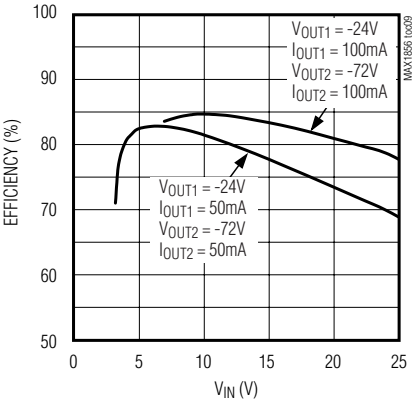
-24V OUTPUT VOLTAGE vs. INPUT VOLTAGE



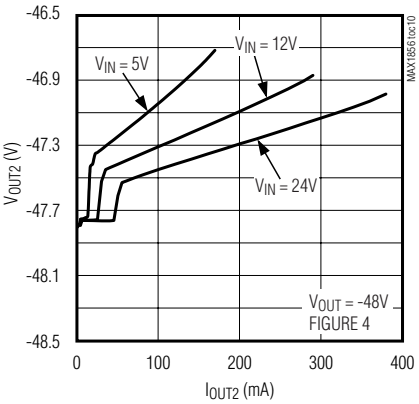
-72V OUTPUT VOLTAGE vs. INPUT VOLTAGE



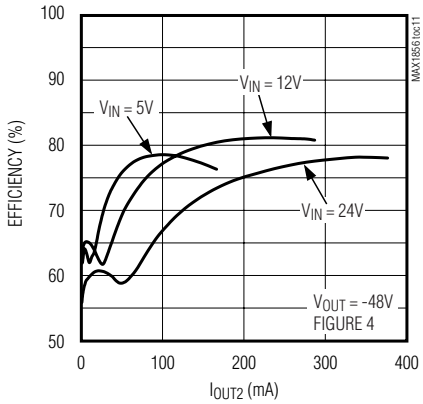
DUAL-OUTPUT EFFICIENCY vs. INPUT VOLTAGE



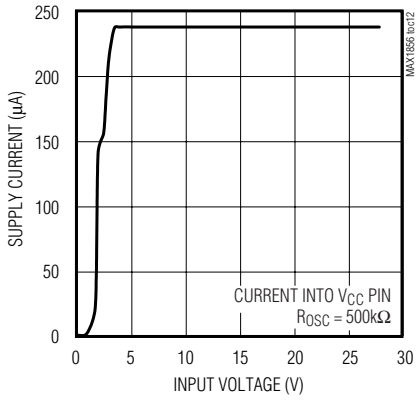
-48V OUTPUT VOLTAGE vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT (-48V OUTPUT)



SUPPLY CURRENT vs. INPUT VOLTAGE

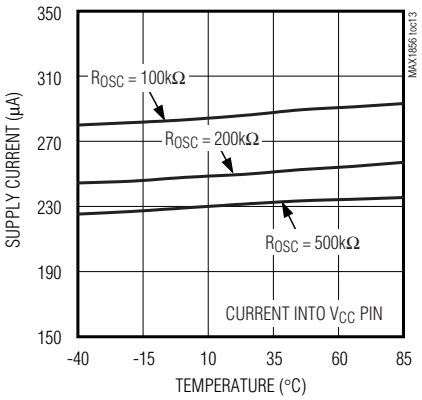


Wide Input Range, Synchronizable, PWM SLIC Power Supply

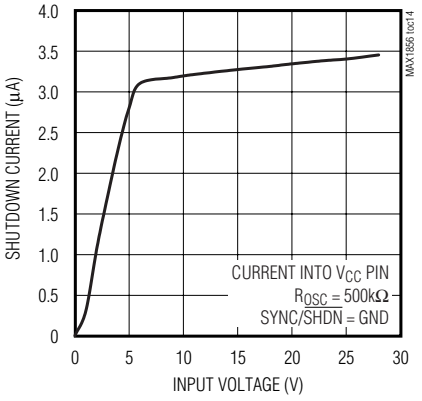
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{CC} = $V_{SYNC/\overline{SHDN}}$ = 12V, V_{OUT1} = -24V, V_{OUT2} = -72V, R_{OSC} = 200kΩ, unless otherwise noted.)

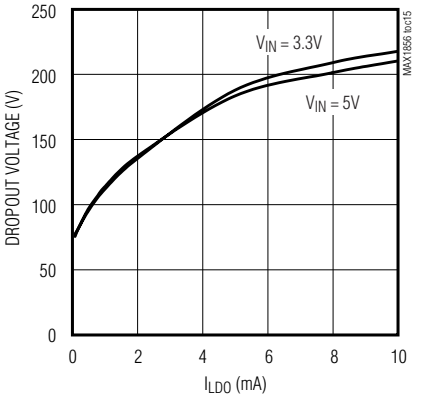
SUPPLY CURRENT vs. TEMPERATURE



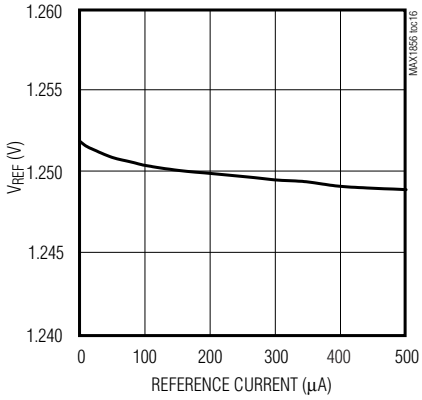
SHUTDOWN CURRENT vs. INPUT VOLTAGE



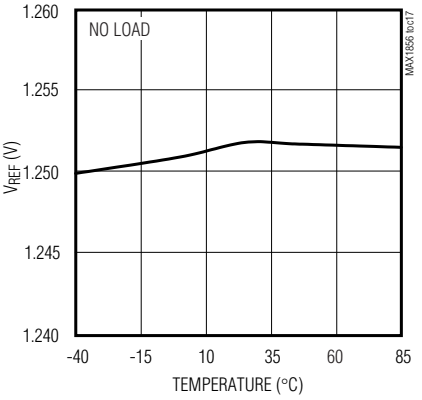
LDO DROPOUT VOLTAGE vs. LOAD CURRENT



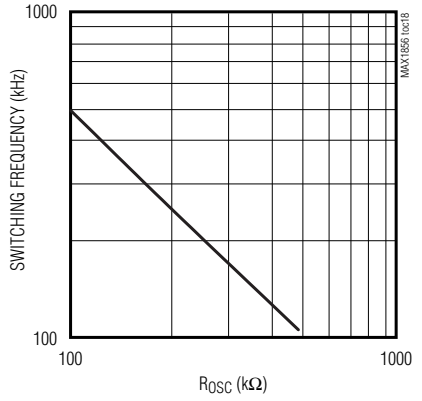
REFERENCE VOLTAGE vs. REFERENCE CURRENT



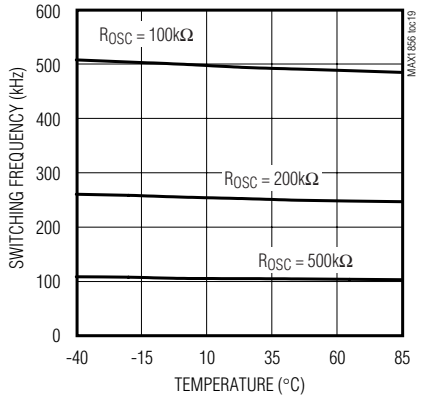
REFERENCE VOLTAGE vs. TEMPERATURE



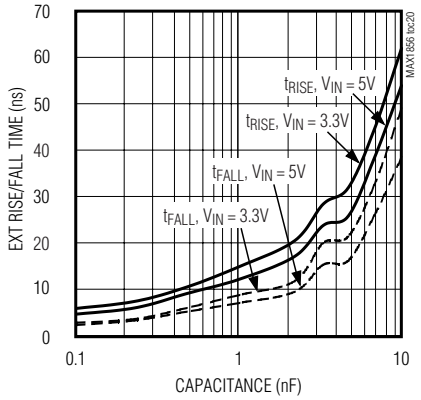
SWITCHING FREQUENCY vs. ROSC



SWITCHING FREQUENCY vs. TEMPERATURE



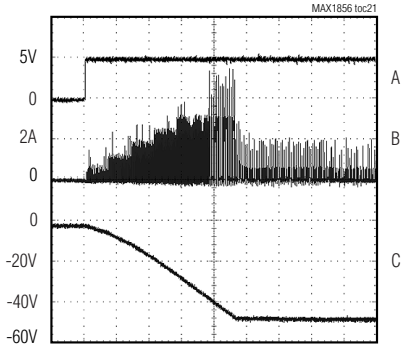
EXT RISE/FALL TIME vs. CAPACITANCE



Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{CC} = $V_{SYNC/\overline{SHDN}}$ = 12V, V_{OUT1} = -24V, V_{OUT2} = -72V, R_{OSC} = 200kΩ, unless otherwise noted.)

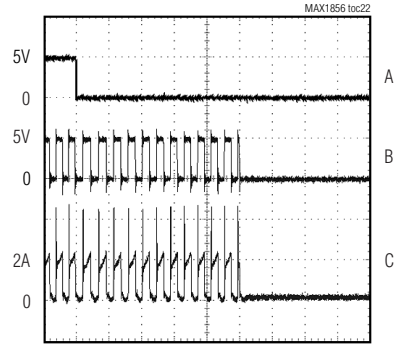
EXITING SHUTDOWN



4ms/div

A. $V_{SYNC/\overline{SHDN}}$ = 0 TO 5V, 5V/div
B. I_{LP}, 2A/div
C. V_{OUT} = -48V, R_{OUT} = 2.4kΩ, 20V/div
CIRCUIT OF FIGURE 4

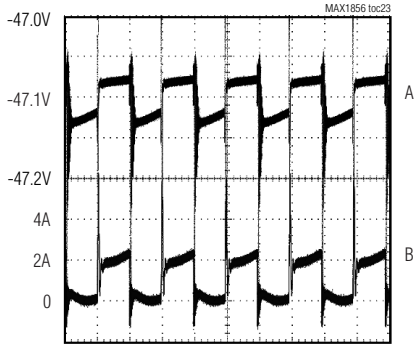
ENTERING SHUTDOWN



10µs/div

A. $V_{SYNC/\overline{SHDN}}$ = 5V TO 0, 5V/div
B. V_{EXT}, 5V/div
C. I_{LP}, 2A/div
V_{OUT} = -48V, R_{OUT} = 240Ω
CIRCUIT OF FIGURE 4

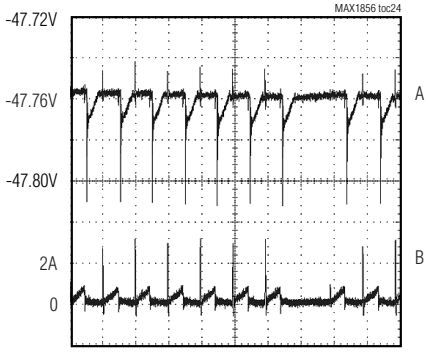
HEAVY-LOAD SWITCHING WAVEFORM



2.0µs/div

A. V_{OUT} = -48V, I_{OUT} = 200mA, 50mV/div
B. I_{LP}, 2A/div
CIRCUIT OF FIGURE 4

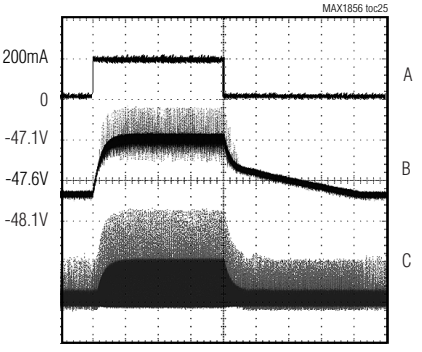
LIGHT-LOAD SWITCHING WAVEFORM



4µs/div

A. V_{OUT} = -48V, I_{OUT} = 20mA, 20mV/div
B. I_{LP}, 2A/div
CIRCUIT OF FIGURE 4

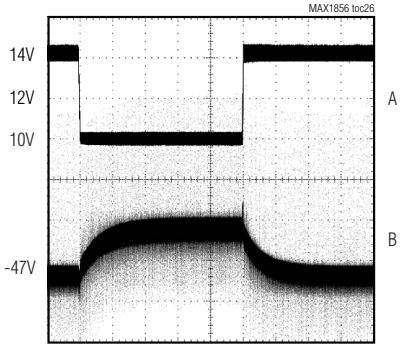
LOAD TRANSIENT



1ms/div

A. I_{OUT} = 20mA TO 200mA, 200mA/div
B. V_{OUT}, = -48V, 500mV/div
C. I_{LP}, 2A/div
CIRCUIT OF FIGURE 4

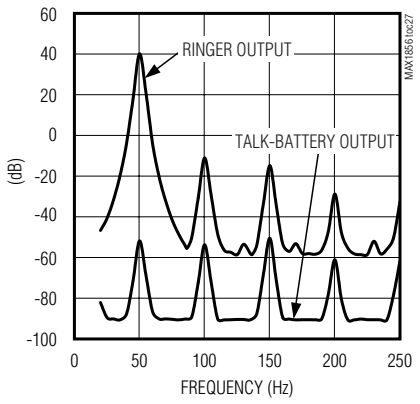
LINE TRANSIENT



400µs/div

A. V_{IN} = 10V TO 14V, 2Vdiv
B. V_{OUT} = -48V, I_{OUT} = 200mA, 100mV/div
CIRCUIT OF FIGURE 4

RINGER TO TALK-BATTERY CROSSTALK



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Pin Description

PIN	NAME	FUNCTION
1	LDO	5V Linear Regulator Output. The regulator powers all of the internal circuitry, including the EXT gate driver. Bypass LDO to GND with a 1µF or greater ceramic capacitor.
2	FREQ	Oscillator Frequency Set Input. A resistor from FREQ to GND sets the oscillator from 100kHz (R_{OSC} = 500kΩ) to 500kHz (R_{OSC} = 100kΩ): f_{OSC} = 50MΩ-kHz / R_{OSC}. The MAX1856 still requires R_{OSC} when an external clock is connected to SYNC/$\overline{SHDN}$.
3	GND	Analog Ground
4	REF	1.25V Reference Output. REF can source up to 400µA. Bypass to GND with a 2.2µF ceramic capacitor.
5	FB	Feedback Input. The feedback voltage threshold is 0.
6	CS	Positive Current-Sense Input. Connect a current-sense resistor (R_{CS}) between CS and PGND.
7	PGND	Power Ground
8	EXT	External MOSFET Gate-Driver Output. EXT swings from LDO to PGND.
9	V_{CC}	Input Supply to the Linear Regulator. V_{CC} accepts inputs up to 28V. Bypass to PGND with a 1µF ceramic capacitor.
10	SYNC/$\overline{SHDN}$	Shutdown Control and Synchronization Input. There are three operating modes: • SYNC/$\overline{SHDN}$ low: shutdown mode • SYNC/$\overline{SHDN}$ high: the DC-to-DC controller operates with the oscillator frequency set at FREQ by R_{OSC} • SYNC/$\overline{SHDN}$ clocked: the DC-to-DC controller operates with the oscillator frequency set by the SYNC clock input. The conversion cycles initiate on the rising edge of the input clock signal. However, the MAX1856 still requires R_{OSC} when SYNC/$\overline{SHDN}$ is externally clocked.

Detailed Description

The MAX1856 current-mode PWM controller uses an inverting flyback configuration that is ideal for generating the high negative voltages required for SLIC power supplies. Optimum conversion efficiency is maintained over a wide range of loads by employing both PWM operation and Maxim's proprietary Idle Mode control to minimize operating current at light loads. Other features include shutdown, adjustable internal operating frequency or synchronization to an external clock, soft-start, adjustable current limit, and a wide (3V to 28V) input range.

PWM Controller

The heart of the MAX1856 current-mode PWM controller is a BiCMOS multi-input comparator that simultaneously processes the output-error signal, the current-sense signal, and a slope-compensation ramp (Figure 2). The main PWM comparator is direct summing, lacking a traditional error amplifier and its associated phase shift. The direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage since there is no conventional error amplifier in the feedback path.

In PWM mode, the controller uses fixed-frequency, current-mode operation where the duty ratio is set by the input-to-output voltage ratio and the transformer's turn ratio. The current-mode feedback loop regulates peak inductor current as a function of the output error signal.

At light loads, the controller enters Idle Mode. During Idle Mode, switching pulses are provided only as necessary to supply the load, and operating current is minimized to provide the best light-load efficiency. The minimum-current comparator threshold is 15mV, or 15% of the full-load value (I_{MAX}) of 100mV. When the controller is synchronized to an external clock, Idle Mode occurs only at very light loads.

Wide Input Range, Synchronizable, PWM SLIC Power Supply

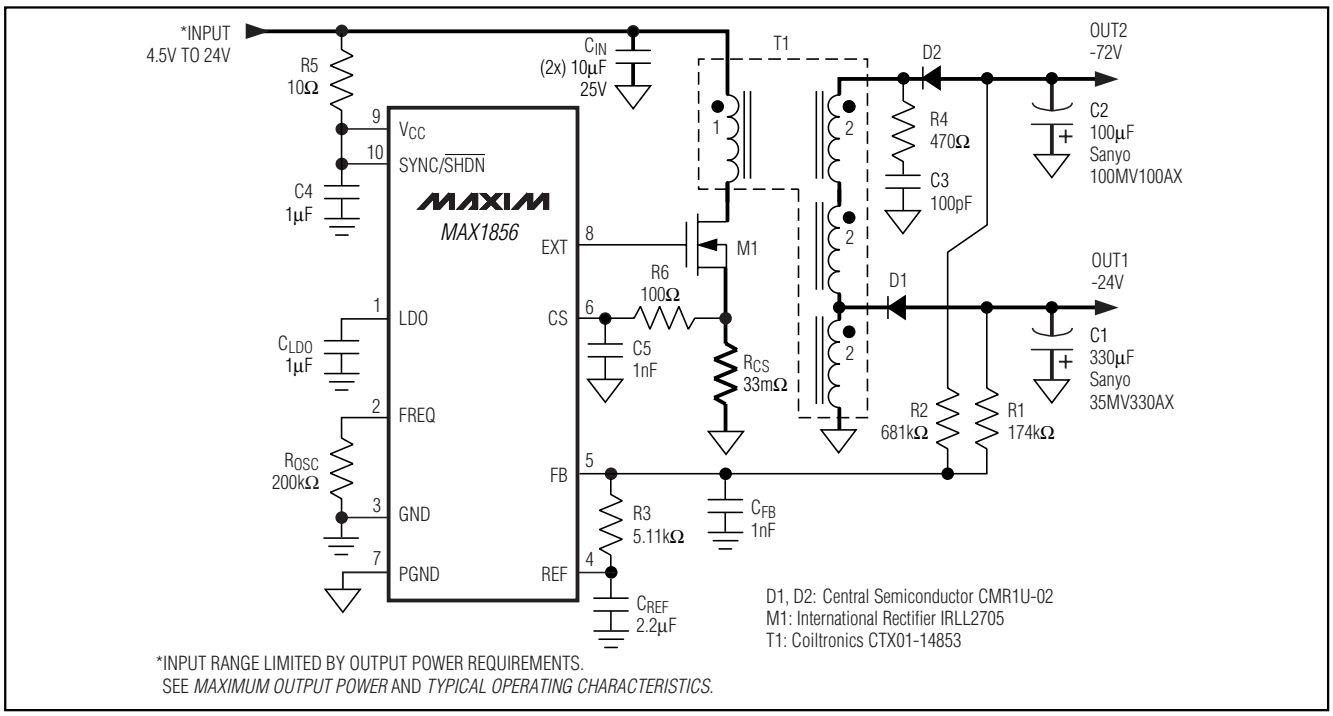

Figure 1. Standard Application Circuit

Low-Dropout Regulator (LDO)

All MAX1856 functions, including EXT, are internally powered from the on-chip, low-dropout 5V regulator. The regulator input is at V_{CC}, while its output is at LDO. The V_{CC}-to-LDO dropout voltage is typically 200mV (300mV max at 12mA), so that when V_{CC} is <5.2V, V_{LDO} is typically V_{CC} - 200mV. When the LDO is in dropout, the MAX1856 still operates with V_{CC} as low as 3V (as long as the LDO exceeds 2.7V), but with reduced amplitude FET drive at EXT. The maximum V_{CC} input voltage is 28V.

LDO can supply up to 12mA to power the IC, supply gate charge through EXT to the external FET, and supply small external loads. When driving particularly large FETs at high switching rates, little or no LDO current may be available for external loads. For example, when switched at 500kHz, a large FET with 20nC gate charge requires 20nC × 500kHz, or 10mA.

Soft-Start

The MAX1856 features a "digital" soft-start that is preset and requires no external capacitor. Upon startup, the peak inductor current increments from 1/5th of the value set by R_{CS}, to the full current-limit value in five steps over 1024 cycles of f_{OSC} or f_{SYNC}. Additionally, the oscillator runs at 1/3 the normal operating frequency ($f_{OSC}/3$) until the output voltage reaches 20% of its nominal value ($V_{FB} \le 1.0V$). See the *Typical Operating Characteristics* for a scope picture of the soft-start operation. Soft-start is implemented: 1) when power is first applied to the IC, 2) when exiting shutdown with power already applied, and 3) when exiting undervoltage lockout. The MAX1856's soft-start sequence does not start until V_{LDO} reaches 2.5V.

Design Procedure

The MAX1856 can operate within a wide input voltage range from 3V to 28V. This allows it to be used with wall adapters. In applications driven by low-power, low-cost and low input and output ripple current requirements, the MAX1856 flyback topology can be used to generate various levels of output voltages and multiple outputs.

Communications over the Internet interface with a standard telephone connection, which includes the Subscriber Line Interface Circuit (SLIC). The SLIC requires a negative power supply for the audio and ringer functions. The circuits discussed here are designed for these applications. The following design discussions are related to the standard application cir-

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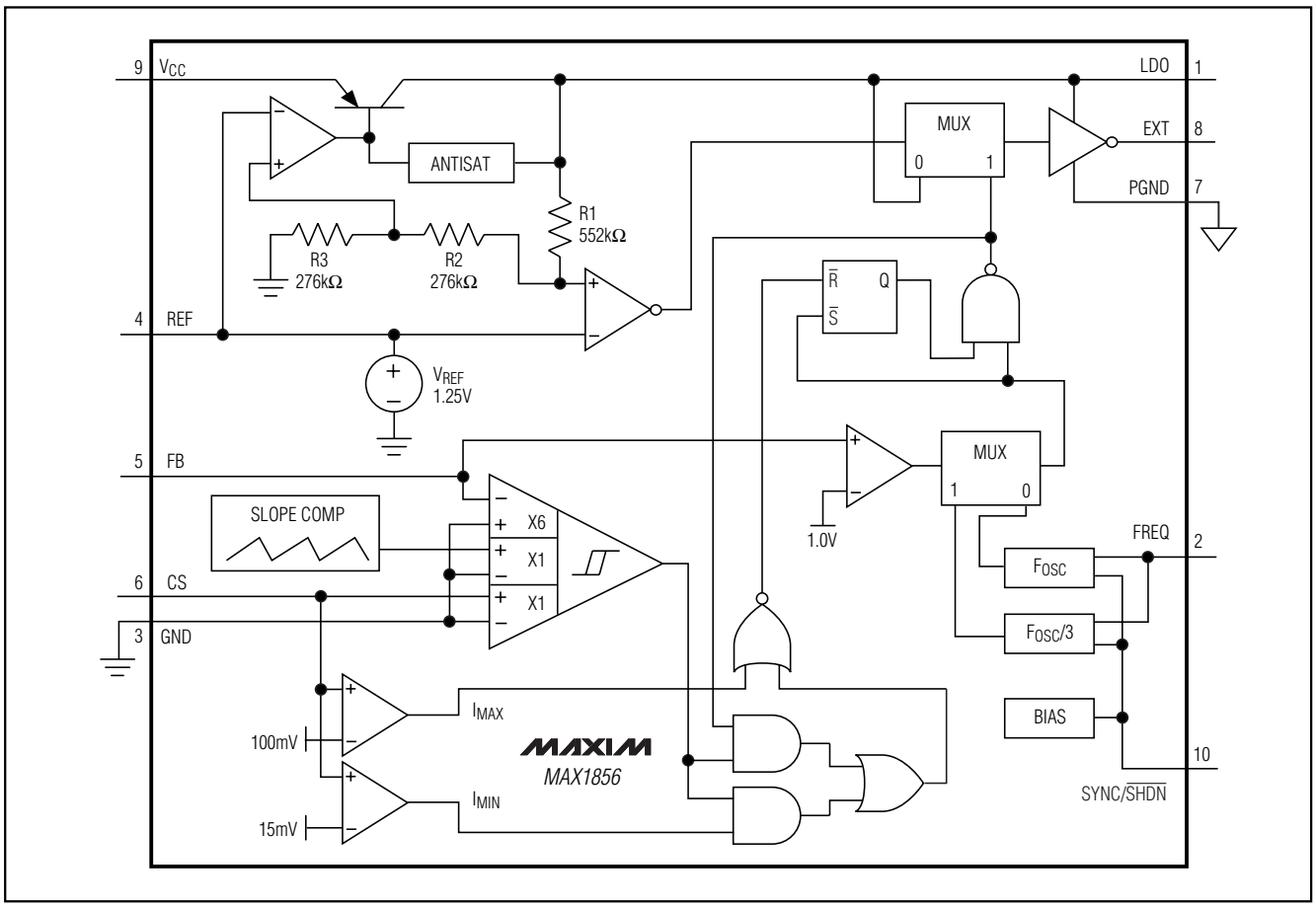

Figure 2. Functional Diagram

cuit (Figure 1) converting a +12V input to a -72V output (maximum load 100mA) and a -24V output (maximum load 400mA).

Maximum Output Power

The maximum output power the MAX1856 can provide depends on the maximum input power available and the circuit's efficiency:

$$P_{OUT(MAX)} = EFFICIENCY \times P_{IN(MAX)}$$

Furthermore, the efficiency and input power are both functions of component selection. Efficiency losses can be divided into three categories: 1) resistive losses across the transformer, MOSFET's on-resistance, current-sense resistor, and the ESR of the input and output capacitors; 2) switching losses due to the MOSFET's transition region, the snubber circuit, which also increases the transition times, and charging the MOSFET's gate capacitance; and 3) transformer core losses. Typically, 80% efficiency can be assumed for initial calculations. The input power depends on the current limit, input voltage, output voltage, inductor value, the transformer's turns ratio, and the switching frequency:

$$P_{IN(MAX)} = V_{IN}D\left[\frac{V_{CS}}{R_{CS}} - \frac{V_{IN}D}{2f_{OSC}L}\right]$$

$$D = \frac{N_P V_{OUT}}{N_P V_{OUT} + N_S V_{IN}}$$

where N_P:N_S is the transformer's turns ratio.

Setting the Operating Frequency (SYNC/SHDN and FREQ)

The SYNC/$\overline{SHDN}$ pin provides both external-clock synchronization (if desired) and shutdown control. When SYNC/$\overline{SHDN}$ is low, all IC functions are shut down. A logic high at SYNC/$\overline{SHDN}$ selects operation at a

100kHz to 500kHz frequency, which is set by a resistor (R_{OSC}) connected from FREQ to GND. The relationship between f_{OSC} and R_{OSC} is:

$$R_{OSC} = \frac{50M\Omega \times kHz}{f_{OSC}(kHz)}$$

Thus, a 250kHz operating frequency, for example, is set with R_{OSC} = 200kΩ. At higher frequencies, the magnetic components will be smaller. Peak currents and, consequently, resistive losses will be lower at the higher switching frequency. However, core losses, gate charge currents, and switching losses increase with higher switching frequencies.

Rising clock edges on SYNC/$\overline{SHDN}$ are interpreted as synchronization input. If the sync signal is lost while SYNC/$\overline{SHDN}$ is high, the internal oscillator takes over at the end of the last cycle, and the frequency is returned to the rate set by R_{OSC}. If the signal is lost with SYNC/$\overline{SHDN}$ low, the IC waits for 50µs before shutting down. This maintains output regulation even with intermittent sync signals. When an external sync signal is used, Idle Mode switchover at the 15mV current-sense threshold is disabled so that Idle Mode only occurs at very light loads. Also, R_{OSC} should be set for a frequency 15% below the SYNC clock rate:

$$R_{OSC(SYNC)} = \frac{50M\Omega \times kHz}{0.85 f_{OSC}(kHz)}$$

Setting the Output Voltage

Set the output voltage using two external resistors forming a resistive divider to FB between the output and REF. First select a value for R3 between 3.3kΩ and 100kΩ. R1 is then given by:

$$R1 = R3 \left[\frac{V_{OUT}}{V_{REF}} \right]$$

For a dual output as shown in Figure 1, a split feedback technique is recommended. Since the feedback voltage threshold is 0, the total feedback current is:

$$I_{TOTAL} = I_{R1} + I_{R2} = \frac{V_{REF}}{R3}$$

Since the feedback resistors are connected to the reference, I_{TOTAL} must be <400µA so that V_{REF} is guaranteed to be in regulation (see *Electrical Characteristics Table*). Therefore, select R3 so the total current value is between 200µA and 250µA as shown in Figure 1. To ensure that the MAX1856 regulates both outputs with the same degree of accuracy over load, select the feedback resistors (R1 and R2) so their current ratio (I_{R1}:I_{R2}) equals the output power ratio (P_{OUT1}:P_{OUT2}) under full load:

$$\frac{I_{R1}}{I_{R2}} = \frac{V_{OUT1} I_{OUT1}}{V_{OUT2} I_{OUT2}}$$

Once R3 and the dual feedback currents (I_{R1} and I_{R2}) are determined from the two equations above, use the following two equations to determine R1 and R2:

$$I_{R1} = \frac{V_{OUT1}}{R1} \text{ and } I_{R2} = \frac{V_{OUT2}}{R2}$$

Selecting the Transformer

The MAX1856 PWM controller works with economical off-the-shelf transformers. The transformer selection depends on the input-to-output voltage ratio, output current capacity, duty cycle, and oscillator frequency. Table 1 shows recommended transformers for the typical applications, and Table 2 gives some recommended suppliers.

Transformer Turns Ratio

The transformer turns ratio is a function of the input-to-output voltage ratio and maximum duty cycle. Under steady-state conditions, the change in flux density during the on-time must equal the return change in flux density during the off-time (or flyback period):

$$\frac{V_{IN} t_{ON}}{N_P} = \frac{V_{OUT} t_{OFF}}{N_S}$$

For example, selecting a 50% duty cycle for the standard application circuit (Figure 1) and a +12V input voltage, the -72V output requires a 1:6 turns ratio, and the -24V output requires a 1:2 turns ratio. Therefore, a transformer with a 1:2:2:2 turns ratio was selected.

Primary inductance

The average input current at maximum load can be calculated as:

$$I_{IN(DC)} = \frac{|V_{OUT}| I_{OUT(MAX)}}{\eta V_{IN(MIN)}}$$

where η = efficiency. For V_{OUT} = -24V, $I_{OUT(MAX)}$ = 400mA, and $V_{IN(MIN)}$ = 10.8V as shown in Figure 1, this

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Table 1. Transformer Selection for Standard Applications

INPUT VOLTS (V)	OUTPUT VOLTS (V)	OUTPUT CURRENT (mA)	TRANSFORMER (VENDOR)
5	-48	100	VP3-0055 (Coiltronics)
12	-48	100	CTX01-14853 (Coiltronics), or ICA-0635 (ICE Components)
12	-24 and -72	400 or 100	CTX01-14853 (Coiltronics), or ICA-0635 (ICE Components)
12	-95 and -30	320 and 150	CTX03-15220 (Coiltronics)

Table 2. Transformer Suppliers

VENDOR	USA PHONE	USA FAX	INTERNET
Coilcraft	847-639-6400	847-639-1469	www.coilcraft.com
Coiltronics	888-414-2645	561-241-9339	www.coiltronics.com
ICE Components	800-729-2099	703-257-7547	www.icecomponents.com
Pulse Engineering	858-674-8100	858-674-8262	www.pulseeng.com
TDK	847-390-4461	847-390-4405	www.tdk.com

gives 1.11A for 80% efficiency. With a duty cycle of 52.5%, the average switch current ($I_{SW(AVG)}$) is 2.114A. Choosing a primary inductance ripple current ΔI_L to be 40% of the average switch current, the primary inductance is given by:

$$L_P = \frac{V_{IN} D}{\Delta I_L f_{OSC}}$$

Selecting f_{OSC} = 250kHz and ΔI_L = 0.4 x $I_{SW(AVG)}$ = 0.846A, the primary inductance value is 27µH, and the peak primary current for this example is therefore 2.5A.

Core Selection

The transformer in a flyback converter is a coupled inductor with multiple windings on the same magnetic core. Flyback topologies operate by storing energy in the transformer magnetics during the on-time and transferring this energy to the output during the off-time.

Core selection depends on the core's power-handling capability. The required output power is first considered. For example, the standard application circuit requires 9.6W. Assuming a typical 80% efficiency, the transformer must support 12W of power. The core material's properties, the core's shape, and the size of the air gap determine the core's power rating. Since the equations relating these properties to the power capability are involved, manufacturers simply provide charts giving "Power vs. Frequency" for different core sizes. For the standard application circuit (f_{OSC} = 250kHz), the EFD15 core from Coiltronics meets the criteria.

Once the core is chosen, the number of turns in the primary is given by:

$$N_P = \sqrt{\frac{L_P}{A_L}}$$

where A_L is the inductance factor. Ensure that the number of ampere-turns ($N_P I_{SAT}$) is below the saturation limit. A significant portion of the total energy is stored in the air gap. Therefore, the larger the air gap, the lower the A_L value and the larger the number of ampere-turns at which saturation starts. Some manufacturers define saturation as the current at which the inductance decreases by 30%.

Current-Sense Resistor Selection

Once the peak inductor current is determined, the current-sense resistor (R_{CS}) is determined by:

$$R_{CS} = \frac{V_{CS(MIN)}}{I_{LPEAK}} = 85mV / I_{LPEAK}$$

Kelvin-sensing should be used to connect CS and PGND to R_{CS}. Connect PGND and GND together at the ground side of R_{CS}.

Due to inductive ringing after the MOSFET turns on, a lowpass filter may be required between R_{CS} and CS to prevent the noise from tripping the current-sense comparator. Connect a 100Ω resistor between CS and the

high side of R_{CS}, and connect a 1000pF capacitor between CS and GND.

Power MOSFET Selection

The MAX1856 drives a wide variety of N-channel power MOSFETs (NFETs). Since the LDO limits the EXT output gate drive to no more than 5V, a logic-level NFET is required. Best performance, especially with input voltages below 5V, is achieved with low-threshold NFETs that specify on-resistance with a gate-to-source voltage (V_{GS}) of 2.7V or less. When selecting an NFET, key parameters include:

1) Total gate charge (Q_G)

2) Reverse transfer capacitance or charge (C_{RSS})

3) On-resistance ($R_{DS(ON)}$)

4) Maximum drain-to-source voltage ($V_{DS(MAX)}$)

5) Minimum threshold voltage ($V_{TH(MIN)}$)

At high switching rates, dynamic characteristics (parameters 1 and 2 above) that predict switching losses may have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_G includes all capacitance associated with charging the gate. In addition, this parameter helps predict the current needed to drive the gate at the selected operating frequency. The continuous LDO current for the FET gate is:

$$I_{GATE} = Q_G \times f_{OSC}$$

For example, the IRLL2705 has a typical Q_G of 17nC (at V_{GS} = 5V); therefore, the I_{GATE} current at 500kHz is 8.5mA.

The switching element in a flyback converter must have a high enough voltage rating to handle the input voltage plus the reflected secondary voltage, as well as any spikes induced by leakage inductance. The reflected secondary voltage is given by:

$$V_{REFLECT} = \frac{N_P}{N_S}(V_{OUT} + V_{DIODE})$$

where V_{DIODE} is the voltage drop across the output diode. For a 10% variation in input voltage and a 30% safety margin, this gives a required 33V voltage rating (V_{DS}) for the switching MOSFET in Figure 1. The IRLL2705 with a V_{DS} of 55V was chosen.

Diode Selection

The MAX1856's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Ensure that the diode's average current rating exceeds the peak secondary current, using the diode manufacturer's data or approximating it with the following formula:

$$I_{D(PK)} = I_{OUT}\left(1 + \frac{V_{OUT}}{N \times V_{IN}}\right) + \frac{\Delta I_L}{2N}$$

where $N = N_S/N_P$ is the secondary-to-primary turns ratio. Additionally, the diode's reverse breakdown voltage must exceed V_{OUT} plus the reflected input voltage plus the leakage inductance spike. For high output voltages (50V or above), Schottky diodes may not be practical because of this voltage requirement. In these cases, use a faster ultra-fast recovery diode with adequate reverse-breakdown voltage.

Capacitor Selection

Output Filter Capacitor

The output capacitor (C_{OUT}) does all the filtering in a flyback converter. Typically, C_{OUT} must be chosen based on the output ripple requirement. The output ripple is due to the variations in the charge stored in the output capacitor with each pulse and the voltage drop across the capacitor's equivalent series resistance (ESR) caused by the current into and out of the capacitor. The ESR-induced ripple usually dominates, so output capacitor selection is actually based upon the capacitor's ESR, voltage rating, and ripple current rating.

Input Filter Capacitor

The input capacitor (C_{IN}) in flyback designs reduces the current peaks drawn from the input supply and reduces noise injection. The value of C_{IN} is largely determined by the source impedance of the input supply. High source impedance requires high input capacitance, particularly as the input voltage falls. Since inverting flyback converters act as "constant-power" loads to their input supply, input current rises as the input voltage falls. Consequently, in low-input-voltage designs, increasing C_{IN} and/or lowering its ESR can add as much as 5% to the conversion efficiency.

Bypass Capacitors

In addition to C_{IN} and C_{OUT}, three ceramic bypass capacitors are also required with the MAX1856. Bypass REF to GND with 2.2µF or more. Bypass LDO to GND with 1µF or more. And bypass V_{CC} to GND with 1µF or more. All bypass capacitors should be located as close to their respective pins as possible.

Compensation Capacitor

Output ripple voltage due to C_{OUT} ESR affects loop stability by introducing a left half-plane zero. A small capacitor connected from FB to GND forms a pole with

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the feedback resistance that cancels the ESR zero. The optimum compensation value is:

$$C_{FB} = \frac{1}{2} C_{OUT} \left[\frac{ESR_{COUT}}{(R1 \times R3)/(R1+R3)} \right]$$

where R1 and R3 are feedback resistors (Figure 3). If the calculated value for C_{FB} results in a nonstandard capacitance value, values from $0.5C_{FB}$ to $1.5C_{FB}$ will also provide sufficient compensation.

Snubber Design

The MAX1856 uses a current-mode controller that employs a current-sense resistor. Immediately after turn-on, the MAX1856 uses a 100ns current-sense blanking period to minimize noise sensitivity. However, when the MOSFET turns on, the secondary inductance and the output diode's parasitic capacitance form a resonant circuit that causes ringing. Reflected back through the transformer to the primary side, these oscillations appear across the current-sense resistor and last well beyond the 100ns blanking period. As shown in Figure 1, a series RC snubber circuit at the output diode increases the damping factor, allowing the ringing to settle quickly. Applications with dual output voltages require only one snubber circuit on the higher voltage output.

The diode's parasitic capacitance can be estimated using the diode's reverse voltage rating (V_{RRM}), current capability (I_O), and recovery time (t_{RR}). A rough approximation is:

$$C_{DIODE} = \frac{I_O t_{RR}}{V_{RRM}}$$

For the CMR1U-02 Central Semiconductor diode used in Figure 1, the capacitance is roughly 172pF. A value less than this (100pF) was chosen since the output snubber only needs to dampen the ringing, so the initial turn-on spike that occurs during the 100ns blanking period is still present. Larger capacitance values require more charge, thereby increasing the power dissipation.

The snubber's time constant (t_{SNUB}) must be smaller than the 100ns blanking time. A typical RC time constant of 50ns was chosen for Figure 1:

$$R4 = \frac{t_{SNUB}}{C3} = \frac{50ns}{C3}$$

When a MOSFET with a transformer load is turned off, the drain will fly to a high voltage as a result of the energy stored in the transformer's leakage inductance. During the switch on-time, current is established in the leakage inductance (L_L) equal to the peak primary current (I_{PEAK}). The energy stored in the leakage inductance is:

$$E_L = \frac{L_L I_{PEAK}^2}{2}$$

When the switch turns off, this energy is transferred to the MOSFET's parasitic capacitance, causing a voltage spike at the MOSFET's drain. For the IRLL2705 MOSFET, the capacitance value (C_{DS}) is 130pF. If all of the leakage inductance energy transfers to this capacitance, the drain would fly up to:

$$V_{COSS} = \sqrt{\frac{L_L I_{PEAK}^2}{C_{DS}}}$$

The leakage inductance is (worst case) 1% of the primary inductance value. For a 0.27µH leakage inductance and a 2.5A peak current, the voltage reaches 114V at the MOSFET's drain, which is much higher than the MOSFET's rated breakdown voltage. This causes the parasitic bipolar transistor to turn on if the dv/dt at the drain is high enough. Note that the inductive spike adds on to the sum of the input voltage and the reflected secondary voltage already present at the drain of the transistor (see *Power MOSFET Selection*).

A series combination RC snubber (R7 and C6 in Figure 3) across the MOSFET (drain to source) reduces this spike. The energy stored in the leakage inductance transfers to the snubber capacitor (C6) as electrostatic energy. Therefore, C6 must be large enough to guarantee the voltage spike will not exceed the breakdown voltage, but not so large as to result in excessive power dissipation:

$$C6 = \frac{L_L I_{PEAK}^2}{V_{C6}^2}$$

Typically, a 30% safety margin is chosen so that V_{C6} is at most equal to about 70% of the MOSFET's V_{DS} rating. For example, the V_{DSS} is 55V for the IRLL2705, so this gives a value of 1000pF for C9. The amount of energy stored in snubber capacitor C6 has to discharge through series resistor R7 in the snubber network. During turn-off, the drain voltage rises in a time period (t_f) characteristic of the MOSFET used, which is 22ns for the IRLL2705. The RC time constant should therefore equal this time. Hence:

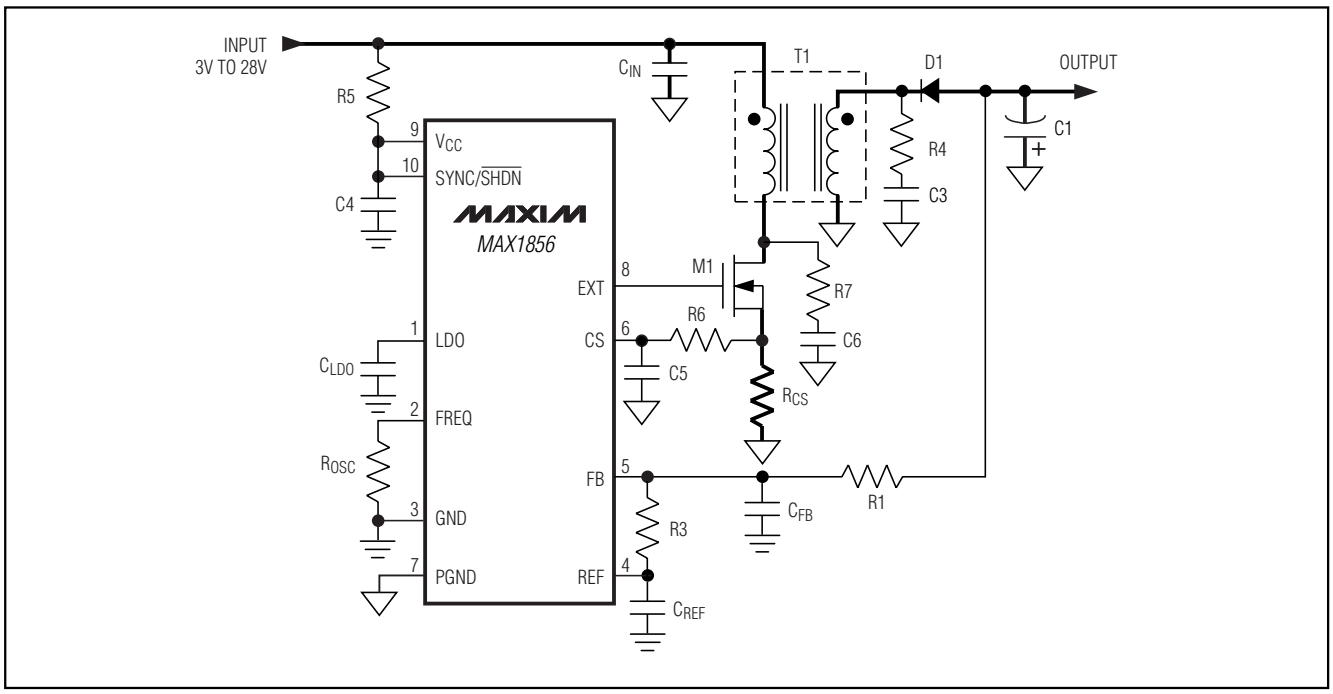

Figure 3. Feedback Compensation and Snubber Circuits

$$R7 = \frac{t_f}{C6}$$

This gives a value of about 22Ω for R7. However, this snubber adds capacity to the MOSFET output, and this in turn increases the dissipation in the MOSFET during turn-on.

The selection of the input and output snubbers is an interactive process. The design procedures above provide initial component recommendations, but the actual values depend on the layout and transformer winding practices used in the actual application.

Applications Information

Voice-over-IP CPE systems have +5V or +12V available from which the talk battery voltage and the ringer voltage must be generated. The examples given below are circuits using these supply voltages to generate the negative power supplies needed in such applications.

Low Input Voltage

IP phones and routers require -48V. For cost-sensitive applications, this needs to be used from an available +5V supply. The circuit in Figure 4 is an example of such a circuit using an off-the-shelf transformer from Coiltronics and ICE components.

SLIC Power Supply with Split Feedback

Telephones in broadband systems use low-power-consuming SLICs that reduce the power drain by providing the option of using two voltages for loop supervision. The load on each output is dependent on the number of lines on- or off-hook. The higher voltage is used to generate ring battery voltage when the subscriber is on-hook, while a second lower voltage is used to generate talk battery voltage when off-hook is detected. The actual value of these two voltages can be adjusted based on system requirements and the specific SLIC used. The design given here specifically addresses the supply requirements for the AMD79R79 SLIC device with on-chip ringing. The input voltage is 12V nominal, and the output voltages are -24V at 400mA and -72V at 100mA. The transformer turns ratio is 1:2:2:2, where 24V appears across each secondary winding. The -72V output is derived from the -24V output by stacking the secondary windings in series as shown in Figure 1. A split feedback is used, using resistors R1, R2, and R3. This allows for accurate regulation of both outputs (see *Typical Operating Characteristics*).

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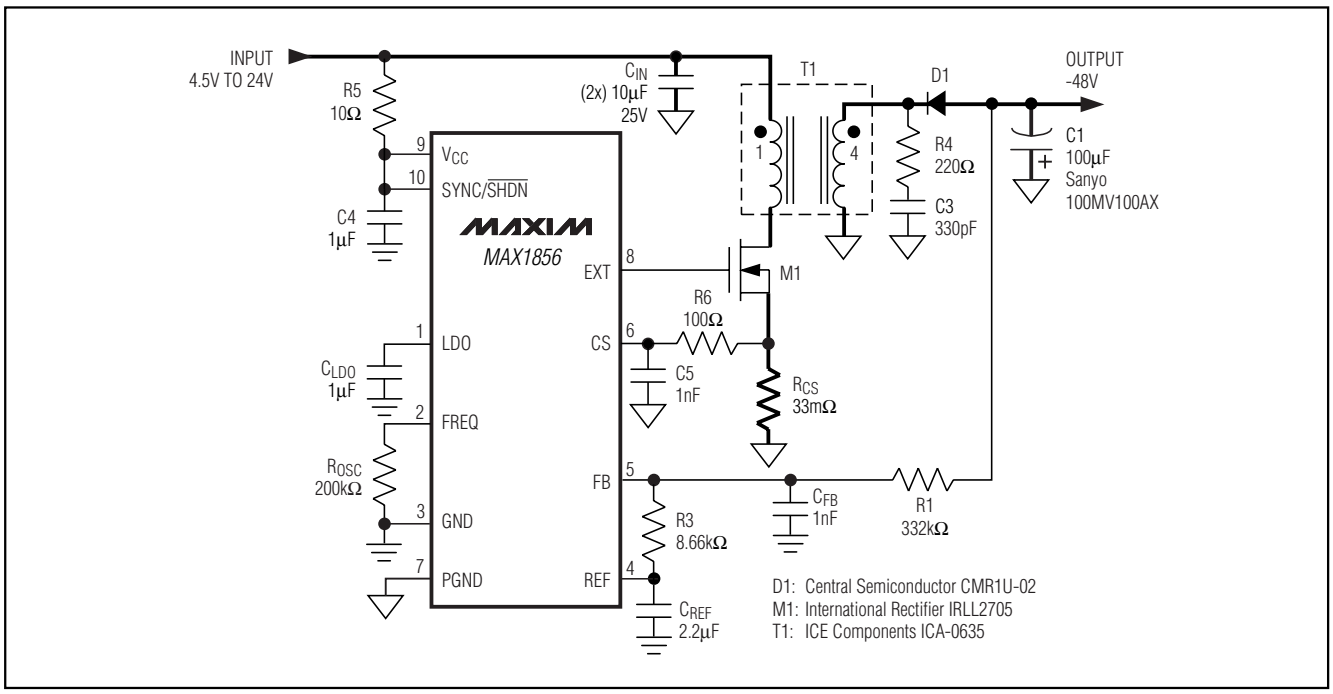
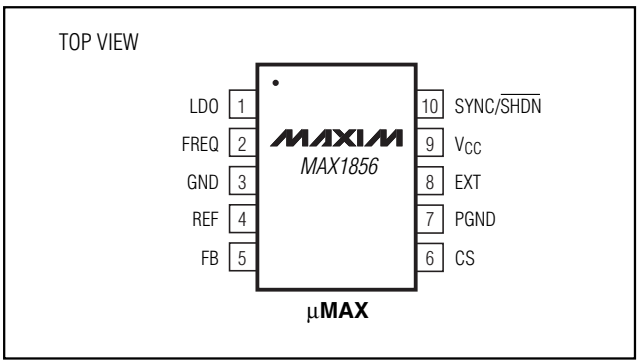


Figure 4. -48V Output Application Circuit

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1538

PROCESS: BiCMOS

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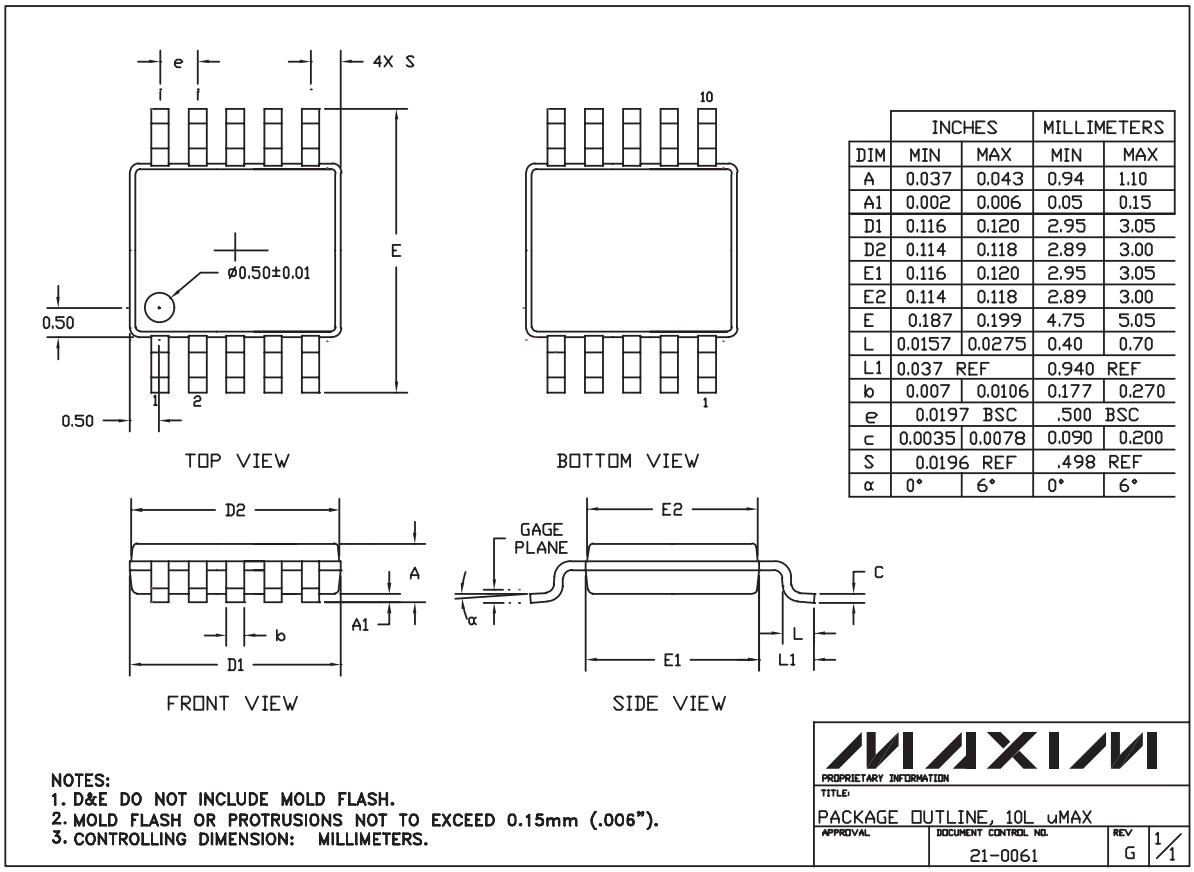
Package Information



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°