Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V_{CC} .....-0.3V to +30V
EN1–EN4 .....-0.3V to (V_{CC} + 0.3V)
OUT1–OUT4 (push-pull).....-0.3V to (V_{CC} + 0.3V)
OUT1–OUT4 (open-drain).....-0.3V to +30V
$\overline{RESET}$ (push-pull) .....-0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (open-drain).....-0.3V to 30V
IN1–IN4.....-0.3V to (V_{CC} + 0.3V)
$\overline{MR}$, TOL, TH1, TH0 .....-0.3V to (V_{CC} + 0.3V)
CDLY1–CDLY4 .....-0.3V to +6V
CRESET .....-0.3V to (V_{CC} + 0.3V)
Input/Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 25mW/°C above +70°C) 2000mW
20-Pin TQFN (derate 25.6mW/°C above +70°C) 2051mW
24-Pin TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.2V to 28V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
Operating Voltage Range	V_{CC}	(Note 2)		2.2		28.0	V
Undervoltage Lockout	UVLO	(Note 2)		1.8	1.9	2.0	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$	V_{CC} falling			50		mV
V_{CC} Supply Current	I_{CC}	All OUT_ and $\overline{RESET}$ at logic-high (IN_ current excluded)	V_{CC} = 3.3V		40	75	µA
			V_{CC} = 12V		47	75	
			V_{CC} = 28V		52	80	
INPUTS (IN_)							
IN_ Thresholds (IN_ Falling)	V_{TH}	3.3V threshold, TOL = GND		2.970	3.052	3.135	V
		3.3V threshold, TOL = V_{CC}		2.805	2.888	2.970	
		2.5V threshold, TOL = GND		2.250	2.313	2.375	
		2.5V threshold, TOL = V_{CC}		2.125	2.187	2.250	
		1.8V threshold, TOL = GND		1.620	1.665	1.710	
		1.8V threshold, TOL = V_{CC}		1.530	1.575	1.620	
		1.5V threshold, TOL = GND		1.350	1.387	1.425	
		1.5V threshold, TOL = V_{CC}		1.275	1.312	1.350	
		1.2V threshold, TOL = GND		1.080	1.110	1.140	
		1.2V threshold, TOL = V_{CC}		1.020	1.050	1.080	
Adjustable Threshold (IN_ Falling)	V_{TH}	TOL = GND		0.492	0.5	0.508	V
		TOL = V_{CC}		0.463	0.472	0.481	
IN_ Hysteresis (IN_ Rising)	V_{HYST}				0.5		%
IN_ Input Resistance		Fixed threshold		500	918		kΩ
IN_ Input Current	I_L	Adjustable threshold only ($V_{IN\_}$ = 1V)		-100		+100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.2V to 28V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRESET AND CDLY_						
CRESET Threshold	$V_{TH-RESET}$	CRESET rising, V_{CC} = 3.3V	0.465	0.5	0.535	V
CRESET Charge Current	$I_{CH-RESET}$	V_{CC} = 3.3V	380	500	620	nA
CDLY_ Threshold	$V_{TH-CDLY}$	CDLY_ rising, V_{CC} = 3.3V	0.95	1	1.05	V
CDLY_ Charge Current	$I_{CH-CDLY}$	V_{CC} = 3.3V	200	250	300	nA
DIGITAL LOGIC INPUTS (EN_, $\overline{MR}$, TOL, TH1, TH0)						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
TH1, TH0 Logic-Input Floating				0.6		V
TOL, TH1, TH0 Logic-Input Current		V_{TOL}, V_{TH1}, V_{TH0} = GND or V_{CC}	-1		+1	µA
EN_ Input Leakage Current		$V_{EN\_}$ = V_{CC} or GND	-100		+100	nA
$\overline{MR}$ Internal Pullup Current		V_{CC} = 3.3V	250	535	820	nA
OUTPUTS (OUT_, $\overline{RESET}$)						
Output Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90µA			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA			0.35	
Output High Voltage (Push-Pull)	V_{OH}	V_{CC} ≥ 3V, I_{SOURCE} = 500µA	0.8 x V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			
Output Leakage Current (Open-Drain)	I_{LKG}	Output not asserted low, V_{OUT} = 28V			1	µA
Reset Timeout Period	t_{RP}	CRESET = V_{CC}, V_{CC} = 3.3V	140	190	260	ms
		CRESET open		0.030		
TIMING						
IN_ to OUT_ Propagation Delay	t_{DELAY+}	IN_ rising, CDLY_ open		35		µs
	t_{DELAY-}	IN_ falling, CDLY_ open		20		
IN_ to $\overline{RESET}$ Propagation Delay	$t_{RST-DELAY}$	IN_ falling		35		µs
$\overline{MR}$ Minimum Input Pulse Width		(Note 3)	2			µs
EN_ or $\overline{MR}$ Glitch Rejection				280		ns
EN_ to OUT_ Delay	t_{OFF}	From device enabled to device disabled		3		µs
	t_{ON}	From device disabled to device enabled (CDLY_ open)		30		
$\overline{MR}$ to $\overline{RESET}$ Delay		$\overline{MR}$ falling		3		µs

Note 1: Devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: Operating below the UVLO causes all outputs to go low. The outputs are guaranteed to be in the correct state for V_{CC} down to 1.2V.

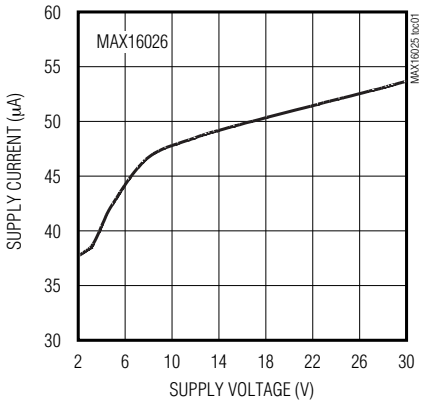
Note 3: In order to guarantee an assertion, the minimum input pulse width must be greater than 2µs.

Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

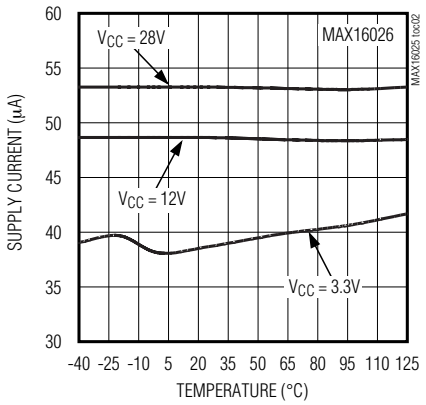
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

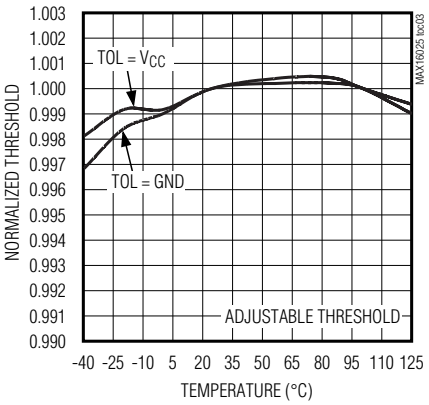
SUPPLY CURRENT vs. SUPPLY VOLTAGE



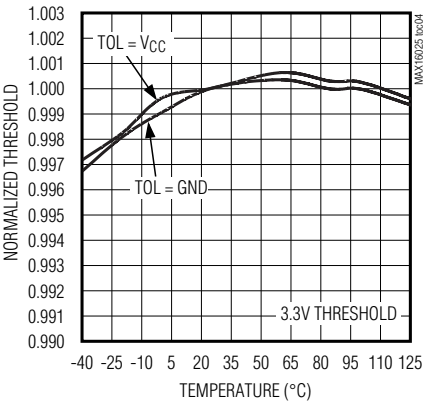
SUPPLY CURRENT vs. TEMPERATURE



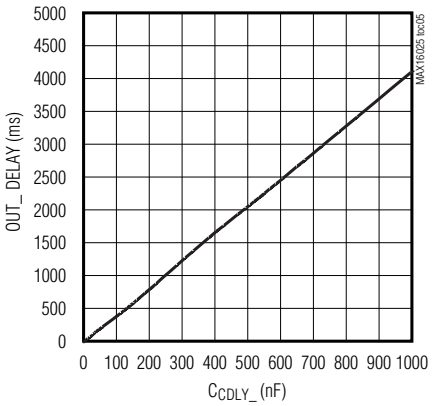
NORMALIZED ADJUSTABLE THRESHOLD vs. TEMPERATURE



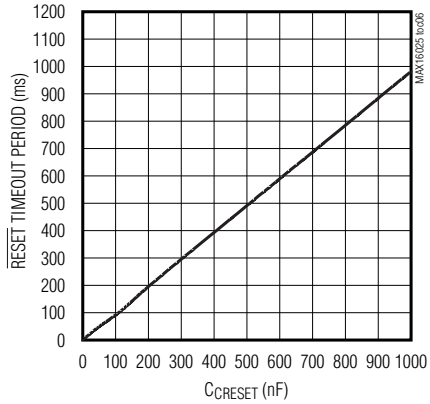
NORMALIZED ADJUSTABLE THRESHOLD vs. TEMPERATURE



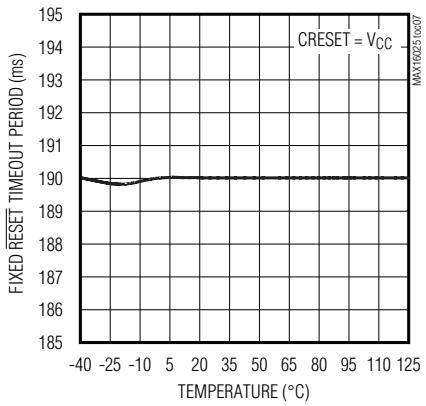
OUT_ DELAY vs. $C_{CDLY\_}$



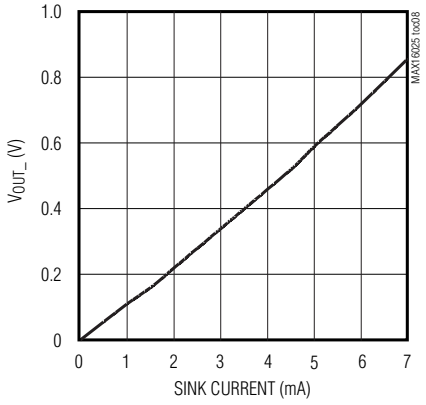
$\overline{RESET}$ TIMEOUT PERIOD vs. C_{CRESET}



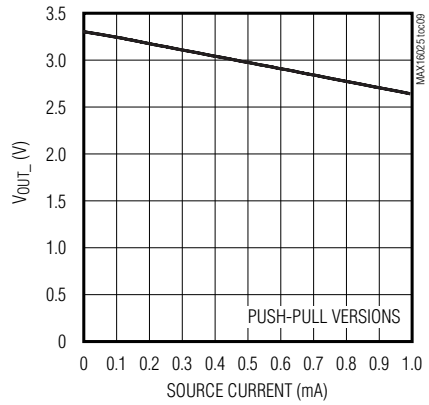
FIXED $\overline{RESET}$ TIMEOUT PERIOD vs. TEMPERATURE



OUT_ LOW VOLTAGE vs. SINK CURRENT



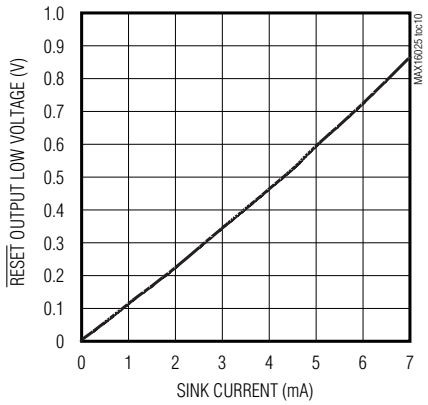
OUT_ HIGH VOLTAGE vs. SOURCE CURRENT



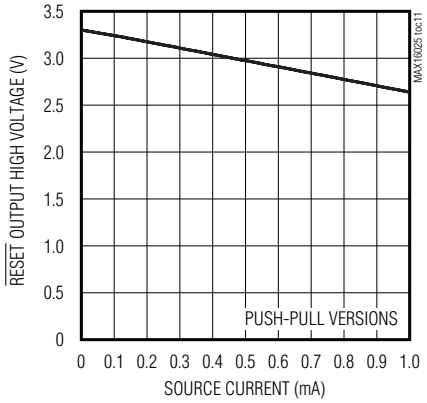
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

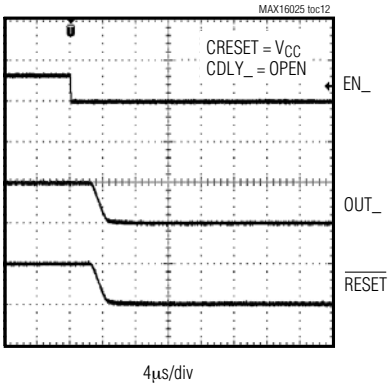
$\overline{RESET}$ OUTPUT LOW VOLTAGE vs. SINK CURRENT



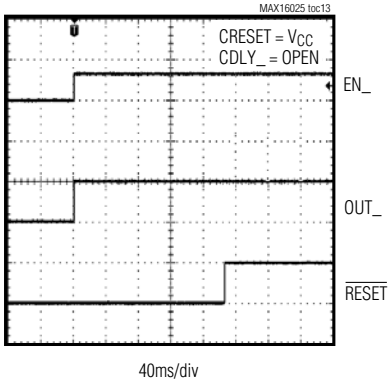
$\overline{RESET}$ OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



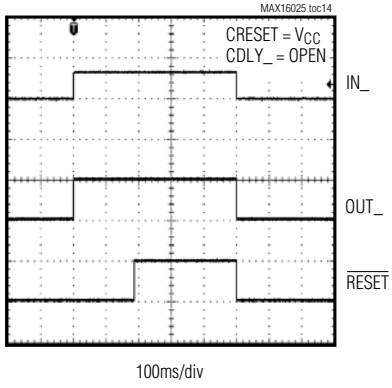
ENABLE TURN-OFF



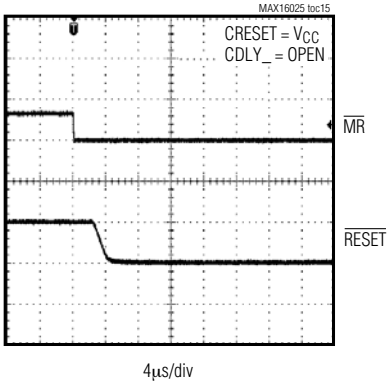
ENABLE TURN-ON



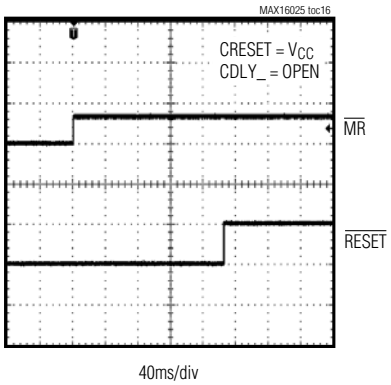
$\overline{RESET}$ TIMEOUT DELAY



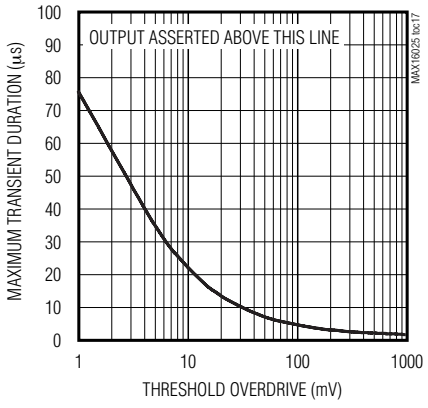
$\overline{MR}$ FALLING vs. $\overline{RESET}$



$\overline{MR}$ RISING vs. $\overline{RESET}$



MAXIMUM TRANSIENT DURATION vs. THRESHOLD OVERDRIVE



Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

Pin Description

PIN			NAME	FUNCTION
MAX16025/ MAX16026	MAX16027/ MAX16028	MAX16029/ MAX16030		
1	1	1	V_{CC}	Supply Voltage Input. Connect a 2.2V to 28V supply voltage to power the device. All outputs are low when V_{CC} is below the UVLO. For noisy systems, bypass V_{CC} to GND with a 0.1µF capacitor.
2	2	2	IN1	Monitored Input 1. When the voltage at IN1 exceeds its threshold, OUT1 goes high after the capacitor-adjustable delay period. When the voltage at IN1 falls below its threshold, OUT1 goes low after a propagation delay.
3	3	3	IN2	Monitored Input 2. When the voltage at IN2 exceeds its threshold, OUT2 goes high after the capacitor-adjustable delay period. When the voltage at IN2 falls below its threshold, OUT2 goes low after a propagation delay.
—	4	4	IN3	Monitored Input 3. When the voltage at IN3 exceeds its threshold, OUT3 goes high after the capacitor-adjustable delay period. When the voltage at IN3 falls below its threshold, OUT3 goes low after a propagation delay.
—	—	5	IN4	Monitored Input 4. When the voltage at IN4 exceeds its threshold, OUT4 goes high after the capacitor-adjustable delay period. When the voltage at IN4 falls below its threshold, OUT4 goes low after a propagation delay.
4	5	6	TOL	Threshold Tolerance Input. Connect TOL to GND to select thresholds 5% below nominal. Connect TOL to V_{CC} to select thresholds 10% below nominal.
5	6	7	GND	Ground
6	7	8	EN1	Active-High Logic-Enable Input 1. Driving EN1 low causes OUT1 to go low regardless of the input voltage. Drive EN1 high to enable the monitoring comparator.
7	8	9	EN2	Active-High Logic-Enable Input 2. Driving EN2 low causes OUT2 to go low regardless of the input voltage. Drive EN2 high to enable the monitoring comparator.
—	9	10	EN3	Active-High Logic-Enable Input 3. Driving EN3 low causes OUT3 to go low regardless of the input voltage. Drive EN3 high to enable the monitoring comparator.
—	—	11	EN4	Active-High Logic-Enable Input 4. Driving EN4 low causes OUT4 to go low regardless of the input voltage. Drive EN4 high to enable the monitoring comparator.
8	10	12	TH1	Threshold Select Input 1. Connect TH1 to V_{CC} or GND, or leave it open to select the input-voltage threshold option in conjunction with TH0 (see Table 2).
9	11	13	TH0	Threshold Select Input 0. Connect TH0 to V_{CC} or GND, or leave it open to select the input-voltage threshold option in conjunction with TH1 (see Table 2).
—	—	14	OUT4	Output 4. When the voltage at IN4 is below its threshold or EN4 goes low, OUT4 goes low.
—	12	15	OUT3	Output 3. When the voltage at IN3 is below its threshold or EN3 goes low, OUT3 goes low.
10	13	16	OUT2	Output 2. When the voltage at IN2 is below its threshold or EN2 goes low, OUT2 goes low.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX16025/ MAX16026	MAX16027/ MAX16028	MAX16029/ MAX16030		
11	14	17	OUT1	Output 1. When the voltage at IN1 is below its threshold or EN1 goes low, OUT1 goes low.
12	15	18	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ asserts low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or $\overline{MR}$ is asserted. $\overline{RESET}$ remains asserted for the reset timeout period after all of the monitored voltages exceed their respective threshold, all EN_ are high, all OUT_ are high, and $\overline{MR}$ is deasserted.
13	16	19	$\overline{MR}$	Active-Low Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$ low. $\overline{RESET}$ remains low for the reset timeout period after $\overline{MR}$ is deasserted (as long as all OUT_ are high).
14	17	20	CRESET	Capacitor-Adjustable Reset Delay Input. Connect an external capacitor from CRESET to GND to set the reset timeout period or connect to V_{CC} for the default 140ms minimum reset timeout period. Leave CRESET open for internal propagation delay.
—	—	21	CDLY4	Capacitor-Adjustable Delay Input 4. Connect an external capacitor from CDLY4 to GND to set the IN4 to OUT4 (and EN4 to OUT4) delay period. Leave CDLY4 open for internal propagation delay.
—	18	22	CDLY3	Capacitor-Adjustable Delay Input 3. Connect an external capacitor from CDLY3 to GND to set the IN3 to OUT3 (and EN3 to OUT3) delay period. Leave CDLY3 open for internal propagation delay.
15	19	23	CDLY2	Capacitor-Adjustable Delay Input 2. Connect an external capacitor from CDLY2 to GND to set the IN2 to OUT2 (and EN2 to OUT2) delay period. Leave CDLY2 open for internal propagation delay.
16	20	24	CDLY1	Capacitor-Adjustable Delay Input 1. Connect an external capacitor from CDLY1 to GND to set the IN1 to OUT1 (and EN1 to OUT1) delay period. Leave CDLY1 open for internal propagation delay.
—	—	—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane.

Table 1. Output State*

EN_	IN_	OUT_
Low	$V_{IN\_} < V_{TH}$	Low
High	$V_{IN\_} < V_{TH}$	Low
Low	$V_{IN\_} > V_{TH}$	Low
High	$V_{IN\_} > V_{TH}$	OUT_ = high (MAX16026/MAX16028/ MAX16030)
		OUT_ = high impedance (MAX16025/MAX16027/ MAX16029)

**When V_{CC} falls below the UVLO, all outputs go low regardless of the state of EN_ and $V_{IN\_}$. The outputs are guaranteed to be in the correct state for V_{CC} down to 1.2V.*

Table 2. Input-Voltage Threshold Selector

TH1/TH0 LOGIC	IN1 (ALL VERSIONS) (V)	IN2 (ALL VERSIONS) (V)	IN3 (MAX16027/ MAX16028) (V)	IN4 (MAX16029/ MAX16030) (V)
Low/Low	3.3	2.5	1.8	1.5
Low/High	3.3	1.8	Adj	Adj
Low/Open	3.3	1.5	Adj	Adj
High/Low	3.3	1.2	1.8	2.5
High/High	2.5	1.8	Adj	Adj
High/Open	3.3	Adj	2.5	Adj
Open/Low	3.3	Adj	Adj	Adj
Open/High	2.5	Adj	Adj	Adj
Open/Open	Adj	Adj	Adj	Adj

Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

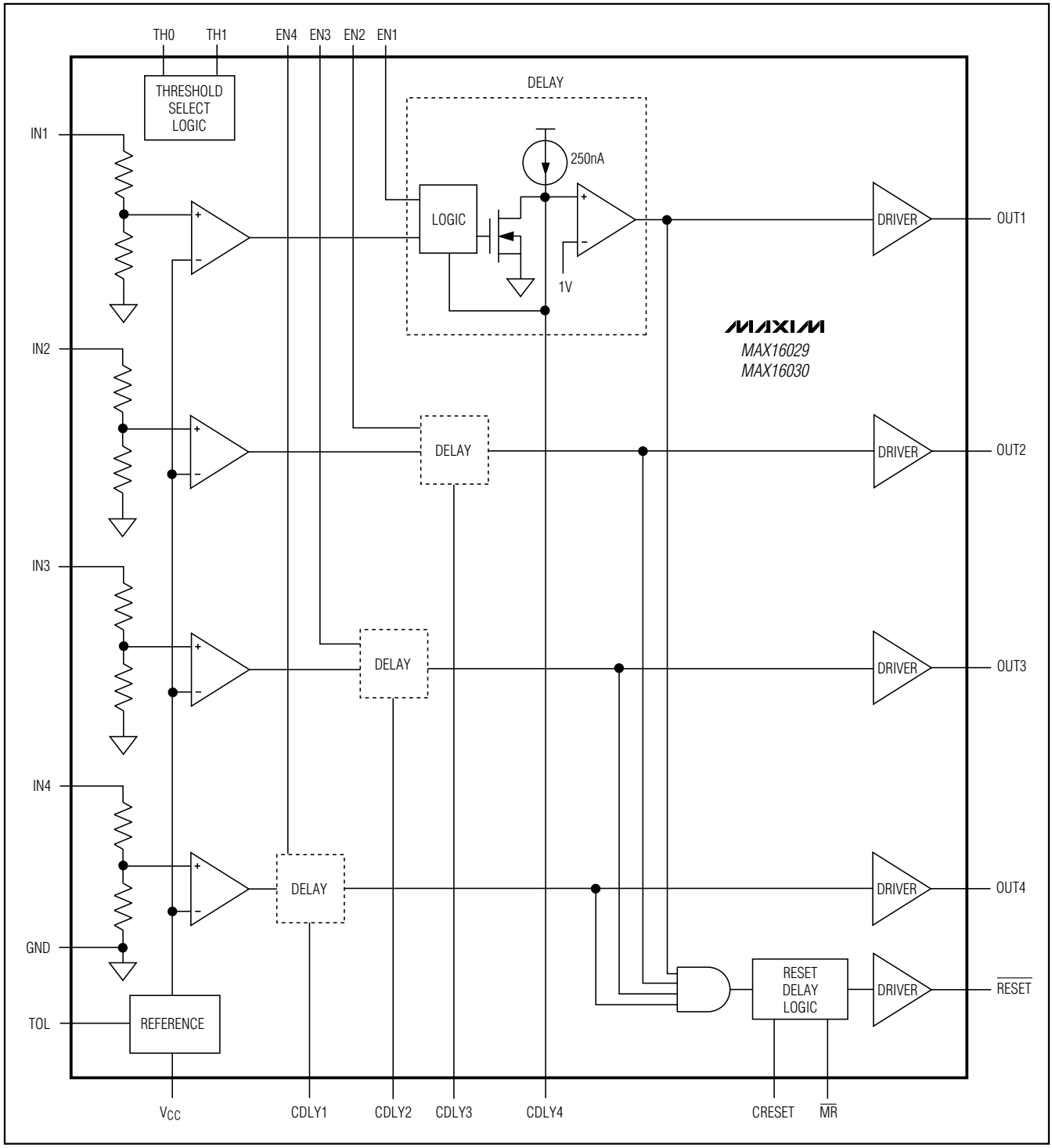


Figure 1. MAX16029/MAX16030 Simplified Functional Diagram

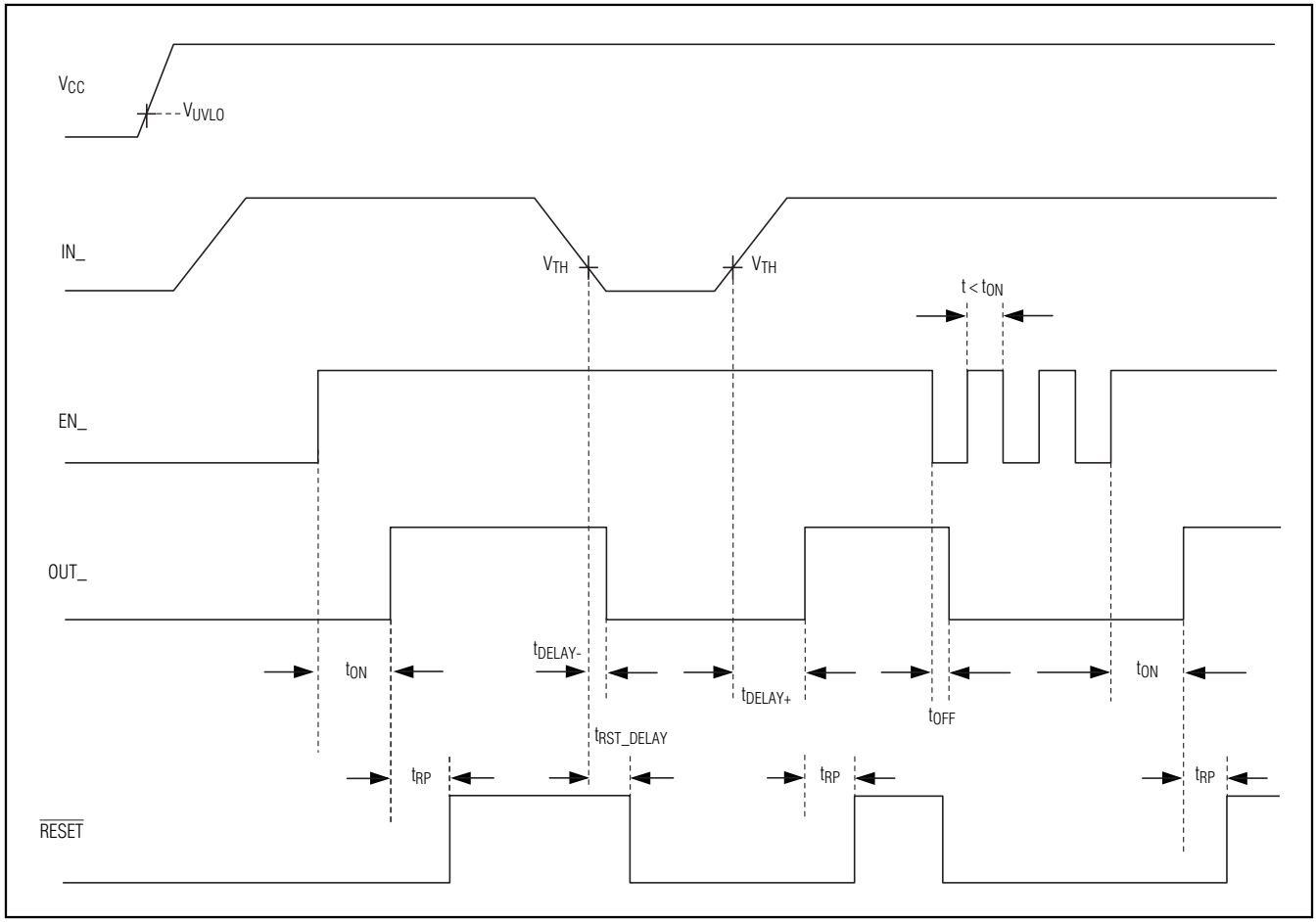


Figure 2. Timing Diagram (CDLY_ Open)

Detailed Description

The MAX16025–MAX16030 are low-voltage, accurate, dual-/triple-/quad-voltage microprocessor (µP) supervisors in a small TQFN package. These devices provide supervisory and sequencing functions for complex multivoltage systems. The MAX16025/MAX16026 monitor two voltages, the MAX16027/MAX16028 monitor three voltages, and the MAX16029/MAX16030 monitor four voltages.

The MAX16025–MAX16030 offer independent outputs and enable functions for each monitored voltage. This configuration allows the device to operate as four separate supervisory circuits or be daisy-chained together to allow controlled sequencing of power supplies during power-up initialization. When all of the monitored voltages exceed their respective thresholds, an independent reset output deasserts to allow the system processor to operate.

These devices offer enormous flexibility as there are nine threshold options that are selected through two threshold-select logic inputs. Each monitor circuit also offers an independent enable input to allow both digital and analog control of each monitor output. A tolerance select input allows these devices to be used in systems requiring 5% or 10% power-supply tolerances. In addition, the time delays and reset timeout can be adjusted using small capacitors. There is also a fixed 140ms minimum reset timeout feature.

Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

Applications Information

Tolerance

The MAX16025–MAX16030 feature a pin-selectable threshold tolerance. Connect TOL to GND to select the thresholds 5% below the nominal value. Connect TOL to V_{CC} to select the threshold tolerance 10% below the nominal voltage. Do not leave TOL unconnected.

Adjustable Input

These devices offer several monitoring options with both fixed and/or adjustable reset thresholds (see Table 2). For the adjustable threshold inputs, the threshold voltage (V_{TH}) at each adjustable IN_ input is typically 0.5V (TOL = GND) or 0.472V (TOL = V_{CC}). To monitor a voltage V_{INTH}, connect a resistive divider network to the circuit as shown in Figure 3 and use the following equation to calculate the threshold voltage:

$$V_{INTH} = V_{TH} \times \left(1 + \frac{R1}{R2}\right)$$

Choosing the proper external resistors is a balance between accuracy and power use. The input to the voltage monitor is a high-impedance input with a small 100nA leakage current. This leakage current contributes to the overall error of the threshold voltage where the output is asserted. This induced error is proportional to the value of the resistors used to set the threshold. With lower value resistors, this error is reduced, but the amount of power consumed in the resistors increases.

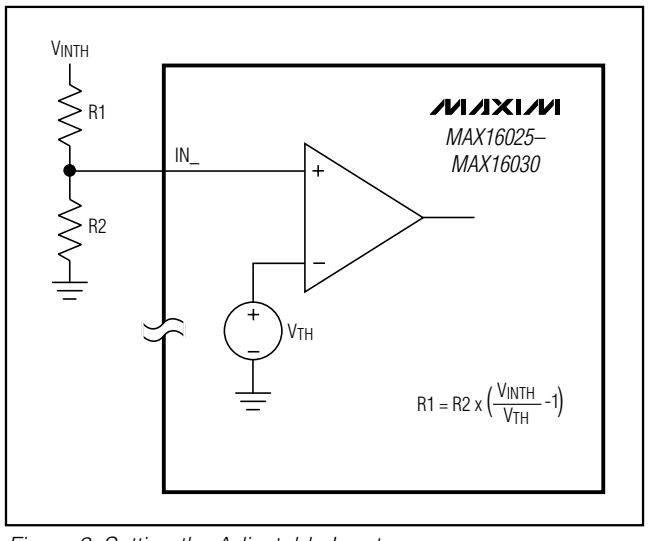


Figure 3. Setting the Adjustable Input

The following equation is provided to help estimate the value of the resistors based on the amount of acceptable error:

$$R_1 = \frac{e_A \times V_{INTH}}{I_L}$$

where e_A is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for ±1%), V_{INTH} is the voltage at which the output (OUT_) should assert, and I_L is the worst-case IN_ leakage current (see the *Electrical Characteristics*). Calculate R2 as follows:

$$R_2 = \frac{V_{TH} \times R1}{V_{INTH} - V_{TH}}$$

Unused Inputs

Connect any unused IN_ and EN_ inputs to V_{CC}.

OUT_ Output

An OUT_ goes low when its respective IN_ input voltage drops below its specified threshold or when its EN_ goes low (see Table 1). OUT_ goes high when EN_ is high and $V_{IN\_}$ is above its threshold after a time delay. The MAX16025/MAX16027/MAX16029 feature open-drain, outputs while the MAX16026/MAX16028/MAX16030 have push-pull outputs. Open-drain outputs require an external pullup resistor to any voltage from 0 to 28V.

$\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ asserts low when any of the monitored voltages (IN_) falls below its respective threshold, any EN_ goes low, or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for the reset timeout period after all of the monitored voltages exceed their respective threshold, all EN_ are high, all OUT_ are high, and $\overline{\text{MR}}$ is deasserted. The MAX16025/MAX16027/MAX16029 have an open-drain, active-low reset output, while the MAX16026/MAX16028/MAX16030 have a push-pull, active-low reset output. Open-drain $\overline{\text{RESET}}$ requires an external pullup resistor to any voltage from 0 to 28V.

Adjustable Reset Timeout Period (CRESET)

All of these parts offer an internally fixed reset timeout (140ms min) by connecting CRESET to V_{CC}. The reset timeout can also be adjusted by connecting a capacitor from CRESET to GND. When the voltage at CRESET reaches 0.5V, $\overline{\text{RESET}}$ goes high. When $\overline{\text{RESET}}$ goes high, CRESET is immediately held low.

Calculate the reset timeout period as follows:

$$t_{RP} = \frac{V_{TH\text{-}RESET}}{I_{CH\text{-}RESET}} \times C_{CRESET} + 35 \times 10^{-6}$$

where $V_{TH\text{-}RESET}$ is 0.5V, $I_{CH\text{-}RESET}$ is 0.5µA, t_{RP} is in seconds, and C_{CRESET} is in Farads. To ensure timing accuracy and proper operation, minimize leakage at C_{CRESET}.

Adjustable Delay (CDLY_)

When V_{IN} rises above V_{TH} with EN_ high, the internal 250nA current source begins charging an external capacitor connected from CDLY_ to GND. When the voltage at CDLY_ reaches 1V, OUT_ goes high. When OUT_ goes high, CDLY_ is immediately held low. Adjust the delay (t_{DELAY}) from when V_{IN} rises above V_{TH} (with EN_ high) to OUT_ going high according to the equation:

$$t_{DELAY} = \frac{V_{TH\text{-}CDLY}}{I_{CH\text{-}CDLY}} \times C_{CDLY} + 35 \times 10^{-6}$$

where $V_{TH\text{-}CDLY}$ is 1V, $I_{CH\text{-}CDLY}$ is 0.25µA, C_{CDLY} is in Farads, t_{DELAY} is in seconds, and t_{DELAY+} is the internal propagation delay of the device. To ensure timing accuracy and proper operation, minimize leakage at CDLY.

Manual-Reset Input ($\overline{MR}$)

Many µP-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{MR}$ asserts $\overline{RESET}$ low. $\overline{RESET}$ remains asserted while $\overline{MR}$ is low and during the reset timeout period (140ms fixed or capacitor adjustable) after $\overline{MR}$ returns high. The $\overline{MR}$ input has a 500nA internal pullup, so it can be left unconnected, if not used. $\overline{MR}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function. External debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Pullup Resistor Values

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{CC} = 2.25V and the pullup voltage is 28V, keep the sink current less than 0.5mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 56kΩ. For a 12V pullup, the resistor should be larger than 24kΩ. Note that the ability to sink current is dependent on the V_{CC} supply voltage.

Power-Supply Bypassing

The device operates with a V_{CC} supply voltage from 2.2V to 28V. When V_{CC} falls below the UVLO threshold, all the outputs go low and stay low until V_{CC} falls below 1.2V. For noisy systems or fast rising transients on V_{CC}, connect a 0.1µF ceramic capacitor from V_{CC} to GND as close to the device as possible to provide better noise and transient immunity.

Ensuring Valid Output with V_{CC} Down to 0V (MAX16026/MAX16028/MAX16030 Only)

When V_{CC} falls below 1.2V, the ability for the output to sink current decreases. In order to ensure a valid output as V_{CC} falls to 0V, connect a 100kΩ resistor from OUT/$\overline{RESET}$ to GND.

Typical Application Circuits

Figures 4 and 5 show typical applications for the MAX16025–MAX16030. In high-power applications, using an n-channel device reduces the loss across the MOSFETs as it offers a lower drain-to-source on-resistance. However, an n-channel MOSFET requires a sufficient V_{GS} voltage to fully enhance it for a low R_{DS_ON}. The application in Figure 4 shows the MAX16027 configured in a multiple-output sequencing application. Figure 5 shows the MAX16029 in a power-supply sequencing application using n-channel MOSFETs.

Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

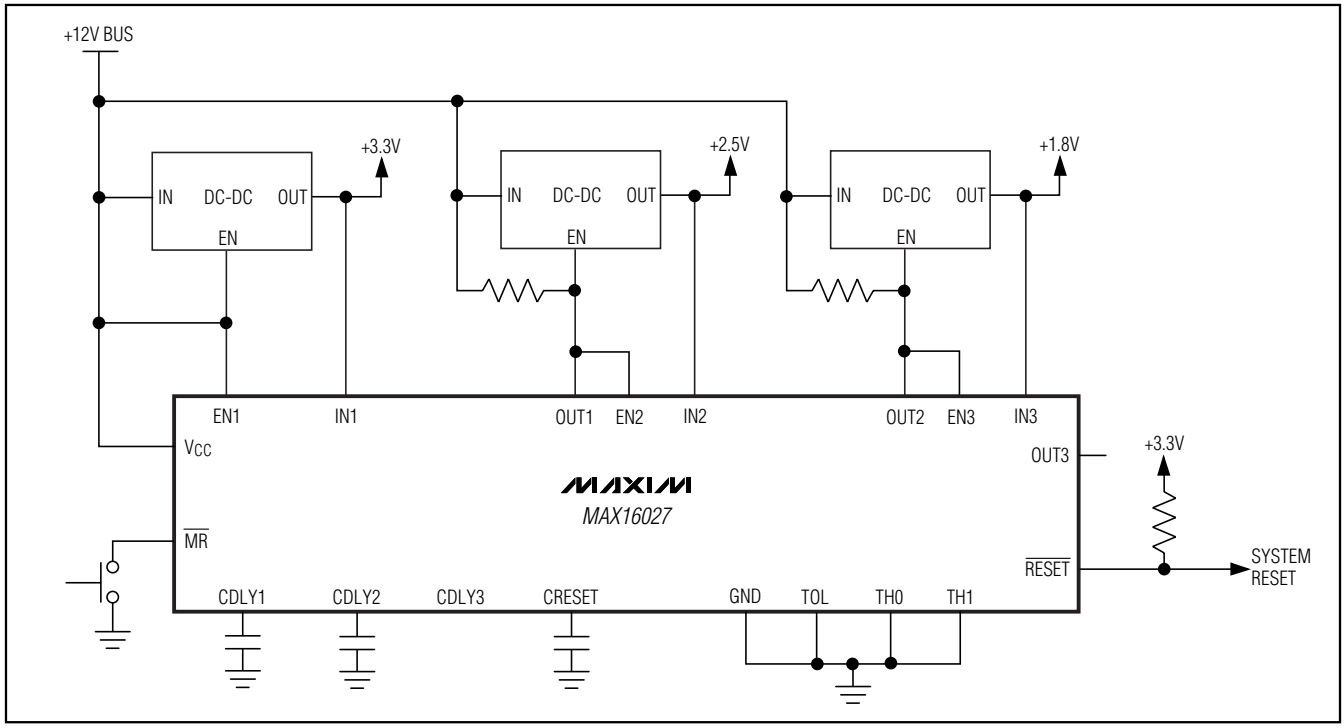


Figure 4. Sequencing Multiple-Voltage System

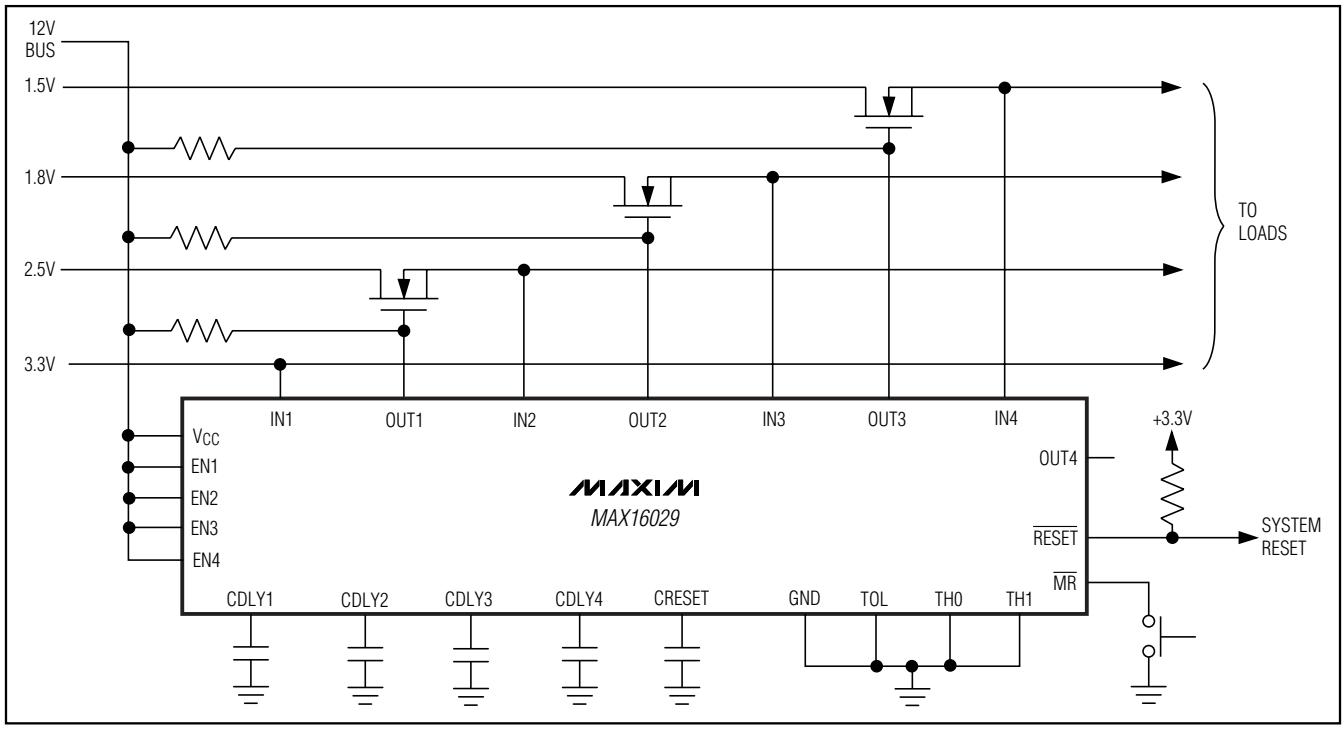
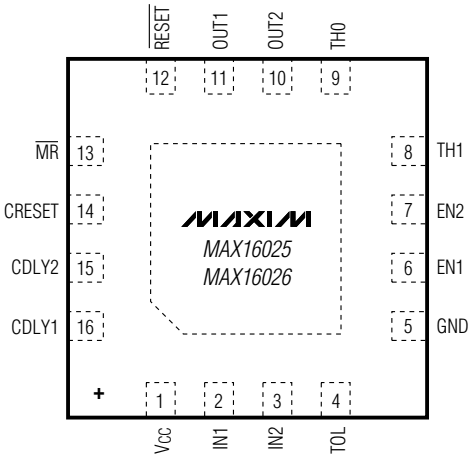


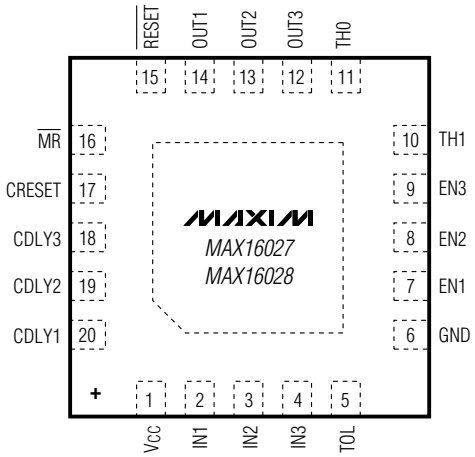
Figure 5. Multiple-Voltage Sequencing Using n-Channel FETs

Pin Configurations (continued)

TOP VIEW



THIN QFN
(4mm x 4mm)



THIN QFN
(4mm x 4mm)

Chip Information

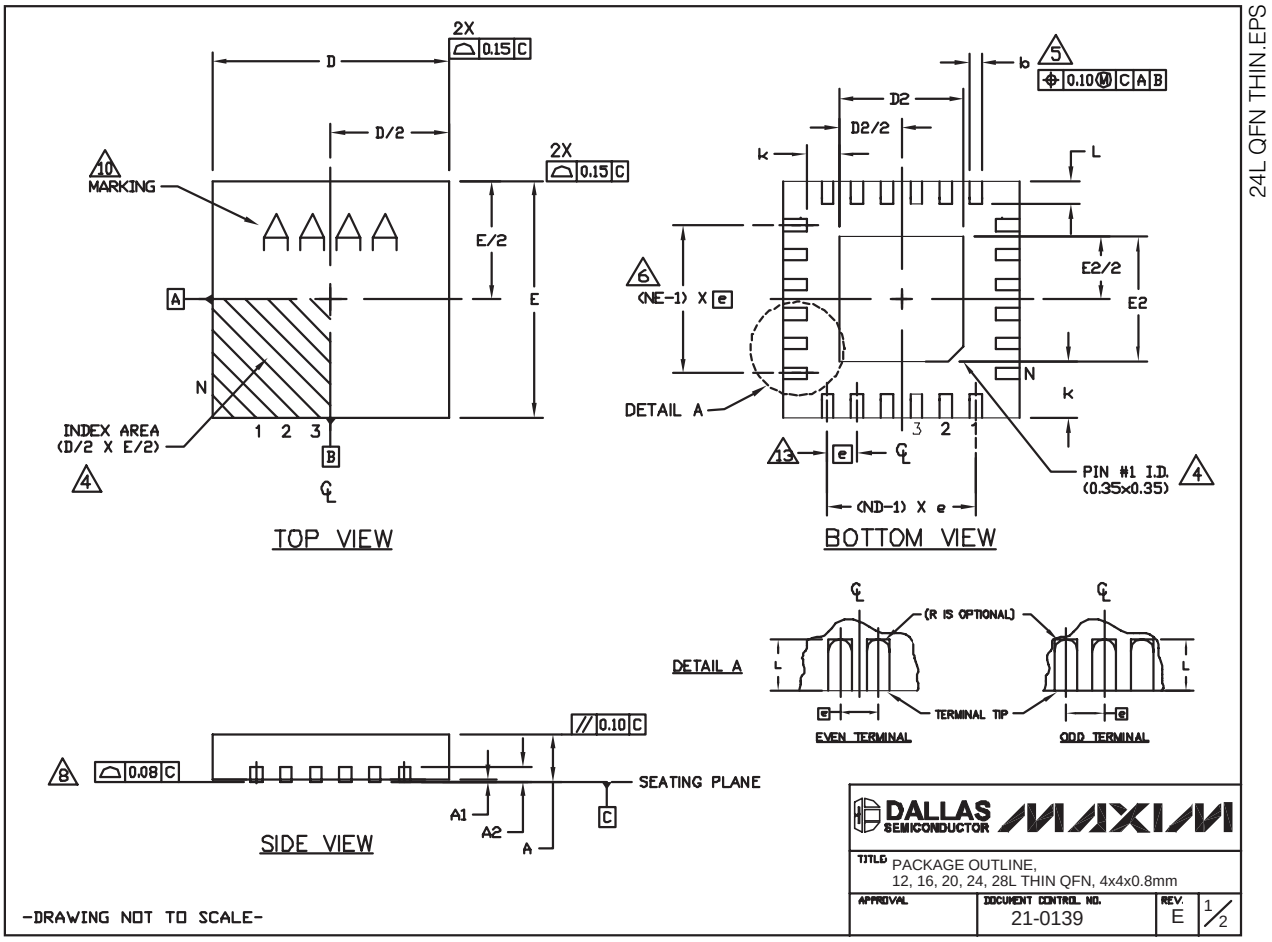
PROCESS: BICMOS

TRANSISTOR COUNT: 3642

Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Dual-/Triple-/Quad-Voltage, Capacitor-Adjustable, Sequencing/Supervisory Circuits

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444–3, T2444–4 AND T2844–1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

Revision History

Pages changed at Rev 1: 1, 3, 15

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