Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{CC} ..... -0.3V to +6V
V_L ..... -0.3V to +4V
I/O V_{CC} ..... -0.3V to (V_{CC} + 0.3V)
I/O V_L ..... -0.3V to (V_L + 0.3V)
$\overline{SHDN}$ ..... -0.3V to +6V
Short-Circuit Duration I/O V_L, I/O V_{CC} to GND ..... Continuous
Power Dissipation (T_A = +70°C)
6-Pin µDFN (derate 2.1mW/°C above +70°C) 168mW
10-Pin UTQFN (derate 6.9mW/°C above +70°C) 559mW

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
6-Pin µDFN ..... 477°C/W
10-Pin UTQFN ..... 20.1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JC}) (Note 1)
6-Pin µDFN ..... 20.1°C/W
10-Pin UTQFN ..... 143.1°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +1.65V to +5.5V, V_L = +1.1V to minimum of either +3.6V or ((V_{CC} + 0.3V)), I/O V_L and I/O V_{CC} are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_L Supply Range	V_L	V_{CC} > 3.3V	1.1		3.6V	V
		V_{CC} ≤ 3.3V	1.1		V_{CC} + 0.3V	
V_{CC} Supply Range	V_{CC}		1.65		5.5	V
Supply Current from V_{CC}	I_{QVCC}				10	µA
Supply Current from V_L	I_{QVL}				15	µA
V_{CC} Shutdown-Mode Supply Current	I_{SD-VCC}	T_A = +25°C, $\overline{SHDN}$ = GND		0.03	1	µA
V_L Shutdown-Mode Supply Current	I_{SD-VL}	T_A = +25°C, $\overline{SHDN}$ = GND		0.03	1	µA
I/O V_L and I/O V_{CC} Shutdown-Mode Leakage Current	I_{SD-LKG}	T_A = +25°C, $\overline{SHDN}$ = GND		0.02	0.5	µA
$\overline{SHDN}$ Input Leakage		T_A = +25°C		0.02	0.1	µA
ESD PROTECTION						
I/O V_{CC} (Note 4)		Human Body Model		±15V		kV
		IEC 61000-4-2 Air-Gap Discharge		±15V		
		IEC 61000-4-2 Contact Discharge		±8V		
All Other Pins		Human Body Model		±2		kV
LOGIC-LEVEL THRESHOLDS						
I/O V_L Input-Voltage High	V_{IHL}		V_L - 0.2			V
I/O V_L Input-Voltage Low	V_{ILL}				0.15	V

Electrical Characteristics (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.1V to minimum of either +3.6V or ((V_{CC} + 0.3V)), I/O V_L and I/O V_{CC} are unconnected, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V_{CC} Input-Voltage High	V_{IHC}		V_{CC} - 0.4			V
I/O V_{CC} Input-Voltage Low	V_{ILC}				0.15	V
I/O V_L Output-Voltage High	V_{OHL}	I/O V_L source current = 20µA, $V_{I/O\ VCC}$ > V_{CC} - 0.4V	0.67 x V_L			V
I/O V_L Output-Voltage Low	V_{OLL}	I/O V_L sink current = 1mA, $V_{I/O\ VCC}$ < 0.15V			0.4	V
I/O V_{CC} Output-Voltage High	V_{OHC}	I/O V_{CC} source current = 20µA, $V_{I/O\ VL}$ > V_L - 0.2V	0.67 x V_{CC}			V
I/O V_{CC} Output-Voltage Low	V_{OLC}	I/O V_{CC} sink current = 1mA, $V_{I/O\ VL}$ < 0.15V			0.4	V
$\overline{SHDN}$ Input-Voltage High	$V_{IH\text{-}\overline{SHDN}}$	V_L > 1.2	V_L - 0.2			V
		1.1 ≤ V_L < 1.2	V_L - 0.1			
$\overline{SHDN}$ Input-Voltage Low	$V_{IL\text{-}\overline{SHDN}}$				0.15	V
I/O V_L-to-I/O V_{CC} Resistance				80	250	Ω
V_{CC} Shutdown Threshold Low	$V_{TH\_L\_VCC}$	V_{CC} falling, V_L = +3.3V	0.5	0.8	1.1	V
V_{CC} Shutdown Threshold High	$V_{TH\_H\_VCC}$	V_{CC} rising, V_L = +3.3V	0.3	0.6	0.9	V
V_L Shutdown Threshold	V_{TH_VL}		0.35	0.75	1.06	V
Pullup Resistance		V_{CC} = V_L = +3.3V	6	10	15.5	kΩ
RISE/FALL-TIME ACCELERATOR STAGE						
Accelerator Pulse Duration				20		ns
I/O V_L Output-Accelerator Source Impedance		V_L = 1.7V		13		Ω
I/O V_{CC} Output-Accelerator Source Impedance		V_{CC} = 2.2V		17		Ω
I/O V_L Output-Accelerator Source Impedance		V_L = 3.2V		6		Ω
I/O V_{CC} Output-Accelerator Source Impedance		V_{CC} = 3.6V		10		Ω

Timing Characteristics For +1.2V ≤ V_L ≤ Minimum Of Either +3.6V OR (V_{CC} + 0.3V)

(V_{CC} ≤ ±5.5V, +1.2V ≤ V_L ≤ minimum of either +3.6V or ((V_{CC} + 0.3V)), R_S = 50Ω, R_L = 1MΩ, C_L = 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I/O V_{CC} Rise Time	t_{RVCC}	Push-pull driving, Figure 1a			7	25	ns
		Open-drain driving, Figure 1c			170	400	
I/O V_{CC} Fall Time	t_{FVCC}	Push-pull driving, Figure 1a			6	37	ns
		Open-drain driving, Figure 1c			20	50	
I/O V_L Rise Time	t_{RVL}	Push-pull driving, Figure 1b			8	30	ns
		Open-drain driving, Figure 1d			180	400	
I/O V_L Fall Time	t_{FVL}	Push-pull driving, Figure 1			3	56	ns
		Open-drain driving, Figure 1d			30	60	
Propagation Delay	$t_{PD-VL-VCC}$	Driving I/O V_L	Push-pull driving		5	30	ns
			Open-drain driving		210	1000	
	$t_{PD-VCC-VL}$	Driving I/O V_{CC}	Push-pull driving		4	30	
			Open-drain driving		190	1000	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded	Push-pull driving			20	ns
			Open-drain driving			50	
Maximum Data Rate		Push-pull driving		8			Mbps
		Open-drain driving		500			kbps

Timing Characteristics For +1.1V ≤ V_L ≤ +1.2V

(V_{CC} ≤ ±5.5V, +1.1V ≤ V_L ≤ +1.2V, R_S = 50Ω, R_L = 1MΩ, C_L = 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I/O V_{CC} Rise Time	t_{RVCC}	Push-pull driving, Figure 1a			7	200	ns
		Open-drain driving, Figure 1c			170	400	
I/O V_{CC} Fall Time	t_{FVCC}	Push-pull driving, Figure 1a			6	37	ns
		Open-drain driving, Figure 1c			20	50	
I/O V_L Rise Time	t_{RVL}	Push-pull driving, Figure 1b			8	30	ns
		Open-drain driving, Figure 1d			180	400	
I/O V_L Fall Time	t_{FVL}	Push-pull driving, Figure 1			3	30	ns
		Open-drain driving, Figure 1d			30	60	
Propagation Delay	$t_{PD-VL-VCC}$	Driving I/O V_L	Push-pull driving		5	200	ns
			Open-drain driving		210	1000	
	$t_{PD-VCC-VL}$	Driving I/O V_{CC}	Push-pull driving		4	200	
			Open-drain driving		190	1000	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded	Push-pull driving			20	ns
			Open-drain driving			50	
Maximum Data Rate		Push-pull driving		1.2			Mbps
		Open-drain driving		500			kbps

Timing Characteristics For +1.8V ≤ V_L ≤ V_{CC} ≤ +3.3V

(+1.8V ≤ V_L ≤ V_{CC} ≤ +3.3V, R_S = 50Ω, R_L = 1MΩ, C_L = 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V at T_A = +25°C.) (Notes 2, 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V_{CC} Rise Time	t_{RVCC}	Push-pull driving, Figure 1a			15	ns
I/O V_{CC} Fall Time	t_{FVCC}	Push-pull driving, Figure 1a			15	ns
I/O V_L Rise Time	t_{RVL}	Push-pull driving, Figure 1b			15	ns
I/O V_L Fall Time	t_{FVL}	Push-pull driving, Figure 1b			15	ns
Propagation Delay	$t_{PD-VL-VCC}$	Push-pull driving, driving I/O V_L			15	ns
	$t_{PD-VCC-VL}$	Push-pull driving, driving I/O V_{CC}			15	
Channel-to-Channel Skew	t_{SKEW}	Push-pull driving, each translator equally loaded			10	ns
Maximum Data Rate		Push-pull driving	16			Mbps

Note 2: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: For normal operation, ensure V_L < (V_{CC} + 0.3V). During power-up, V_L > (V_{CC} + 0.3V) does not damage the device.

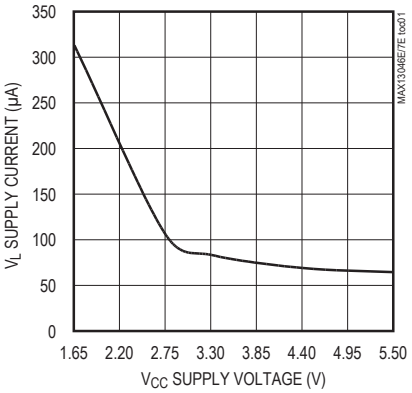
Note 4: ESD protection is guaranteed by design. To ensure maximum ESD protection, place a 1µF ceramic capacitor between V_{CC} and GND. See *Typical Application Circuits*.

Note 5: Timing is measured using 10% of input to 90% of output.

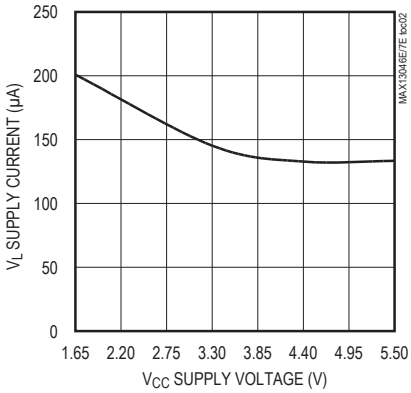
Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = +1.8V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

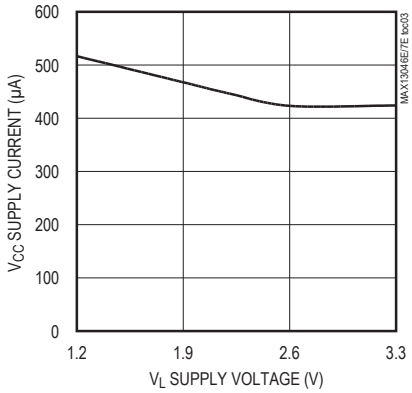
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE I/O V_L)



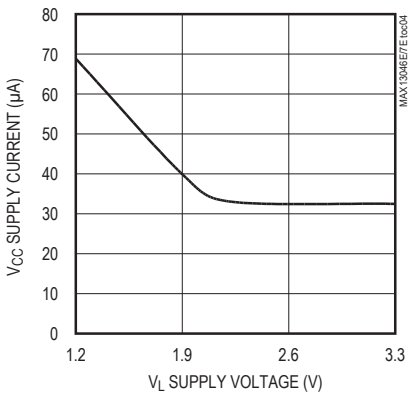
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE I/O V_{CC})



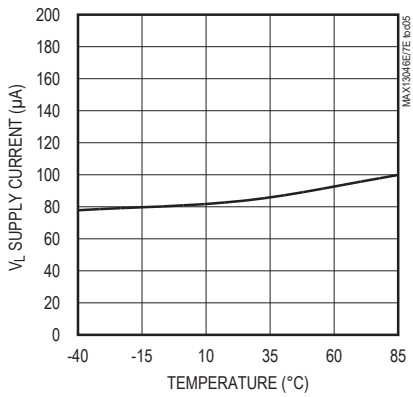
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE I/O V_L)



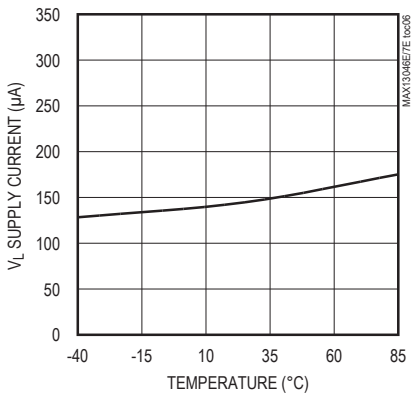
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE I/O V_{CC})



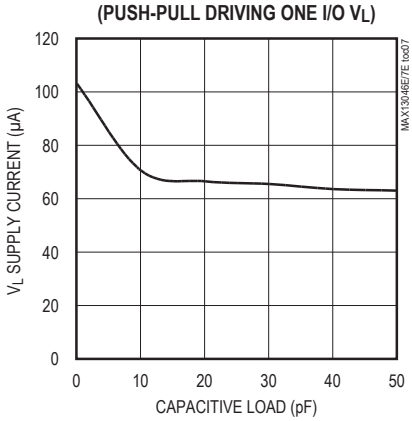
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL DRIVING ONE I/O V_L)



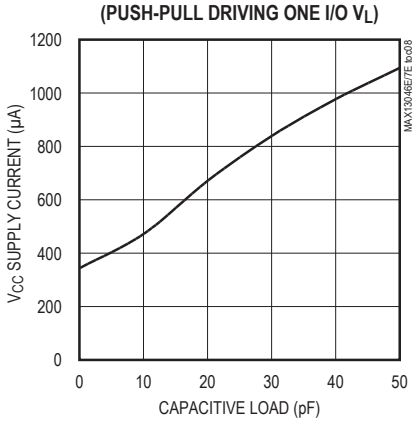
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL DRIVING ONE I/O V_{CC})



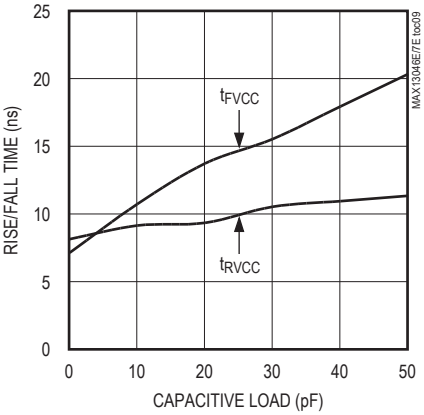
V_L DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_L)



V_{CC} DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_L)



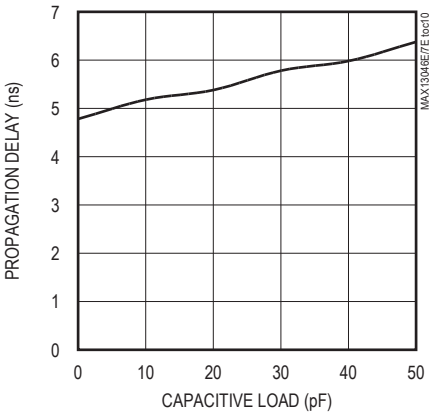
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_L)



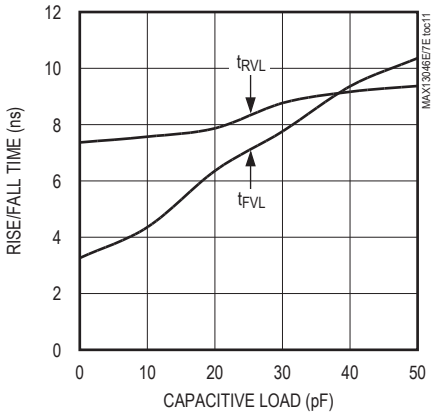
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, R_L = 1MΩ, C_L = 15pF, push-pull driving data rate = 8Mbps, T_A = +25°C, unless otherwise noted.)

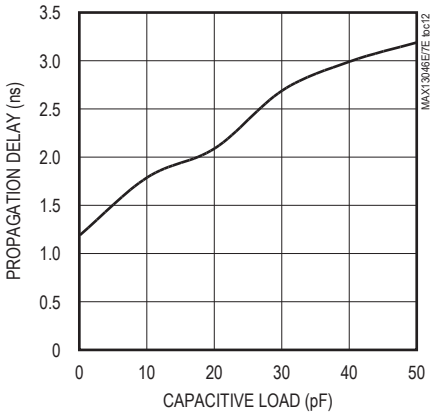
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_L)



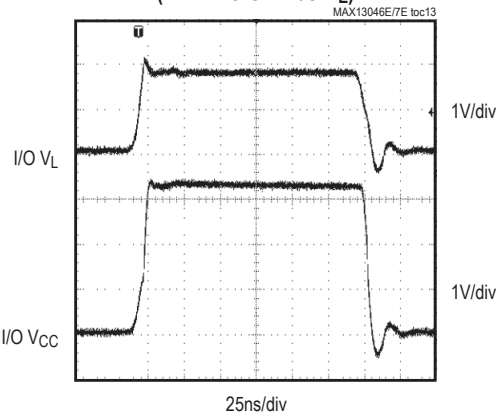
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_{CC})



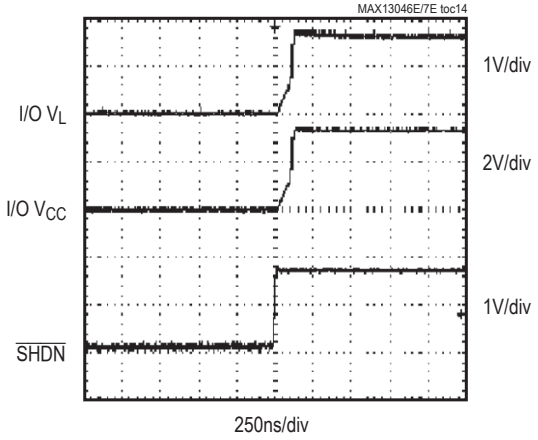
PROPAGATION DELAY vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE I/O V_{CC})



RAIL-TO-RAIL DRIVING (DRIVING ONE I/O V_L)



EXISTING SHUTDOWN MODE



MAX13046E Pin Description

MAX13046E		FUNCTION
µDFN	NAME	
1	V_L	V_L Input Supply Voltage. Bypass V_L with a 0.1µF ceramic capacitor located as close as possible to the input.
2	GND	Ground
3	I/O V_L	Input/Output. Referenced to V_L.
4	I/O V_{CC}	Input/Output. Referenced to V_{CC}.
5	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ high to enable the device. Drive $\overline{SHDN}$ low to put the device in shutdown mode.
6	V_{CC}	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.

MAX13047E Pin Description

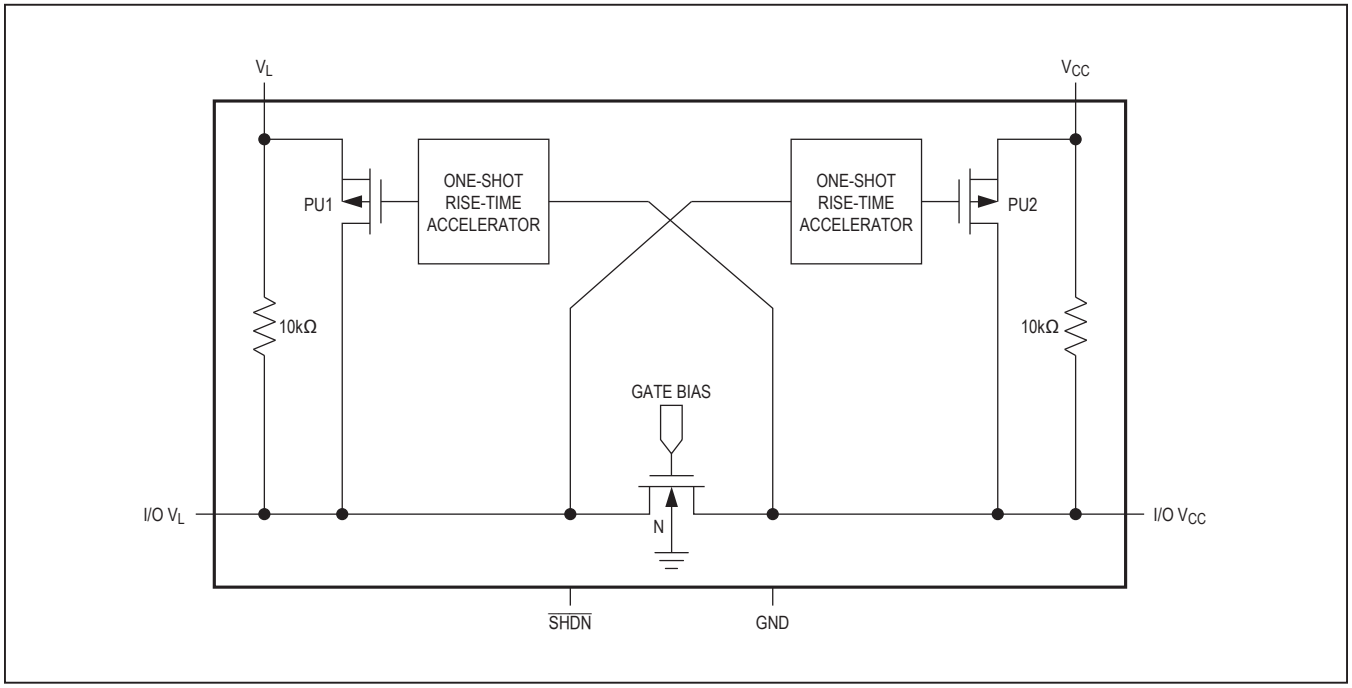
MAX13047E		FUNCTION
UTQFN	NAME	
1	I/O V_{L2}	Input/Output 2. Referenced to V_L.
2	V_L	V_L Input Supply Voltage. Bypass V_L with a 0.1µF ceramic capacitor located as close as possible to the input.
3, 7	N.C.	Not Connected. Internally not connected.
4	$\overline{SHDN}$	Enable Input. Drive $\overline{SHDN}$ high to enable the device. Drive $\overline{SHDN}$ low to put the device in shutdown mode.
5	I/O V_{CC2}	Input/Output 2. Referenced to V_{CC}.
6	V_{CC}	V_{CC} Input Supply Voltage. Bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the input for full ESD protection. If full ESD protection is not required, bypass V_{CC} with a 0.1µF ceramic capacitor.
8	I/O V_{CC1}	Input/Output 1. Referenced to V_{CC}.
9	GND	Ground
10	I/O V_{L1}	Input/Output 1. Referenced to V_L.

Detailed Description

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator and the MAX13047E is a dual-channel translator. Externally applied voltages, V_{CC} and V_L, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX13046E/MAX13047E accept V_L from +1.1V to the minimum of either +3.6V or (V_{CC} + 0.3V) and V_{CC} from +1.65V to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1µA thermal short-circuit protection, and ±15kV ESD protection on the V_{CC} side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when push-pull driving is used. See the *Functional Diagram*.

Functional Diagram



Level Translation

For proper operation, ensure that +1.65V ≤ V_{CC} ≤ +5.5V and +1.1V ≤ V_L ≤ the minimum of either +3.6V or (V_{CC} + 0.3V). During power-up sequencing, V_L ≥ (V_{CC} + 0.3V) does not damage the device. The speed of the rise time accelerator circuitry limits the maximum data rate for the MAX13046E/MAX13047E to 16Mbps.

Rise-Time Accelerators

The MAX13046E/MAX13047E have an internal rise-time accelerator, allowing operation up to 16Mbps. The rise-time accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To guarantee operation of the rise time accelerators the maximum parasitic capacitance should be less than 200pF on the I/O lines.

Shutdown Mode

Drive $\overline{SHDN}$ low to place the MAX13046E/MAX13047E in shutdown mode and drive $\overline{SHDN}$ high for normal operation. Activating the shutdown mode disconnects the internal 10kΩ pullup resistors on the I/O V_{CC} and I/O V_L lines. This forces the I/O lines to a high-impedance state, and decreases the supply current to less than 1µA. The high-impedance I/O lines in shutdown mode allow for use in a multidrop network. The MAX13046E/MAX13047E have a diode from each I/O to the corresponding supply rail and GND. Therefore, when in shutdown mode, do not allow the voltage at I/O V_L to exceed (V_L + 0.3V), or the voltage at I/O V_{CC} to exceed (V_{CC} + 0.3V).

Operation with One Supply Disconnected

Certain applications require sections of circuitry to be disconnected to save power. When V_L is connected and V_{CC} is disconnected or connected to ground, the device enters shutdown mode. In this mode, I/O V_L can still be driven without damage to the device; however, data does not translate from I/O V_L to I/O V_{CC}. If V_{CC} falls more than $V_{TH\_L\_VCC}$ below V_L, the device disconnects the pullup resistors at I/O V_L and I/O V_{CC}. To achieve the lowest possible supply current from V_L when V_{CC} is disconnected, it is recommended that the voltage at the V_{CC} supply input be approximately equal to GND.

When V_{CC} is connected and V_L is less than V_{TH_VL}, the device enters shutdown mode. In this mode, I/O V_{CC} can still be driven without damage to the device; however, data does not translate from I/O V_{CC} to I/O V_L.

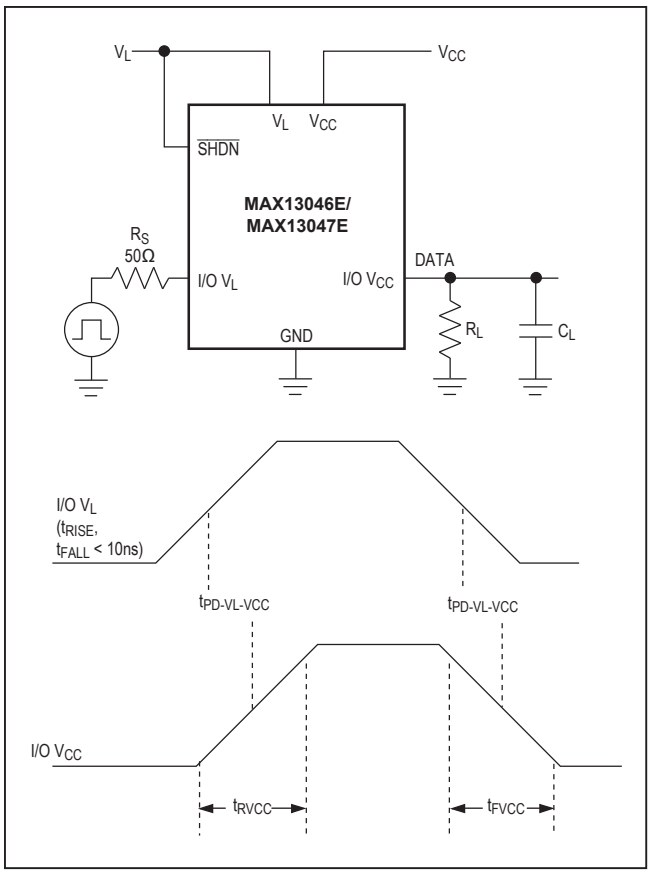


Figure 1a. Rail-to-Rail Driving I/O V_L

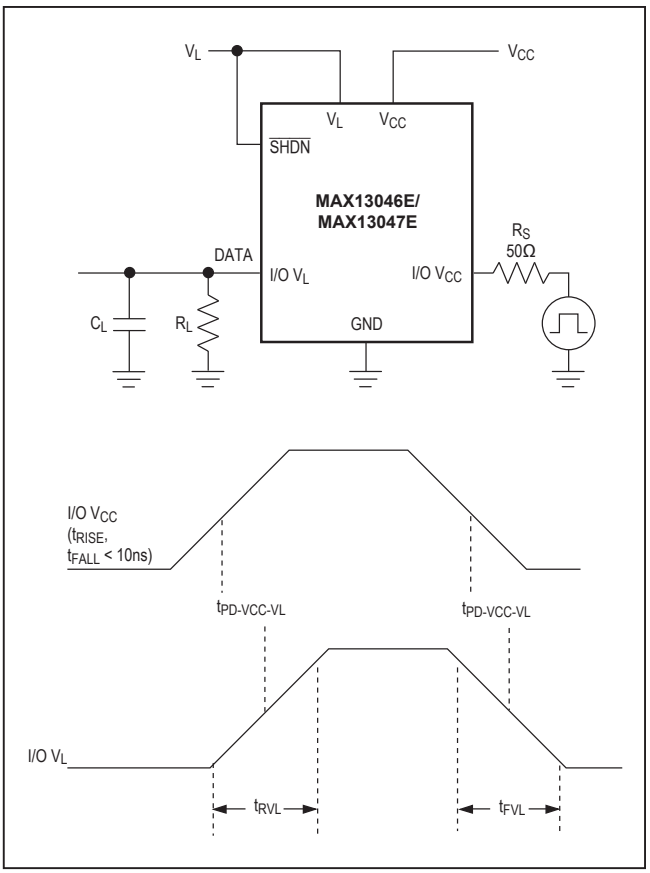


Figure 1b. Rail-to-Rail Driving I/O V_{CC}

When V_{CC} is disconnected or connected to ground, I/O V_{CC} must not be driven more than V_{CC} + 0.3V. When V_L is disconnected or connected to ground, I/O V_L must not be driven more than V_L + 0.3V.

Short-Circuit Protection

Thermal-overload detection protects the MAX13046E/MAX13047E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature (T_J) exceeds +150°C, the device enters shutdown mode. When the device has cooled to below +140°C, normal operation resumes.

±15kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The ESD structures withstand electrostatic discharge in all states: normal operation, shutdown mode, and powered down. The I/O V_{CC} lines of the MAX13046E/MAX13047E are characterized for protection to the following limit:

- ±15kV using the Human Body Model

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a 1.5kΩ resistor.

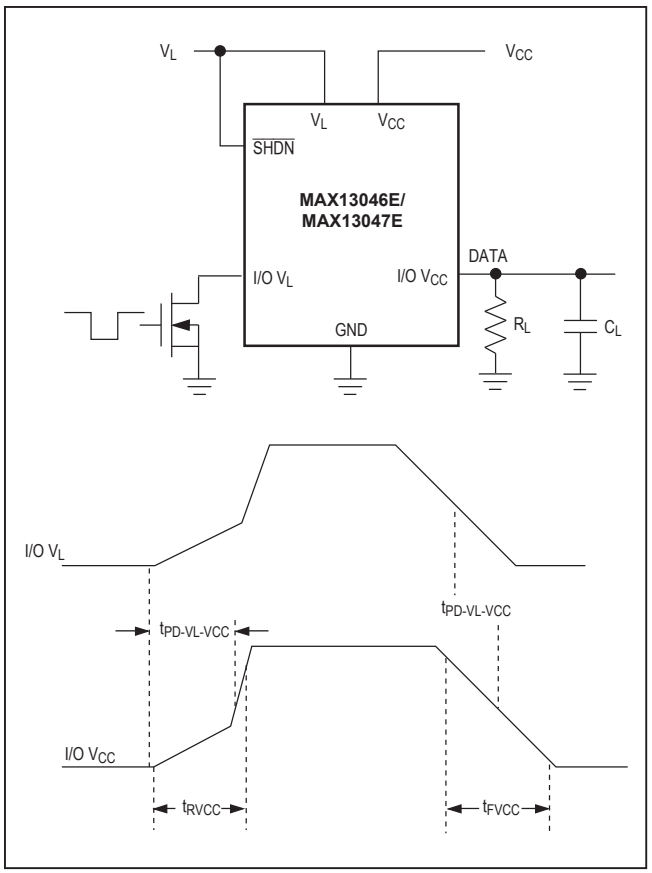


Figure 1c. Open-Drain Driving I/O V_L

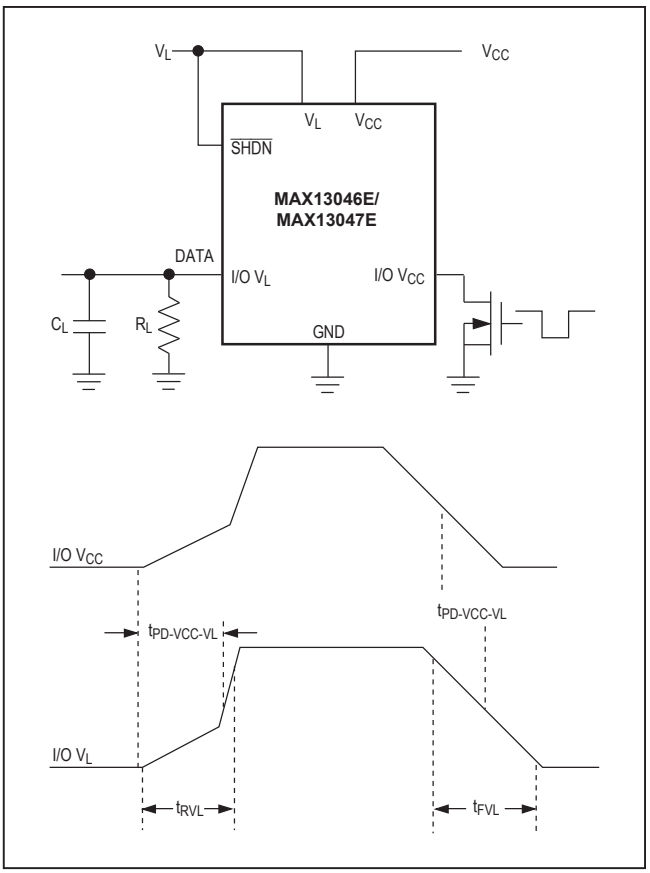


Figure 1d. Open-Drain Driving I/O V_{CC}

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX13046E/MAX13047E help to design equipment that meets Level 4 of IEC 61000-4-2 without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 can be lower than that measured using the Human Body Model. Figure 3a shows the IEC 61000-4-2 model, and Figure 3b shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD contact-discharge test. The Air-Gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1µF ceramic capacitor. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF ceramic capacitor. Place all capacitors as close as possible to the power-supply inputs.

I²C Level Translation

The MAX13046E/MAX13047E level shifts the data present on the I/O lines between +1.1V and +5.5V, making them ideal for level translation between a low-voltage ASIC and an I²C device. A typical application involves interfacing a low-voltage microprocessor to a +3V or +5V D/A converter, such as the MAX517.

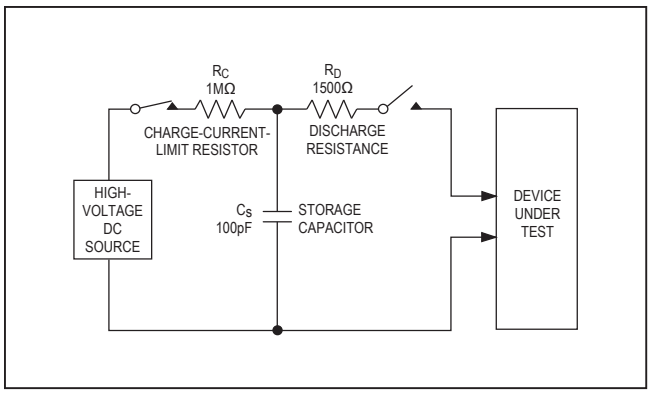


Figure 2a. Human Body ESD Test Model

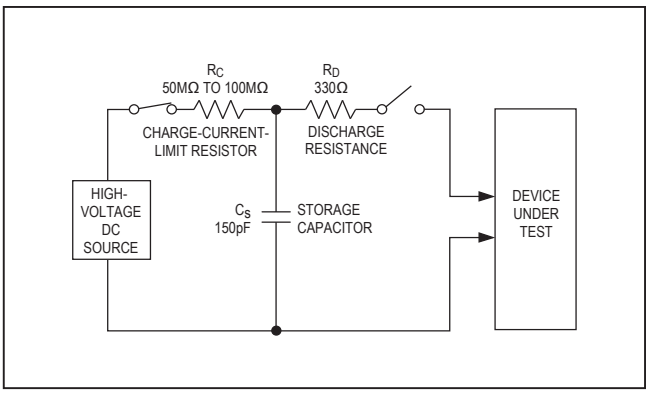


Figure 3a. IEC 61000-4-2 ESD Test Model

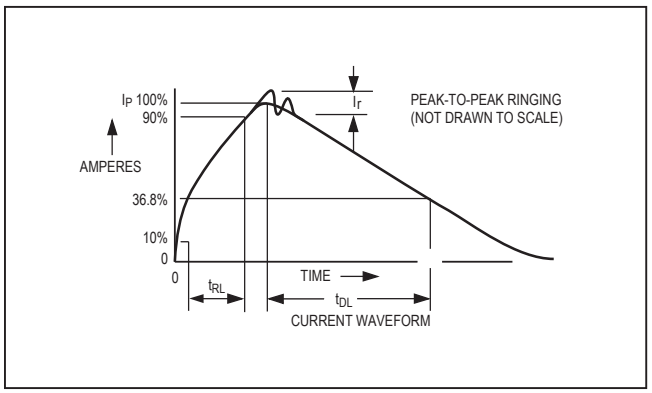


Figure 2b. Human Body Current Waveform

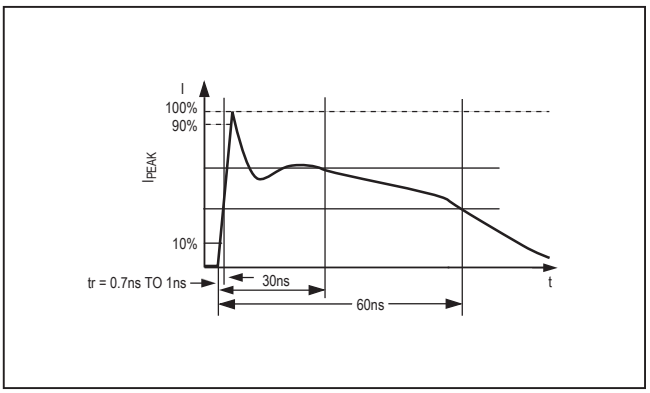


Figure 3b. IEC 61000-4-2 ESD Generator Current Waveform

1-Wire Interface Translation

The MAX13046E/MAX13047E are ideal for level translation between a low-voltage ASIC and 1-Wire device. A typical application involves interfacing a low-voltage microprocessor to an external memory, such as the DS2502. The maximum data rate depends on the 1-Wire device. For the DS2502, the maximum data rate is 16.3kbps. A 5kΩ pullup resistor is recommended when interfacing with the DS2502.

Push-Pull vs. Open-Drain Driving

The MAX13046E/MAX13047E can be driven in a pushpull or open-drain configurations. For open-drain configuration, internal 10kΩ resistors pull up I/O V_L and I/O V_{CC} to their respective power supplies. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers.

PCB Layout

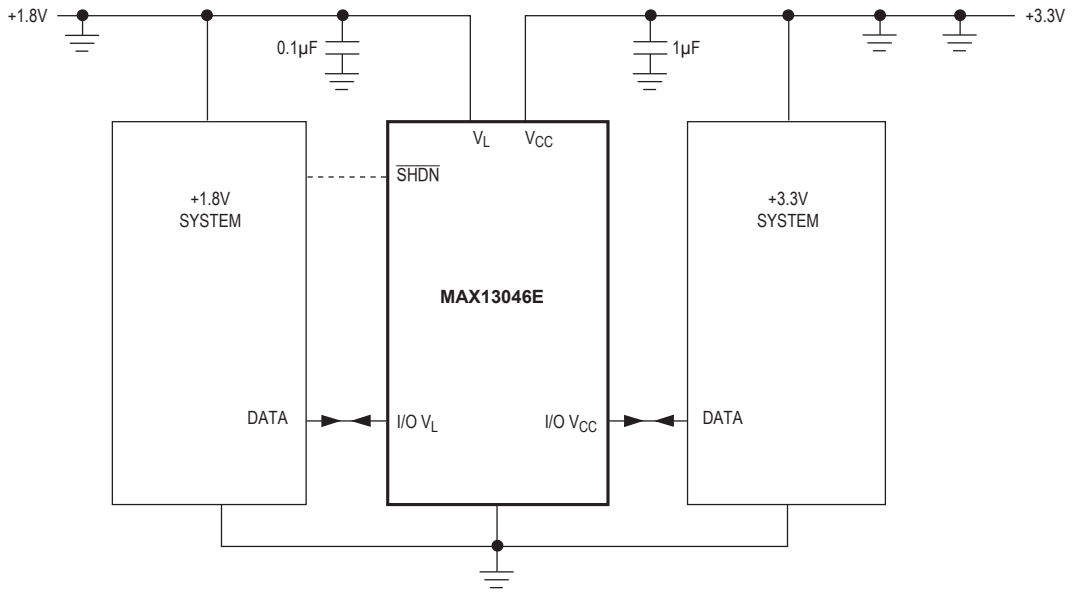
The MAX13046E/MAX13047E require good PCB layout for proper operation and optimal rise/fall time performance. Ensure proper high-frequency PCB layout even when operating at low data rates.

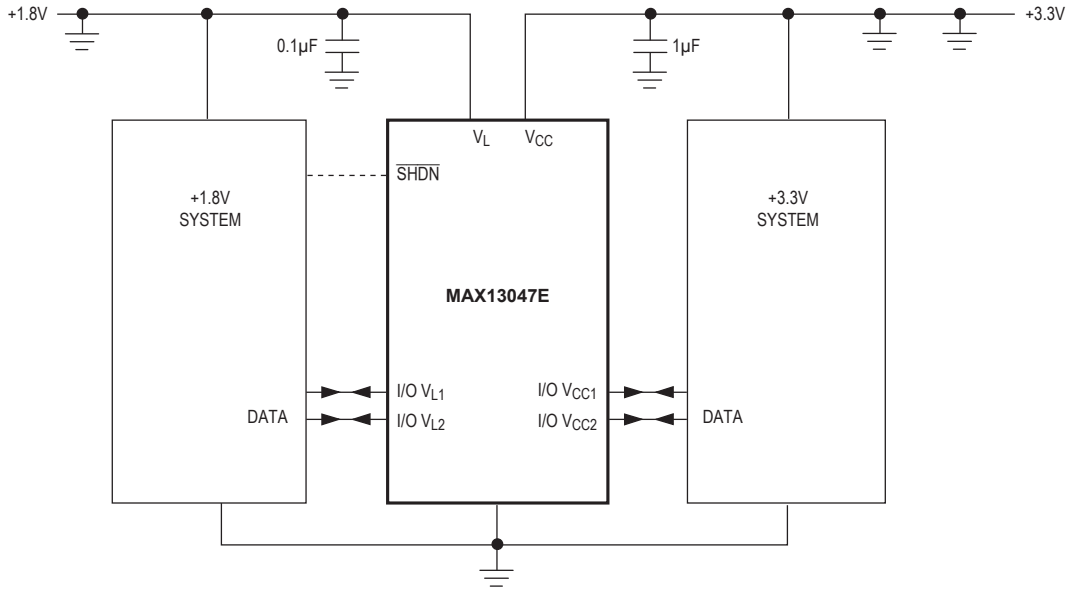
Driving High-Capacitive Load

Capacitive loading on the I/O lines impacts the rise time (and fall time) of the MAX13046E/MAX13047E when driving the signal lines. The actual rise time is a function of the load capacitance, parasitic capacitance, the supply voltage, and the drive impedance of the MAX13046E/MAX13047E.

Operating the MAX13046E/MAX13047E at a low data rate does **NOT** increase capacitive load driving capability.

Typical Application Circuits





Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO
6 µDFN	L611-1	**21-0147**
10 UTQFN	V101A1CN-1	**21-0028**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	8/08	Removing future product asterisks from MAX13047, changing *Electrical Characteristics* Table, packaging changes, changing ESD information	1–4, 6, 10
2	10/19	Updated *MAX13047E Pin Description* table	8
3	7/21	Updated *Pin Configurations*.	1