Allowable Operating Conditions at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage (VM pin)	VM		1.5 to 15.0	V
Power supply voltage (V_{CC} pin)	V_{CC}		2.8 to 5.5	V
Input signal voltage	V_{IN}		0 to V_{CC}	V
Input signal frequency	f max		200	kHz

Electrical Characteristics Ta = 25°C, V_{CC} = 3.0V, VM = VS = 6.0V, SGND = PGND = 0V, unless otherwise specified.

Parameter		Symbol	Conditions	Remarks	Ratings			Unit
					min	typ	max	
Standby load current drain		IMO	EN = 0V	1			1.0	µA
Standby control current drain		ICO	EN = IN1 = IN2 = IN3 = IN4 = 0V	2			1.0	µA
Standby load current drain2		IMO2	V_{CC} = 0V, VM = VS = 6V				1.0	µA
Operating control current drain		IC1	EN = 3V, with no load	3		0.85	1.2	mA
High-level input voltage		V_{IH}	2.7 ≤ V_{CC} ≤ 5.5V		0.6×V_{CC}		V_{CC}	V
Low-level input voltage		V_{IL}	2.7 ≤ V_{CC} ≤ 5.5V		0		0.2×V_{CC}	V
High-level input current (EN1, EN2, IN1, IN2, IN3, IN4)		$I_{IH}1$	V_{IN} = 3V	4		15	25	µA
Low-level input current (EN1, EN2, IN1, IN2, IN3, IN4)		$I_{IL}1$	V_{IN} = 0V	4	-1.0			µA
Pull-down resistance value		RDN	EN1, EN2, IN1, IN2, IN3, IN4		100	200	400	kΩ
Charge pump voltage		VG	V_{CC} + VS		8.5	9.0	9.5	V
Output ON resistance 1		RON1	Sum of top and bottom sides ON resistance.	5		0.75	1.2	Ω
Output ON resistance 2		RON2	Sum of top and bottom sides ON resistance. V_{CC} = 2.8V	5		1.0	1.5	Ω
Low-voltage detection voltage		VCS	V_{CC} pin voltage is monitored	6	2.15	2.30	2.45	V
Thermal shutdown temperature		Tth	Design guarantee value *	7	150	180	210	°C
Output block	Turn-on time	TPLH		8		0.2	0.4	µS
	Turn-off time	TPHL		8		0.2	0.4	µS

* : Design guarantee value and no measurement is preformed.

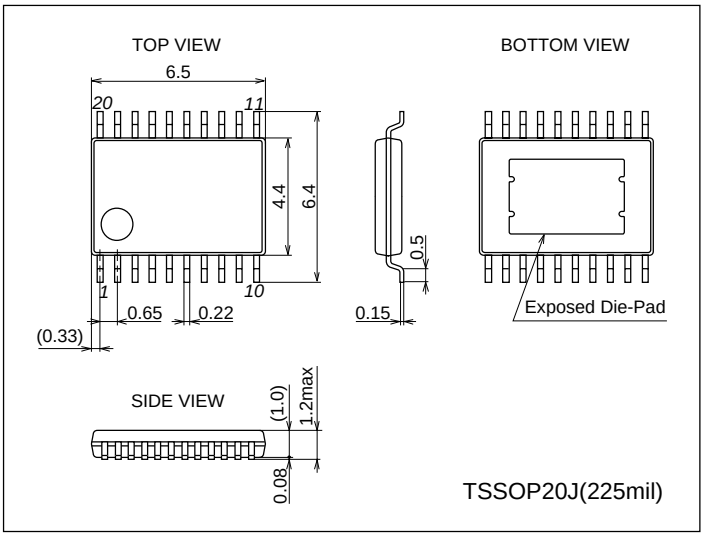
Remarks

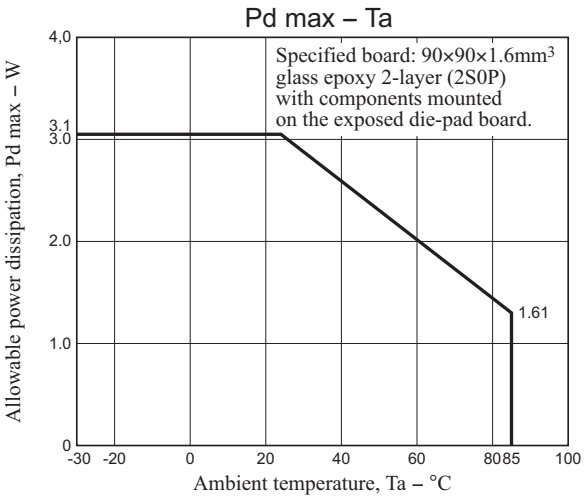
1. Current consumption when output at the VM pin is off.
2. Current consumption when the V_{CC} pin when in standby mode.
3. Current consumption at the V_{CC} pin when EN is 3V (standby mode).
4. Pins EN1, 2, IN1, 2, 3, and 4 are all pulled down.
5. Sum of upper and lower saturation voltages of OUT pin divided by the current.
6. All power transistors are turned off if a low V_{CC} condition is detected.
7. All output transistors are turned off if the thermal protection circuit is activated. They are turned on again as the temperature goes down.
8. Rising time from 10 to 90% and falling time from 90 to 10% are specified.

Package Dimensions

unit : mm (typ)

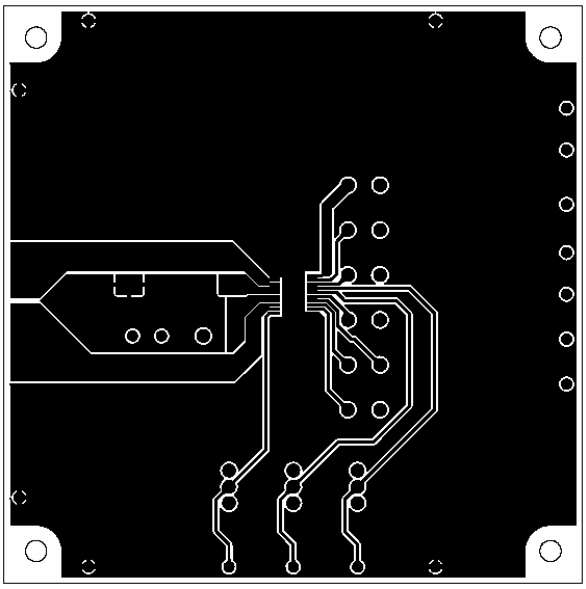
3279



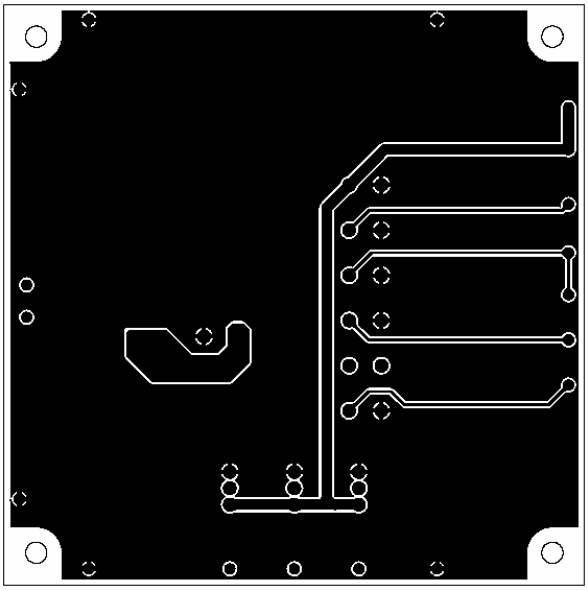


Substrate Specifications

Size : 90mm × 90mm × 1.6mm (2-layer substrate [2S0P])
Material : Glass epoxy
Copper wiring density : L1 = 95% / L2 = 95%



L1 : Copper wiring pattern diagram



L2 : Copper wiring pattern diagram

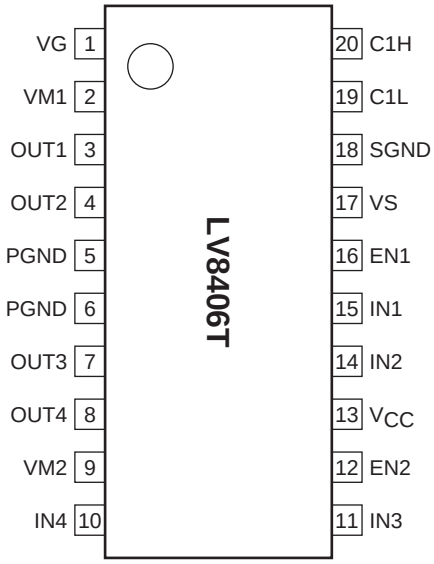
Cautions

1) The data for the case with the Exposed Die-Pad substrate mounted shows the values when 90% or more of the Exposed Die-Pad is wet.

2) For the set design, employ the derating design with sufficient margin.
Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension. Accordingly, the design must ensure these stresses to be as low or small as possible.
The guideline for ordinary derating is shown below :
(1)Maximum value 80% or less for the voltage rating
(2)Maximum value 80% or less for the current rating
(3)Maximum value 80% or less for the temperature rating

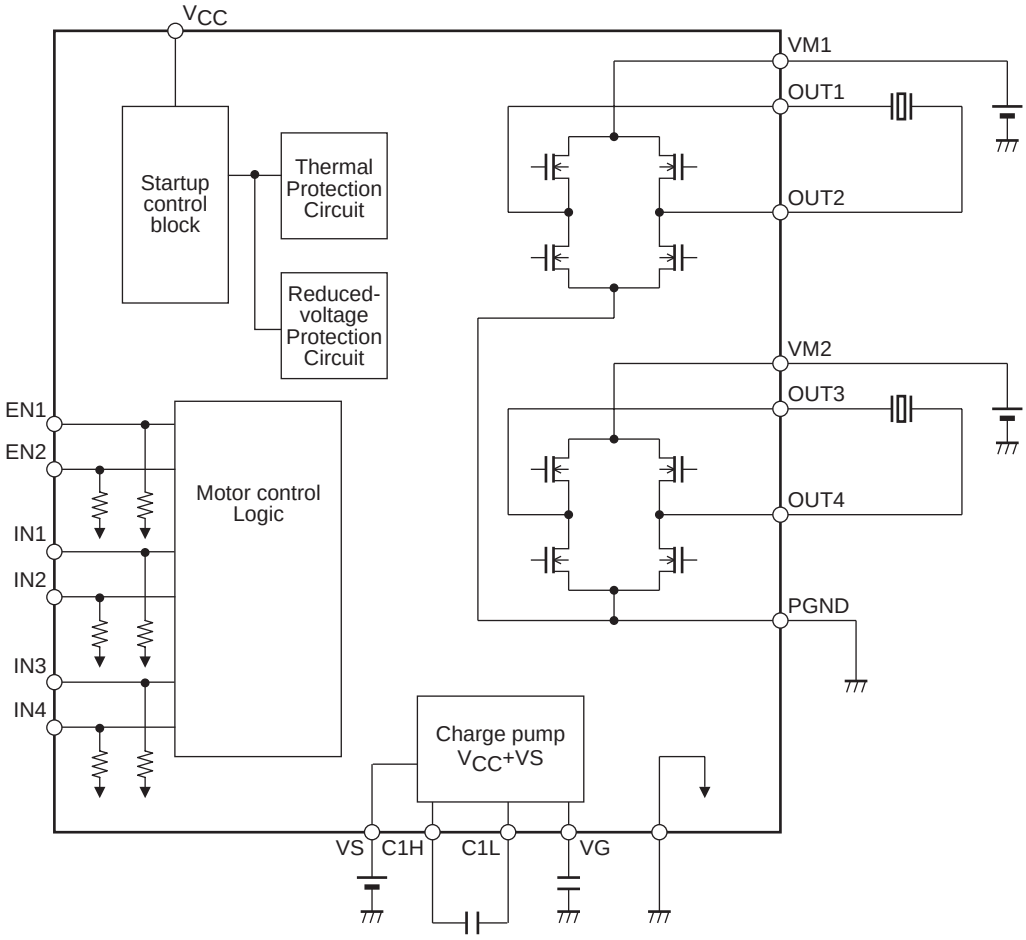
3) After the set design, be sure to verify the design with the actual product.
Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc.
Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Pin Assignment



Top view

Block Diagram



* Connect a kickback absorption capacitor as near as possible to the IC. Coil kickback may cause increase in VM line voltage, and a voltage exceeding the maximum rating may be applied momentarily to the IC, which results in deterioration or damage of the IC

* The pin VS is a terminal that supplies a source power supply of the charge pump circuit.
The charge pump voltage, VG = VS + V_{CC} is generated.
Apply the high voltage of VM1 or VM2.

Truth Table

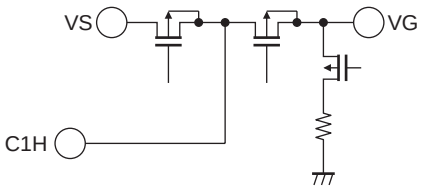
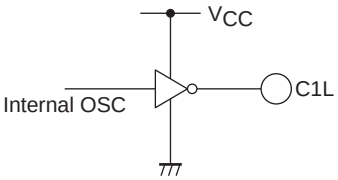
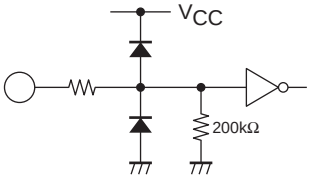
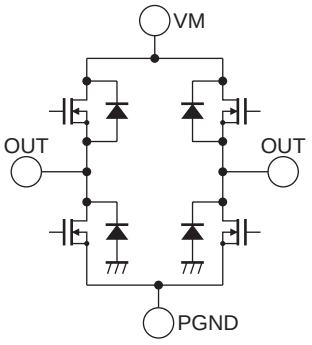
EN1 (EN2)	IN1 (IN3)	IN2 (IN4)	OUT1 (OUT3)	OUT2 (OUT4)	Charge pump	Mode
H	H	H	L	L	ON	Brake
	H	L	H	L		Forward
	L	H	L	H		Reverse
	L	L	Z	Z		Standby
L	-	-	Z	Z	OFF	All function stop

- : denotes a don't care value. Z : High-impedance

• In standby mode, consumption current serves as zero..

* All power transistors turn off and the motor stops driving when the IC is detected in low voltage or thermal protection mode.

Pin Functions

Pin No.	Pin name	Description	Equivalent circuit
20 1 17	C1H VG VS	Step-up capacitor connection pin. Charge pump source voltage supply pin.	
19	C1L	Step-up capacitor connection pin.	
16 12 15 14 11 10	EN1 EN2 IN1 IN2 IN3 IN4	Logic enable pin. (Pull-down resistor incorporated) Driver output switching.	
3 4 7 8	OUT1 OUT2 OUT3 OUT4	Driver output.	
2 9	VM1 VM2	Motor block power supply.	
13	V_{CC}	Logic block power supply.	
18	SGND	Control block ground.	
5 6	PGND PGND	Driver block ground.	