

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Conditions	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		36	V
Peak supply voltage	V _{CC} peak	See below for the waveform applied.	50	V
Allowable Power dissipation	Pd max	Independent IC	1.5	W
		AI heat sink *	5.6	W
		With an infinity heat sink	32.5	W
Junction temperature	Tj max		150	°C
Operating ambient temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* : When the Aluminum heat sink (50mm × 50mm × 1.5mm) is used

Allowable Operating range at Ta = 25°C

Parameter	Conditions	Ratings	Unit
Operating supply voltage 1	V _{DD} output, SW output, ACC output	7.5 to 16	V
Operating supply voltage 2	ILM output at 10V	12 to 16	V
	ILM output at 8V	10 to 16	V
Operating supply voltage 3	Audio output at 9V	10 to 16	V
Operating supply voltage 4	CD output (CD output current = 1.3A)	10.5 to 16	V
	CD output (CD output current ≤ 1A)	10 to 16	V

Electrical Characteristics at V_{CC} = 14.4V, Ta = 25°C(*6)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I _{CC}	V _{DD} no load, CTRL1/2 = $\lceil L/L \rceil$, ACC = 0V		400	800	μA
CTRL1 Input						
Low input voltage	V _{IL1}		0		0.5	V
M1 input voltage	V _{IM1}		0.8	1.1	1.4	V
M2 input voltage	V _{IM2}		1.9	2.2	2.5	V
High input voltage	V _{IH1}		2.9	3.3	5.5	V
Input impedance	R _{IH1}		350	500	650	kΩ
CTRL2 Input						
Low input voltage	V _{IL2}		0		0.5	V
M input voltage	V _{IM2}		1.1	1.65	2.1	V
High input voltage	V _{IH2}		2.5	3.3	5.5	V
Input impedance	R _{IH2}		350	500	650	kΩ
V_{DD} 5V Output *1 The V_{DD} 5V output supplies the output currents of SW 5V and ACC 5V.						
Output voltage 1	V _{O1}	I _{O1} = 200mA, I _{O7} , I _{O8} = 0A	4.75	5.0	5.25	V
Output voltage 2	V _{O1'}	I _{O1} = 200mA, I _{O7} = 200mA, I _{O8} = 100mA	4.75	5.0	5.25	V
Output total current	I _{to1}	V _{O1} ≥ 4.75V, I _{to1} = I _{O1} + I _{O7} + I _{O8}	500			mA
Line regulation	ΔV _{OLN1}	7.5V < V _{CC} < 16V, I _{O1} = 200mA *2		30	90	mV
Load regulation	ΔV _{OLD1}	1mA < I _{O1} < 200mA *2		70	150	mV
Dropout voltage 1	V _{DROP1}	I _{O1} = 200mA *2		1.0	1.5	V
Dropout voltage 2	V _{DROP1'}	I _{O1} = 100mA *2		0.7	1.05	V
Dropout voltage 3	V _{DROP1''}	I _{O1} + I _{O7} + I _{O8} = 500mA		2.5	3.75	V
Ripple rejection	R _{REJ1}	f = 120Hz, I _{O1} = 200mA *2	40	50		dB
CD Output ; CTRL2 = $\lceil H \rceil$						
Output voltage	V _{O2}	I _{O2} = 1000mA	7.6	8.0	8.4	V
Output current	I _{O2}	V _{O2} ≥ 7.6V	1300			mA
Line regulation	ΔV _{OLN2}	10.5V < V _{CC} < 16V, I _{O2} = 1000mA		50	100	mV

*1 : The V_{DD} 5V output also supplies the output currents of SW 5V and ACC 5V. Therefore, the current supply capability of the V_{DD} 5V output and its other electrical characteristics are affected by the output statuses of SW 5V and ACC 5V.

*2 : SW 5V and ACC 5V are not subject to a load.

Continued on next page.

LV5680P

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Load regulation	ΔV_{OLD2}	$10mA < I_{O2} < 1000mA$		100	200	mV
Dropout voltage 1	V_{DROP2}	$I_{O2} = 1000mA$		1.0	1.5	V
Dropout voltage 2	$V_{DROP2'}$	$I_{O2} = 500mA$		0.5	0.75	V
Ripple rejection	R_{REJ2}	$f = 120Hz, I_{O2} = 1000mA$	40	50		dB
AUDIO (8-9V) Output ; CTRL2 = [M]						
AUDIO_F pin voltage	V_{I3}		1.222	1.260	1.298	V
AUDIO_F pin inflow current	I_{IN3}		-1		1	μA
AUDIO output voltage 1	V_{O3}	$I_{O3} = 200mA, R2 = 30k\Omega, R3 = 5.6k\Omega *3$	7.65	8.0	8.35	V
AUDIO output voltage 2	$V_{O3'}$	$I_{O3} = 200mA, R2 = 27k\Omega, R3 = 4.7k\Omega *3$	8.13	8.5	8.87	V
AUDIO output voltage 3	$V_{O3''}$	$I_{O3} = 200mA, R2 = 24k\Omega, R3 = 3.9k\Omega *3$	8.6	9.0	9.4	V
AUDIO output current	I_{O3}		300			mA
Line regulation	ΔV_{OLN3}	$10V < V_{CC} < 16V, I_{O3} = 200mA$		30	90	mV
Load regulation	ΔV_{OLD3}	$1mA < I_{O3} < 200mA$		70	150	mV
Dropout voltage 1	V_{DROP3}	$I_{O3} = 200mA$		0.3	0.45	V
Dropout voltage 2	$V_{DROP3'}$	$I_{O3} = 100mA$		0.15	0.23	V
Ripple rejection	R_{REJ3}	$f = 120Hz, I_{O3} = 200mA$	40	50		dB
ILM (8-12V) Output ; CTRL1 = [M1]						
ILM_F pin voltage	V_{I4}		1.222	1.260	1.298	V
ILM output voltage 1	V_{O4}	$I_{O4} = 200mA$	11.4	12.0	12.6	V
ILM output voltage 2	$V_{O4'}$	$I_{O4} = 200mA, R1 = 270k\Omega *4$	8.5	10.0	11.5	V
ILM output voltage 3	$V_{O4''}$	$I_{O4} = 200mA, R1 = 100k\Omega *4$	6.8	8.0	9.2	V
ILM output current	I_{O4}	$R1 = 270k\Omega$	300			mA
Line regulation	ΔV_{OLN4}	$12V < V_{CC} < 16V, I_{O4} = 200mA, R1 = 270k\Omega$		30	90	mV
Load regulation	ΔV_{OLD4}	$1mA < I_{O4} < 200mA$		70	150	mV
Dropout voltage 1	V_{DROP4}	$I_{O4} = 200mA$		0.7	1.05	V
Dropout voltage 2	$V_{DROP4'}$	$I_{O4} = 100mA$		0.35	0.53	V
Ripple rejection	R_{REJ4}	$f = 120Hz, I_{O4} = 200mA$	40	50		dB
Remoto (EXT) ; CTRL1 = [M2]						
Output voltage	V_{O5}	$I_{O5} = 350mA$	$V_{CC}-1.0$	$V_{CC}-0.5$		V
Output current	I_{O5}	$V_{O5} \geq V_{CC}-1.0$	350			mA
ANT remoto ; CTRL1 = [H]						
Output voltage	V_{O6}	$I_{O6} = 300mA$	$V_{CC}-1.0$	$V_{CC}-0.5$		V
Output current	I_{O6}	$V_{O6} \geq V_{CC}-1.0$	300			mA
SW 5V Output ; CTRL2 = [M]						
Output voltage 1	V_{O7}	$I_{O7} = 1mA, I_{O1}, I_{O8} = 0A *5$	$V_{O1}-0.25$	V_{O1}		V
Output voltage 2	$V_{O7'}$	$I_{O7} = 200mA, I_{O1}, I_{O8} = 0A *5$	$V_{O1}-0.45$	$V_{O1}-0.2$		V
Output current	I_{O7}	$V_{O7} \geq 4.55$	200			mA
ACC Detection ; ACC Integration 5V output						
ACC detection voltage	V_{TH8}		2.8	3.0	3.2	V
Hysteresis width	V_{HIS8}		0.2	0.3	0.4	V
Input impedance	Z_{I8}	(Pull-down resistance internal)	42	60	78	$k\Omega$
ACC output voltage 1	V_{O8}	$I_{O8} = 0.5mA, I_{O1}, I_{O7} = 0A *5$	$V_{O1}-0.25$	V_{O1}		V
ACC output voltage 2	$V_{O8'}$	$I_{O8} = 100mA, I_{O1}, I_{O7} = 0A *5$	$V_{O1}-0.45$	$V_{O1}-0.2$		V
ACC output voltage	I_{O8}	$V_{O8} \geq 4.55$	100			mA

*3 : When a component with a resistance accuracy of $\pm 1\%$ is used

<Reference> When a component with a resistance accuracy of $\pm 0.5\%$ is used, $V_{O3''}$ is $8.67V \leq 9.0V \leq 9.33V$.

*4 : When a component with a resistance accuracy of $\pm 1\%$ is used

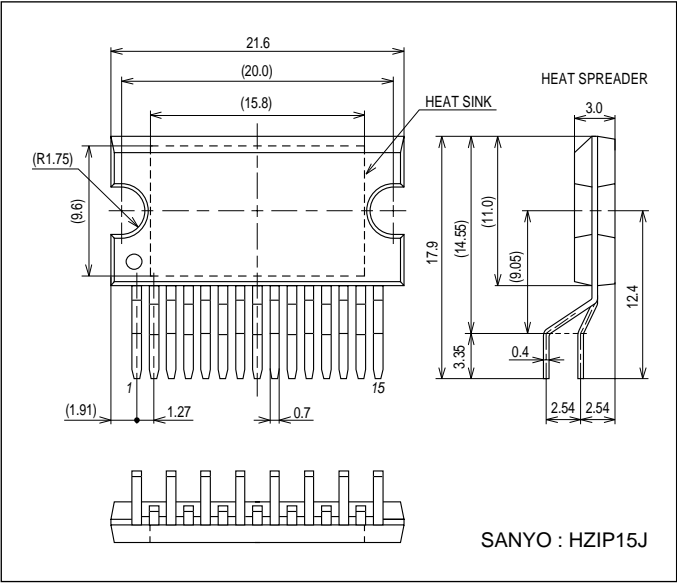
The absolute accuracy of the internal resistance is $\pm 15\%$.

*5 : Since the SW 5V and ACC 5V are output from V_{DD} 5V through the SW, the voltage drops by an amount equivalent to the ON resistance of the SW.

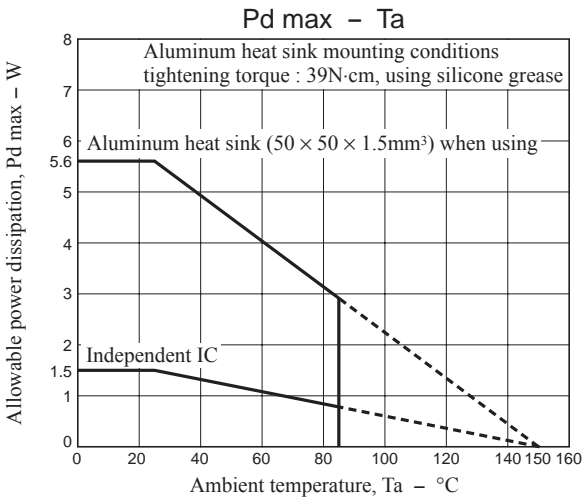
*6: The entire specification has been defined based on the tests performed under the conditions where T_j and T_a ($=25^\circ C$) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (T_j).

Package Dimensions

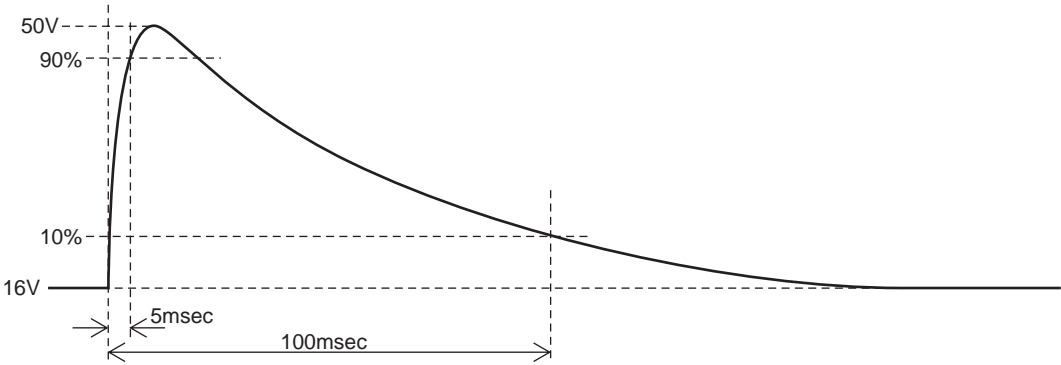
unit : mm (typ)
3395



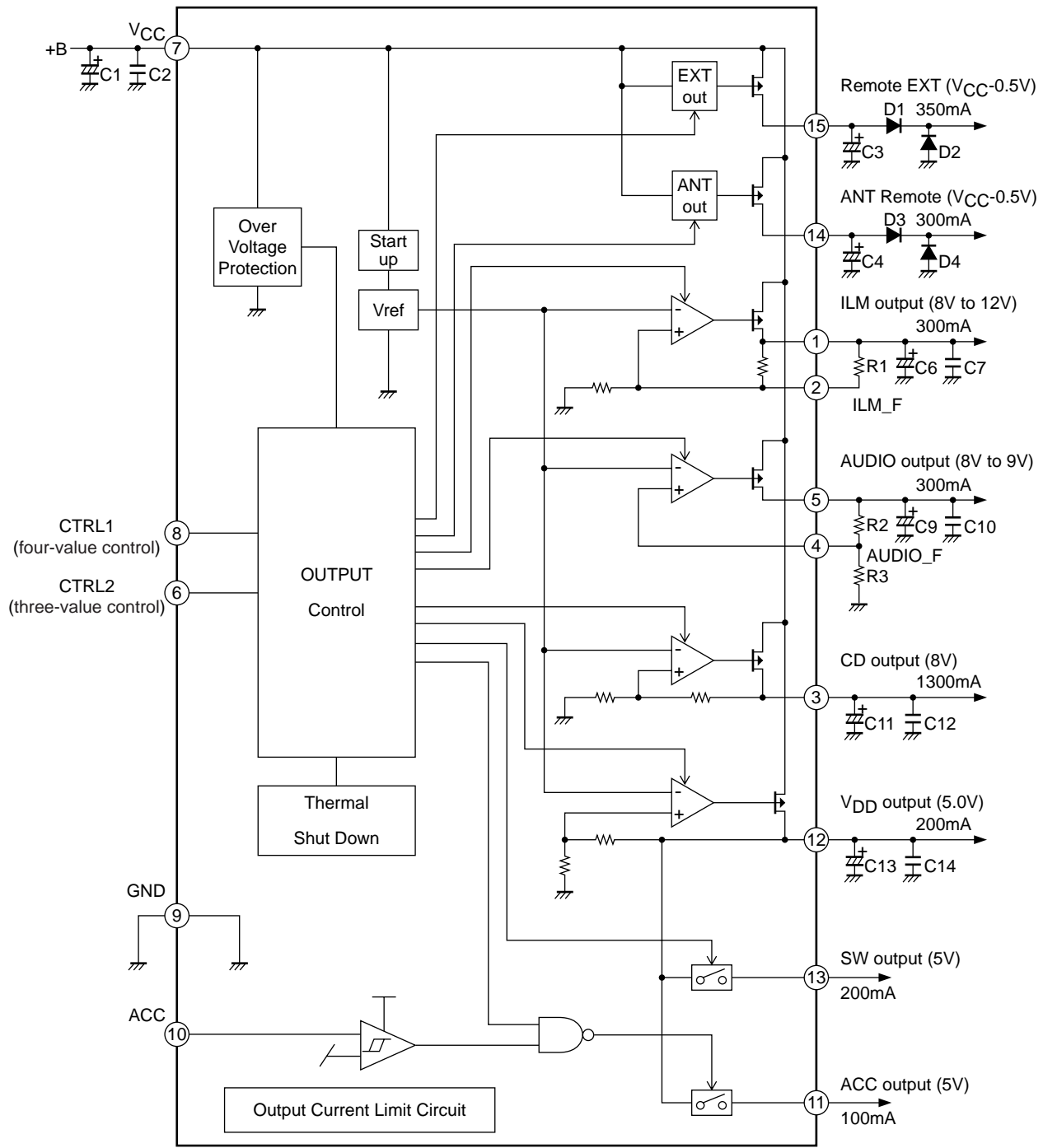
• Allowable power dissipation derating curve



• Waveform applied during surge test



Block Diagram



Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL1 = M1, M2, H 12.0V/300mA	<p>The equivalent circuit diagram shows the internal structure for pins 1, 2, and 9. It includes a VCC input at pin 7, a GND connection at pin 9, and a network of resistors (59.67kΩ, 7kΩ) and capacitors connected to pins 1 and 2. The circuit also shows the internal transistors and diodes that form the output drivers for these pins.</p>
2	ILM_F	ILM output voltage adjustment pin	

Continued on next page.

LV5680P

Continued from preceding page.

Pin No.	Pin name	Description	Equivalent Circuit
3	CD	CD output pin ON when CTRL2 = M, H 8.0V/1.3A	
4	AUDIO_F	AUIDO output voltage adjustment pin	
5	AUDIO	AUDIO output pin ON when CTRL2 = M, H	
6	CTRL2	CTRL2 input pin three-value input	
7	VCC	Supply terminal	
8	CTRL1	CTRL1 input pin four-value input	
9	GND	GND pin	

Continued on next page.

LV5680P

Continued from preceding page.

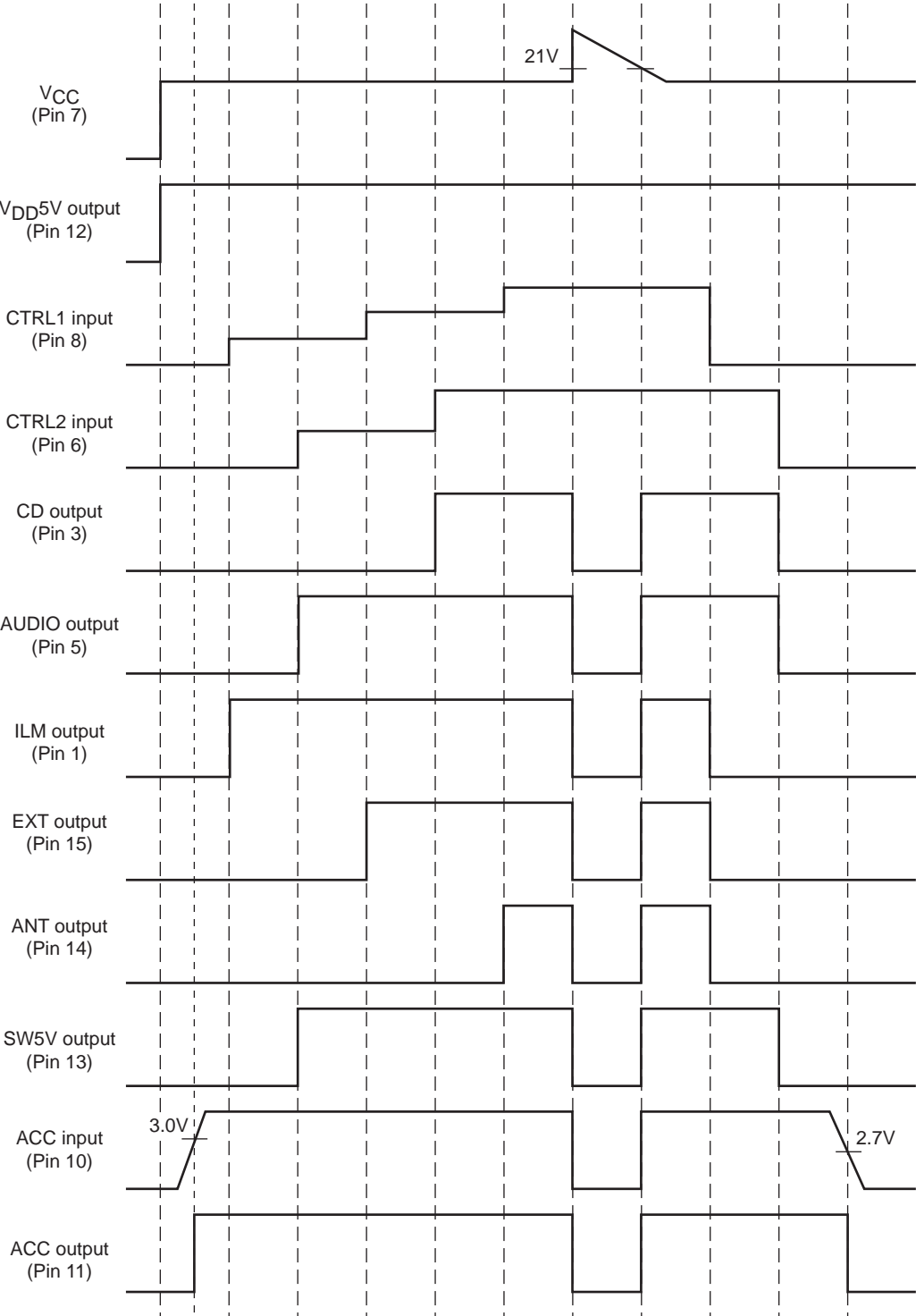
Pin No.	Pin name	Description	Equivalent Circuit
10	ACC	Accessory input	
11	ACC5V	Accessory detection output ON when ACC > 3V	
12	V _{DD} 5V	V _{DD} 5V output pin 5.0V/200mA	
13	SW5V	SW5V output pin ON when CTRL2 = M, H	
14	ANT	ANT output pin ON when CTRL1 = H V _{CC} -0.5V/300mA	
15	EXT	EXT output pin ON when CTRL1 = M2, H V _{CC} -0.5V/350mA	

LV5680P

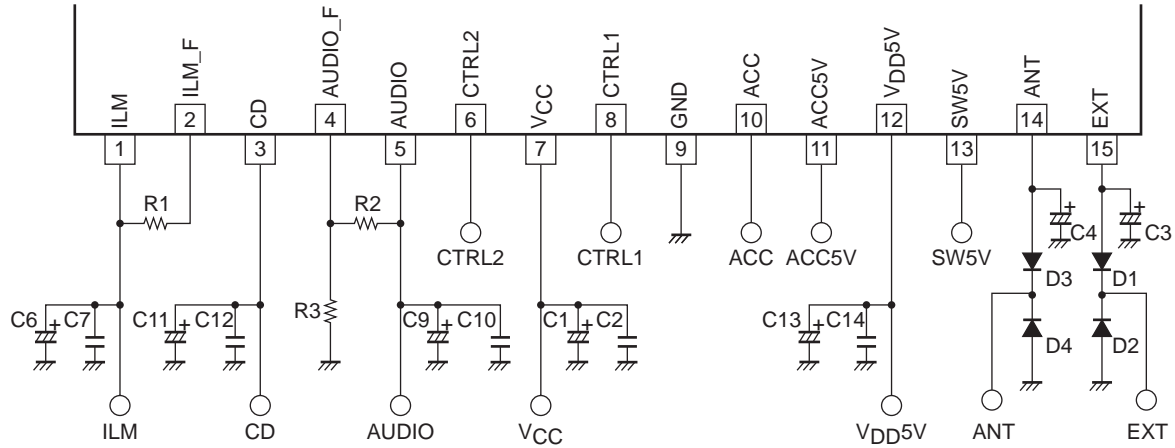
CTRL Pin Output Truth Table

CTRL1	ANT	EXT	ILM	CTRL2	CD	AUDIO	SW5
L	OFF	OFF	OFF	L	OFF	OFF	OFF
M1	OFF	OFF	ON	M	OFF	ON	ON
M2	OFF	ON	ON	H	ON	ON	ON
H	ON	ON	ON				

Timing Chart



Recommended Operation Circuit



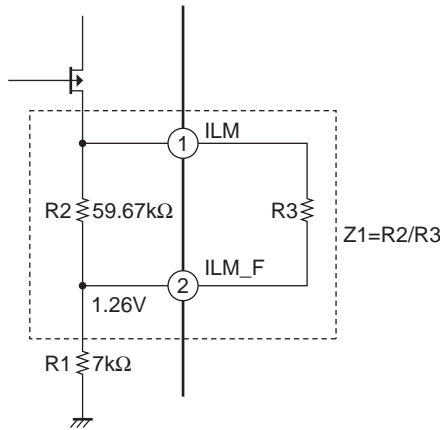
Peripheral parts list

Name of part	Description	Recommended value	Remarks
C1	Power supply bypass capacitor	100 μ F or more	These capacitors must be placed near the V _{CC} and GND pins.
C2	Oscillation prevention capacitor	0.22 μ F or more	
C3	EXT output stabilization capacitor	2.2 μ F or more	
C4	ANT output stabilization capacitor	2.2 μ F or more	
C6, C9, C11, C13	Output stabilization capacitor	4.7 μ F or more	Electrolytic capacitor *
C7, C10, C12, C14	Output stabilization capacitor	0.22 μ F or more	Ceramic capacitor *
R1	Resistor for ILM voltage adjustment	ILM output voltage R1:without = 12.0V :270k Ω = 10.0V :100k Ω = 8.0V	A resistor with resistance accuracy as low as less than $\pm 1\%$ must be used.
R2, R3	Resistor for AUDIO voltage setting	AUDIO output voltage R2/R3:30k Ω /5.6k Ω = 8.0V :27k Ω /4.7k Ω = 8.5V :24k Ω /3.9k Ω = 9.0V	A resistor with resistance accuracy as low as less than $\pm 1\%$ must be used.
D1, D2, D3, D4	Diode for internal device breakdown protection		

* : In order to stabilize the regulator outputs, it is recommended that the electrolytic capacitor and ceramic capacitor be connected in parallel.

Furthermore, the values listed above do not guarantee stabilization during the overcurrent protection operations of the regulator, so oscillation may occur during an overcurrent protection operation.

• ILM output voltage setting method



The ILM_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for ILM voltage calculation

$$Z_1 = R_2 // R_3 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

$$ILM = \frac{1.26[V]}{R_1} \times Z_1 + 1.26[V]$$

$$Z_1 = \frac{(ILM - 1.26) \cdot R_1}{1.26} \quad R_3 = \frac{R_2 \cdot Z_1}{R_2 - Z_1}$$

Example : ILM = 9V setting method

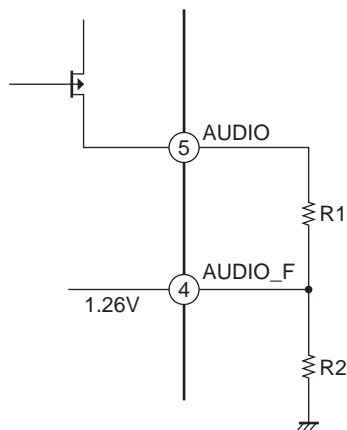
$$Z_1 = \frac{(9V - 1.26V) \cdot 7k\Omega}{1.26V} \cong 43k\Omega$$

When R3 = 150k, the ILM output voltage will be as follows:

$$Z_1' = \frac{59.67k\Omega \cdot 150k\Omega}{59.67k\Omega + 150k\Omega} \cong 42.69k\Omega$$

$$ILM = \frac{1.26V}{7k\Omega} \times 42.69k\Omega + 1.26V \cong 8.94V$$

• AUDIO output voltage setting method



The AUDIO_F voltage is determined by the internal band gap voltage of the IC (typ = 1.26V).

Formula for AUDIO voltage calculation

$$AUDIO = \frac{1.26[V]}{R_2} \times R_1 + 1.26[V]$$

$$\frac{R_1}{R_2} = \frac{(AUDIO - 1.26)}{1.26}$$

The circuit must be designed in such a way that the R1:R2 ratio satisfies the formula given above for the AUDIO voltage that has been set.

Example : AUDIO = 8.5V setting method

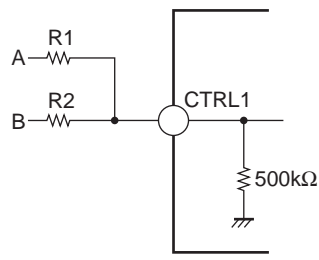
$$\frac{R_1}{R_2} = \frac{(8.5 - 1.26)}{1.26} \cong 5.75$$

$$\frac{R_1}{R_2} = \frac{27k\Omega}{4.7k\Omega} \cong 5.74$$

$$AUDIO = 1.26V \times 5.74 + 1.26V \cong 8.49V$$

Note : In the above, the typical values are given in all instances for the values used and, as such, they will vary due to the effects of production-related variations of the IC and external resistors.

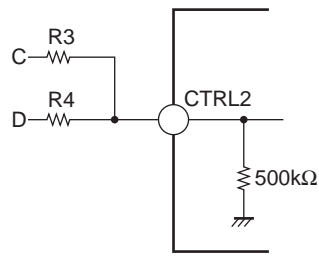
• CTRL1 Application Circuit Example



(1) 3.3V input: $R1 = 4.7k\Omega$, $R2 = 10k\Omega$

A	B	CTRL1
0V	0V	0V
0V	3.3V	1.05V
3.3V	0V	2.23V
3.3V	3.3V	3.20V

• CTRL2 Application Circuit Example



(1) 3.3V input: $R3 = R4 = 4.7k\Omega$

A	B	CTRL2
0V	0V	0V
0V	3.3V	1.61V
3.3V	0V	1.61V
3.3V	3.3V	3.29V

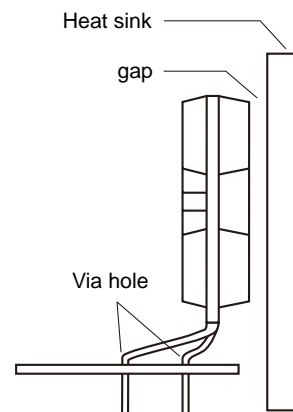
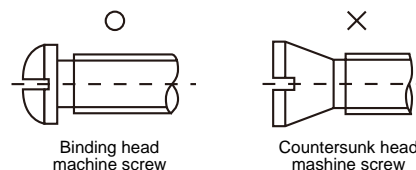
HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the heat generated by the device to the outer environment and dissipating that heat.

- a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

- b. Heat sink attachment

- Use flat-head screws to attach heat sinks.
- Use also washer to protect the package.
- Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
- If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Take care a position of via hole .
- Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Verify that there are no press burrs or screw-hole burrs on the heat sink.
- Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- Twisting must be limited to under 0.05 mm.
- Heat sink and semiconductor device are mounted in parallel.
- Take care of electric or compressed air drivers
- The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.



- c. Silicone grease

- Spread the silicone grease evenly when mounting heat sinks.
- Sanyo recommends YG-6260 (Momentive Performance Materials Japan LLC)

- d. Mount

- First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

- e. When mounting the semiconductor device to the heat sink using jigs, etc.,

- Take care not to allow the device to ride onto the jig or positioning dowel.
- Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

- f. Heat sink screw holes

- Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

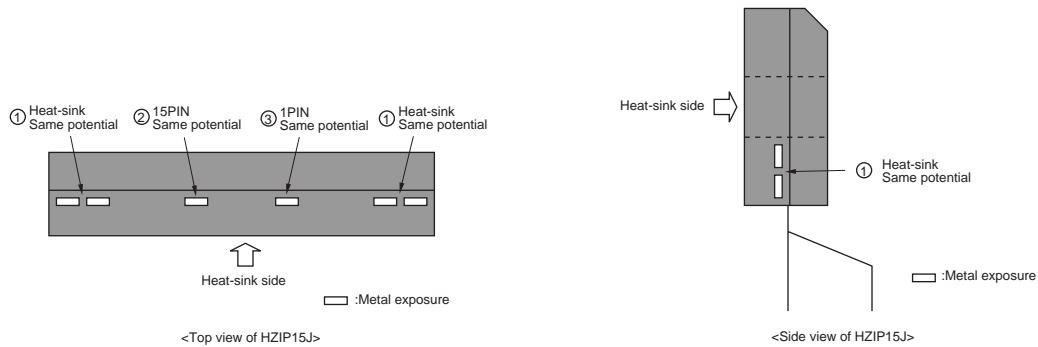
- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

Caution for implementing LV5680P to a system board

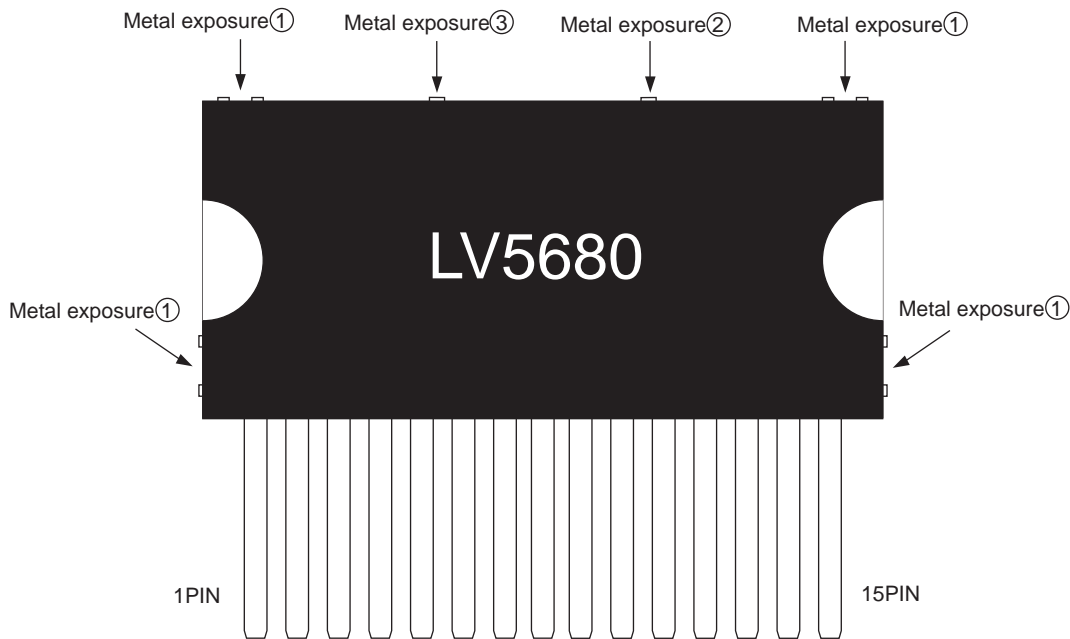
The package of LV5680P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC} . The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

LV5680P

- HZIP15J outline



- Frame diagram (LV5680P) *In the system power supply other than LV5680P, pin assignment may differ.



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of October, 2011. Specifications and information herein are subject to change without notice.