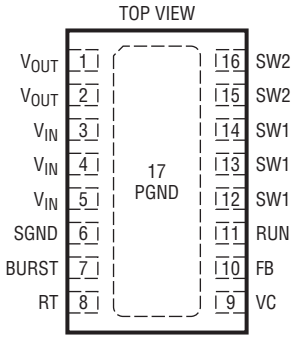
ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

V_{IN}, V_{OUT}, SW1, SW2 Voltage (DC)..... –0.3V to 6V
SW1, SW2 Voltage, Pulsed (<100ns) (Note 4).....7V
VC, RUN, BURST Voltage..... –0.3V to 6V
FB .....–0.3V to V_{IN}
RT Voltage..... –0.3V to 1V

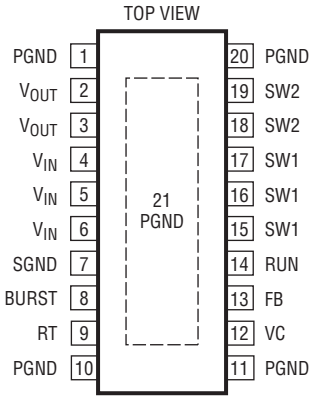
Operating Junction Temperature Range
(Notes 2, 5)..... –40°C to 125°C
Maximum Junction Temperature..... 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

PIN CONFIGURATION



DHD PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 36.5°C/W, θ_{JC} = 3.6°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 31.5°C/W, θ_{JC} = 4.1°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3113EDHD#PBF	LTC3113EDHD#TRPBF	3113	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3113IDHD#PBF	LTC3113IDHD#TRPBF	3113	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3113EFE#PBF	LTC3113EFE#TRPBF	LTC3113FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3113IFE#PBF	LTC3113IFE#TRPBF	LTC3113FE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V, V_{OUT} = 3.8V unless otherwise noted.

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Input Operating Range		●	1.8		5.5	V
Output Voltage Adjust Range		●	1.8		5.5	V
Feedback Voltage	V_{BURST} = 0V	●	588	600	612	mV
Feedback Input Current	V_{FB} = 0.7V			0	50	nA
Quiescent Current–Burst Mode Operation	V_{BURST} = 3.3V			40	55	µA
Quiescent Current–Shutdown	V_{OUT} = 0V, V_{RUN} = 0V, Not Including Switch Leakage			0.1	1	µA
Quiescent Current–Active	V_{FB} = 0.7V, V_{BURST} = 0V, R_T = 90.9k			300	500	µA
Input Current Limit		●	5.8	7.8	9.8	A
Peak Current Limit			6.5	11.1	16.0	A
Burst Mode Peak Current Limit			0.9	1.9	2.9	A
Reverse Current Limit			–1.6	–1	–0.4	A
NMOS Switch Leakage	Switch B, SW1 = 5.5V, V_{IN} = 5.5V, V_{OUT} = 5.5V Switch C, SW2 = 5.5V, V_{IN} = 5.5V, V_{OUT} = 5.5V			0.01 0.01	10 10	µA µA
PMOS Switch Leakage	Switch A, V_{IN} = 5.5V, V_{OUT} = 5.5V, SW1 = 0V Switch D, V_{IN} = 5.5V, V_{OUT} = 5.5V, SW2 = 0V			0.01 0.01	20 20	µA µA
NMOS Switch On-Resistance	Switch B, V_{OUT} = 3.8V Switch C, V_{OUT} = 3.8V			25 35		mΩ mΩ
PMOS Switch On-Resistance	Switch A, V_{IN} = 3.3V Switch D, V_{OUT} = 3.8V			30 40		mΩ mΩ
Maximum Duty Cycle	Boost (% Switch C On) Buck (% Switch A On)	● ●	80 100	90		% %
Minimum Duty Cycle		●			0	%
Frequency Accuracy	R_T = 90.9k	●	0.8	1	1.2	MHz
Error Amp AVOL				100		dB
Error Amp Source Current	V_C = 0V, V_{FB} = 0V			500		µA
Error Amp Sink Current	V_C = 1.2V, V_{FB} = 0.7V			160		µA
BURST Input Logic Threshold		●	0.3	0.7	1.2	V
BURST Input Current	V_{BURST} = 5.5V			0	1	µA
RUN Input Logic Threshold		●	0.3	0.7	1.2	V
RUN Input Current	V_{RUN} = 5.5V			0	1	µA
Soft-Start Time				2		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3113 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3113E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3113I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when the protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Voltage transients on the switch pins beyond the DC limit specified in the absolute maximum ratings are non-disruptive to normal operation when using good layout practices, as shown on the demo board or described in the data sheet and application notes.

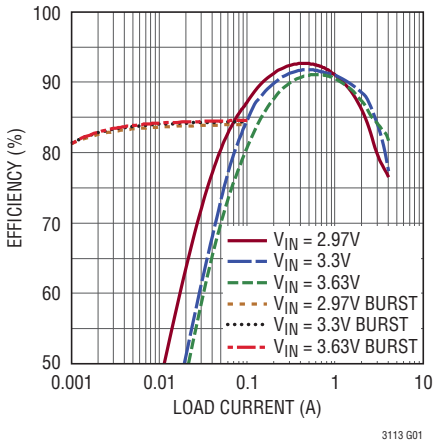
Note 5: The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and the power dissipation (P_D in Watts) as follows:

$$T_J = T_A + (P_D) \bullet (\theta_{JA}°C/W)$$

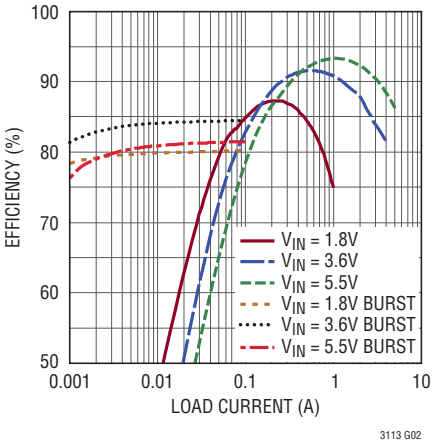
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{IN} = 3.3V, V_{OUT} = 3.8V unless otherwise specified)

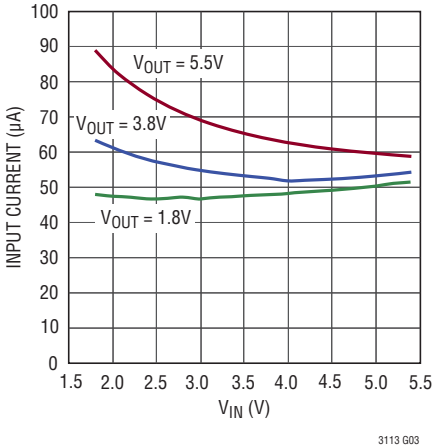
Efficiency 3.3V ±10% to 3.8V



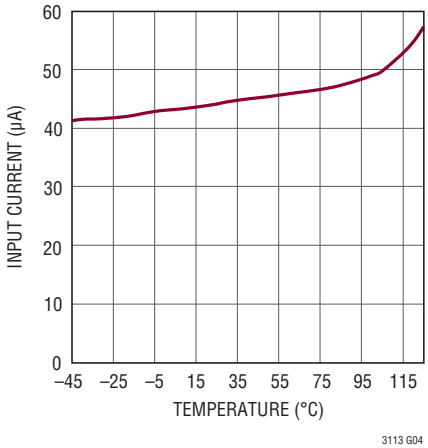
Efficiency 1.8V, 3.6V, 5.5V to 3.8V



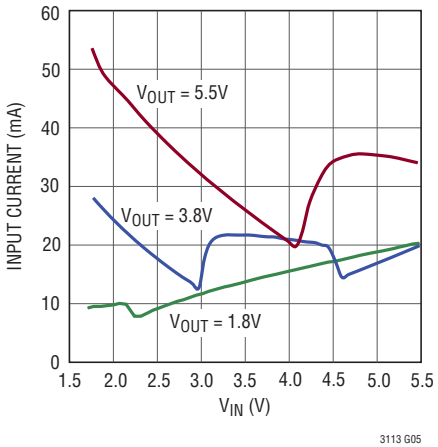
Burst Mode No-Load Input Current vs V_{IN}



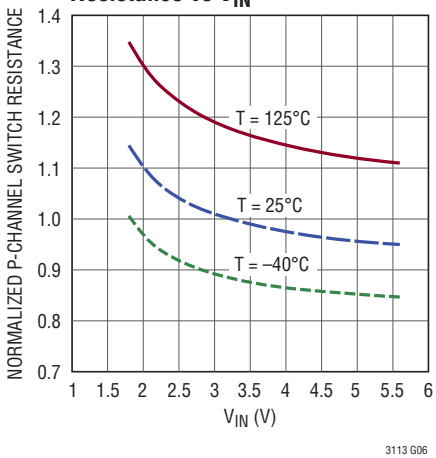
Burst Mode No-Load Input Current vs Temperature



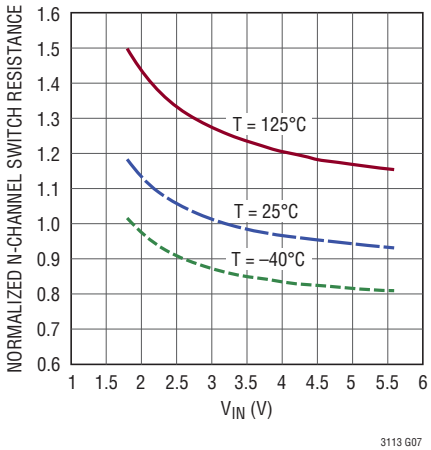
PWM Mode No-Load Input Current vs V_{IN}



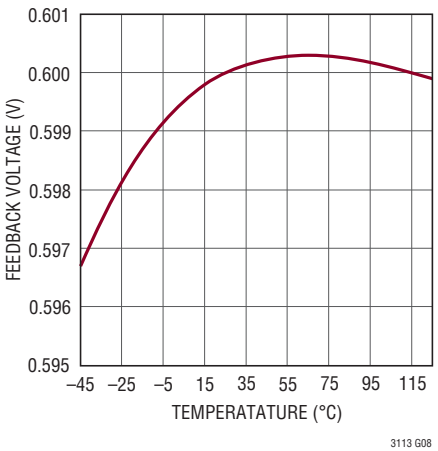
Normalized P-Channel Switch Resistance vs V_{IN}



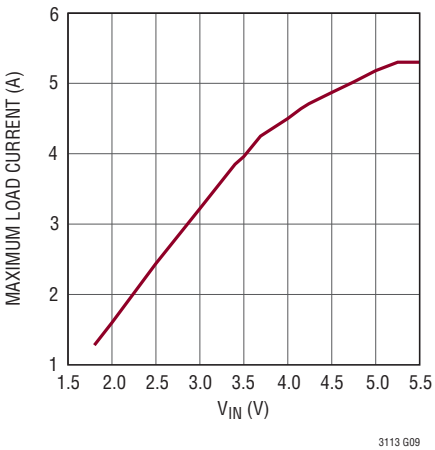
Normalized N-Channel Switch Resistance vs V_{IN}



Feedback Voltage vs Temperature



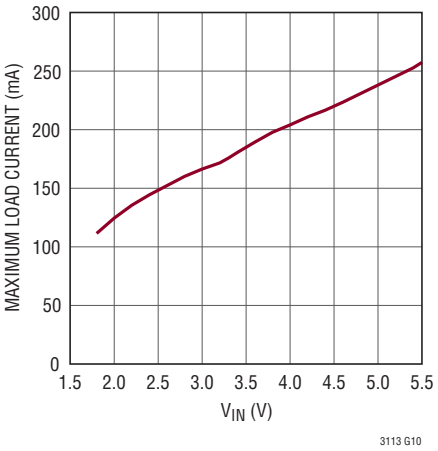
Maximum Load Current in PWM Mode vs V_{IN} (Input Current limit 5.8A)



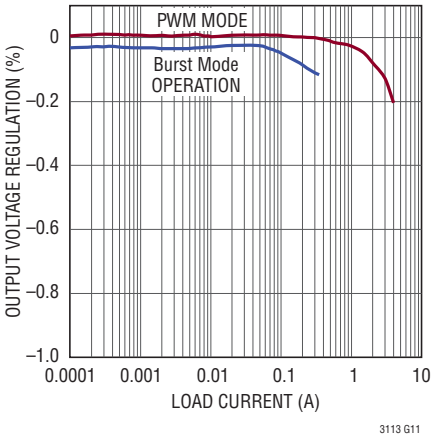
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{IN} = 3.3V, V_{OUT} = 3.8V unless otherwise specified)

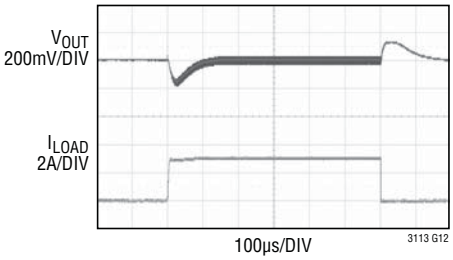
Maximum Load Current in Burst Mode Operation vs V_{IN} (Burst Mode Peak Current Limit 0.9A)



Output Voltage Regulation vs Load Current

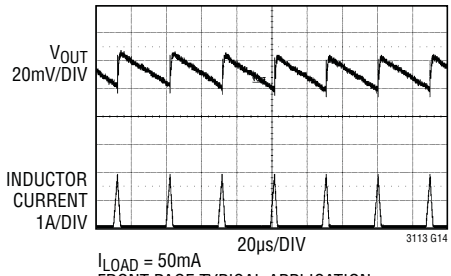


Load Step, 0A to 3A



BACK PAGE TYPICAL APPLICATION

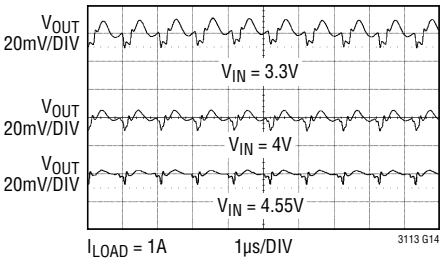
Output Voltage Ripple in Burst Mode Operation



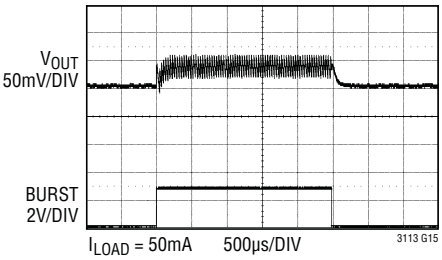
I_{LOAD} = 50mA

FRONT PAGE TYPICAL APPLICATION

Output Voltage Ripple in PWM Mode

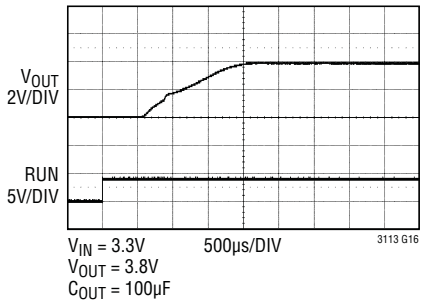


Burst to PWM Mode Transient

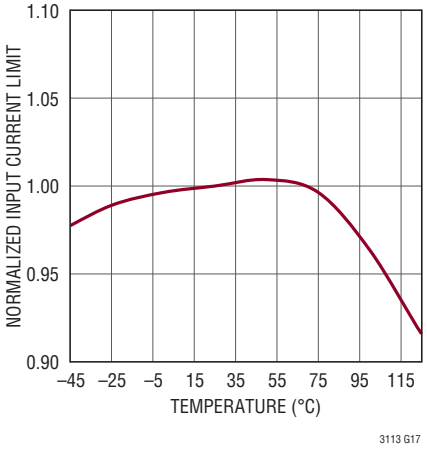


FRONT PAGE TYPICAL APPLICATION

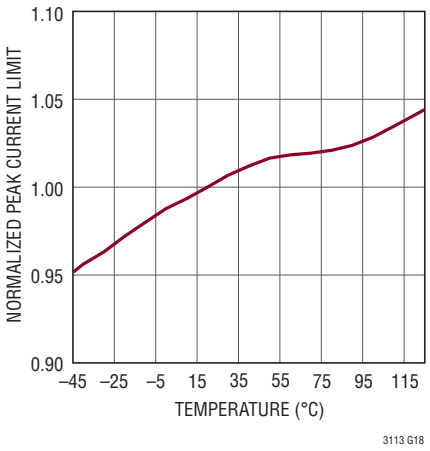
Soft-Start



Normalized Input Current Limit vs Temperature (7.8A Typical)



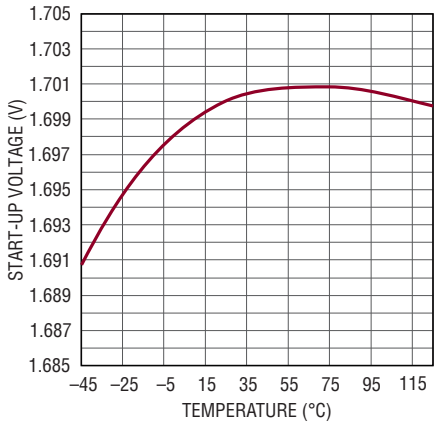
Normalized Peak Current Limit vs Temperature (11.1A Typical)



TYPICAL PERFORMANCE CHARACTERISTICS

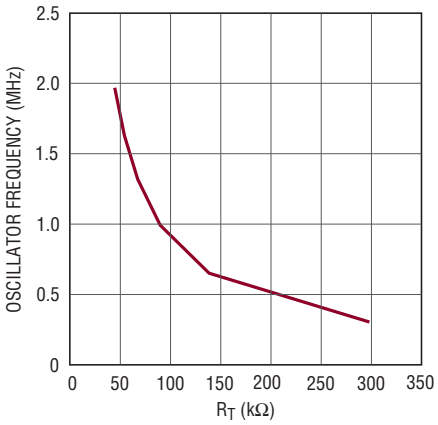
(T_A = 25°C, V_{IN} = 3.3V, V_{OUT} = 3.8V unless otherwise specified)

Minimum Start-Up Voltage vs Temperature



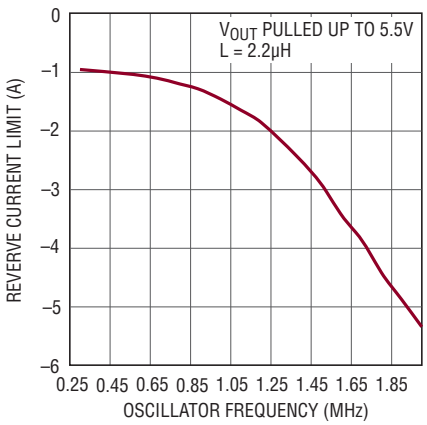
3113 G19

Oscillator Frequency vs R_T



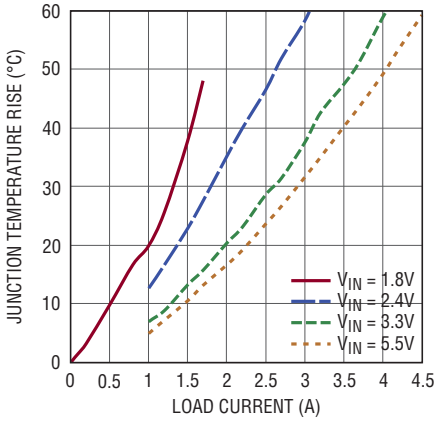
3113 G20

Negative Inductor Current vs Oscillator Frequency



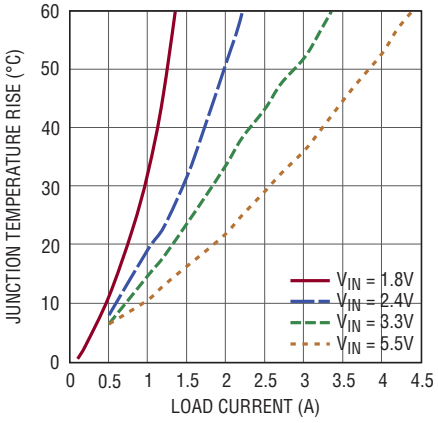
3113 G21

Junction Temperature Rise vs Continuous Load Current for V_{OUT} = 1.8V



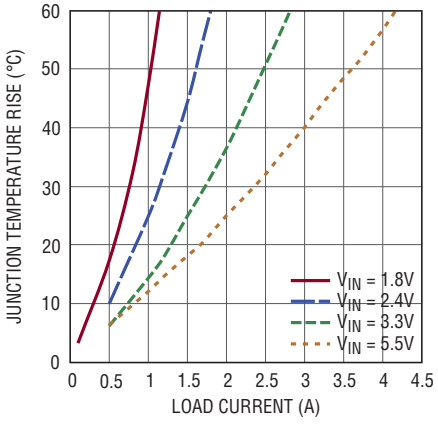
3113 G22

Junction Temperature Rise vs Continuous Load Current for V_{OUT} = 3.3V



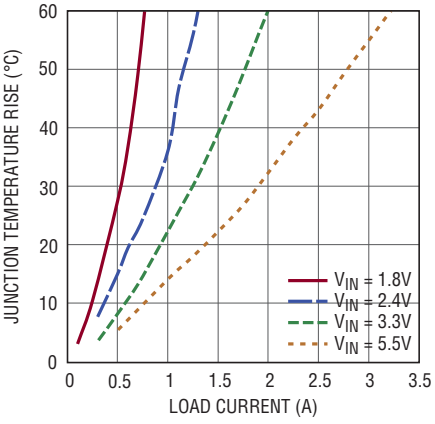
3113 G23

Junction Temperature Rise vs Continuous Load Current for V_{OUT} = 3.8V



3113 G24

Junction Temperature Rise vs Continuous Load Current for V_{OUT} = 5.5V



3113 G25

PIN FUNCTIONS (DFN/TSSOP)

V_{OUT} (Pins 1, 2/Pins 2, 3): Buck-Boost Output Voltage. A low ESR capacitor should be placed from V_{OUT} to PGND. The capacitor should be placed as close to the IC as possible and have a short return path to ground.

V_{IN} (Pins 3, 4, 5/Pins 4, 5, 6): Power Input for the Converter. A 47µF or larger bypass capacitor should be connected between V_{IN} and PGND. The bypass capacitor should located as close to V_{IN} and PGND as possible and should via directly to the ground plane.

SGND (Pin 6/Pin 7): Signal Ground. Terminate the frequency setting resistor and output voltage divider to SGND.

BURST (Pin 7/Pin 8): Pulse Width Modulation/Burst Mode Selection Input. Forcing this pin low causes the switching converter to operate in low noise fixed frequency PWM mode. Forcing this pin high enables constant Burst Mode operation for the converter. During Burst Mode operation, the converter can only support a reduced maximum load current.

RT (Pin 8/Pin 9): Programs the Frequency of the Internal Oscillator. Connect a resistor from RT to ground (SGND). The R_T resistor value for a given frequency is given by the following equation.

$$R_T \cong \frac{90}{f(MHz)} (k\Omega)$$

VC (Pin 9/Pin 12): Error Amp Output. An R-C network is connected from this pin to FB for loop compensation. Refer to the Closing the Feedback Loop section for component selection guidelines.

FB (Pin 10/Pin 13): Feedback Voltage for the Buck-Boost Converter Derived from a Resistor Divider on the Buck-Boost Output Voltage. The buck-boost output voltage is given by the following equation:

$$V_{OUT} = 0.600\left(1+\frac{R2}{R1}\right)(V)$$

where R1 is a resistor connected between FB and SGND, and R2 is a resistor connected between FB and V_{OUT}. The buck-boost output voltage can be adjusted from 1.8V to 5.5V.

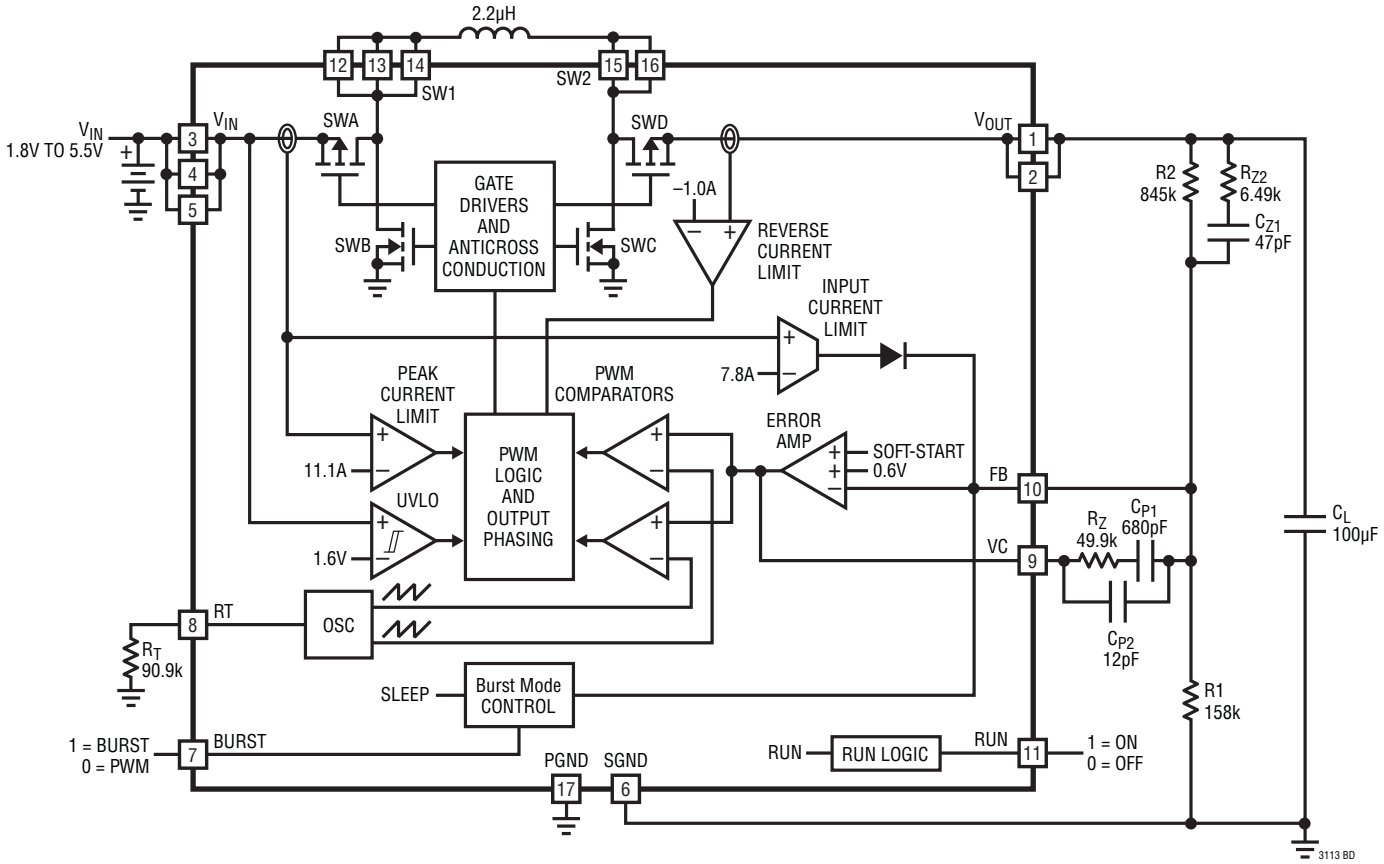
RUN (Pin 11/Pin 14): Active High Converter Enable Input. Applying a voltage <0.3V to this pin shuts down the LTC3113. Applying a voltage >1.2V to this pin enables the LTC3113.

SW1 (Pins 12, 13, 14/Pins 15, 16, 17): Switch Pin Where Internal Switches A and B are Connected. Connect the inductor from SW1 to SW2. Minimize trace length to reduce EMI.

SW2 (Pins 15, 16/Pins 18, 19): Switch Pin Where Internal Switches C and D are Connected. Connect the inductor from SW1 to SW2. Minimize trace length to reduce EMI.

PGND (Exposed Pad Pin 17/Pins 1, 10, 11, 20, Exposed Pad Pin 21): The exposed pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible. In most applications the bulk of the heat flow out of the LTC3113 is through this pad, so printed circuit board design has an impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations section for more details.

DETAILED BLOCK DIAGRAM (DFN Package)



OPERATION

INTRODUCTION

The LTC3113 is a low noise, high power synchronous buck-boost DC/DC converter optimized for demanding applications. The LTC3113 utilizes a proprietary switching algorithm, which allows its output voltage to be regulated above, below or equal to the input voltage. The error amplifier output (VC) determines the output duty cycle of each switch. The low $R_{DS(ON)}$, low gate charge, synchronous power switches provide high frequency pulse width modulation control. High efficiency is achieved at light loads when Burst Mode operation is commanded.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation can be programmed between 300kHz and 2MHz by an external resistor from the RT pin to ground, according to the following equation:

$$R_T \cong \frac{90}{f(MHz)}\ (k\Omega)$$

Error Amplifier

The error amplifier is a high gain voltage mode amplifier. The loop compensation components are configured around the amplifier (from FB to VC) to obtain stable converter operation. For improved bandwidth, an additional RC feedforward network can be placed across the upper feedback divider resistor. Refer to the Applications Information section of this data sheet under Closing the Feedback Loop for information on selecting compensation type and components.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which sources current into FB to reduce the output voltage, should the input current exceed 7.8A. Due to the high gain of the feedback loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in current limit will have a dependency on the duty cycle (i.e., on the input and output voltages) in the overcurrent condition. For this current limit feature to be most effective, the Thevenin resistance from FB to ground should exceed 100k.

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it is possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A if the current ever exceeds approximately 142% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Should the output voltage become less then 1.2V nominally, both the current limits are reduced compared to the normal operating current limits.

Reverse Current Limit

During fixed frequency operation, a reverse-current comparator on switch D monitors the current entering V_{OUT}. When this current exceeds 1A (typical) switch D will be turned off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is held above the regulation voltage by an external source.

In applications where the oscillator frequency is programmed above 1MHz and the output voltage is held above its programmed regulation value, reverse currents greater than 1A (typical) may be observed. In conjunction with oscillator frequencies higher than 1MHz, higher output voltages will also increase the magnitude of observed reverse current. Refer to the Negative Inductor Current vs Oscillator Frequency graph in the Typical Performance Characteristics section for typical variations.

OPERATION

Internal Soft-Start

The LTC3113 buck-boost converter has an independent internal soft-start circuit with a nominal duration of 2ms. The converter remains in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current during start-up. During soft-start, the buck-boost is forced into PWM mode operation regardless of the state of the BURST pin.

Thermal Shutdown

If the die temperature exceeds 155°C the LTC3113 buck-boost converter will be disabled. All power devices are turned off and the switch nodes will be forced into a high impedance state. The soft-start circuit for the converter is reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. When the die temperature drops to approximately 145°C the LTC3113 will restart. For recommendations regarding thermal design of the LTC3113 PCB, refer to the PCB Thermal Considerations section in Applications Information.

Undervoltage Lockout

If the supply voltage decreases below 1.6V (typical) then the LTC3113 buck-boost converter will be disabled and all power devices are turned off. The soft-start circuit is reset during undervoltage lockout to provide a smooth restart once the input voltage rises above 1.7V (typical) the undervoltage lockout increasing threshold.

When operating the LTC3113 at low input voltages, care must be taken under heavy loads to prevent the part from cycling into and out of UVLO. When operating at low input voltages the voltage drop created by the source resistance can trigger the UVLO, resetting the part. Operation near the undervoltage lockout is not recommended, but if requirements dictate, the source resistance should be less than $100mV/I_{IN(MAX)}$ (where $I_{IN(MAX)}$ is the maximum input current) to ensure proper operation.

Inductor Damping

When the LTC3113 is in burst operation and sleep mode, active circuits "damp" the inductor voltage through 165Ω (typical) impedance from both SW1 and SW2 to ground minimizing EMI.

PWM Mode Operation

When the BURST pin is held low, the LTC3113 buck-boost converter operates in a fixed-frequency pulse width modulation (PWM) mode using voltage mode control. Full output current is only available in PWM mode. A proprietary switching algorithm allows the converter to transition between buck, buck-boost, and boost modes without discontinuity in inductor current. The switch topology for the buck-boost converter is shown in Figure 1.

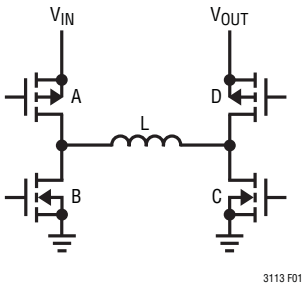


Figure 1. Buck-Boost Switch Topology

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. As the input voltage drops below the output voltage, the

OPERATION

AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all three operational modes. These advantages result in increased efficiency and stability in comparison to the traditional four-switch buck-boost converters.

Burst Mode Operation

With the BURST pin held high, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses and as a result only a fraction of the maximum output current can be delivered when in this mode.

These current pulses are repeated as often as necessary to maintain the output regulation voltage. The maximum output current, I_{MAX}, which can be supplied in Burst Mode operation is dependent upon the input and output voltage as given by the following formula:

$$I_{MAX} \cong \frac{I_{PK}}{2} \bullet \frac{V_{IN}}{V_{IN} + V_{OUT}} \bullet \eta \ (A)$$

where I_{PK} is the Burst Mode peak current limit in amps and is the η efficiency.

If the buck-boost load exceeds the maximum Burst Mode current capability, the output rail will lose regulation. In Burst Mode operation, the error amplifier is configured in a low power mode of operation and used to hold the compensation pin, VC, to reduce transients that may occur during transitions from Burst Mode to PWM mode operation.

APPLICATIONS INFORMATION

The basic LTC3113 application circuit is shown as the typical application on the front page of this data sheet. The external component selection is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, output voltage, output current, output ripple voltage and efficiency. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

OUTPUT VOLTAGE PROGRAMMING

The buck-boost output voltage is set via an external resistor divider connected to the FB pin as shown in Figure 2.

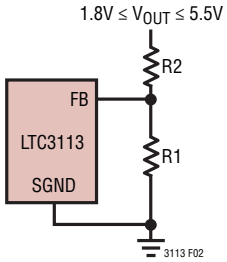


Figure 2. Setting the Output Voltage

The resistor divider values determine the buck-boost output voltage according to the following formula:

$$V_{OUT} = 0.600\left(1+\frac{R2}{R1}\right)\ (V)$$

As noted in the Current Limit Operation section: “for the current limit feature to be most effected, the Thevenin resistance (R1||R2) from FB to ground should exceed 100k.”

INDUCTOR SELECTION

To achieve high efficiency, a low ESR inductor should be selected for the buck-boost converter. In addition, the inductor must have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple will be larger in buck and boost mode than in the buck-boost region. The peak-to-peak inductor current ripple for each mode can be calculated from the following formulas, where f is the frequency in MHz and L is the inductance in µH:

$$\Delta I_{L,P\text{-}P,BUCK} = \frac{V_{OUT}}{f \bullet L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)(A)$$

$$\Delta I_{L,P\text{-}P,BOOST} = \frac{V_{IN}}{f \bullet L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)(A)$$

To ensure operation without triggering the reverse current comparator under no load conditions it is recommended that the peak-to-peak inductor ripple not exceed 800mA taking into account the maximum reverse current limit of –0.4A specified in the Electrical Characteristics section. Utilizing this recommendation for applications operating at a switching frequency of 300kHz requires a minimum inductance of 6.8µH, similarly an application operation at a frequency of 2MHz would require a minimum of 1µH.

In addition to affecting output current ripple, the value of the inductor can also impact the stability of the feedback loop. In boost and buck-boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop.

In addition to affecting the efficiency of the buck-boost converter, the inductor DC resistance can also impact the maximum output capability of the buck-boost converter at low input voltage. In buck mode, the buck-boost output current is limited only by the inductor current reaching the current limit value. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the graph in the Typical Performance Characteristics section of this data sheet.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry.

APPLICATIONS INFORMATION

The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3113 buck-boost converter applications. All inductor specifications are listed at an inductance value of 2.2µH for comparison purposes but other values within these inductor families are generally well suited to this application. Within each family (i.e. at a fixed size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Table 1. Representative Buck-Boost Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
CoilCraft (www.coilcraft.com)				
MSS1048	2.2	7.2	8.4	10 × 10.3 × 4
MSS1260	2.2	12	13.9	12.3 × 12.3 × 6
SER1052	2.2	4	10	10.6 × 10.6 × 5.2
Toko (www.toko.com)				
D106C	2.4	7.7	10	10.3 × 10.3 × 6.7
FDA1055	2.2	4.8	10.5	11.6 × 10.8 × 5.5
FDA1254	2.2	4.5	14.7	13.5 × 12.6 × 5.4
Cooper (www.cooperbussmann.com)				
HCP0703	2.2	18	14	7 × 7.3 × 3
HCP0704	2.3	16.5	11.5	6.8 × 6.8 × 4.2
HC8	2.6	11.4	10	10.9 × 10.4 × 4
TDK (www.component.tdk.com)				
VLF100040	2.2	7.9	8.2	9.7 × 10 × 4
RLF12560	2.7	4.5	12	13 × 13 × 6
VLF12060	2.7	6.4	10	11.7 × 12 × 6
Wurth (www.we-online.com)				
744066	2.2	10.5	6.8	10 × 10 × 3.8
744355	2	8	13	13.2 × 12.8 × 6.2
744324	2.4	4.8	17	10.5 × 10.2 × 4.7

OUTPUT CAPACITOR SELECTION

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in µF, L is the inductance in µH, V_{IN} is the input voltage in volts, V_{OUT} is the output voltage in volts. ΔV_{P-P} is the output ripple in volts and I_{LOAD} is the output current in amps.

$$C_{OUT} \geq \frac{1}{\Delta V_{P-P,BUCK} \bullet 8 \bullet L \bullet f^2} \bullet \frac{(V_{IN} - V_{OUT}) \bullet V_{OUT}}{V_{IN}} (\mu F)$$

$$C_{OUT} \geq \frac{I_{LOAD}(V_{OUT} - V_{IN})}{\Delta V_{P-P,BOOST} \bullet V_{OUT} \bullet f} (\mu F)$$

Given that the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode.

INPUT CAPACITOR SELECTION

It is recommended that a low ESR ceramic capacitor with a value of at least 47µF be located as close to V_{IN} as possible. In addition, the return trace from the pin to the ground plane should be made as short as possible. It is important to minimize any stray resistance from the converter to the battery or other power sources. If cabling is required to connect the LTC3113 to the battery or power supply, a higher ESR capacitor or a series resistor with low ESR capacitor in parallel with the low ESR capacitor may be needed to damp out ringing caused by the cable inductance.

CAPACITOR VENDOR INFORMATION

Both the input bypass capacitors and output capacitors used with the LTC3113 must be low ESR and designed to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce output ripple. Many modern low voltage ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose 50% or more of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating than required in order to actually realize the intended capacitance at the full operating voltage. For details, consult the capacitor vendor's curve of capacitance versus DC bias voltage.

APPLICATIONS INFORMATION

The capacitors listed in Table 2 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3113 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss over temperature is minimized.

Table 2. Representative Buck-Boost Surface Input Mount Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE (mm) W × L × H (FOOTPRINT)
AVX (www.avx.com)			
1812D476KAT2A	47	6.3	3.2 × 4.5 × 2.5 (1812)
18126D107KAT2A	100	6.3	3.2 × 4.5 × 2.8 (1812)
Murata (www.murata.com)			
GRM43ER60J476ME01	47	6.3	3.2 × 4.5 × 2.5 (1812)
GRM43SR60J107ME20	100	6.3	3.2 × 4.5 × 2.8 (1812)
GRM55FR60J107KA01L	100	6.3	5 × 5.7 × 3.2 (2220)
Taiyo Yuden (www.t-yuden.com)			
JMK432BJ476MM-T	47	6.3	3.2 × 4.5 × 2.5 (1812)
JMK432C107MM-T	100	6.3	3.2 × 4.5 × 2.8 (1812)
TDK (www.component.tdk.com)			
C4532X5R0J476M	47	6.3	3.2 × 4.5 × 2.5 (1812)
C4532X5R0J107M	100	6.3	3.2 × 4.5 × 2.5 (1812)
C5750X5R1C476M	47	16	5 × 5.7 × 2.5 (2220)
C5750X5R1A686M	68	10	5 × 5.7 × 2.5 (2220)
C5750X5R0J107M	100	6.3	5 × 5.7 × 2.5 (2220)

PCB LAYOUT CONSIDERATIONS

The LTC3113 switches large currents at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit. Figure 3 presents a representative 4-layer PCB layout to outline some of the primary considerations. A few key guidelines are outlined below:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all highlighted components in Figure 3 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on V_{IN} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The Exposed Pad is the power ground connection for the LTC3113. Multiple vias should connect the backpad directly to the ground plane. In addition maximization of the metallization connected to the backpad will improve the thermal environment and improve the power handling capabilities of the IC. Refer to Figure 3d bottom layer as an example of proper exposed pad power ground and via layout to provide good thermal and ground connection performance.
3. The components shown highlighted and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Connections to all of the components shown highlighted should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
5. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned to the ground plane using a via placed close to the IC and away from the power connections.
6. Keep the connection from the resistor dividers to the feedback pins, FB, as short as possible and away from the switch pin connections.
7. Crossover connections should be made on inner copper layers if available. If it is necessary to place these on the ground plane, make the trace on the ground plane as short as possible to minimize the disruption to the ground plane.

Thermal Considerations

The LTC3113 output current may need to be derated if it is required to operate in a high ambient temperature or delivering a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output voltage and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by mounting the LTC3113 to a 4-layer FR4 demo board shown in Figure 3. Boards of other sizes and layer count can exhibit different thermal behavior, so

APPLICATIONS INFORMATION

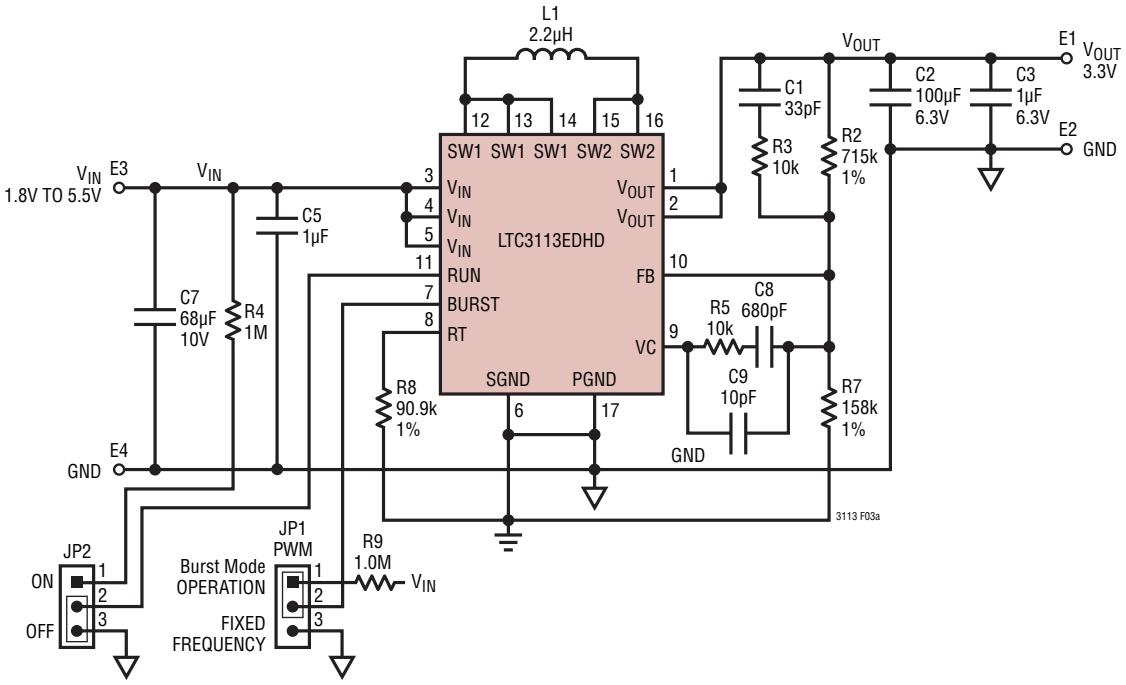


Figure 3a

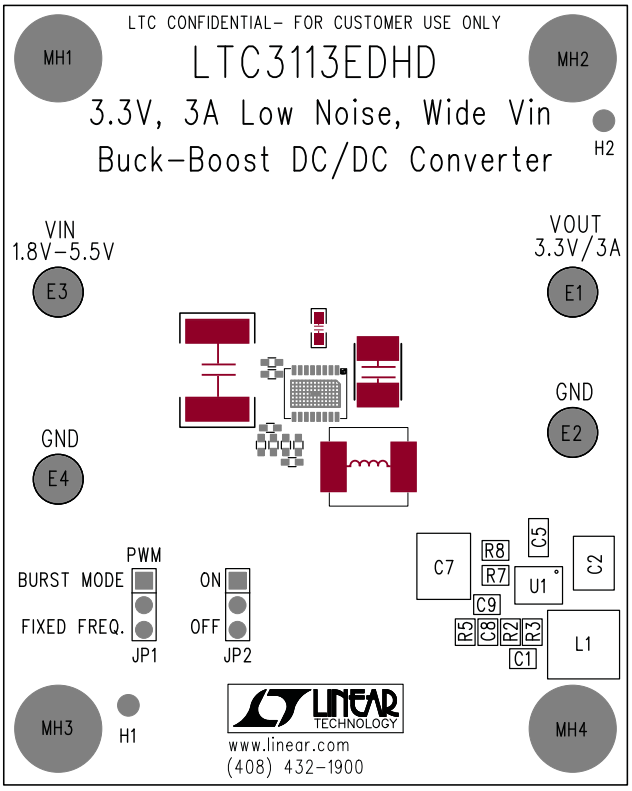


Figure 3b. Fabrication Layer of Example PCB

APPLICATIONS INFORMATION

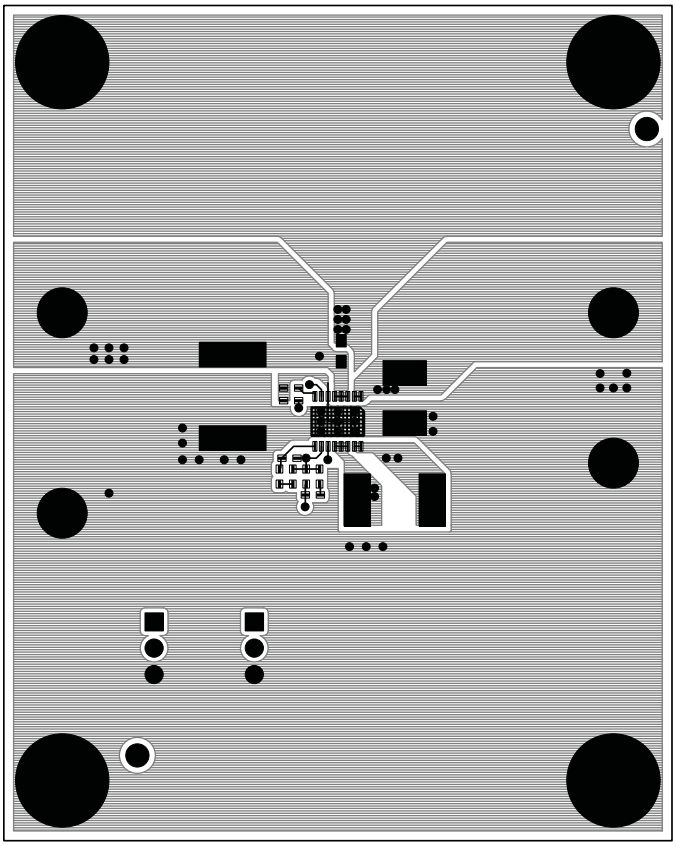


Figure 3c. Top Layer of Example PCB

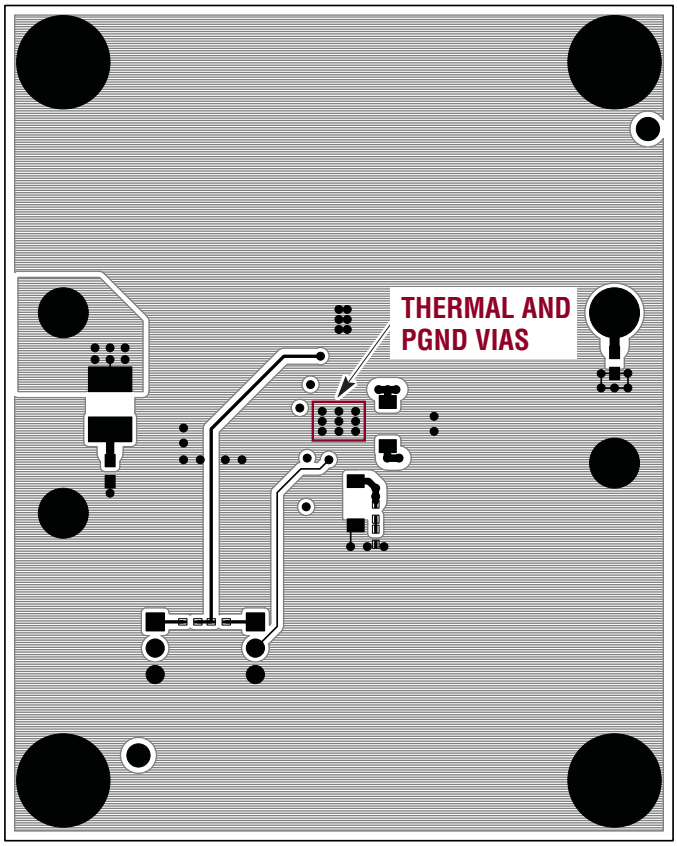


Figure 3d. Bottom Layer of Example PCB

it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The junction-to-air (θ_{JA}) and junction-to-case (θ_{JC}) thermal resistance given in the "Pin Configuration" diagram may also be used to estimate the LTC3113 internal temperature. These thermal coefficients are determined using a 4-layer PCB. Bear in mind that the actual thermal resistance of the LTC3113 to the printed circuit board depends upon the design of the circuit board.

The die temperature of the LTC3113 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit board to ensure good heat sinking of the LTC3113. The bulk of the heat flow is through the bottom exposed pad of the part into the printed circuit board. Consequently, a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Refer to the PCB Layout Considerations section for printed circuit board design suggestions.

As described in the Thermal Shutdown section, the LTC3113 is equipped with a thermal shutdown circuit that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above the 125°C rating to avoid interfering with normal operation. Thus, it follows that prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the die is subjected to temperatures above the 125°C rating for prolonged or repetitive intervals, which may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

CLOSING THE FEEDBACK LOOP

The LTC3113 incorporates voltage mode PWM control. The control-to-output gain varies with the operation region (buck, buck-boost, boost), but is usually no greater than 15. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2\pi\sqrt{LC_{OUT}}} (Hz)$$

(In Buck Region)

$$f_{FILTER\_POLE} = \frac{1}{2\pi\sqrt{LC_{OUT}}} \frac{V_{IN}}{V_{OUT}} (Hz)$$

(In Boost Region)

where L is in Henries and C_{OUT} is in Farads. The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2\pi R_{ESR} C_{OUT}} (Hz)$$

where R_{ESR} is the equivalent series resistance out the output capacitor in ohms.

A troublesome feature in the boost and buck-boost region is the right-half plane (RHP) zero, given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2\pi I_{OUT} L V_{OUT}} (Hz)$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop at the cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole. Referring to Figure 4, the unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2\pi R2 C_{P1}} (Hz)$$

Most applications demand an improved transient response to allow a smaller output capacitor. To achieve a higher bandwidth, Type III compensation is required, providing two zeros to compensate for the double-pole response of the output filter. Referring to Figure 5, the location of the poles and zeros are given by:

$$f_{POLE1} = \frac{1}{2\pi 10^5 R2 C_{P1}} (Hz)$$

$$f_{ZERO1} = \frac{1}{2\pi R_Z C_{P1}} (Hz)$$

$$f_{ZERO2} = \frac{1}{2\pi R2 C_{Z1}} (Hz)$$

$$f_{POLE2} = \frac{1}{2\pi R_Z C_{P2}} (Hz)$$

$$f_{POLE3} = \frac{1}{2\pi R_P C_{Z1}} (Hz)$$

where resistance is in Ohms and capacitance is in Farads.

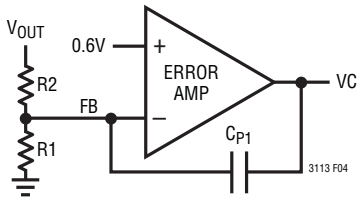


Figure 4. Error Amplifier with Type I Compensation

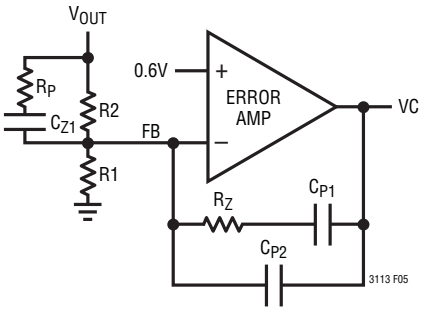
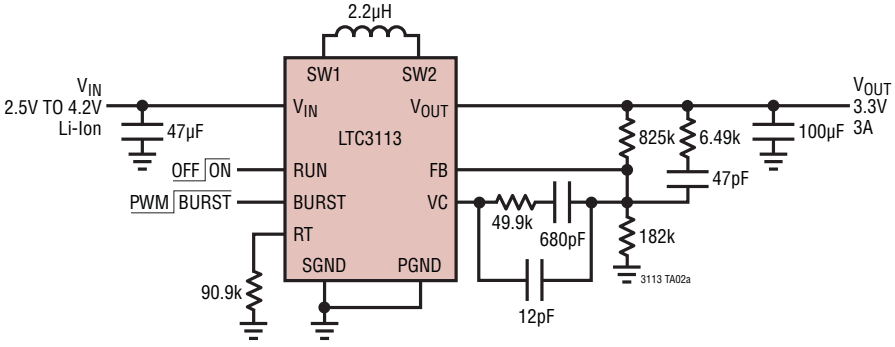


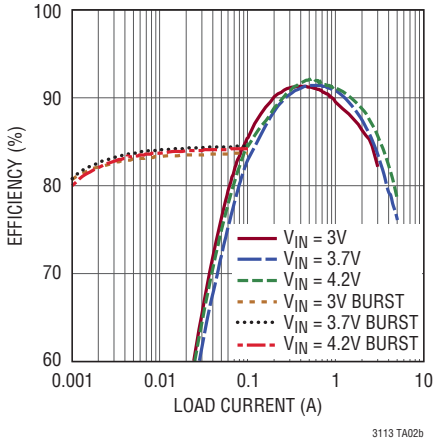
Figure 5. Error Amplifier with Type III Compensation

TYPICAL APPLICATIONS

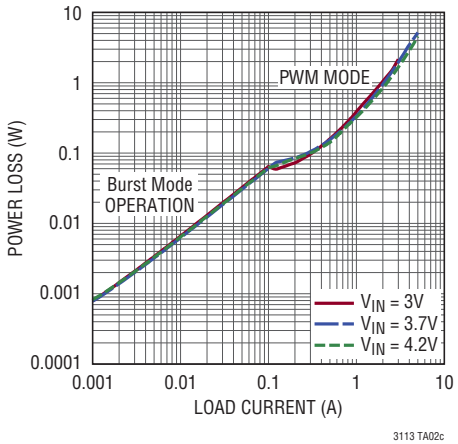
Li-Ion to 3.3V/3A



Efficiency Li-Ion (3V, 3.7V, 4.2V) to 3.3V

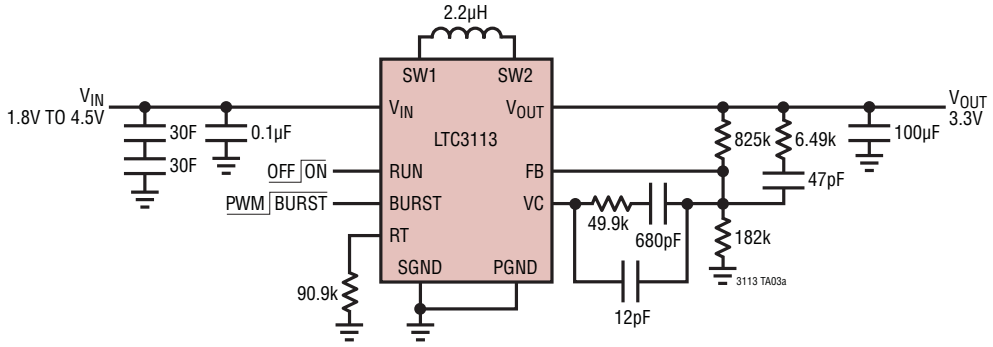


Power Loss Li-Ion (3V, 3.7V, 4.2V) to 3.3V

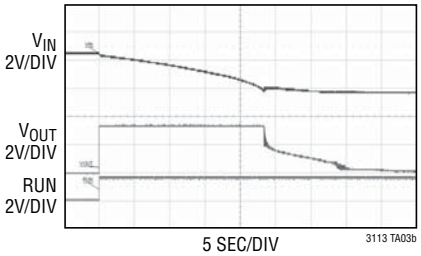


TYPICAL APPLICATIONS

Supercap Powered Backup Supply

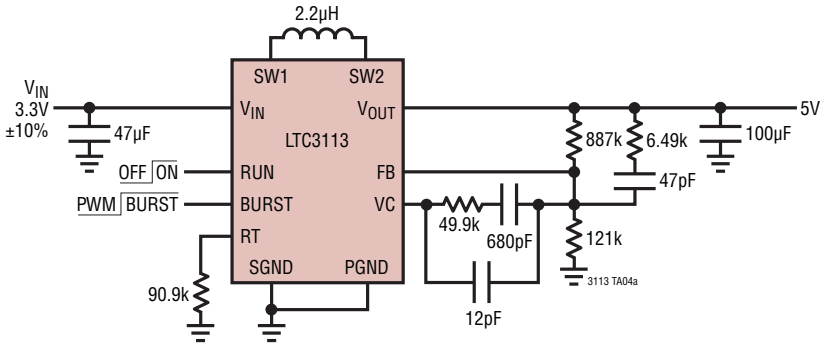


Typical Output Response with 1.5A Load

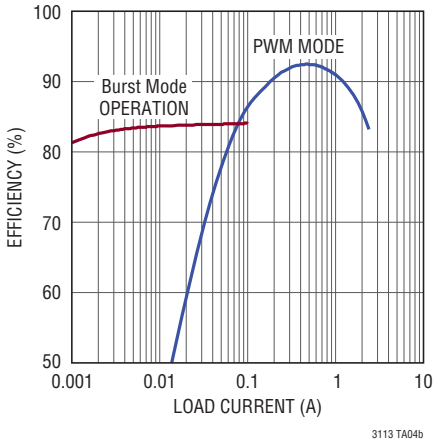


TYPICAL APPLICATIONS

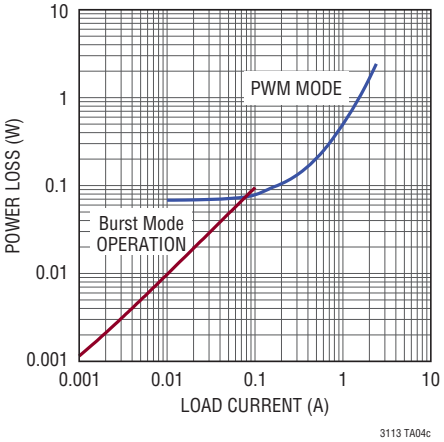
3.3V to 5V/2.5A Boost Converter with Output Disconnect



Efficiency vs Load Current

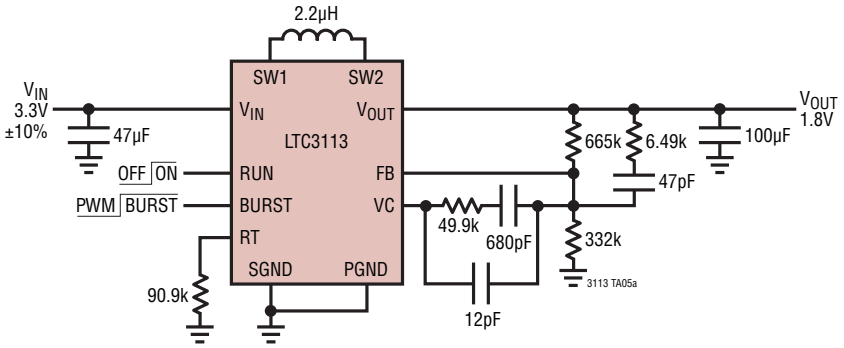


Power Loss vs Load Current

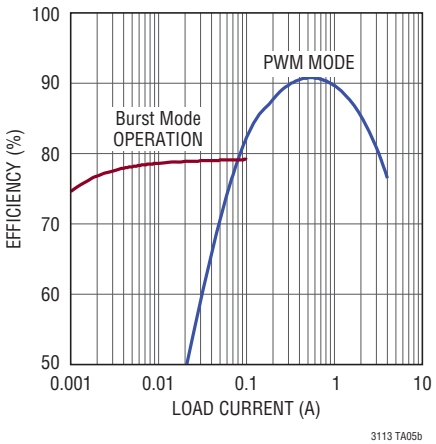


TYPICAL APPLICATIONS

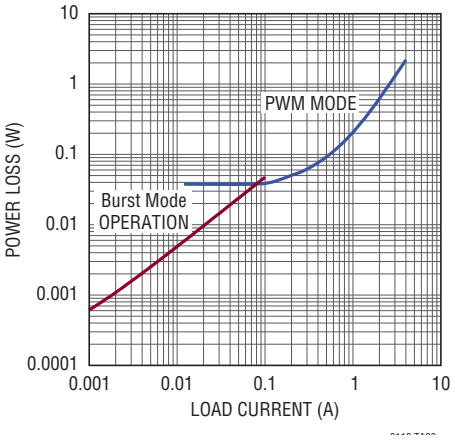
3.3V to 1.8V/5A Buck Converter



Efficiency vs Load Current

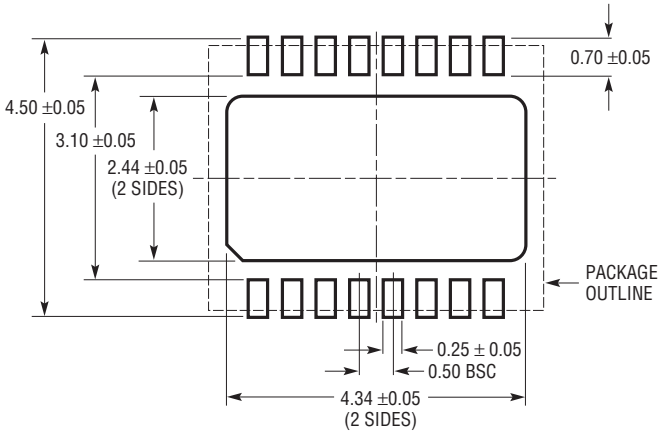


Power Loss vs Load Current

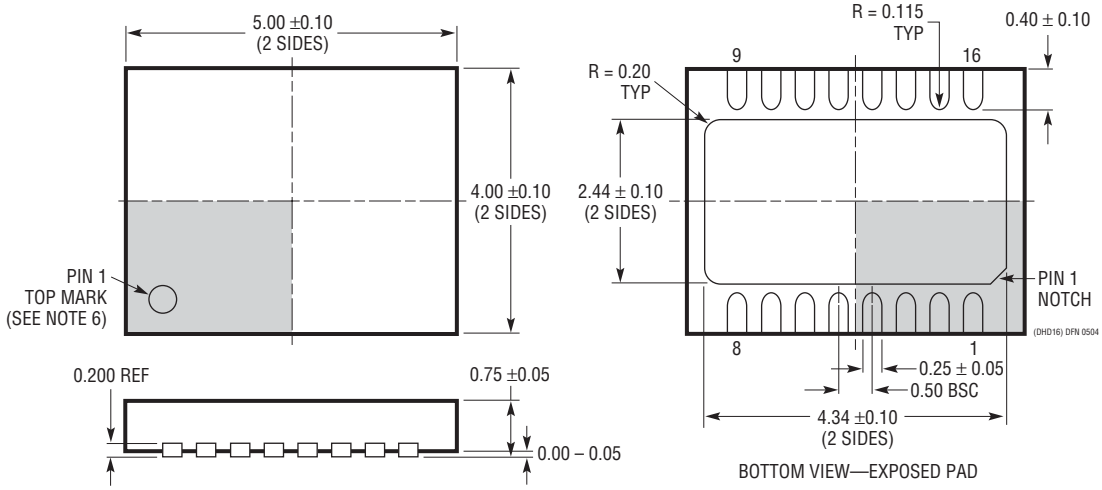


PACKAGE DESCRIPTION

DHD Package
16-Lead Plastic DFN (5mm × 4mm)
(Reference LTC DWG # 05-08-1707)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

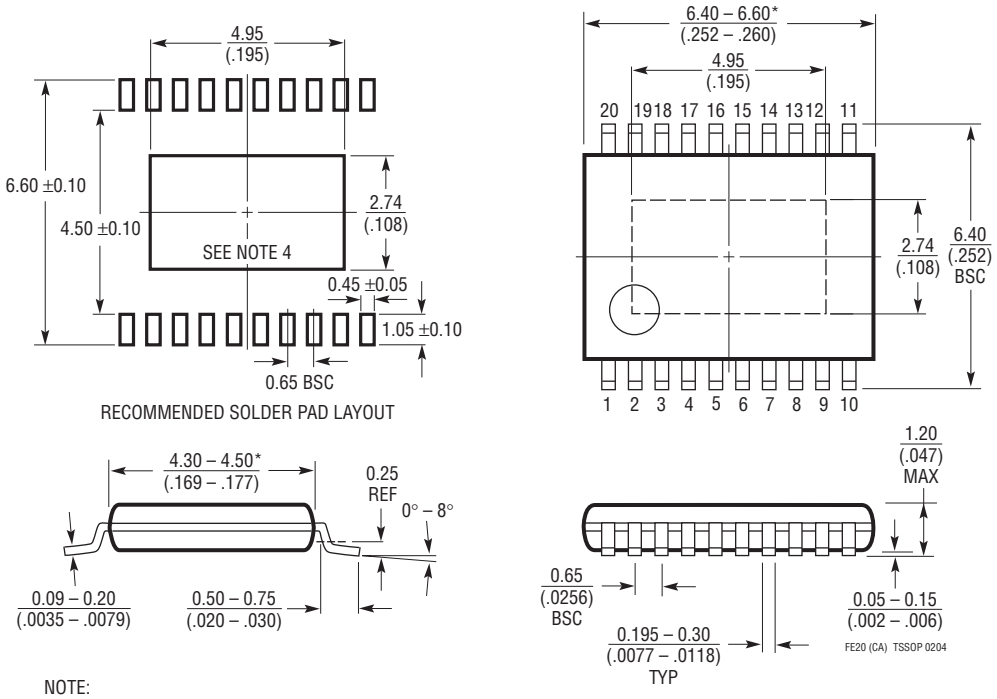


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

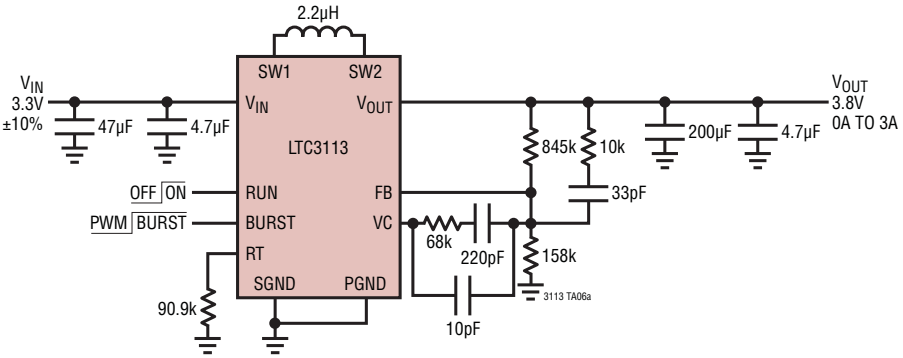
FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CA



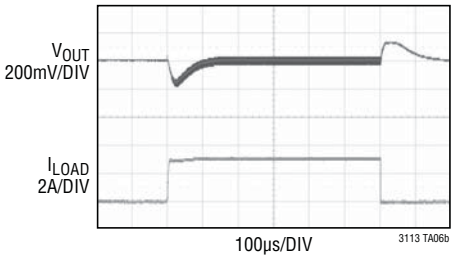
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Pulsed Load or Portable RF Power Amplifier Application



Typical Output Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3112	15V, 2.5A (I_{OUT}) Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 15V, V_{OUT}: 2.5V to 14V, I_Q = 50µA, I_{SD} < 1µA, DFN Package
LTC3127	1A Buck-Boost DC/DC Converter with Programmable Input Current Limit	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, DFN Package
LTC3531	200mA Buck-Boost Synchronous DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT} = 3.3V, I_Q =16µA, I_{SD} < 1µA, DFN Package
LTC3533	2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA, DFN Package
LTC3534	7V, 500mA Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 7V, V_{OUT}: 1.8V to 7V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.5V to 5.25V, I_Q = 25µA, I_{SD} < 1µA, MSOP and DFN Packages
LTC3441	1.2A (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter with Programmable Burst Mode Operation	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, DFN Package
LTC3785	10V, High Efficiency, Synchronous, No R_{SENSE}™ Buck-Boost Controller	V_{IN}: 2.7V to 10V, V_{OUT}: 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA, QFN Package
LTC3101	Wide V_{IN}, Multi-Output DC/DC Converter and PowerPath™ Controller	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.5V to 5.25V, I_Q = 38µA, I_{SD} < 15µA, QFN Package
LTC3530	Wide Input Voltage Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA, DFN Package

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