

LTC2904/LTC2905

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

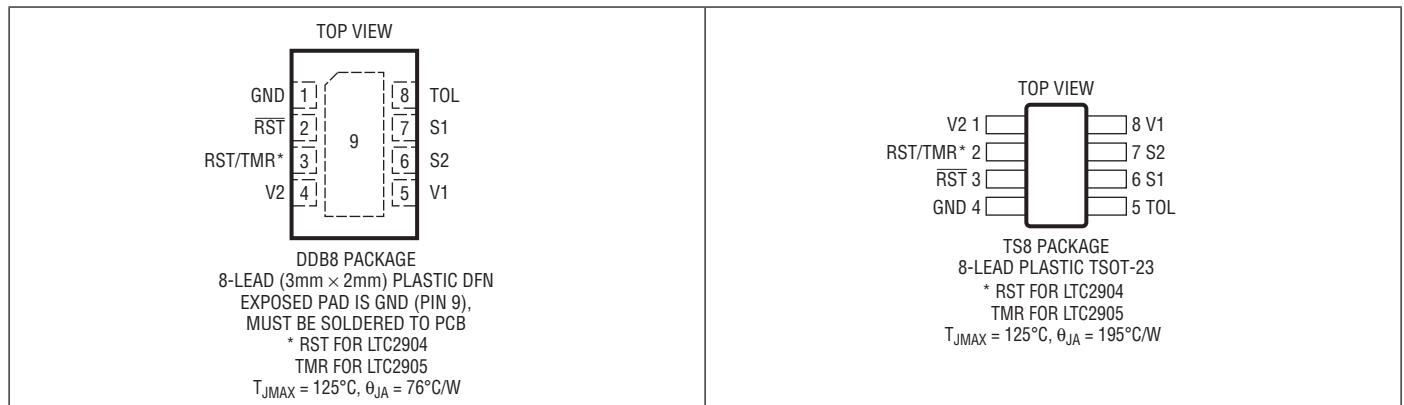
Terminal Voltages

V1, V2	–0.3V to 7V
S1, S2, TOL	–0.3V to ($V_{CC} + 0.3V$)
RST	–0.3V to 7V
RST (LTC2904)	–0.3V to 7V
TMR (LTC2905)	–0.3V to 7V

Operating Temperature Range

LTC2904C/LTC2905C	0°C to 70°C
LTC2904I/LTC2905I	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C
TSOT Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2904CDDDB#TRMPBF	LTC2904CDDDB#TRPBF	LBCZ	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2904IDDB#TRMPBF	LTC2904IDDB#TRPBF	LBDB	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2905CDDDB#TRMPBF	LTC2905CDDDB#TRPBF	LAJF	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2905IDDB#TRMPBF	LTC2905IDDB#TRPBF	LBCY	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2904CTS8#TRMPBF	LTC2904CTS8#TRPBF	LTBCJ	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2904ITS8#TRMPBF	LTC2904ITS8#TRPBF	LTBCK	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2905CTS8#TRMPBF	LTC2905CTS8#TRPBF	LTAJD	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2905ITS8#TRMPBF	LTC2905ITS8#TRPBF	LTAJE	8-Lead Plastic TSOT-23	–40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2904CDDDB#TRM	LTC2904CDDDB#TR	LBCZ	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2904IDDB#TRM	LTC2904IDDB#TR	LBDB	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2905CDDDB#TRM	LTC2905CDDDB#TR	LAJF	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2905IDDB#TRM	LTC2905IDDB#TR	LBCY	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2904CTS8#TRM	LTC2904CTS8#TR	LTBCJ	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2904ITS8#TRM	LTC2904ITS8#TR	LTBCK	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2905CTS8#TRM	LTC2905CTS8#TR	LTAJD	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2905ITS8#TRM	LTC2905ITS8#TR	LTAJE	8-Lead Plastic TSOT-23	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeand reel/>

29045fc

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_1 = 2.5\text{V}$, $V_2 = 1\text{V}$, $S_1 = \text{TOL} = V_1$, $S_2 = 0\text{V}$, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
	5V, 7.5% Reset Threshold		●	4.475	4.550	4.625	V
	5V, 10% Reset Threshold		●	4.350	4.425	4.500	V
V_{RT33}	3.3V, 5% Reset Threshold	V1, V2 Input Threshold	●	3.036	3.086	3.135	V
	3.3V, 7.5% Reset Threshold		●	2.954	3.003	3.053	V
	3.3V, 10% Reset Threshold		●	2.871	2.921	2.970	V
V_{RT25}	2.5V, 5% Reset Threshold	V1, V2 Input Threshold	●	2.300	2.338	2.375	V
	2.5V, 7.5% Reset Threshold		●	2.238	2.275	2.313	V
	2.5V, 10% Reset Threshold		●	2.175	2.213	2.250	V
V_{RT18}	1.8V, 5% Reset Threshold	V2 Input Threshold	●	1.656	1.683	1.710	V
	1.8V, 7.5% Reset Threshold		●	1.611	1.638	1.665	V
	1.8V, 10% Reset Threshold		●	1.566	1.593	1.620	V
V_{RT15}	1.5V, 5% Reset Threshold	V2 Input Threshold	●	1.380	1.403	1.425	V
	1.5V, 7.5% Reset Threshold		●	1.343	1.365	1.388	V
	1.5V, 10% Reset Threshold		●	1.305	1.328	1.350	V
V_{RT12}	1.2V, 5% Reset Threshold	V2 Input Threshold	●	1.104	1.122	1.140	V
	1.2V, 7.5% Reset Threshold		●	1.074	1.092	1.110	V
	1.2V, 10% Reset Threshold		●	1.044	1.062	1.080	V
V_{RT10}	1V, 5% Reset Threshold	V2 Input Threshold	●	0.920	0.935	0.950	V
	1V, 7.5% Reset Threshold		●	0.895	0.910	0.925	V
	1V, 10% Reset Threshold		●	0.870	0.885	0.900	V
V_{CCMIN}	Minimum Internal Operating Voltage (Note 2)	$\overline{\text{RST}}$ in Correct Logic State	●			1	V
I_{V1}	V1 Input Current	Includes Input Current to Three-State Pins	●		65	130	μA
I_{V2}	V2 Input Current		●		0.4	1.0	μA
$I_{TMR(UP)}$	TMR Pull-Up Current (LTC2905)	$V_{TMR} = 0\text{V}$	●	-1.5	-2.1	-2.7	μA
$I_{TMR(DOWN)}$	TMR Pull-Down Current (LTC2905)	$V_{TMR} = 1.4\text{V}$	●	1.5	2.1	2.7	μA
t_{RST}	Reset Time-Out Period (LTC2904)		●	140	200	260	ms
t_{RST}	Reset Time-Out Period (LTC2905)	$C_{TMR} = 22\text{nF}$	●	140	200	260	ms
t_{UV}	Vx Undervoltage Detect to RST or $\overline{\text{RST}}$	Vx Less than Reset Threshold V_{RTX} by More than 1%			150		μs
V_{OL}	Output Voltage Low $\overline{\text{RST}}$, $\overline{\text{RST}}$	$I = 2.5\text{mA}$	●		0.15	0.4	V
		$I = 100\mu\text{A}$; $V_1 = 1\text{V}$ ($\overline{\text{RST}}$ Only)	●		0.05	0.3	V
V_{OH}	Output Voltage High $\overline{\text{RST}}$, $\overline{\text{RST}}$ (Notes 2, 5)	$I = -1\mu\text{A}$	●	$V_{CC}-1$			V

Three-State Inputs S1, S2, TOL

V_{IL}	Low Level Input Voltage		●			0.4	V
V_{IH}	High Level Input Voltage		●	1.4			V
V_Z	Pin Voltage when Left in Open State	$I = -10\mu\text{A}$	●	0.7			V
		$I = 0\mu\text{A}$			0.9		V
		$I = 10\mu\text{A}$	●			1.1	V
I_{VPG}	Programming Input Current (Note 6)		●			± 25	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The greater of V_1 , V_2 is the internal supply voltage (V_{CC}).

Note 3: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 4: For reset thresholds test conditions refer to the voltage threshold

programming table in the Applications Information section.

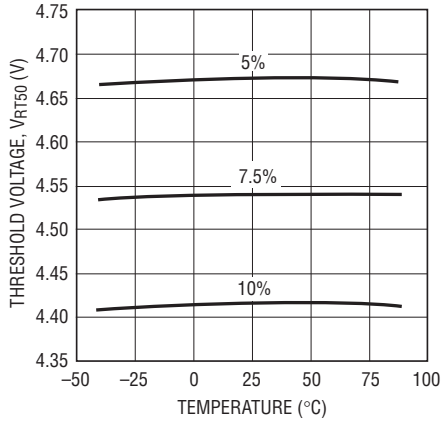
Note 5: The output pins $\overline{\text{RST}}$ and RST have an internal pull-up to V_{CC} of typically $-6\mu\text{A}$. However, an external pull-up resistor may be used when faster rise time is required or for V_{OH} voltages greater than V_{CC} .

Note 6: The input current to the three-state input pins are the pull-up and the pull-down current when the pins are either set to V_1 or GND respectively. In the open state, the maximum leakage current to V_1 or GND permissible is $10\mu\text{A}$.

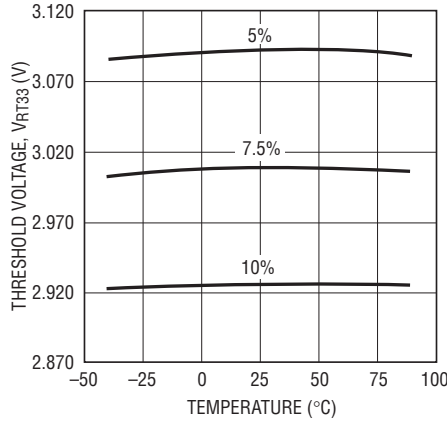
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

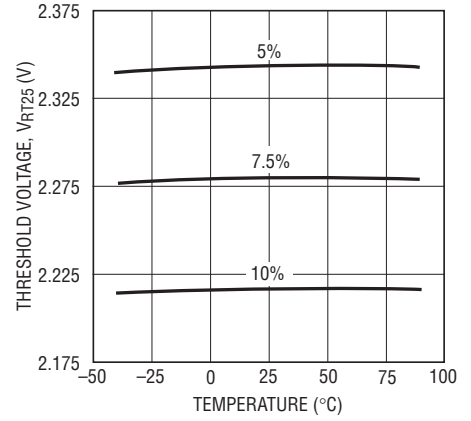
5V Threshold Voltage vs Temperature



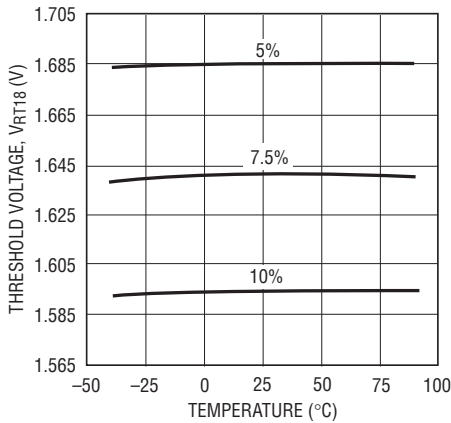
3.3V Threshold Voltage vs Temperature



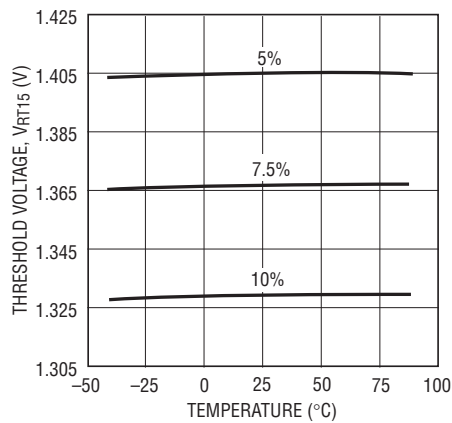
2.5V Threshold Voltage vs Temperature



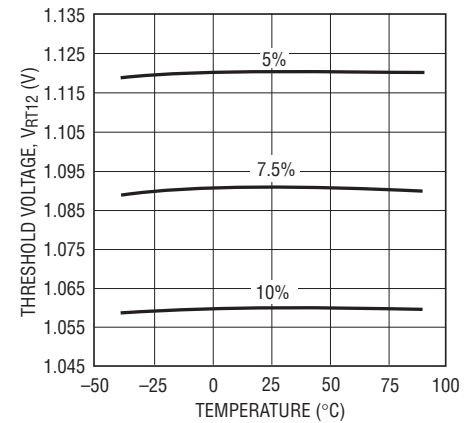
1.8V Threshold Voltage vs Temperature



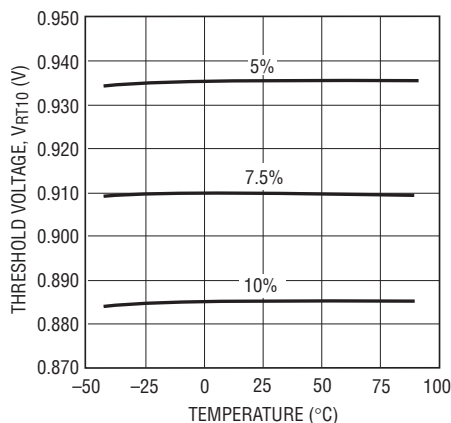
1.5V Threshold Voltage vs Temperature



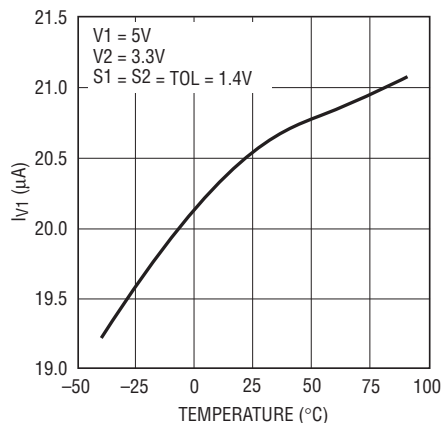
1.2V Threshold Voltage vs Temperature



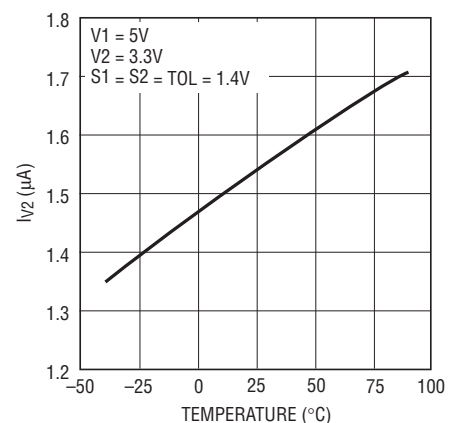
1V Threshold Voltage vs Temperature



I_{V1} vs Temperature



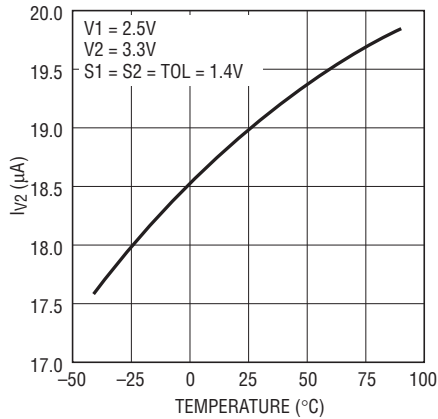
I_{V2} vs Temperature



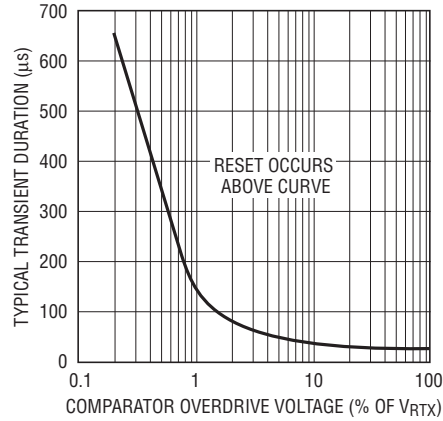
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

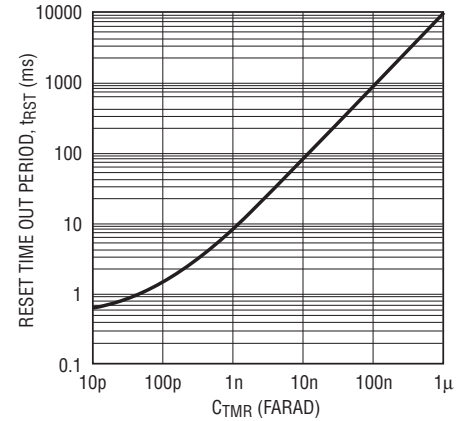
I_{V2} vs Temperature



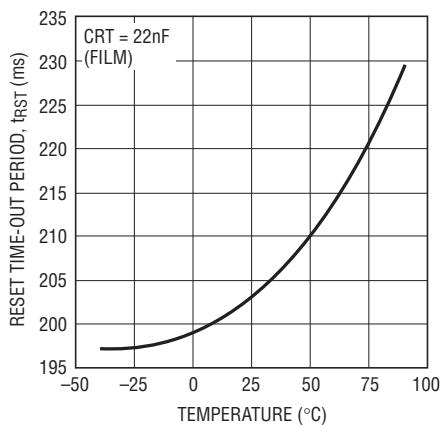
Typical Transient Duration vs Comparator Overdrive (V_1 , V_2)



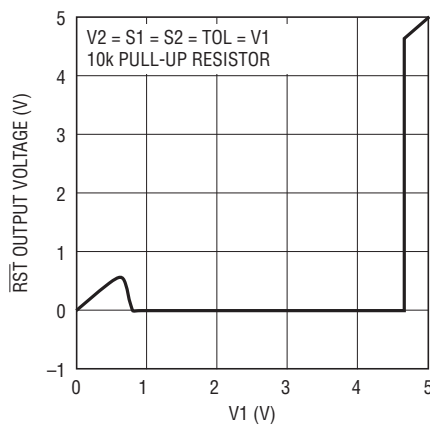
Reset Time Out Period (t_{RST}) vs Capacitance (C_{TMR})



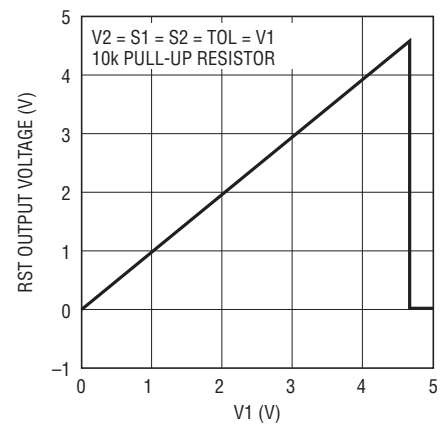
Reset Time-Out Period (t_{RST}) vs Temperature



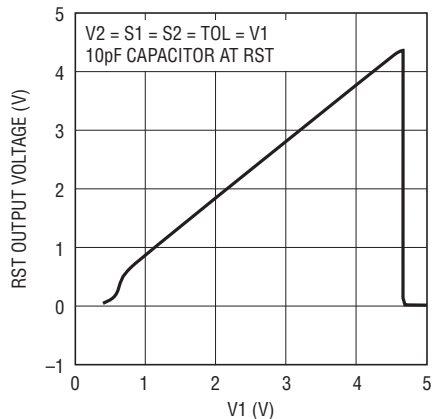
\overline{RST} Output Voltage vs V_1



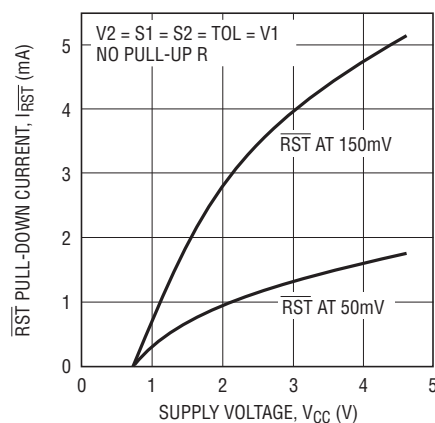
\overline{RST} Output Voltage vs V_1



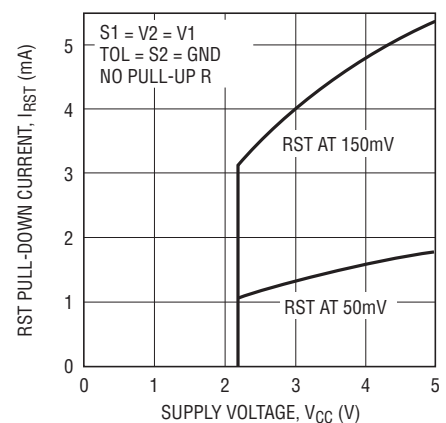
\overline{RST} Output Voltage vs V_1



\overline{RST} Pull-Down Current (I_{RST}) vs Supply Voltage (V_{CC})



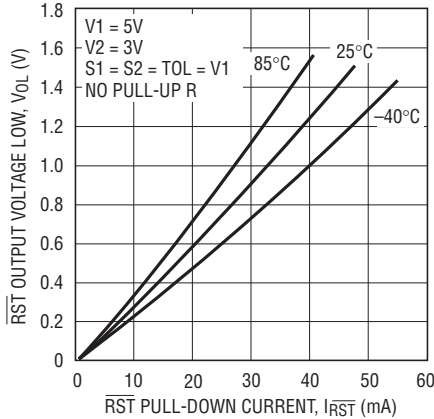
\overline{RST} Pull-Down Current (I_{RST}) vs Supply Voltage (V_{CC})



TYPICAL PERFORMANCE CHARACTERISTICS

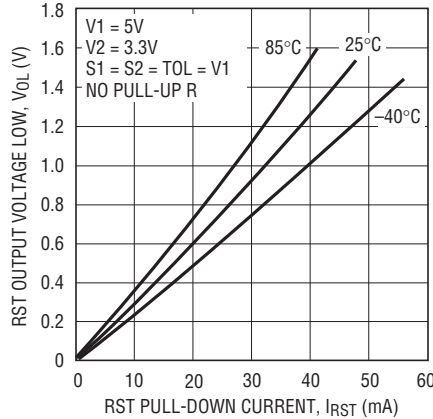
Specifications are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

RST Output Voltage Low (V_{OL}) vs RST Pull-Down Current (I_{RST})



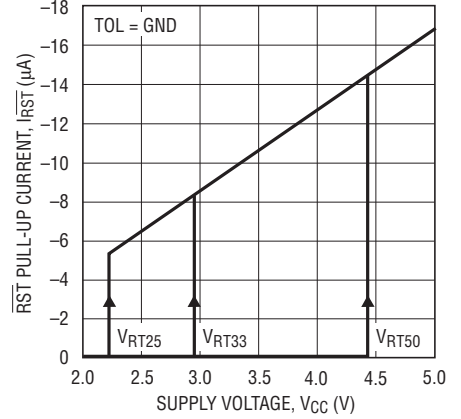
29045 G19

RST Output Voltage Low (V_{OL}) vs RST Pull-Down Current (I_{RST})



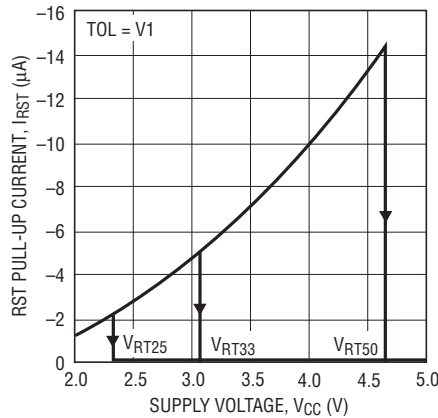
29045 G20

RST Pull-Up Current (I_{RST}) vs Supply Voltage (V_{CC})



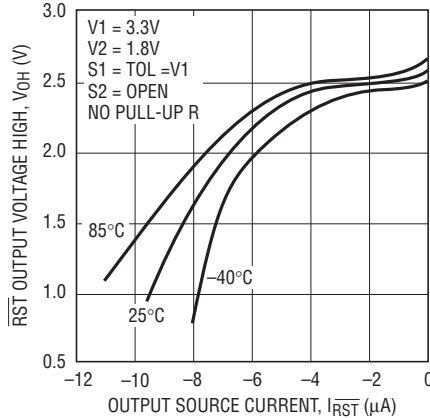
29045 G21

RST Pull-Up Current (I_{RST}) vs Supply Voltage (V_{CC})



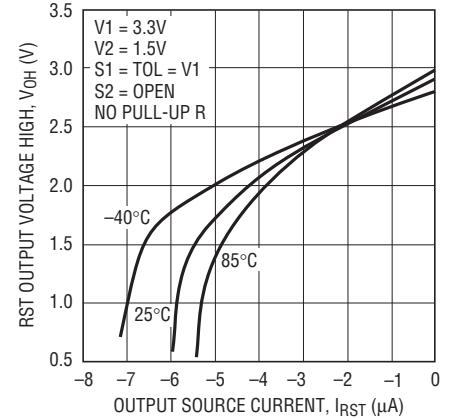
29045 G22

RST Output Voltage High (V_{OH}) vs RST Output Source Current (I_{RST})



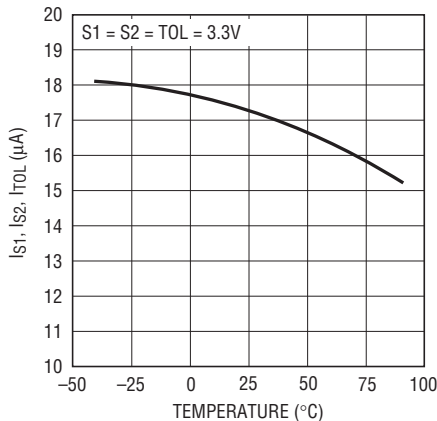
29045 G23

RST Output Voltage High (V_{OH}) vs RST Output Source Current (I_{RST})



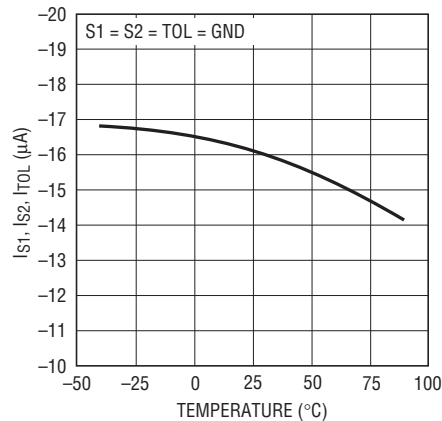
29045 G24

I_{S1} , I_{S2} , I_{TOL} vs Temperature



29045 G25

I_{S1} , I_{S2} , I_{TOL} vs Temperature



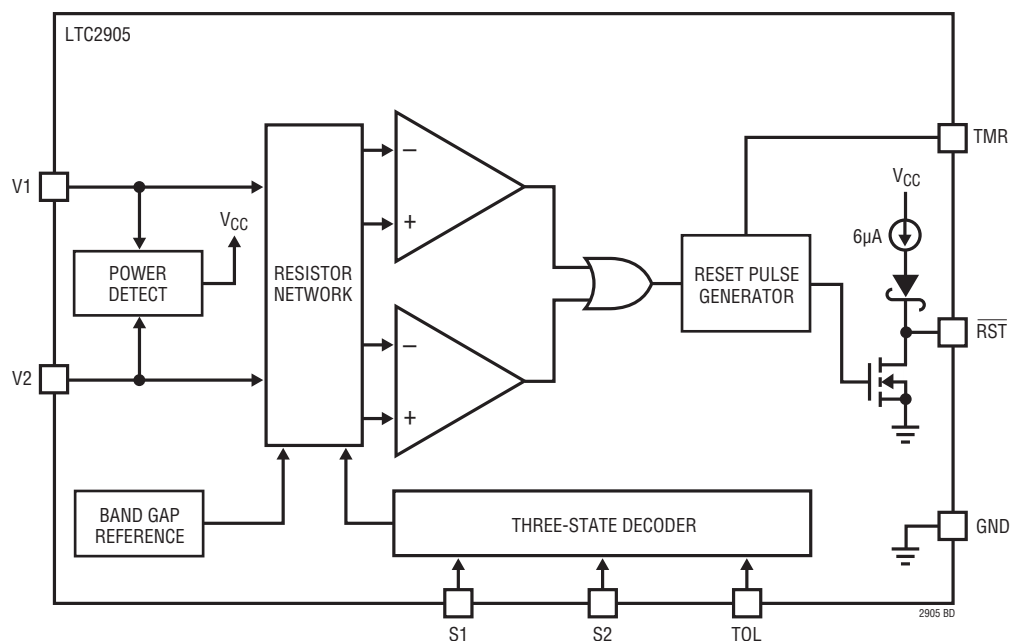
29045 G26

RST (Pin 3/Pin 2): Inverted Reset Logic Output. Pulls low when any voltage input is below the reset threshold and is held low for programmed delay time after all voltage inputs

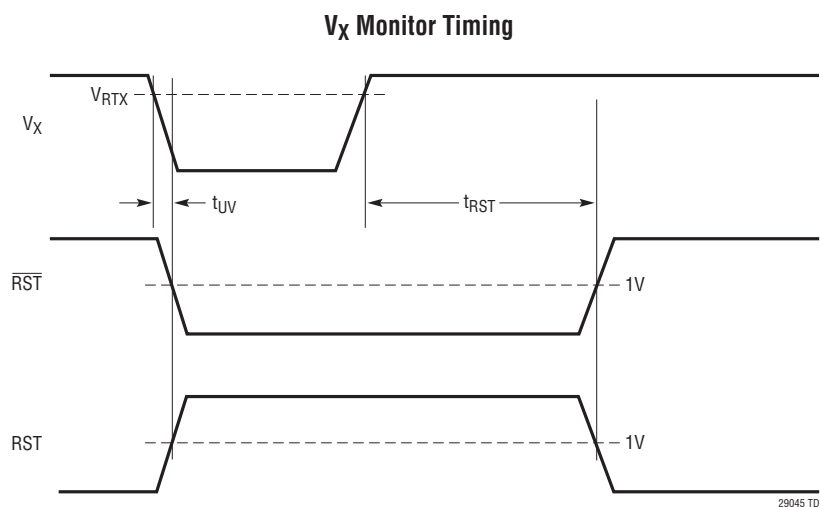
V1 (Pin 8/Pin 5): Voltage Input 1. Input for V1 monitor. Select from 5V, 3.3V, or 2.5V. See Table 1 for details. The greater of V1, V2 is also the internal supply voltage, V_{CC}. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

The schematic diagram illustrates the internal architecture of the LTC2904. It shows a resistor network connected to two comparators. The comparators' outputs are combined via an AND gate to trigger a 200ms reset pulse generator. This generator produces a reset pulse that is inverted and used to drive two NPN transistors, each in series with a 6µA current source, connected to the RST pins. A power detect block monitors the input voltages V1 and V2. A band gap reference provides a stable reference voltage to the resistor network. A three-state decoder, controlled by S1, S2, and TOL pins, manages the output bus, which is connected to the S1, S2, and TOL pins. The output bus is also connected to the RST pins and the GND pin.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Supply Monitoring

The LTC2904/LTC2905 are low power, high accuracy dual supply monitors with a common reset output and selectable thresholds. Reset delay is set to a nominal of 200ms for the LTC2904 and is adjustable using an external capacitor for the LTC2905.

The two 3-state input pins (S1 and S2) select one of nine possible threshold voltage combinations. Another three-state input pin sets the supply tolerance (5%, 7.5% or 10%). Both input voltages (V1 and V2) must be above predetermined thresholds for the reset not to be invoked. The LTC2904/LTC2905 assert the reset outputs during power-up, power-down and brownout conditions on either of the voltage inputs.

Power-Up

The greater of V1, V2 is the internal supply voltage (V_{CC}). V_{CC} powers the drive circuits for the \overline{RST} pin. Therefore as soon as V1 or V2 reaches 1V during power-up, the \overline{RST} output asserts low.

V_{CC} also powers the drive circuits for the RST pin in the LTC2904. Therefore, RST weakly pulls high when V1 or V2 reaches at least 1V.

Threshold programming is complete when V1 reaches at least 2.17V. After programming, if either V1 or V2 falls below its programmed threshold, \overline{RST} asserts low (RST weakly pulls high) as long as V_{CC} is at least 1V.

Once V1 and V2 rise above their thresholds, an internal timer is started. After the programmed delay time, \overline{RST} weakly pulls high (RST asserts low).

Power-Down

On power-down, once either V1 or V2 inputs drops below its threshold, \overline{RST} asserts logic low and RST weakly pulls high. V_{CC} of at least 1V guarantees a logic low of 0.4V at \overline{RST} .

Programming Pins

The three 3-state input pins: S1, S2 and TOL should be connected to GND, V1 or left unconnected during normal operation. Note that when left unconnected, the maximum

leakage current allowable from the pin to either GND or V1 is 10 μ A.

In margining applications, all the 3-state input pins can be driven using a tri-state buffer. Note however the low and high output of the tri-state buffer has to satisfy the V_{IL} and V_{IH} of the 3-state pin listed in the Electrical Characteristics Table. Moreover, when the tri-state buffer is in the high impedance state, the maximum leakage current allowed from the pin to either GND or V1 is 10 μ A.

Monitor Programming

Connecting S1 and S2 to GND, V1 or leaving them open selects the LTC2904/LTC2905 input voltage combinations. Table 1 shows the nine possible combinations of nominal input voltages and their corresponding S1, S2 connections.

Table 1. Voltage Threshold Programming

V1	V2	S1	S2
5.0	3.3	V1	V1
3.3	2.5	Open	GND
3.3	1.8	V1	Open
3.3	1.5	Open	V1
3.3	1.2	Open	Open
2.5	1.8	GND	GND
2.5	1.5	GND	Open
2.5	1.2	GND	V1
2.5	1.0	V1	GND

Note: Open = open circuit or driven by a three state buffer in high impedance state with leakage current less than 10 μ A.

Tolerance Programming

The three-state input pin, TOL programs the common supply tolerance for both V1 and V2 input voltages (5%, 7.5% or 10%). The larger the tolerance the lower the trip threshold. Table 2 shows the tolerances selection corresponding to a particular connection at the TOL pin.

Table 2. Tolerance Programming

Tolerance	TOL
5%	V1
7.5%	Open
10%	GND

APPLICATIONS INFORMATION

Threshold Accuracy

Reset threshold accuracy is of the utmost importance in a supply sensitive system. Ideally such a system should not reset while supply voltages are within a specified margin below the rated nominal level. Both of the LTC2904/LTC2905 inputs have the same relative threshold accuracy. The specification for LTC2904/LTC2905 is $\pm 1.5\%$ of the programmed nominal input voltage (over the full operating temperature range).

For example, when the LTC2904/LTC2905 are programmed to handle a 5V input with 10% tolerance ($S1 = S2 = V1$ and $TOL = GND$, refer to Table 1 and Table 2), it does not issue a reset command when V1 is above 4.5V. The typical 10% trip threshold is at 11.5% below the nominal input voltage level. Therefore, the typical trip threshold for the 5V input is 4.425V. With $\pm 1.5\%$ accuracy, the trip threshold range is $4.425V \pm 75mV$ over temperature (i.e. 10% to 13% below 5V). This implies that the monitored system must operate reliably down to 4.35V over temperature.

The same system using a supervisor with only $\pm 2.5\%$ accuracy needs to work reliably down to 4.25V ($4.375V \pm 125mV$) or 15% below 5V, requiring the monitored system to work over a much wider operating voltage range.

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage is near the reset threshold. A less desirable but common solution to this problem is to introduce hysteresis around the nominal threshold. Notice however, this hysteresis introduces an error term in the threshold accuracy. Therefore, a $\pm 2.5\%$ accurate monitor with $\pm 1.0\%$ hysteresis is equivalent to a $\pm 3.5\%$ monitor with no hysteresis.

The LTC2904/LTC2905 takes a different approach to solve this problem of supply noise causing spurious reset. The first line of defense against this spurious reset is a first order low pass filter at the output of the comparator. Thus, the comparator output goes through a form of integration before triggering the output logic. Therefore, any kind of

transient at the input of the comparator needs to be of sufficient magnitude and duration before it can trigger a change in the output logic.

The second line of defense is the programmed delay time t_{RST} (200ms for LTC2904 and using an external capacitor for LTC2905). This delay will eliminate the effect of any supply noise whose frequency is above $1/t_{RST}$ on the \overline{RST} and RST output.

When either V1 or V2 drops below its programmed threshold, the \overline{RST} pin asserts low (RST weakly pulls high). Then when the supply recovers above the programmed threshold, the reset-pulse-generator timer starts counting.

If the supply remains above the programmed threshold when the timer finishes counting, the \overline{RST} pin weakly pulls high (RST asserts low). However, if the supply falls below the programmed threshold any time during the period when the timer is still counting, the timer resets and it starts fresh when the supply next rises above the programmed threshold.

Note that this second line of defense is only effective for a rising supply and does not affect the sensitivity of the system to a falling supply. Therefore, the first line of defense that works for both cases of rising and falling is necessary. These two approaches prevent spurious reset caused by supply noise without sacrificing the threshold accuracy.

Selecting the Reset Timing Capacitor

The reset time-out period for LTC2905 is adjustable in order to accommodate a variety of microprocessor applications. Connecting a capacitor, C_{TMR} , between the TMR pin and ground sets the reset time-out period, t_{RST} . The following formula determines the value of capacitor needed for a particular reset time-out period:

$$C_{TMR} = t_{RST} \cdot 110 \cdot 10^{-9} [F/s]$$

For example, using a standard capacitor value of 22nF would give a $22000/110 = 200ms$ delay.

APPLICATIONS INFORMATION

Figure 1 shows the desired delay time as a function of the value of the timer capacitor that should be used:

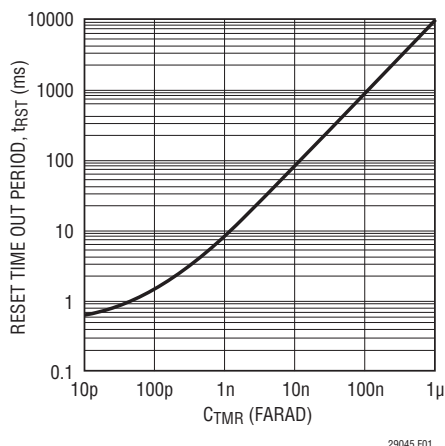


Figure 1. Reset Time-Out Period vs Capacitance

Leaving the TMR pin open with no external capacitor generates a reset time-out of approximately 200μs. For long reset time-out, the only limitation is the availability of large value capacitor with low leakage. The TMR capacitor will never charge if the leakage current exceeds the minimum TMR charging current of 2.1μA (typical).

RST and $\overline{\text{RST}}$ Output Characteristics

The DC characteristics of the RST and $\overline{\text{RST}}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics section. Both RST and $\overline{\text{RST}}$ have a weak internal pull-up to $V_{CC} = \text{Max}(V1, V2)$ and a strong pull-down to ground.

The weak pull-up and strong pull-down arrangement allow these two pins to have open-drain behavior while possessing several other beneficial characteristics.

The weak pull-ups eliminate the need for external pull-up resistors when the rise time on these pins is not critical. On the other hand, the open-drain $\overline{\text{RST}}$ configuration allows for wired-OR connections and can be useful when more than one signal needs to pull down on the $\overline{\text{RST}}$ line.

As noted in the Power-Up and Power-Down sections the circuits that drive RST and $\overline{\text{RST}}$ are powered by V_{CC} . During fault condition, V_{CC} of at least 1V guarantees a maximum $V_{OL} = 0.4V$ at $\overline{\text{RST}}$. However, at $V_{CC} = 1V$ the weak pull-up current on RST is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the RST pin if the state and pull-up strength of the RST pin is crucial at very low V_{CC} .

Note however, by adding an external pull-up resistor, the pull-up strength on the RST pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device needs to accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The RST and $\overline{\text{RST}}$ outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \cdot R_{PD} \cdot C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor estimated to be typically 40Ω at room temperature (25°C) and C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is about 13ns.

The rise time, on the RST and $\overline{\text{RST}}$ pins is limited by weak internal pull-up current sources to V_{CC} . The following formula estimates the output rise time (10% to 90%) at the RST and $\overline{\text{RST}}$ pins:

$$t_{RISE} \approx 2.2 \cdot R_{PU} \cdot C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. Notice that this pull-up transistor is modeled as a 6μA current source in the Block Diagram as a typical representation.

APPLICATIONS INFORMATION

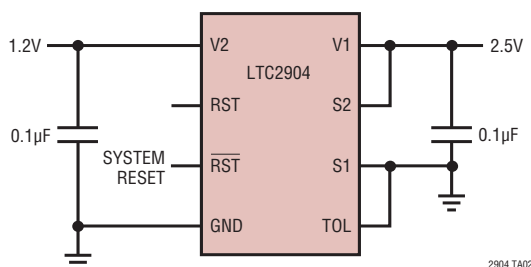
The on-resistance as a function of the $V_{CC} = \text{Max}(V1, V2)$ voltage (for $V_{CC} > 1V$) at room temperature is estimated as follows:

$$R_{PU} = \frac{6 \cdot 10^5}{\text{MAX}(V1, V2) - 1V} \Omega$$

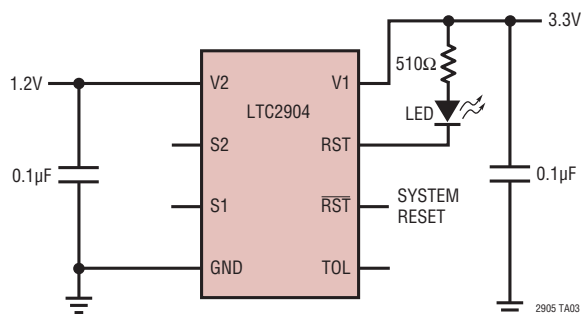
At $V_{CC} = 3.3V$, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86μs. An external pull-up resistor may be used if the output needs to pull up faster and/or to a higher voltage, for example: the rise time reduces to 3.3μs for a 150pF load capacitance, when using a 10k pull-up resistor.

TYPICAL APPLICATIONS

2.5V, 1.2V Supply Monitor, 10% Tolerance

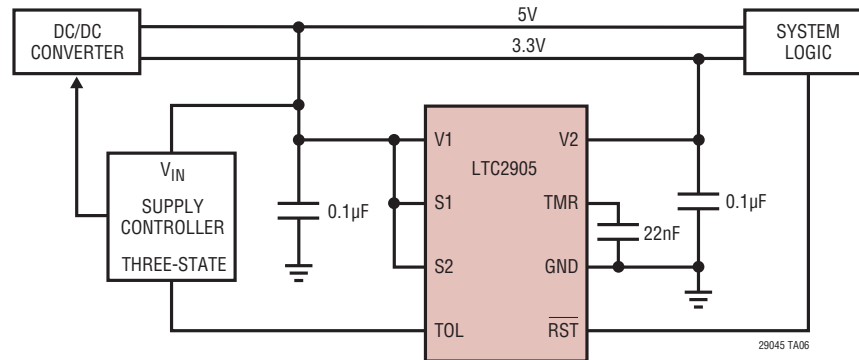


3.3V, 1.2V Dual Supply Monitor with LED Power Good Indicator, 7.5% Tolerance and Adjustable Timer

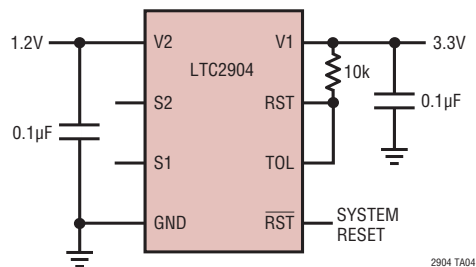


TYPICAL APPLICATIONS

5V, 3.3V Dual Supply Monitor with Voltage Margining for Automated On-Board Testing

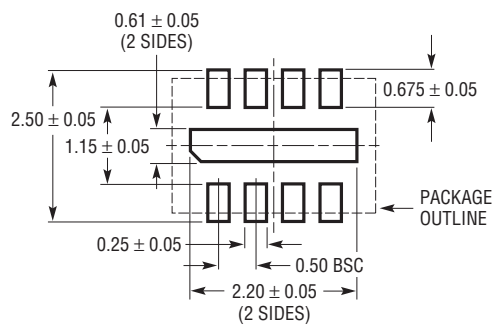


3.3V, 1.2V Dual Supply Monitor with Asymmetric Hysteresis, 5% Tolerance (Supplies Rising), 10% Tolerance (After RST Goes Low)

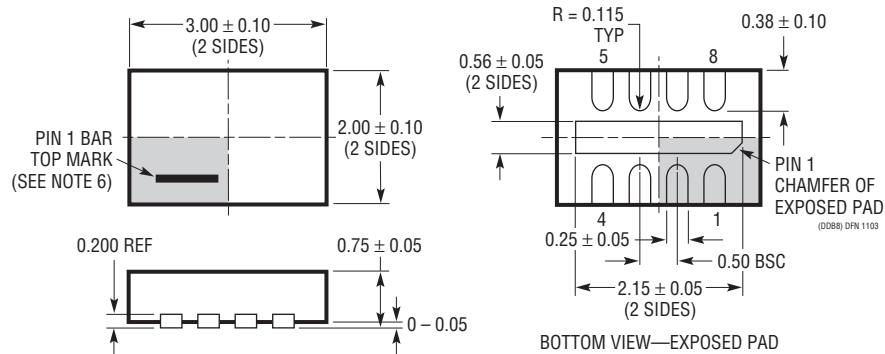


PACKAGE DESCRIPTION

DDB Package 8-Lead Plastic DFN (3mm × 2mm) (Reference LTC DWG # 05-08-1702)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

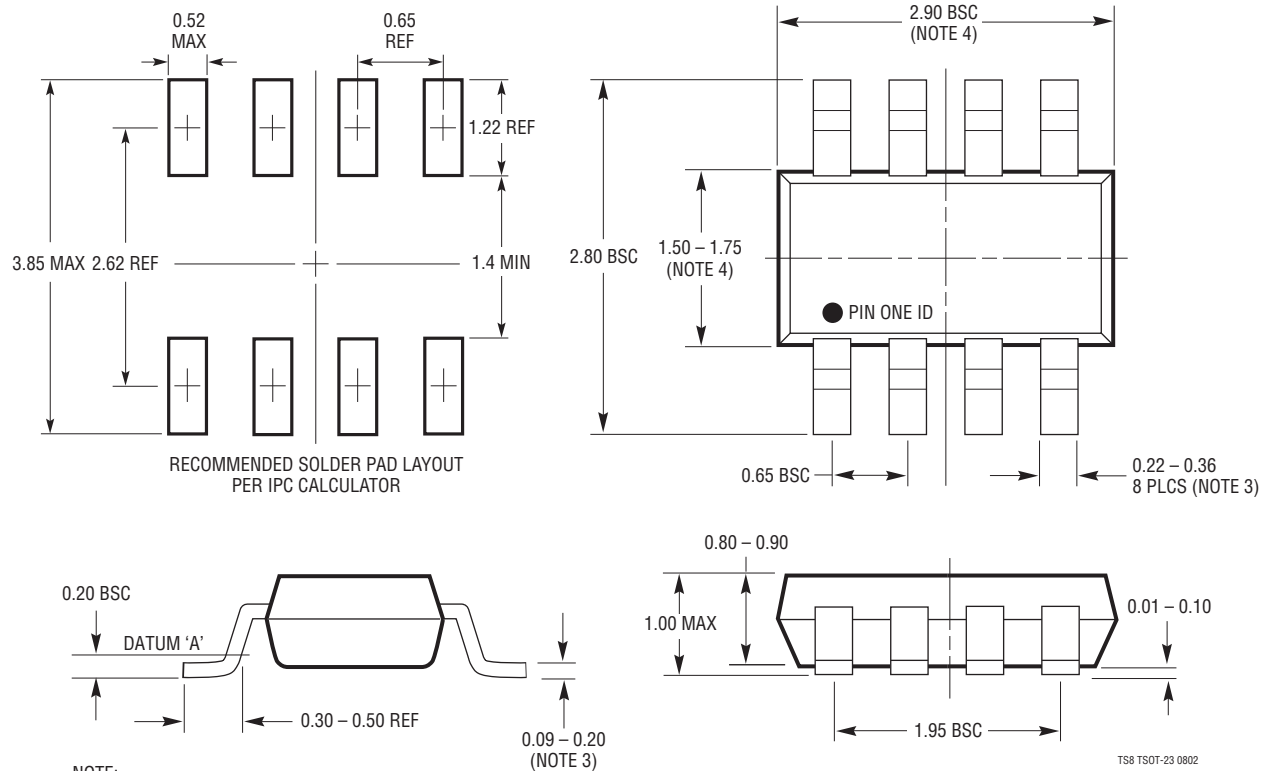


NOTE:

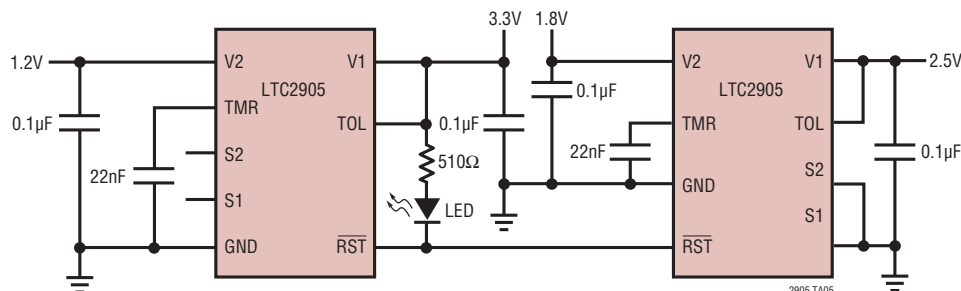
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1637)



TYPICAL APPLICATION

3.3V, 1.2V Dual Supply Monitor with LED Power Good Indicator,
7.5% Tolerance and Adjustable Timer

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65V Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65V Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Push-Button Reset	4.37V/4.62V Threshold
LTC1326/LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold ($\pm 0.75\%$)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1726-2.5/LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable $\overline{\text{RESET}}$ and Watchdog Time-Outs
LTC1727-2.5/LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$, 10-Lead MSOP, DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable $\overline{\text{RESET}}$ and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Selectable Tolerance, $\overline{\text{RESET}}$ Disable for Margining Functions, 16-Lead SSOP Package
LTC2903-1	Precision Quad Supply Monitor	Ultra Low Voltage $\overline{\text{RESET}}$, 6-Lead SOT-23 Package
LTC2906	Dual Supply Monitor with One Pin-Selectable Threshold and One Adjustable Input	0.5V Adjustable Threshold and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages
LTC2907	Dual Supply Monitor with One Pin-Selectable Threshold and One Adjustable Input	0.5V Adjustable Threshold, Adjustable $\overline{\text{RESET}}$ Timer and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages
LTC2908	Precision Six Supply Monitors	Ultra Low Voltage $\overline{\text{RESET}}$, 8-Lead SOT-23 and DFN Packages