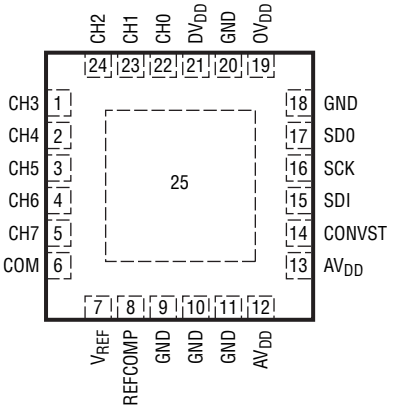
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (AV_{DD}, DV_{DD}, OV_{DD}) 6V
Analog Input Voltage (Note 3)
CH0-CH7, COM, REF,
REFCOMP .....(GND – 0.3V) to (AV_{DD} + 0.3V)
Digital Input Voltage
(Note 3)..... (GND – 0.3V) to (DV_{DD} + 0.3V)
Digital Output Voltage.... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2308C ..... 0°C to 70°C
LTC2308I .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2308#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2308CUF#PBF	LTC2308CUF#TRPBF	2308	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC2308IUF#PBF	LTC2308IUF#TRPBF	2308	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 6)	●		±0.3	±1	LSB
Differential Linearity Error		●		±0.25	±1	LSB
Bipolar Zero Error	(Note 7)	●		±1	±6	LSB
Bipolar Zero Error Drift				0.002		LSB/°C
Bipolar Zero Error Match		●		±0.3	±3	LSB
Unipolar Zero Error	(Note 7)	●		±0.5	±3	LSB
Unipolar Zero Error Drift				0.002		LSB/°C
Unipolar Zero Error Match		●		±0.3	±2	LSB

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bipolar Full-Scale Error	External Reference (Note 8)	●		±1	±9	LSB
Bipolar Full-Scale Error Drift	External Reference			0.05		LSB/°C
Bipolar Full-Scale Error Match		●		±0.5	±3	LSB
Unipolar Full-Scale Error	External Reference (Note 8)	●		±1.5	±8	LSB
Unipolar Full-Scale Error Drift	External Reference			0.05		LSB/°C
Unipolar Full-Scale Error Match		●		±0.4	±3	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (CH0 to CH7)	(Note 9)	●	–0.05		REFCOMP	V
V_{IN}^-	Absolute Input Range (CH0 to CH7, COM)	Unipolar (Note 9) Bipolar (Note 9)	● ●	–0.05 –0.05		0.25 • REFCOMP 0.75 • REFCOMP	V V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ – V_{IN}^-$ (Unipolar) $V_{IN} = V_{IN}^+ – V_{IN}^-$ (Bipolar)	● ●		0 to REFCOMP ±REFCOMP/2		V V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			55 5		pF pF
CMRR	Input Common Mode Rejection Ratio				70		dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1kHz	●	71	73.3		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1kHz	●	71	73.4		dB
THD	Total Harmonic Distortion	f_{IN} = 1kHz, First 5 Harmonics	●		–90	–78	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1kHz	●	80	90		dB
	Channel-to-Channel Isolation	f_{IN} = 1kHz			–109		dB
	Full Linear Bandwidth	(Note 11)			700		kHz
	–3dB Input Linear Bandwidth				25		MHz
	Aperture Delay				13		ns
	Transient Reponse	Full-Scale Step			240		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	●	2.47	2.50	2.53	V
V_{REF} Output Tempco	I_{OUT} = 0			±25		ppm/°C
V_{REF} Output Impedance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			8		kΩ
$V_{REFCOMP}$ Output Voltage	I_{OUT} = 0			4.096		V
V_{REF} Line Regulation	AV_{DD} = 4.75V to 5.25V			0.8		mV/V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	DV_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	DV_{DD} = 4.75V	●			0.8	V
I_{IN}	High Level Input Current	V_{IN} = V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	OV_{DD} = 4.75V, I_{OUT} = –10µA OV_{DD} = 4.75V, I_{OUT} = –200µA	 ●	 4	4.74		V V
V_{OL}	Low Level Input Voltage	OV_{DD} = 4.75V, I_{OUT} = 160µA OV_{DD} = 4.75V, I_{OUT} = 1.6mA	 ●		0.05	 0.4	V V
I_{OZ}	Hi-Z Output Leakage	V_{OUT} = 0V to OV_{DD}, CONVST High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance	CONVST High			15		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AV_{DD}	Analog Supply Voltage			4.75	5	5.25	V
DV_{DD}	Digital Supply Voltage			4.75	5	5.25	V
OV_{DD}	Output Driver Supply Voltage			2.7		5.25	V
I_{DD}	Supply Current Nap Mode Sleep Mode	C_L = 25pF CONVST = 5V, Conversion Done CONVST = 5V, Conversion Done	● ● ●		3.5 180 7	4.2 400 20	mA µA µA
P_D	Power Dissipation Nap Mode Sleep Mode				17.5 0.9 35		mW mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●			500	kHz
f_{SCK}	Shift Clock Frequency		●			40	MHz
t_{WHCONV}	CONVST High Time	(Note 9)	●	20			ns
t_{HD}	Hold Time SDI After SCK↑		●	2.5			ns
t_{SUDI}	Setup Time SDI Valid Before SCK↑		●	0			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$	●	10			ns
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$	●	10			ns
$t_{WLCONVST}$	CONVST Low Time During Data Transfer	(Note 9)	●	410			ns
$t_{HCONVST}$	Hold Time CONVST Low After Last SCK↓	(Note 9)	●	20			ns
t_{CONV}	Conversion Time		●		1.3	1.6	µs
t_{ACQ}	Acquisition Time	7th SCK↑ to CONVST↑ (Note 9)	●	240			ns
$t_{REFWAKE}$	REFCOMP Wakeup Time (Note 12)	$C_{REFCOMP}$ = 10µF, C_{REF} = 2.2µF			200		ms
t_{dDO}	SDO Data Valid After SCK↓	C_L = 25pF (Note 9)	●		10.8	12.5	ns
t_{hDO}	SDO Hold Time After SCK↓	C_L = 25pF	●	4			ns
t_{en}	SDO Valid After CONVST↓	C_L = 25pF	●		11	15	ns
t_{dis}	Bus Relinquish Time	C_L = 25pF	●		11	15	ns
t_r	SDO Rise Time	C_L = 25pF			4		ns
t_f	SDO Fall Time	C_L = 25pF			4		ns
t_{CYC}	Total Cycle Time				2		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with AV_{DD}, DV_{DD} and OV_{DD} wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. These products can handle input currents greater than 100mA below ground or above V_{DD} without latchup.

Note 4: AV_{DD} = 5V, DV_{DD} = 5V, OV_{DD} = 5V, f_{SMPL} = 500kHz, internal reference unless otherwise specified.

Note 5: Linearity, offset and full-scale specifications apply for a single-ended analog input with respect to COM.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. Unipolar zero error is the offset voltage measured from +0.5LSB when the output code flickers between 0000 0000 0000 and 0000 0000 0001.

Note 8: Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error.

Note 9: Guaranteed by design, not subject to test.

Note 10: All specifications in dB are referred to a full-scale ±2.048V input with a 2.5V reference voltage.

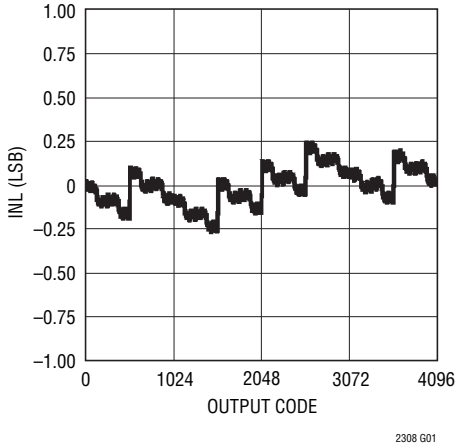
Note 11: Full linear bandwidth is defined as the full-scale input frequency at which the SINAD degrades to 60dB or 10 bits of accuracy.

Note 12: REFCOMP wakeup time is the time required for the REFCOMP pin to settle within 0.5LSB at 12-bit resolution of its final value after waking up from SLEEP mode.

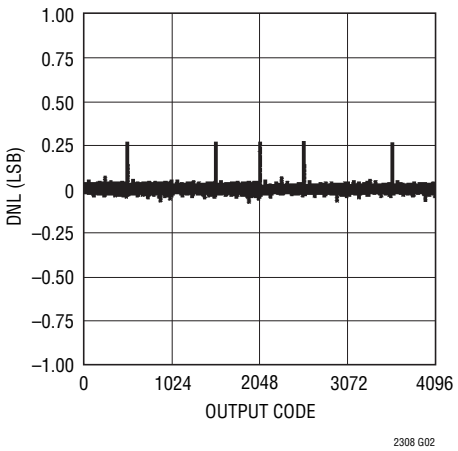
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AV_{DD} = DV_{DD} = OV_{DD} = 5V, f_{SMPL} = 500ksps, Internal Reference, unless otherwise noted.

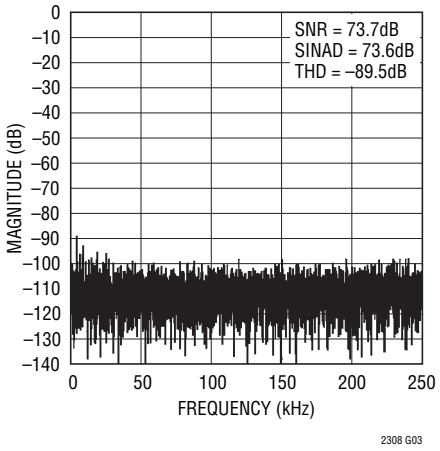
Integral Nonlinearity vs Output Code



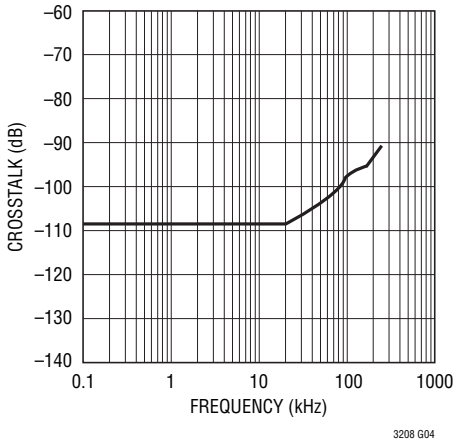
Differential Nonlinearity vs Output Code



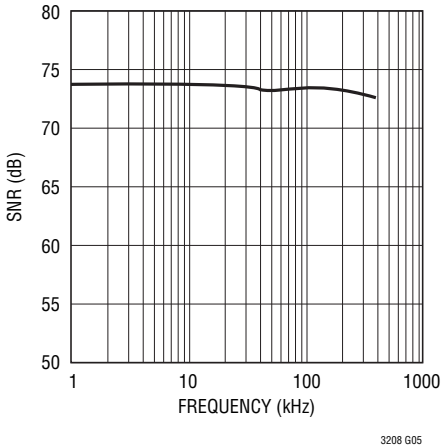
1kHz Sine Wave 8192 Point FFT Plot



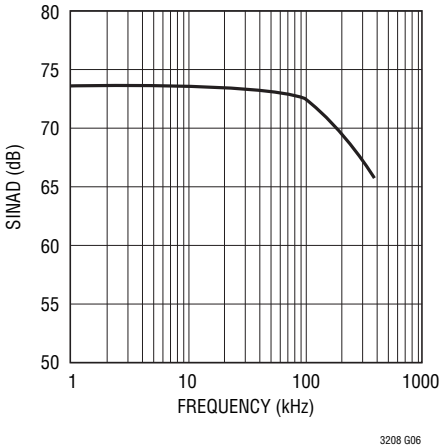
Crosstalk vs Frequency for an Adjacent Pair



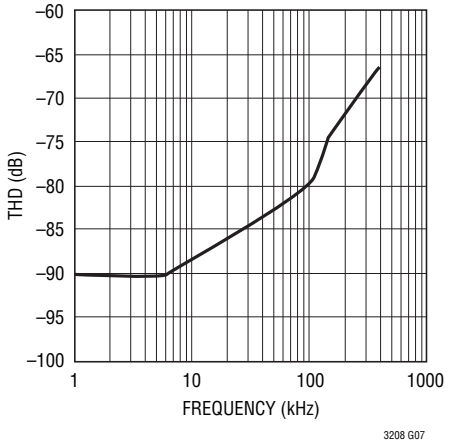
SNR vs Input Frequency



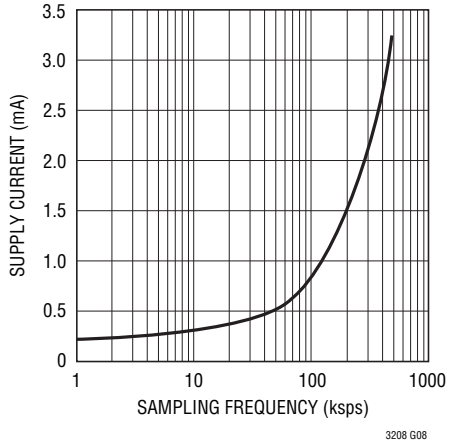
SINAD vs Input Frequency



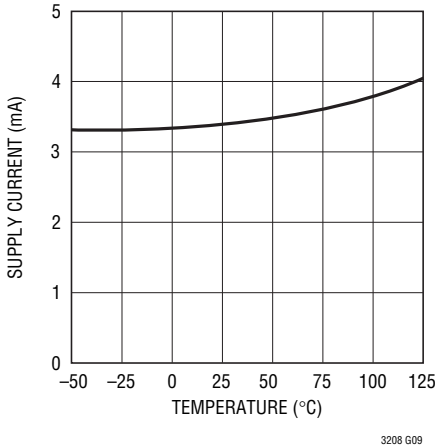
THD vs Input Frequency



Supply Current vs Sampling Frequency



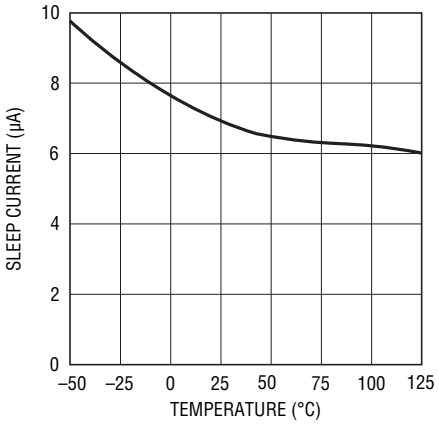
Supply Current vs Temperature



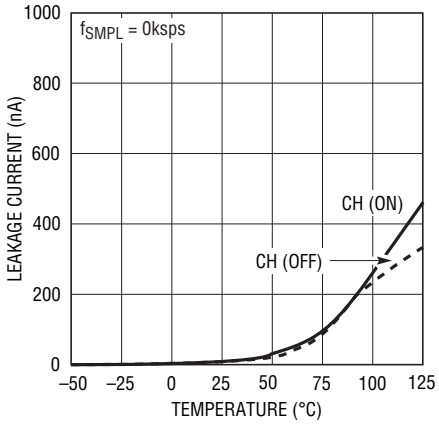
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AV_{DD} = DV_{DD} = OV_{DD} = 5V, f_{SMPL} = 500ksps, Internal Reference, unless otherwise noted.

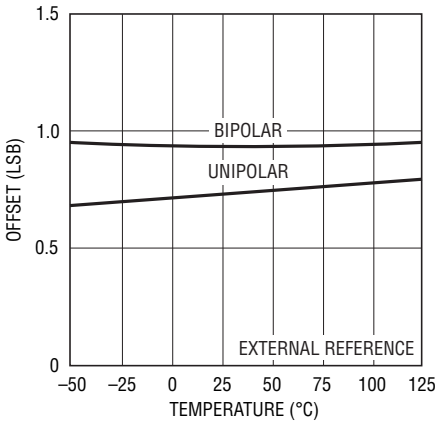
Sleep Current vs Temperature



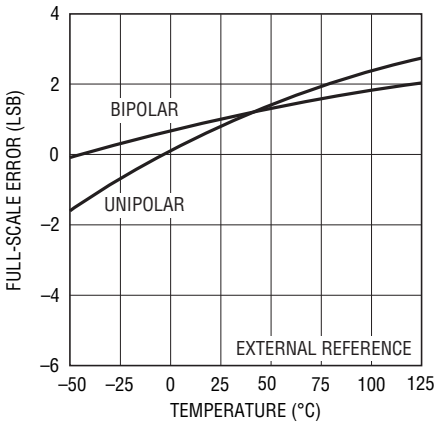
Analog Input Leakage Current vs Temperature



Offset vs Temperature



Full-Scale Error vs Temperature



PIN FUNCTIONS

CH3-CH7 (Pins 1, 2, 3, 4, 5): Channel 3 to Channel 7 Analog Inputs. CH3-CH7 can be configured as single-ended or differential input channels. See the Analog Input Multiplexer section.

COM (Pin 6): Common Input. This is the reference point for all single-ended inputs. It must be free of noise and connected to ground for unipolar conversions and midway between GND and REFCOMP for bipolar conversions.

V_{REF} (Pin 7): 2.5V Reference Output. Bypass to GND with a minimum 2.2µF tantalum capacitor or low ESR ceramic capacitor. The internal reference may be over driven by an external 2.5V reference at this pin.

REFCOMP (Pin 8): Reference Buffer Output. Bypass to GND with a 10µF tantalum and 0.1µF ceramic capacitor in parallel. Nominal output voltage is 4.096V. The internal reference buffer driving this pin is disabled by grounding V_{REF}, allowing REFCOMP to be overdriven by an external source (see Figure 6c).

GND (Pins 9, 10, 11, 18, 20): Ground. All GND pins must be connected to a solid ground plane.

AV_{DD} (Pins 12, 13): 5V Analog Supply. The range of AV_{DD} is 4.75V to 5.25V. Bypass AV_{DD} to GND with a 0.1µF ceramic and a 10µF tantalum capacitor in parallel.

CONVST (Pin 14): Conversion Start. A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends.

SDI (Pin 15): Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses.

SCK (Pin 16): Serial Data Clock. SCK synchronizes the serial data transfer. The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK.

SDO (Pin 17): Serial Data Out. SDO outputs the data from the previous conversion. SDO is shifted out serially on the falling edge of each SCK pulse.

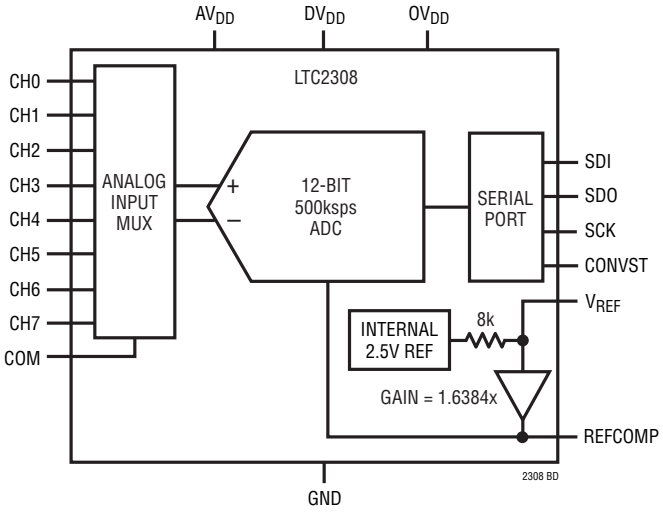
OV_{DD} (Pin 19): Output Driver Supply. Bypass OV_{DD} to GND with a 0.1µF ceramic capacitor close to the pin. The range of OV_{DD} is 2.7V to 5.25V.

DV_{DD} (Pin 21): 5V Digital Supply. The range of DV_{DD} is 4.75V to 5.25V. Bypass DV_{DD} to GND with a 0.1 µF ceramic and a 10µF tantalum capacitor in parallel.

CH0-CH2 (Pins 22, 23, 24): Channel 0 to Channel 2 Analog Inputs. CH0-CH2 can be configured as single-ended or differential input channels. See the Analog Input Multiplexer section.

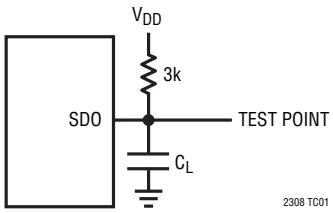
GND (Pin 25): Exposed Pad Ground. Must be soldered directly to ground plane.

BLOCK DIAGRAM

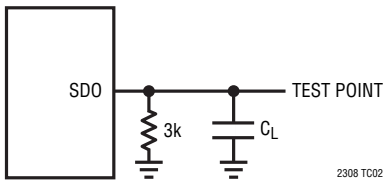


TEST CIRCUIT

Load Circuit for t_{dis} WAVEFORM 1

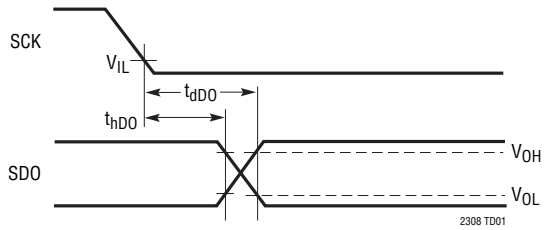


Load Circuit for t_{dis} WAVEFORM 2, t_{en}

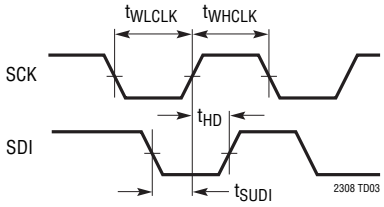


TIMING DIAGRAM

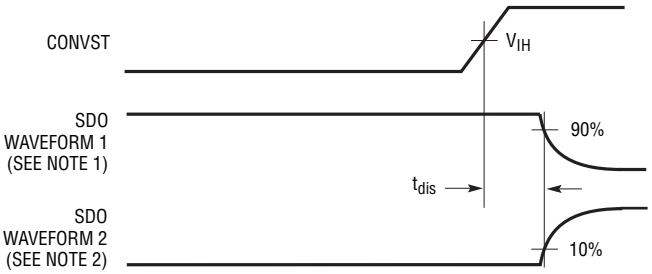
Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



t_{WLCLK} (SCK Low Time)
t_{WHCLK} (SCK High Time)
t_{HD} (Hold Time SDI After SCK↑)
t_{SUDI} (Setup Time SDI Stable Before SCK↑)



Voltage Waveforms for t_{dis}

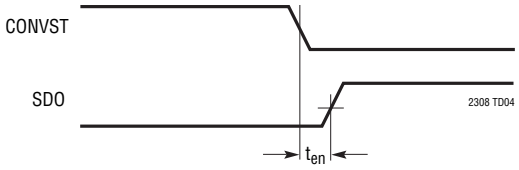


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

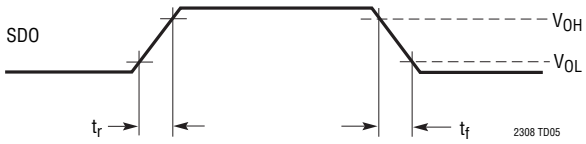
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

2308 TD02

Voltage Waveforms for t_{en}



Voltage Waveforms for SDO Rise and Fall Times t_r, t_f



APPLICATIONS INFORMATION

Overview

The LTC2308 is a low noise, 500ksps, 8-channel, 12-bit successive approximation register (SAR) A/D converter. The LTC2308 includes a precision internal reference, a configurable 8-channel analog input multiplexer (MUX) and an SPI-compatible serial port for easy data transfers. The ADC may be configured to accept single-ended or differential signals and can operate in either unipolar or bipolar mode. A sleep mode option is also provided to save power during inactive periods.

Conversions are initiated by a rising edge on the CONVST input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, a 6-bit input word (D_{IN}) at the SDI input configures the MUX and programs various modes of operation. As the D_{IN} bits are shifted in, data from the previous conversion is shifted out on SDO. After the 6 bits of the D_{IN} word have been shifted in, the ADC begins acquiring the analog input in preparation for the next conversion as the rest of the data is shifted out. The acquire phase requires a minimum time of 240ns for the sample-and-hold capacitors to acquire the analog input signal.

During the conversion, the internal 12-bit capacitive charge-redistribution DAC output is sequenced through a successive approximation algorithm by the SAR starting from the most significant bit (MSB) to the least significant bit (LSB). The sampled input is successively compared with binary weighted charges supplied by the capacitive DAC using a differential comparator. At the end of a conversion, the DAC output balances the analog input. The SAR contents (a 12-bit data word) that represent the sampled analog input are loaded into 12 output latches that allow the data to be shifted out.

Programming the LTC2308

The various modes of operation of the LTC2308 are programmed by a 6-bit D_{IN} word. The SDI data bits are loaded on the rising edge of SCK, with the S/D bit loaded on the first rising edge and the SLP bit on the sixth rising edge (see Figure 8 in the Timing and Control section). The input data word is defined as follows:

S/D	O/S	S1	S0	UNI	SLP

S/D = SINGLE-ENDED/$\overline{\text{DIFFERENTIAL}}$ BIT

O/S = ODD/$\overline{\text{SIGN}}$ BIT

S1 = ADDRESS SELECT BIT 1

S0 = ADDRESS SELECT BIT 0

UNI = UNIPOLAR/$\overline{\text{BIPOLAR}}$ BIT

SLP = SLEEP MODE BIT

Analog Input Multiplexer

The analog input MUX is programmed by the S/D, O/S, S1 and S0 bits of the D_{IN} word. Table 1 lists the MUX configurations for all combinations of the configuration bits. Figure 1a shows several possible MUX configurations and Figure 1b shows how the MUX can be reconfigured from one conversion to the next.

Table 1. Channel Configuration

S/D	O/S	S1	S0	0	1	2	3	4	5	6	7	COM
0	0	0	0	+	–							
0	0	0	1			+	–					
0	0	1	0					+	–			
0	0	1	1							+	–	
0	1	0	0	–	+							
0	1	0	1			–	+					
0	1	1	0					–	+			
0	1	1	1							–	+	
1	0	0	0	+								–
1	0	0	1			+						–
1	0	1	0					+				–
1	0	1	1							+		–
1	1	0	0		+							–
1	1	0	1				+					–
1	1	1	0						+			–
1	1	1	1								+	–

APPLICATIONS INFORMATION

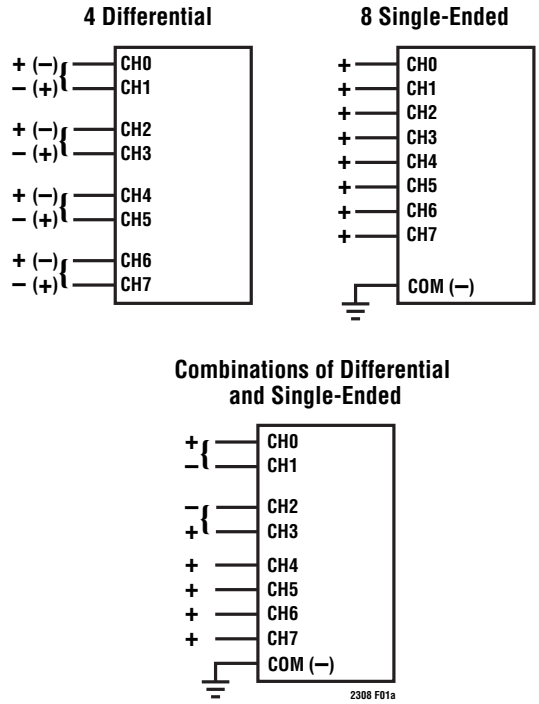


Figure 1a. Example MUX Configurations

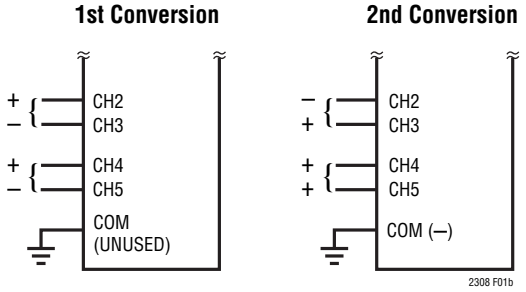


Figure 1b. Changing the MUX Assignment "On the Fly"

Driving the Analog Inputs

The analog inputs of the LTC2308 are easy to drive. Each of the analog inputs can be used as a single-ended input relative to the COM pin (CH0-COM, CH1-COM, etc.) or in differential input pairs (CH0 and CH1, CH2 and CH3, CH4 and CH5, CH6 and CH7). Figure 2 shows how to drive COM for single-ended inputs in unipolar and bipolar modes. Regardless of the MUX configuration, the "+" and "–" inputs are sampled at the same instant. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors during the acquire

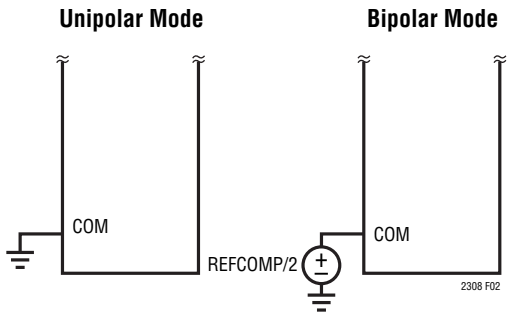


Figure 2. Driving COM in UNIPOLAR and BIPOLAR Modes

mode. In conversion mode, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, the ADC inputs can be driven directly. Otherwise, more acquisition time should be allowed for a source with higher impedance.

Input Filtering

The noise and distortion of the input amplifier and other circuitry must be considered since they will add to the ADC noise and distortion. Therefore, noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

The analog inputs of the LTC2308 can be modeled as a 55pF capacitor (C_{IN}) in series with a 100Ω resistor (R_{ON}) as shown in Figure 3a. C_{IN} gets switched to the selected input once during each conversion. Large filter RC time constants will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to 12-bit resolution within the acquisition time (t_{ACQ}) if DC accuracy is important.

When using a filter with a large C_{FILTER} value (e.g. 1µF), the inputs do not completely settle and the capacitive input switching currents are averaged into a net DC current (I_{DC}). In this case, the analog input can be modeled by an equivalent resistance ($R_{EQ} = 1/(f_{SMPL} \bullet C_{IN})$) in series with an ideal voltage source ($V_{REFCOMP}/2$) as shown in Figure 3b. The magnitude of the DC current is then approximately $I_{DC} = (V_{IN} – V_{REFCOMP}/2)/R_{EQ}$, which is roughly proportional to V_{IN}. To prevent large DC drops across the resistor R_{FILTER}, a filter with a small resistor and large capacitor should be chosen. When running at the minimum cycle time of 2µs, the input current equals 106µA at V_{IN} = 5V,

APPLICATIONS INFORMATION

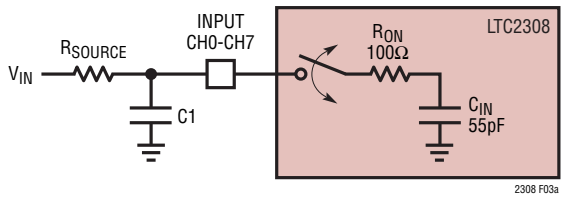


Figure 3a. Analog Input Equivalent Circuit

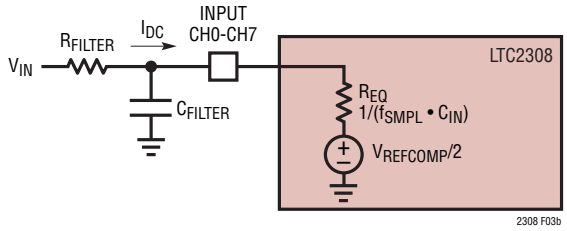


Figure 3b. Analog Input Equivalent Circuit for Large Filter Capacitances

which amounts to a full-scale error of 0.5LSBs when using a filter resistor (R_{FILTER}) of 4.7Ω. Applications requiring lower sample rates can tolerate a larger filter resistor for the same amount of full-scale error.

Figures 4a and 4b show respective examples of input filtering for single-ended and differential inputs. For the single-ended case in Figure 4a, a 50Ω source resistor and a 2000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

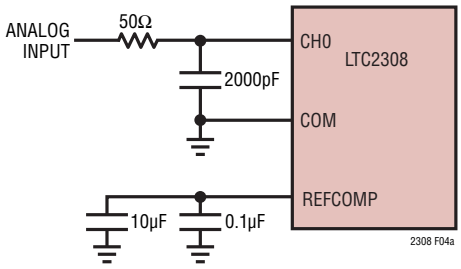


Figure 4a. Optional RC Input Filtering for Single-Ended Input

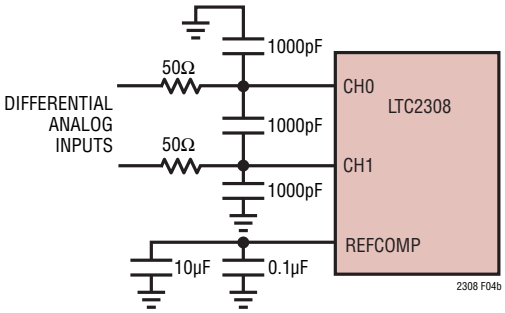


Figure 4b. Optional RC Input Filtering for Differential Inputs

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 5 shows a typical SINAD of 73.3dB with a 500kHz sampling rate and a 1kHz input. A SNR of 73.4dB can be achieved with the LTC2308.

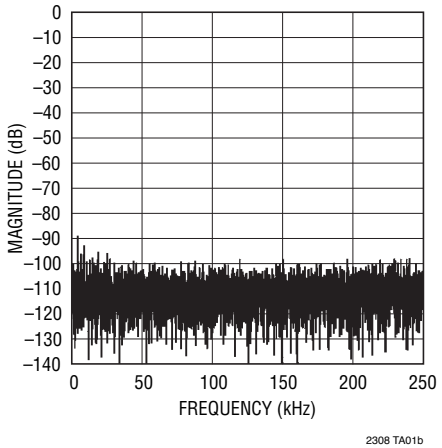


Figure 5. 1kHz Sine Wave 8192 Point FFT Plot

APPLICATIONS INFORMATION

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Internal Reference

The LTC2308 has an on-chip, temperature compensated bandgap reference that is factory trimmed to 2.5V (Refer to Figure 6a). It is internally connected to a reference amplifier and is available at V_{REF} (Pin 7). V_{REF} should be bypassed to GND with a 2.2µF tantalum capacitor to minimize noise. An 8k resistor is in series with the output so that it can be easily overdriven by an external reference if more accuracy and/or lower drift are required as shown in Figure 6b. The reference amplifier gains the V_{REF} voltage by 1.638 to 4.096V at REFCOMP (Pin 8). To compensate the reference amplifier, bypass REFCOMP with a 10µF ceramic or tantalum capacitor in parallel with a 0.1µF ceramic capacitor for best noise performance. The internal reference buffer can also be overdriven from 1V to AV_{DD} with an external reference at REFCOMP as shown in Figure 6c. To do so V_{REF} must be grounded to disable the reference buffer. This will result in an input range of 0V to $V_{REFCOMP}$ in unipolar mode and ±0.5 • $V_{REFCOMP}$ in bipolar mode.

Internal Conversion Clock

The internal conversion clock is factory trimmed to achieve a typical conversion time (t_{CONV}) of 1.3µs and a maximum conversion time of 1.6µs over the full operating temperature range. With a typical acquisition time of 240ns, a throughput sampling rate of 500ksps is tested and guaranteed.

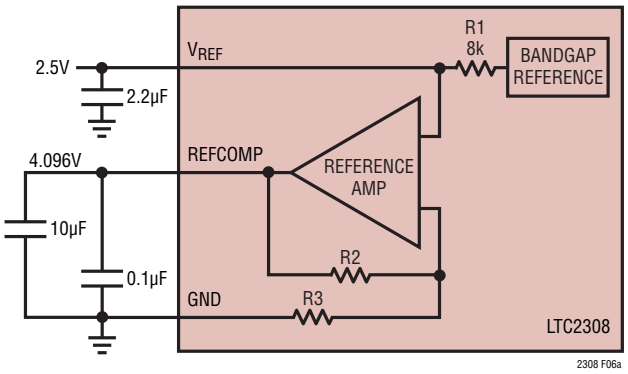


Figure 6a. LTC2308 Reference Circuit

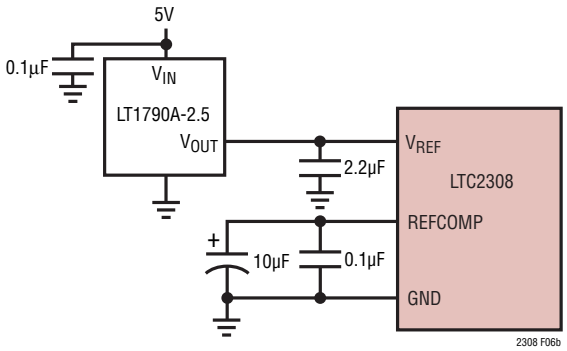


Figure 6b. Using the LT1790A-2.5 as an External Reference

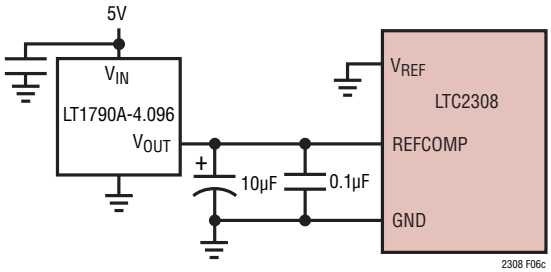


Figure 6c. Overdriving REFCOMP Using the LT1790A-4.096

Digital Interface

The LTC2308 communicates via a standard 4-wire SPI compatible digital interface. The rising edge of CONVST initiates a conversion. After the conversion is finished, pull CONVST low to enable the serial output (SDO). The ADC shifts out the digital data in 2's complement format when operating in bipolar mode or in straight binary format when in unipolar mode, based on the setting of the UNI bit.

APPLICATIONS INFORMATION

For best performance, ensure that CONVST returns low within 40ns after the conversion starts (i.e., before the first bit decision) or after the conversion ends. If CONVST is low when the conversion ends, the MSB bit will appear at SDO at the end of the conversion and the ADC will remain powered up.

Timing and Control

The start of a conversion is triggered by a rising edge at CONVST. Once initiated, a new conversion cannot be restarted until the current conversion is complete. Figures 8 and 9 show the timing diagrams for two different examples of CONVST pulses. Example 1 (Figure 8) shows CONVST staying HIGH after the conversion ends. If CONVST is high after the t_{CONV} period, the LTC2308 enters NAP or SLEEP mode, depending on the setting of SLP bit from the D_{IN} word that was shifted in after the previous conversion. (see Nap Mode and Sleep Mode for more detail).

When CONVST returns low, the ADC wakes up and the most significant bit (MSB) of the output data sequence at SDO becomes valid after the serial data bus is enabled. All other data bits from SDO transition on the falling edge of each SCK pulse. Configuration data (D_{IN}) is loaded into the LTC2308 at SDI, starting with the first SCK rising edge after CONVST returns low. The S/D bit is loaded on the first SCK rising edge.

Example 2 (Figure 9) shows CONVST returning low before the conversion ends. In this mode, the ADC and all internal circuitry remain powered up. When the conversion is complete, the MSB of the output data sequence at SDO becomes valid after the data bus is enabled. At this point(t_{CONV} 1.3µs after the rising edge of CONVST), pulsing SCK will shift data out at SDO and load configuration data (D_{IN}) into the LTC2308 at SDI. The first SCK rising edge loads the S/D bit into the LTC2308. SDO transitions on the falling edge of each SCK pulse.

Figures 10 and 11 are the transfer characteristics for the bipolar and unipolar modes. Data is output at SDO in 2's complement format for bipolar readings and in straight binary for unipolar readings.

Nap Mode

The ADC enters nap mode when CONVST is held high after the conversion is complete (t_{CONV}) if the SLP bit is set to a logic 0. The supply current decreases to 180µA in nap mode between conversions, thereby reducing the average power dissipation as the sample rate decreases. For example, the LTC2308 draws an average of 200µA with a 1ksps sampling rate. The LTC2308 keeps only the reference(V_{REF}) and reference buffer(REFCOMP) circuitry active when in nap mode.

Sleep Mode

The ADC enters sleep mode when CONVST is held high after the conversion is complete (t_{CONV}) if the SLP bit is set to a logic 1. The ADC draws only 7µA in sleep mode, provided that none of the digital inputs are switching. When CONVST returns low, the LTC2308 is released from the SLEEP mode and requires 200ms to wake up and charge the respective 2.2µF and 10µF bypass capacitors on the V_{REF} and REFCOMP pins.

Board Layout and Bypassing

To obtain the best performance, a printed circuit board with a solid ground plane is required. Layout for the printed circuit board should ensure digital and analog signal lines are separated as much as possible. Care should be taken not to run any digital signal alongside an analog signal. All analog inputs should be shielded by GND. V_{REF}, REFCOMP and AV_{DD} should be bypassed to the ground plane as close to the pin as possible. Maintaining a low impedance path for the common return of these bypass capacitors is essential to the low noise operation of the ADC. These traces should be as wide as possible. See Figure 7 for a suggested layout.

APPLICATIONS INFORMATION

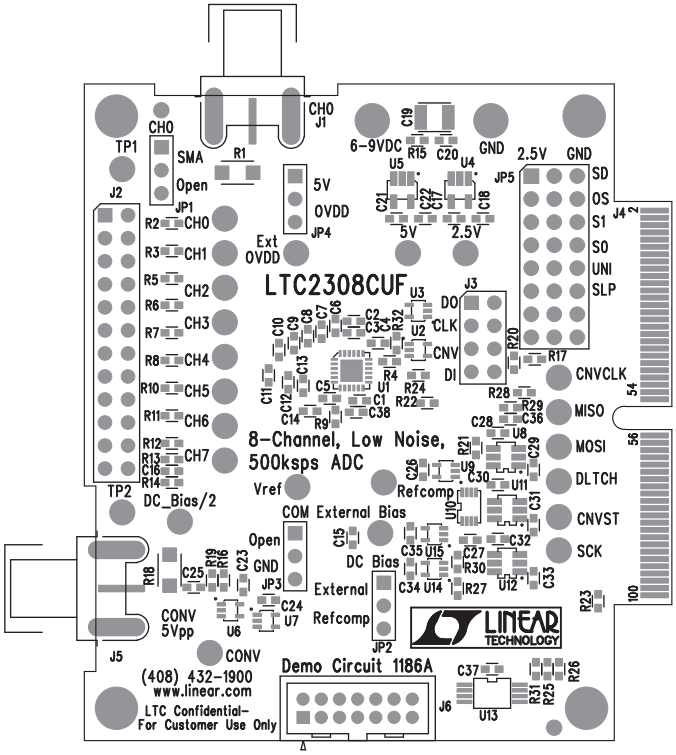


Figure 7a. Top Silkscreen

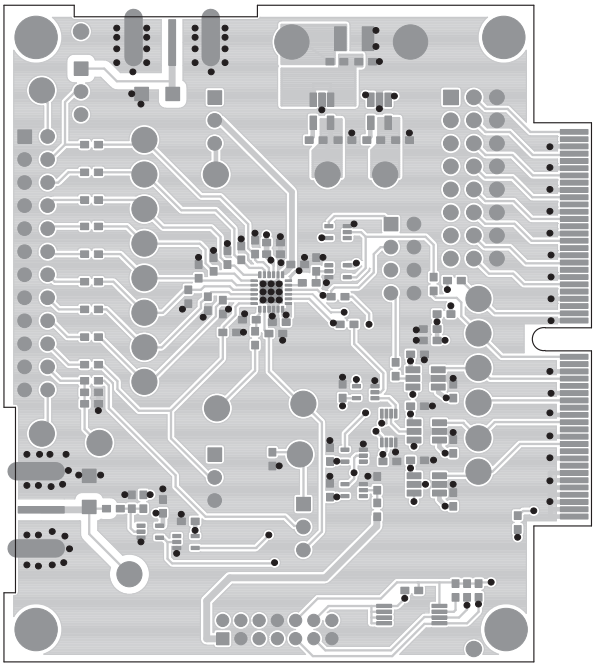


Figure 7b. Layer 1 Component Side

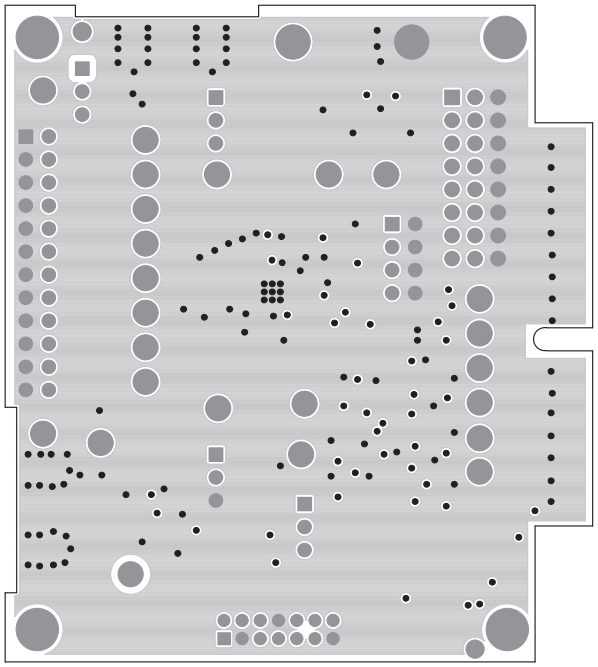


Figure 7c. Layer 2 Ground Plane

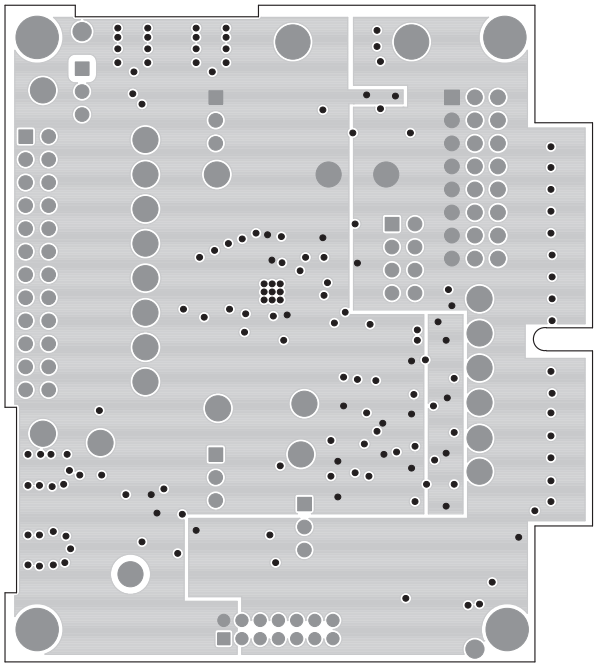


Figure 7d. Layer 3 Power Plane

APPLICATIONS INFORMATION

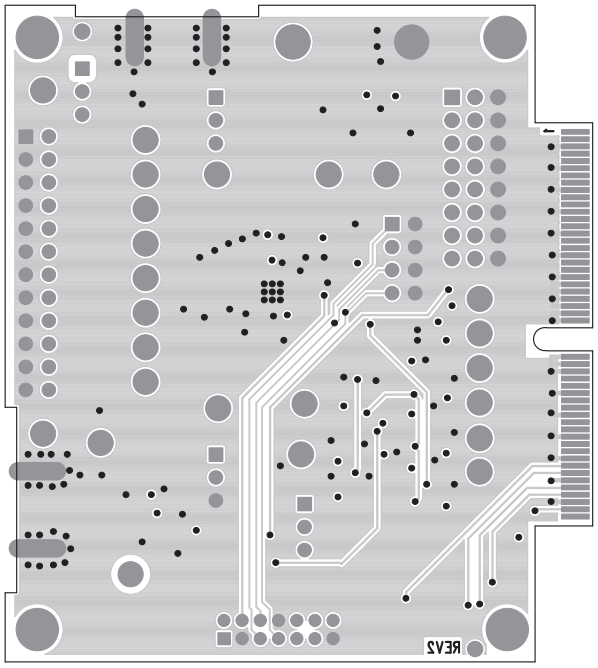


Figure 7e. Layer Back Solder Side

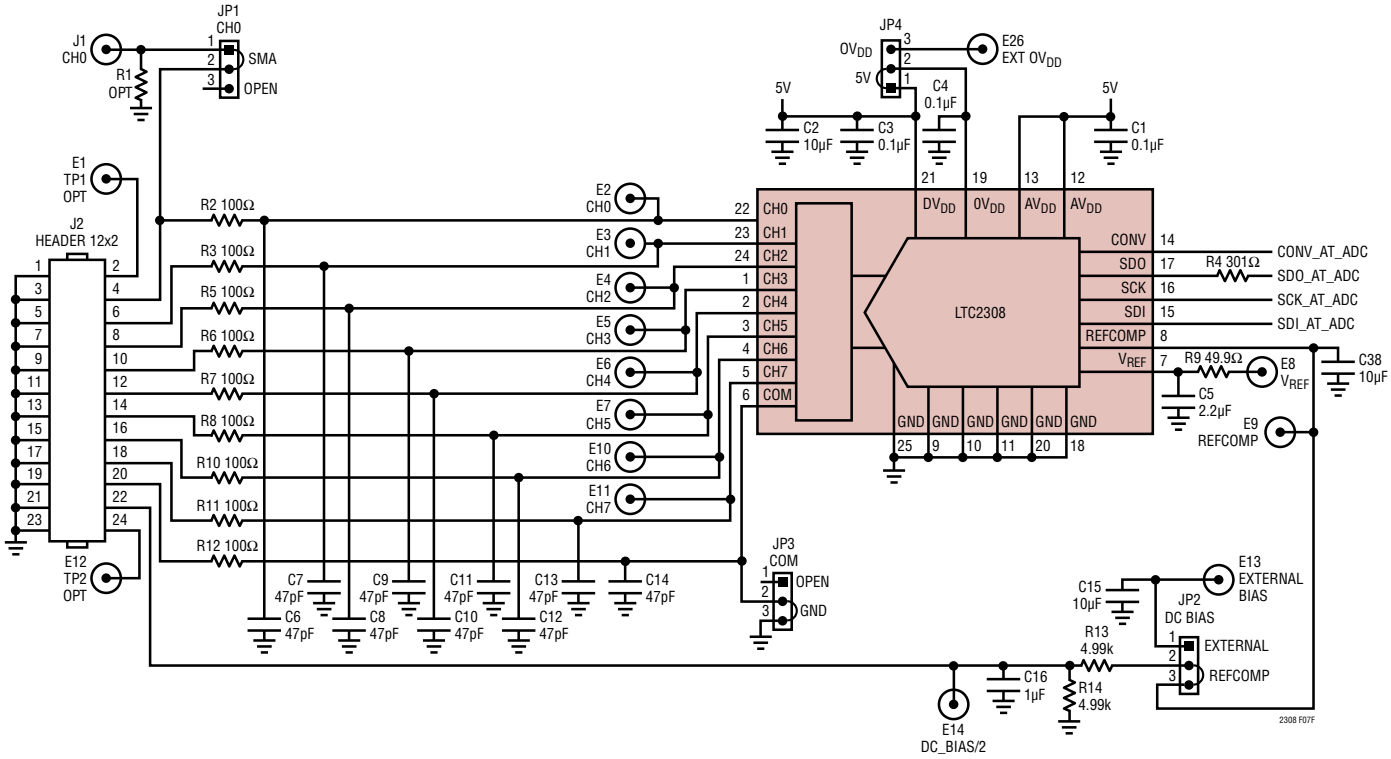


Figure 7f. Partial Demo Board Schematic

APPLICATIONS INFORMATION

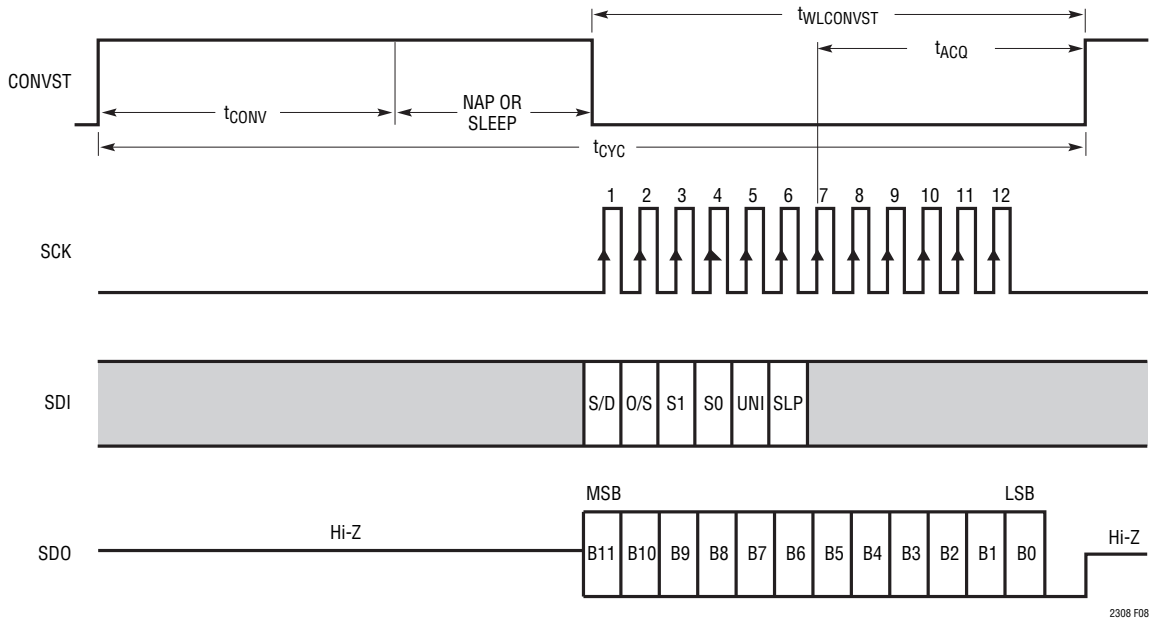


Figure 8. LTC2308 Timing with a Long CONVST Pulse

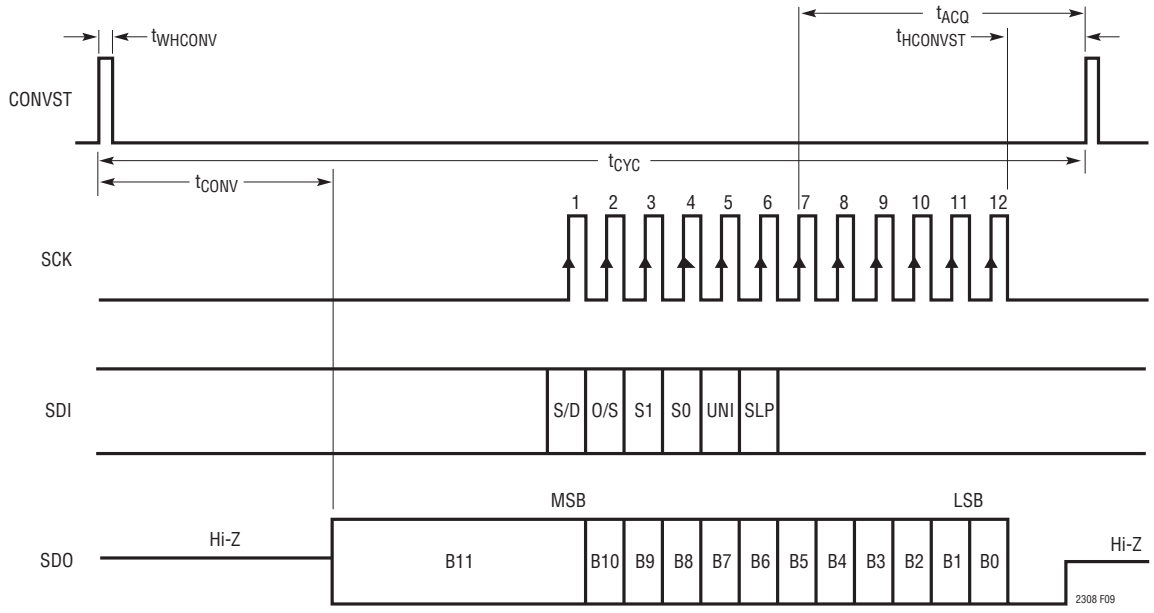


Figure 9. LTC2308 Timing with a Short CONVST Pulse

APPLICATIONS INFORMATION

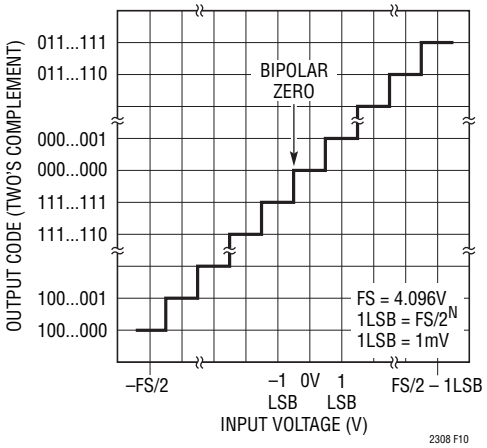


Figure 10. LTC2308 Bipolar Transfer Characteristics (2's Complement)

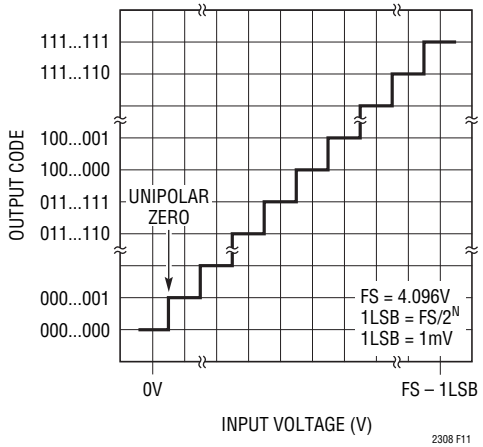
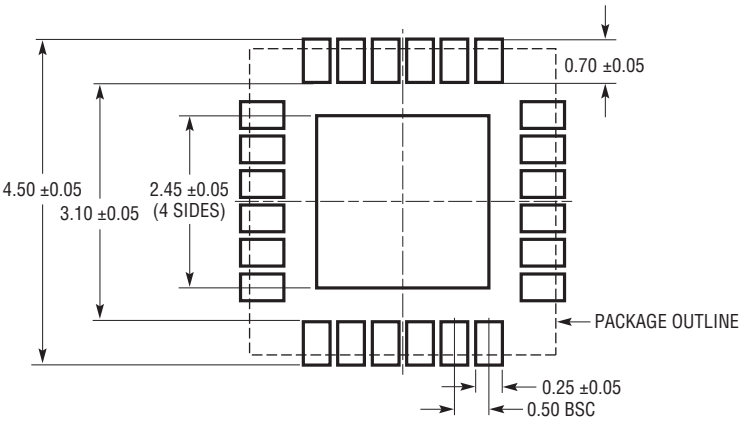


Figure 11. LTC2308 Unipolar Transfer Characteristics (Straight Binary)

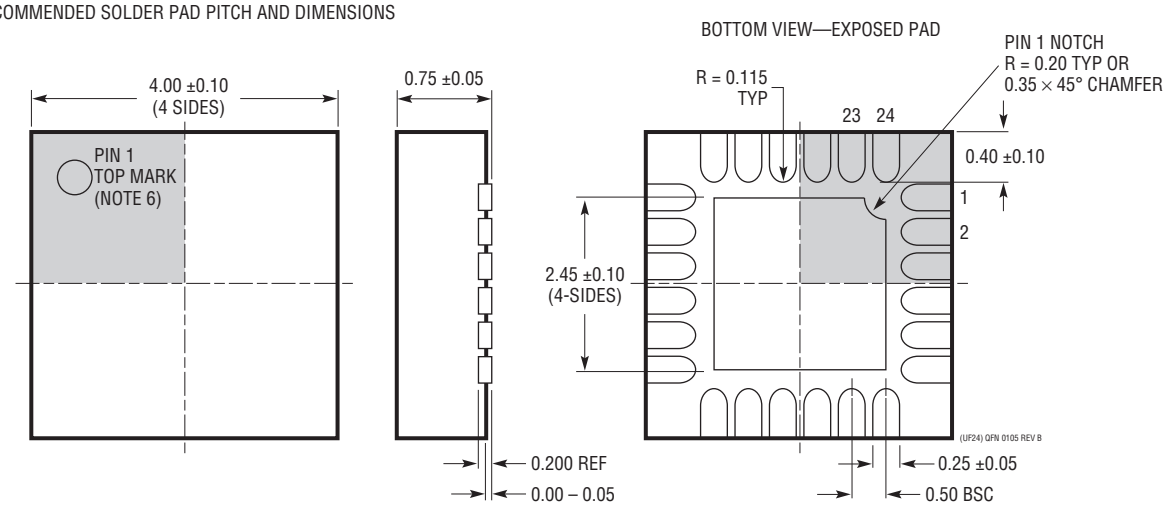
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2308#packaging for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



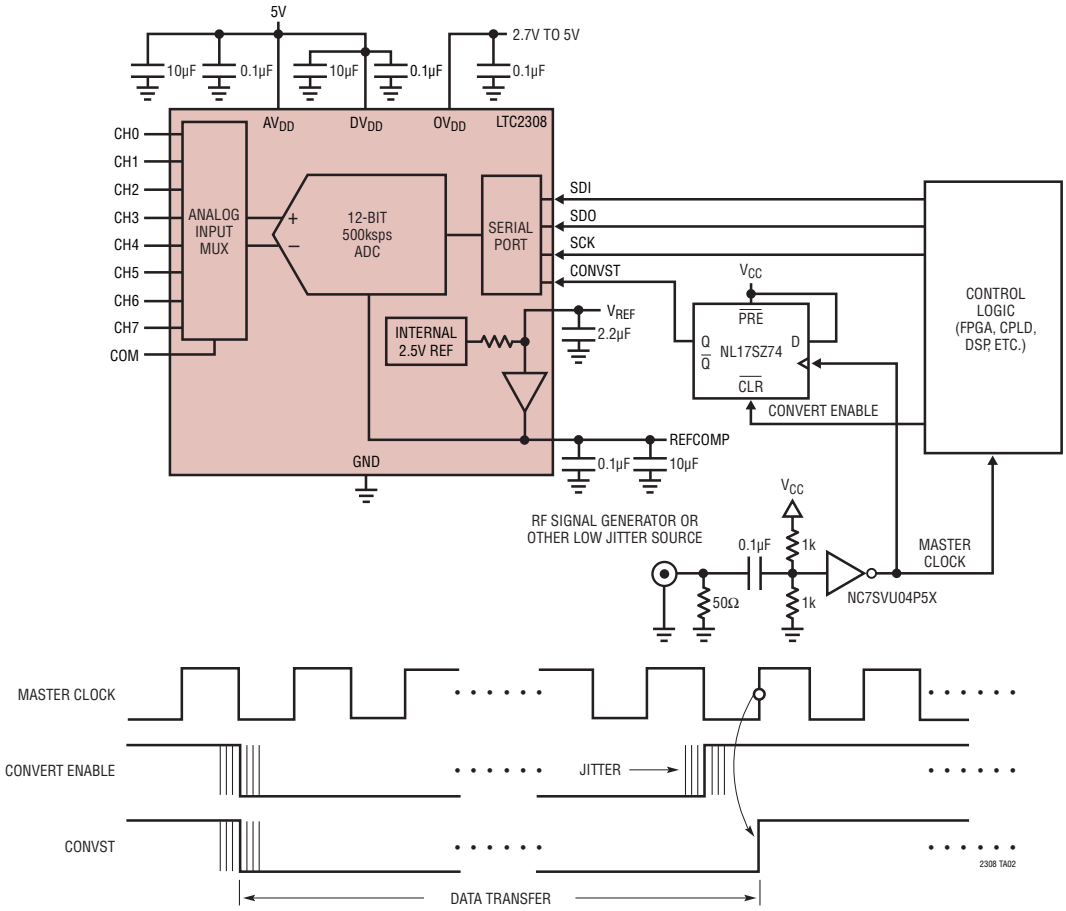
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	10/16	Updated t_{ACQ} in Figure 8.	18

TYPICAL APPLICATION

Clock Squaring/Level Shifting Circuit Allows Testing with RF Sine Generator, Convert Re-Timing Flip-Flop Preserves Low Jitter Clock Timing



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1417	14-Bit, 400ksps Serial ADC	20mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LT1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amps	Low Input Offset: 75µV/125µV
LTC1609	16-Bit, 200ksps Serial ADC	65mW, Configurable Bipolar and Unipolar Input Ranges, 5V Supply
LT1790	Micropower Low Dropout Reference	60µA Supple Current, 10ppm/°C, SOT-23 Package
LTC1850/LTC1851	10-Bit/12-Bit, 8-Channel, 1.25Msps ADC	Parallel Output, Programmable MUX and Sequencer, 5V Supply
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps ADC	Parallel Output, Programmable MUX and Sequencer, 3V or 5V Supply
LTC1860/LTC1861	12-Bit, 1-/2-Channel, 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	3V, 12-Bit, 1-/2-Channel, 150ksps ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1863/LTC1867	12-/16-Bit, 8-Channel, 200ksps ADC	6.5mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1863L/LTC1867L	3V, 12-/16-Bit, 8-Channel, 175ksps ADC	2mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1864/LTC1865	16-Bit, 1-/2-Channel, 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	3V, 16-Bit, 1-/2-Channel, 150ksps ADC in MSOP	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC2308
LT 1016 REV C • PRINTED IN USA