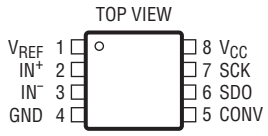
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Ground Voltage Difference
AGND, DGND LTC1865 MSOP Package..... ±0.3V
Analog Input ..... (GND – 0.3V) to (V_{CC} + 0.3V)
Digital Input ..... (GND – 0.3V) to 7V
Digital Output ..... (GND – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation..... 400mW

Operating Temperature Range
LTC1864C/LTC1865C/
LTC1864AC/LTC1865AC.....0°C to 70°C
LTC1864I/LTC1865I/
LTC1864AI/LTC1865AI ..... –40°C to 85°C
LTC1864H/LTC1865H
LTC1864AH/LTC1865AH ..... –40°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

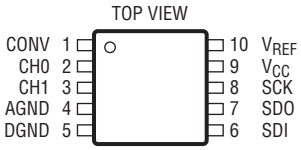
PIN CONFIGURATION

LTC1864



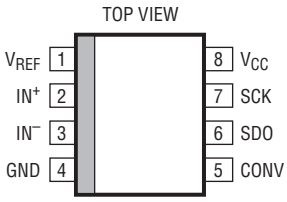
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 210°C/W

LTC1865



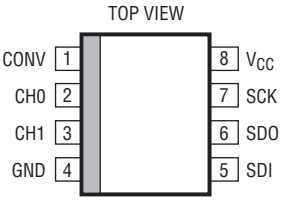
MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 210°C/W

LTC1864



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

LTC1865



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1864CMS8#PBF	LTC1864CMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8#PBF	LTC1864IMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864HMS8#PBF	LTC1864HMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864ACMS8#PBF	LTC1864ACMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8#PBF	LTC1864AIMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864AHMS8#PBF	LTC1864AHMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864CS8#PBF	LTC1864CS8#TRPBF	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8#PBF	LTC1864IS8#TRPBF	1864I	8-Lead Plastic SO	–40°C to 85°C
LTC1864ACS8#PBF	LTC1864ACS8#TRPBF	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1684AIS8#PBF	LTC1684AIS8#TRPBF	1864AI	8-Lead Plastic SO	–40°C to 85°C
LTC1865CMS#PBF	LTC1865CMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS#PBF	LTC1865IMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 85°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1865HMS#PBF	LTC1865HMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865ACMS#PBF	LTC1865ACMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS#PBF	LTC1865AIMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865AHMS#PBF	LTC1865AHMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865CS8#PBF	LTC1865CS8#TRPBF	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8#PBF	LTC1865IS8#TRPBF	1865I	8-Lead Plastic SO	–40°C to 85°C
LTC1865ACS8#PBF	LTC1865ACS8#TRPBF	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8#PBF	LTC1865AIS8#TRPBF	1865AI	8-Lead Plastic SO	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC1864CMS8	LTC1864CMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8	LTC1864IMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864HMS8	LTC1864HMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864ACMS8	LTC1864ACMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8	LTC1864AIMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864AHMS8	LTC1864AHMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864CS8	LTC1864CS8#TR	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8	LTC1864IS8#TR	1864I	8-Lead Plastic SO	–40°C to 85°C
LTC1864ACS8	LTC1864ACS8#TR	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1684AIS8	LTC1684AIS8#TR	1864AI	8-Lead Plastic SO	–40°C to 85°C
LTC1865CMS	LTC1865CMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS	LTC1865IMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865HMS	LTC1865HMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865ACMS	LTC1865ACMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS	LTC1865AIMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865AHMS	LTC1865AHMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865CS8	LTC1865CS8#TR	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8	LTC1865IS8#TR	1865I	8-Lead Plastic SO	–40°C to 85°C
LTC1865ACS8	LTC1865ACS8#TR	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8	LTC1865AIS8#TR	1865AI	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER AND MULTIPILEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1864/LTC1865 MIN	LTC1864/LTC1865 TYP	LTC1864/LTC1865 MAX	LTC1864A/LTC1865A MIN	LTC1864A/LTC1865A TYP	LTC1864A/LTC1865A MAX	UNITS
Resolution		●	16			16			Bits
No Missing Codes Resolution		●	14			15			Bits
INL	(Note 3) H-Grade (Note 3)	● ●			±8 ±8.5			±6 ±6.5	LSB LSB
Transition Noise				1.1			1.1		LSB_{RMS}
Gain Error		●			±20			±20	mV
Offset Error	LTC1864 SO-8 and MSOP, LTC1865 MSOP LTC1865 SO-8	● ●		±2 ±3	±5 ±7		±2 ±3	±5 ±7	mV mV
Input Differential Voltage Range	$V_{IN} = IN^+ - IN^-$	●	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	IN^+ Input IN^- Input		–0.05 –0.05		V_{CC} + 0.05 V_{CC}/2	–0.05 –0.05		V_{CC} + 0.05 V_{CC}/2	V V
V_{REF} Input Range	LTC1864 SO-8 and MSOP, LTC1865 MSOP		1		V_{CC}	1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			±1			±1	µA
C_{IN} Input Capacitance	In Sample Mode During Conversion			12 5			12 5		pF pF

DYNAMIC ACCURACY

T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{SAMPLE} = 250kHz, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1864/LTC1865 MIN	LTC1864/LTC1865 TYP	LTC1864/LTC1865 MAX	UNITS
SNR	Signal-to-Noise Ratio			87		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	10kHz Input Signal 100kHz Input Signal		83 76		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	10kHz Input Signal 100kHz Input Signal		88 77		dB dB
	Full Power Bandwidth			20		MHz
	Full Linear Bandwidth	S/(N+D) ≥ 75dB		125		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1864/LTC1865 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.5 2.4	4.74 4.72		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	CONV = V_{CC}	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			20		mA
I_{REF}	Reference Current (LTC1864 SO-8 and MSOP, LTC1865 MSOP)	CONV = VCC $f_{SMPL} = f_{SMPL(MAX)}$	● ●		0.001 0.05	3 0.1	µA mA
I_{CC}	Supply Current	CONV = V_{CC} After Conversion CONV = V_{CC} After Conversion, H-Grade $f_{SMPL} = f_{SMPL(MAX)}$	● ● ●		0.001 0.001 0.85	3 5 1.3	µA µA mA
P_D	Power Dissipation	$f_{SMPL} = f_{SMPL(MAX)}$			4.25		mW

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC1864/LTC1865 MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			4.75		5.25	V
f_{SCK}	Clock Frequency	 H-Grade	 ●			20 16.7	MHz MHz
t_{CYC}	Total Cycle Time			16 • SCK + t_{CONV}			µs
t_{SMPL}	Analog Input Sampling Time	LTC1864 (Note 5) LTC1865 (Note 5)		16 14			SCK SCK
t_{suCONV}	Setup Time CONV↓ Before First SCK↑ (See Figure 1)	 H-Grade		60 65	30 30		ns ns
t_{hDI}	Hold Time SDI After SCK↑	LTC1865		15			ns
t_{suDI}	Setup Time SSDI Stable Before SCK↑	LTC1865		15			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$		40%			$1/f_{SCK}$
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$		40%			$1/f_{SCK}$
t_{WHCONV}	CONV High Time Between Data Transfer Cycles	(Note 5)		t_{CONV}			µs
t_{WLCONV}	CONV Low Time During Data Transfer	(Note 5)		16			SCK
t_{hCONV}	Hold Time CONV Low After Last SCK↑				13		ns

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{SCK} = $f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1864/LTC1865 MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figure 1)		●		2.75	3.2	µs
		H-Grade	●		2.75	3.3	µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	250			kHz
		H-Grade	●	234			kHz
t_{dDO}	Delay Time, SCK↓ to SDO Data Valid	C_{LOAD} = 20pF			15	20	ns
		C_{LOAD} = 20pF	●			25	ns
		C_{LOAD} = 20pF, H-Grade	●			30	ns
t_{dis}	Delay Time, CONV↑ to SDO Hi-Z		●		30	60	ns
		H-Grade	●		30	65	ns
t_{en}	Delay Time, CONV↓ to SDO Enabled	C_{LOAD} = 20pF	●		30	60	ns
		C_{LOAD} = 20pF, H-Grade	●		30	65	ns
t_{hDO}	Time Output Data Remains Valid After SCK↓	C_{LOAD} = 20pF	●	5	10		ns
t_r	SDO Rise Time	C_{LOAD} = 20pF			8		ns
t_f	SDO Fall Time	C_{LOAD} = 20pF			4		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

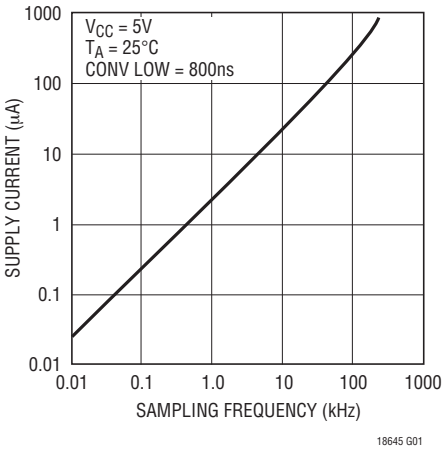
Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

Note 5: Guaranteed by design, not subject to test.

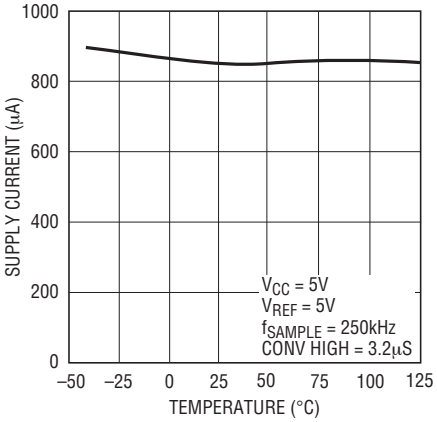
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sampling Frequency



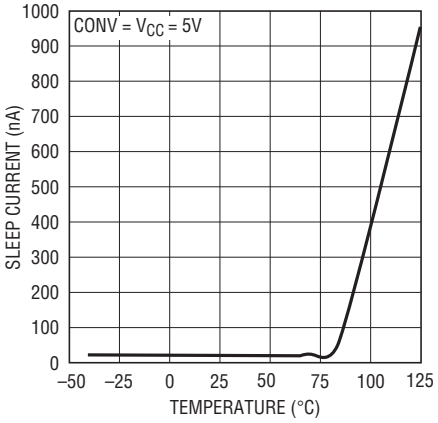
18645 G01

Supply Current vs Temperature



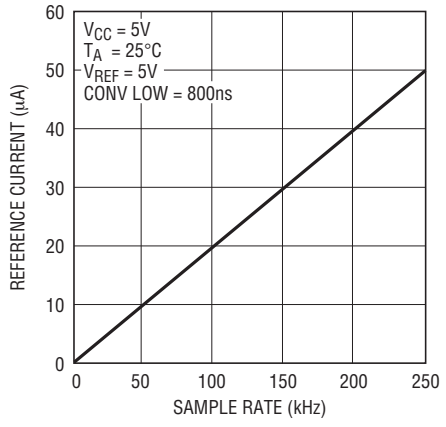
18645 G02

Sleep Current vs Temperature



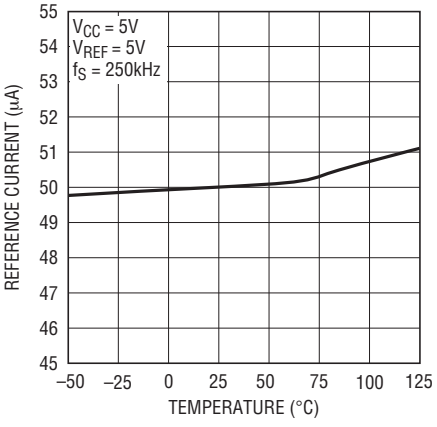
18645 G03

Reference Current vs Sampling Rate



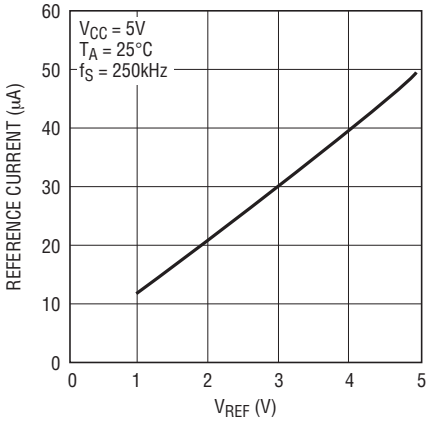
18645 G04

Reference Current vs Temperature



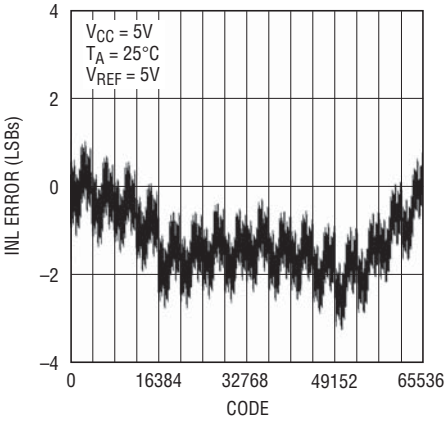
18645 G05

Reference Current vs Reference Voltage



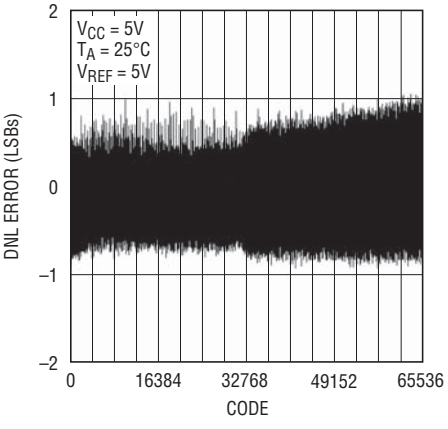
18645 G06

Typical INL Curve



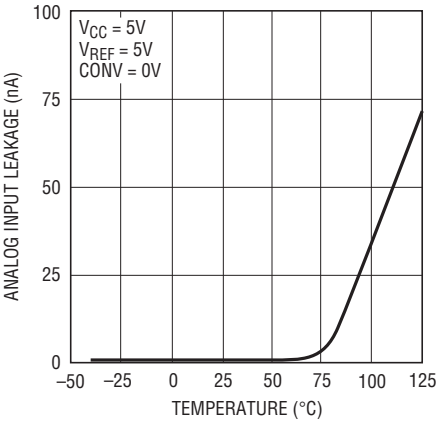
18645 G07

Typical DNL Curve



18645 G08

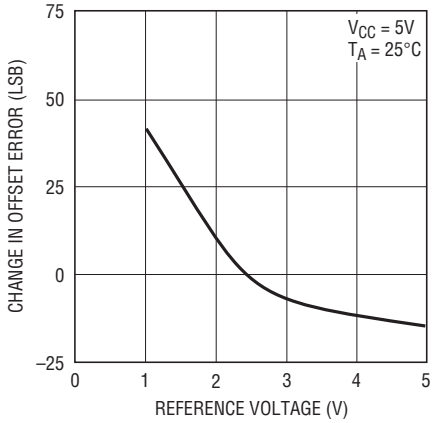
Analog Input Leakage Current vs Temperature



18645 G09

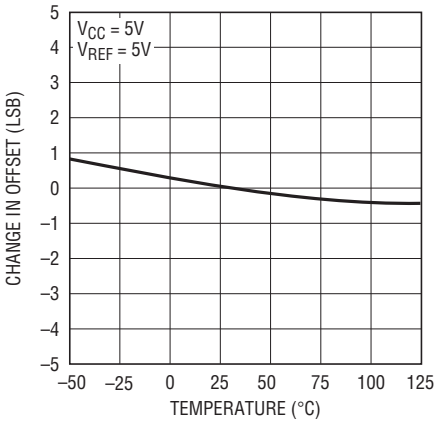
TYPICAL PERFORMANCE CHARACTERISTICS

Change in Offset Error vs Reference Voltage



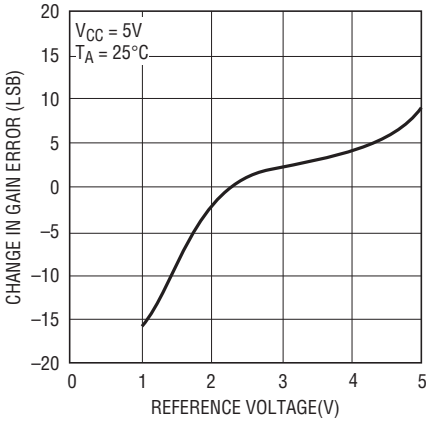
18645 G10

Change in Offset vs Temperature



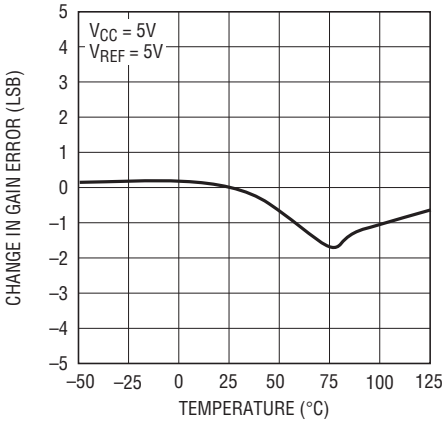
18645 G11

Change in Gain Error vs Reference Voltage



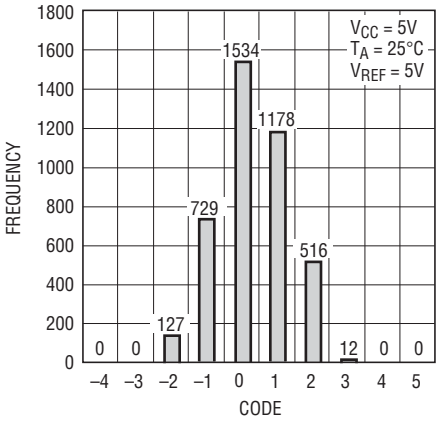
18645 G12

Change in Gain Error vs Temperature



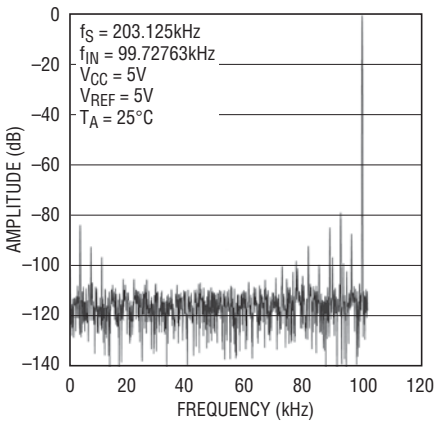
18645 G13

Histogram of 4096 Conversions of a DC Input Voltage



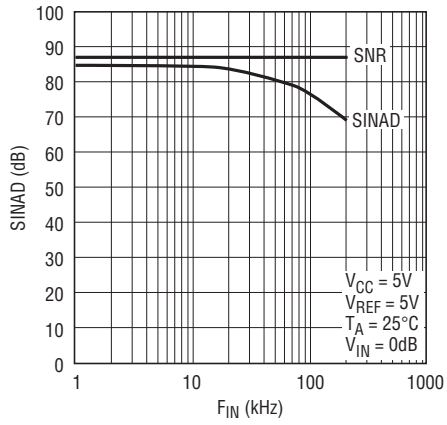
18645 G14

4096 Point FFT Nonaveraged



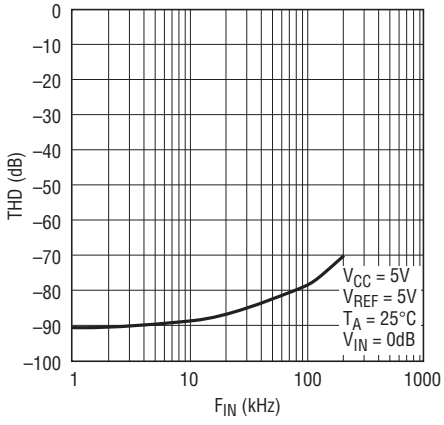
18645 G15

SINAD vs Frequency



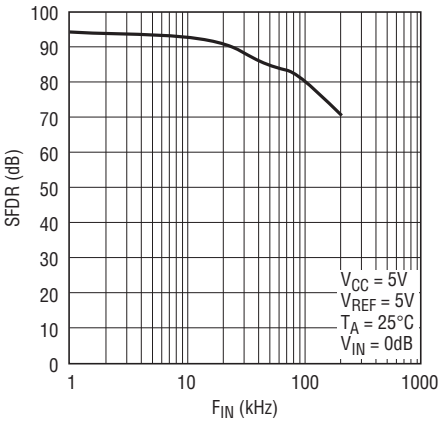
18645 G16

THD vs Frequency



18645 G17

SFDR vs Frequency



18645 G18

PIN FUNCTIONS

LTC1864

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN^+, IN^- (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1865 (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

LTC1865 (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

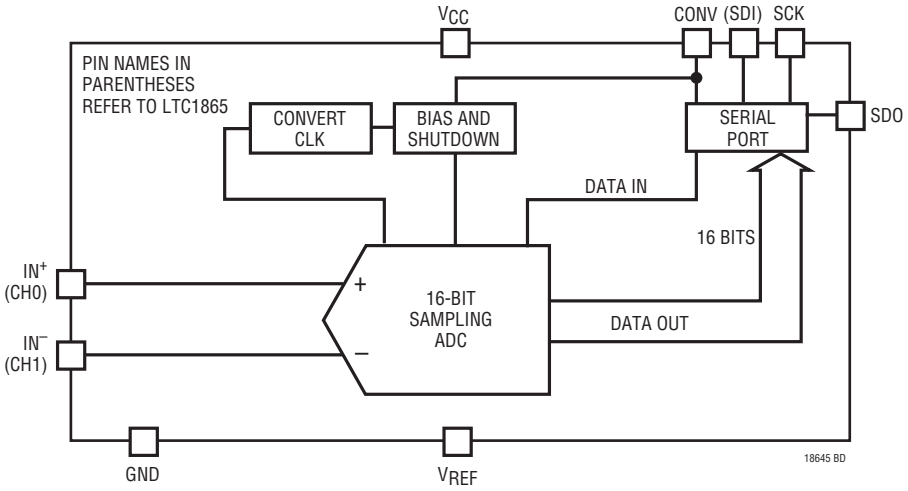
SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

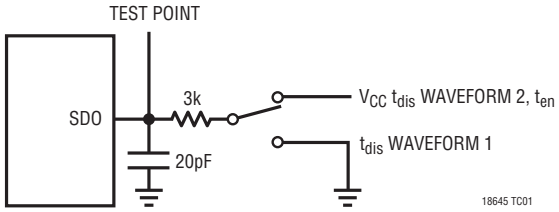
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.

FUNCTIONAL BLOCK DIAGRAM

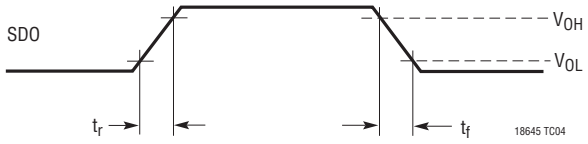


TEST CIRCUITS

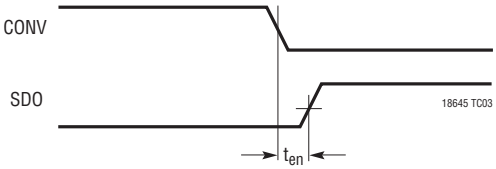
Load Circuit for t_{dDO}, t_r, t_f, t_{dis} and t_{en}



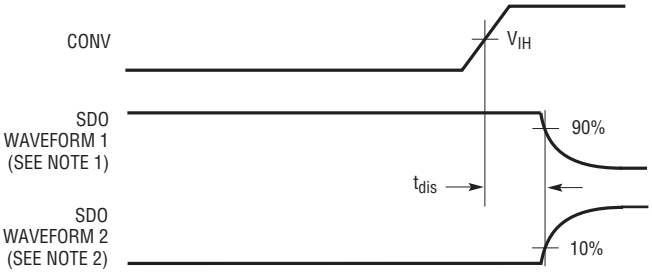
Voltage Waveforms for SDO Rise and Fall Times, t_r, t_f



Voltage Waveforms for t_{en}



Voltage Waveforms for t_{dis}

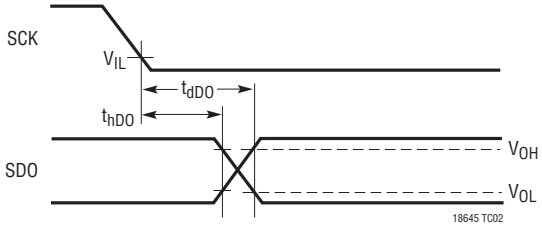


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

18645 TC05

Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



APPLICATIONS INFORMATION

LTC1864 OPERATION

Operating Sequence

The LTC1864 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1864 goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1864 goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1864 has a unipolar differential analog input. The converter will measure the voltage between the "IN^+" and "IN^-" inputs. A zero code will occur when IN^+ minus IN^- equals zero. Full scale occurs when IN^+ minus IN^- equals V_{REF} minus 1LSB. See Figure 2. Both the "IN^+" and "IN^-" inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If "IN^-" is grounded and V_{REF} is tied to V_{CC}, a rail-to-rail input span will result on "IN^+" as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1864 defines the full-scale range of the A/D converter. The LTC1864 can operate with reference voltages from V_{CC} to 1V.

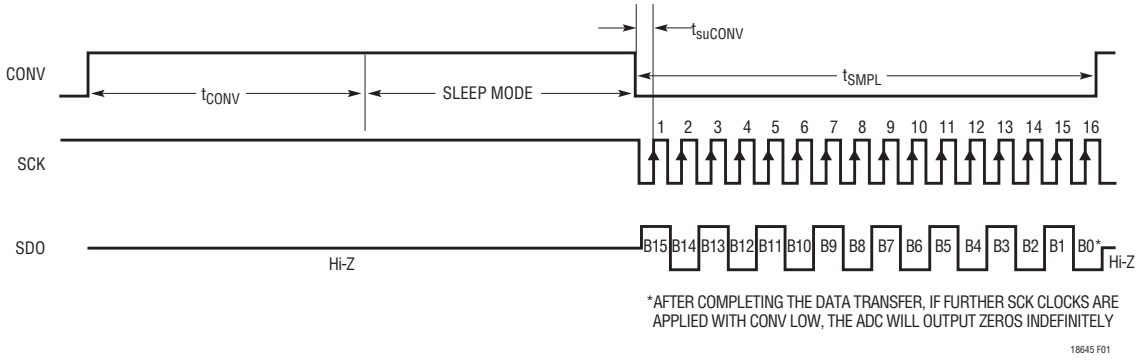


Figure 1. LTC1864 Operating Sequence

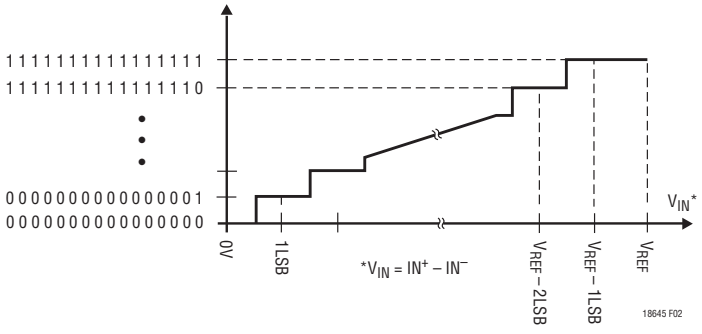


Figure 2. LTC1864 Transfer Curve

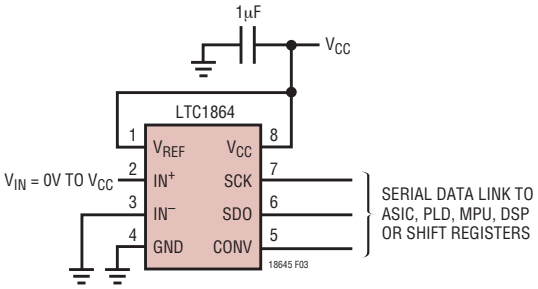


Figure 3. LTC1864 with Rail-to-Rail Input Span

APPLICATIONS INFORMATION

LTC1865 OPERATION

Operating Sequence

The LTC1865 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV}, the conversion is finished. If CONV is left high after this time, the LTC1865 goes into sleep mode drawing only leakage current. The LTC1865's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND. A zero code will occur when the "+" input minus the "–" input equals zero. Full scale occurs when the "+" input minus the "–" input equals V_{REF} minus 1LSB. See Figure 5. Both the "+" and "–" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{REF} = V_{CC}$. If the "–" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

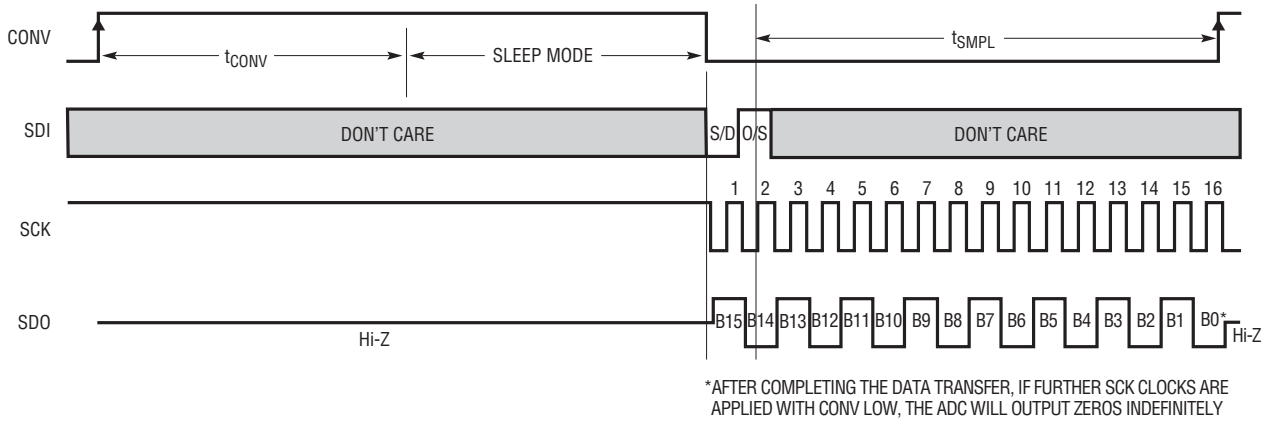
Reference Input

The reference input of the LTC1865 SO-8 package is internally tied to V_{CC}. The span of the A/D converter is therefore equal to V_{CC}. The voltage on the reference input of the LTC1865 MSOP package defines the span of the A/D converter. The LTC1865 MSOP package can operate with reference voltages from 1V to V_{CC}.

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

18645 TBL1



18645 F04

Figure 4. LTC1865 Operating Sequence

APPLICATIONS INFORMATION

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1864/LTC1865 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1865 MSOP package and GND for the LTC1864 and LTC1865 SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1µF tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1864/LTC1865 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200Ω or high speed op amps are used (e.g., the LT®1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

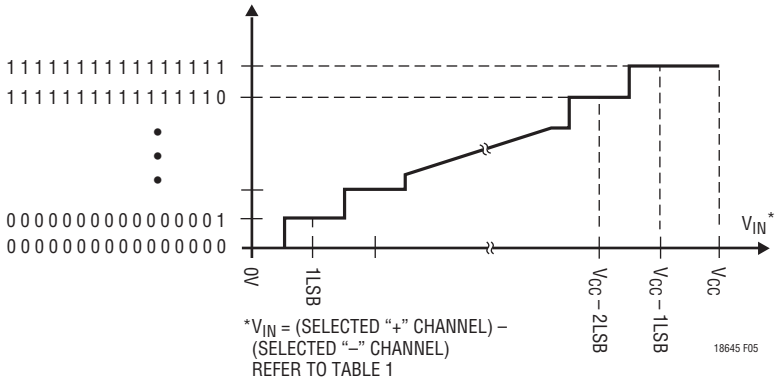
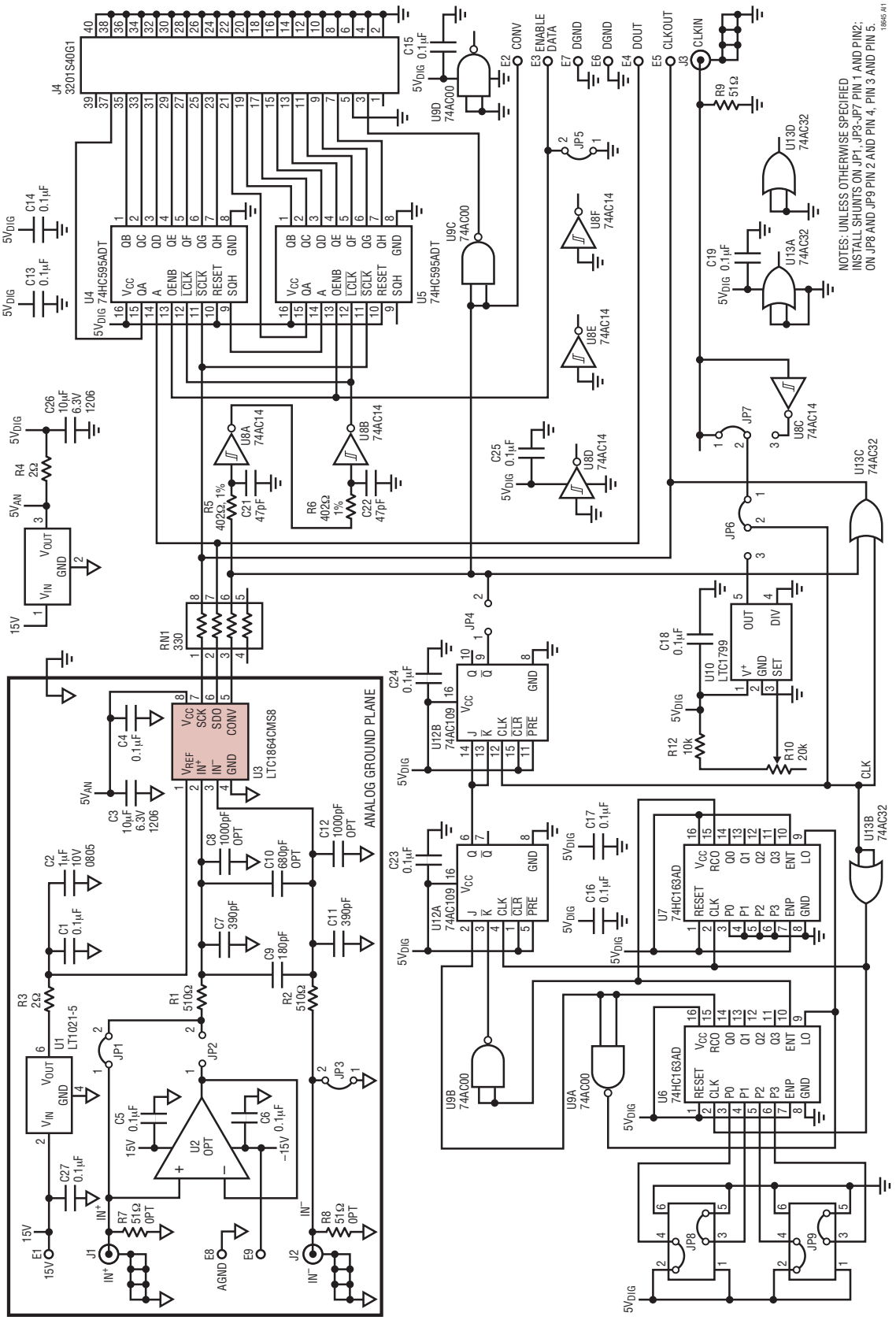


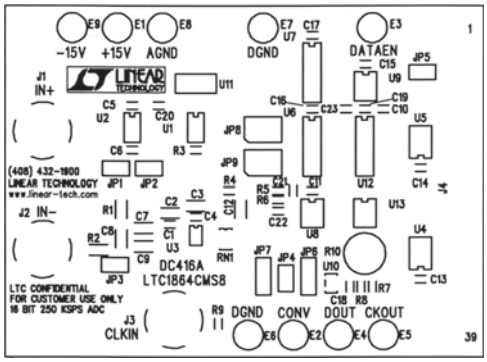
Figure 5. LTC1865 Transfer Curve

APPLICATIONS INFORMATION

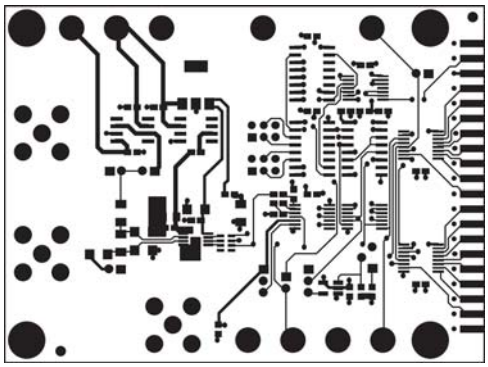
LTC1864 Evaluation Circuit Schematic



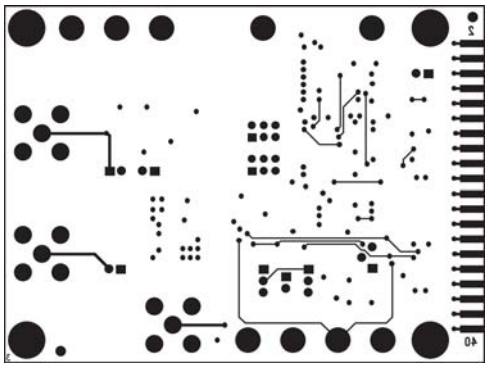
APPLICATIONS INFORMATION



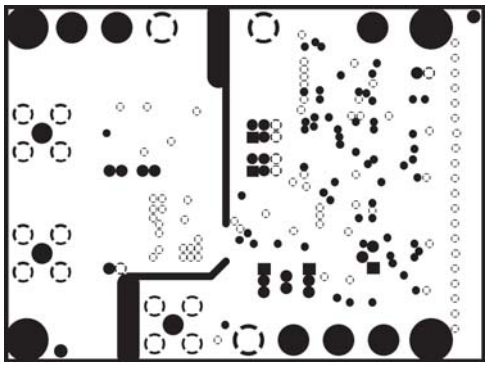
Component Side Silk Screen for LTC1864 Evaluation Circuit



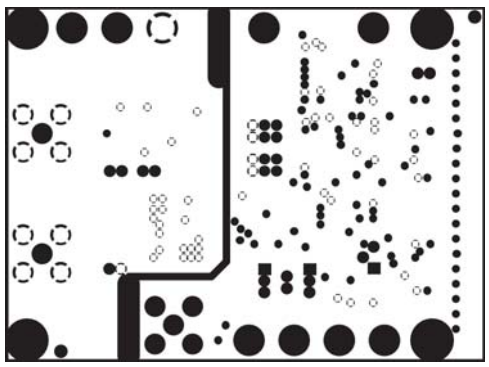
Component Side Showing Traces
(Note Sider Traces on Analog Side)



Bottom Side Showing Traces
(Note Almost No Analog Traces on Board Bottom)



Ground Layer with Separate Analog and Digital Grounds



Supply Layer with 5V Digital Supply and
Analog Ground Repeated

APPLICATIONS INFORMATION

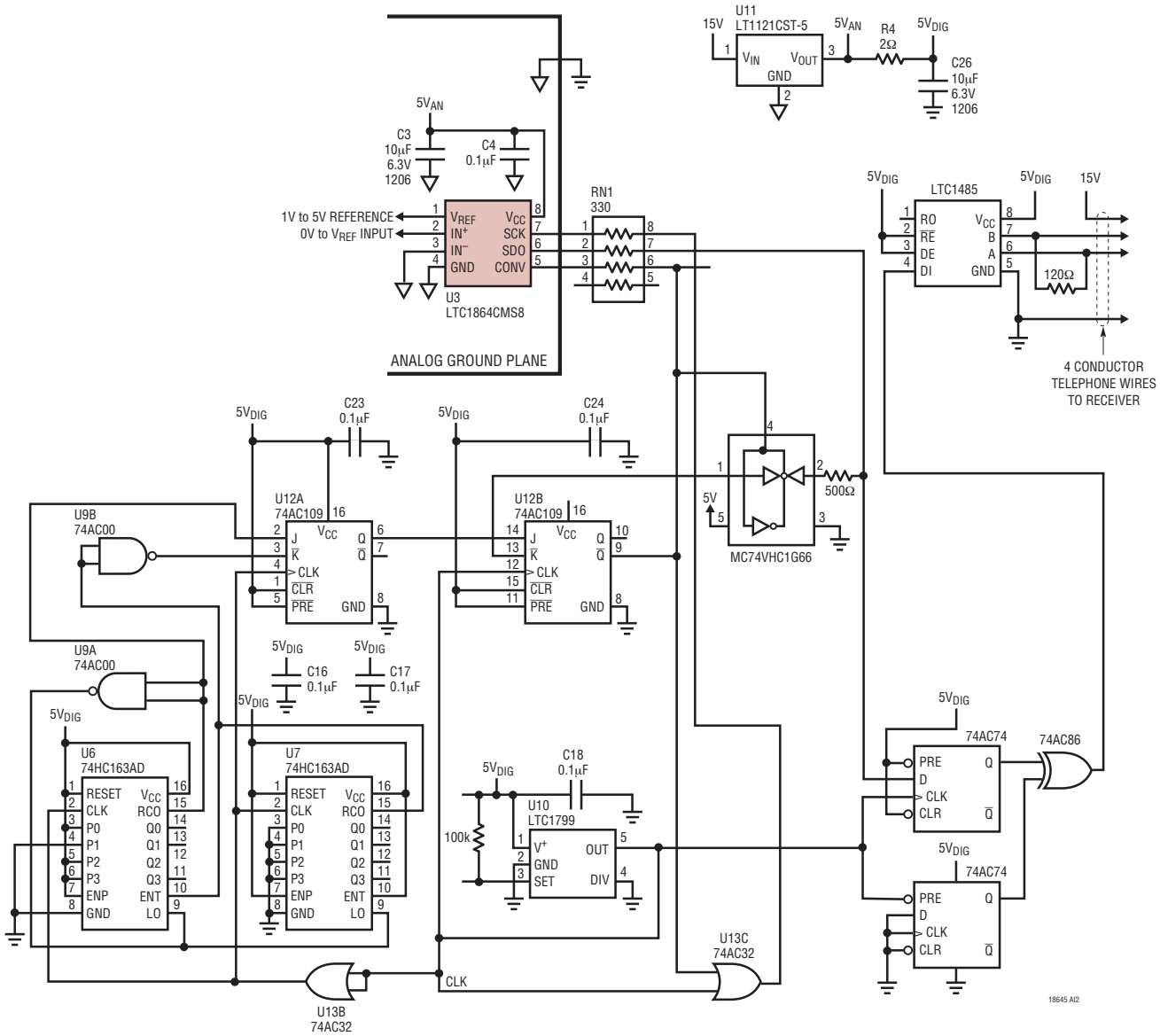


Figure 6. LTC1864 Manchester Transmitter

APPLICATIONS INFORMATION

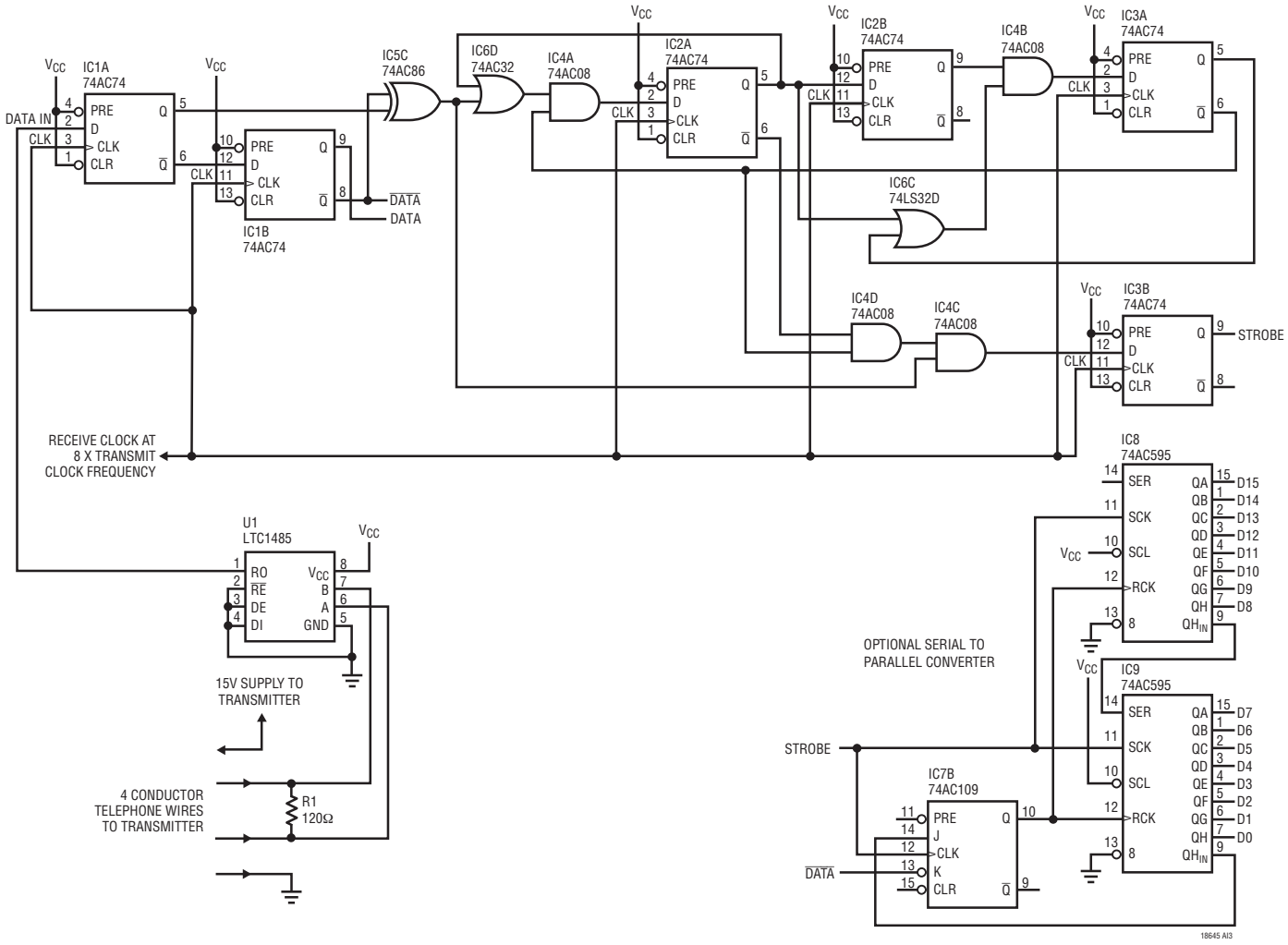


Figure 7. LTC1864 Manchester Receiver

APPLICATIONS INFORMATION

Transmit LTC1864 Data Over Modular Telephone Wire Using Simple Transmitter/Receiver

Figure 6 shows a simple Manchester encoder and differential transmitter suitable for use with the LTC1864. This circuit allows transmission of data over inexpensive telephone wire. This is useful for measuring a remote sensor, particularly when the cost of preserving the analog signal over a long distance is high.

Manchester encoding is a clock signal that is modulated by exclusive ORing with the data signal. The resulting signal contains both clock and data information and has an average duty cycle of 50%, that also allows transformer coupling. In practice, generating a Manchester encoded signal with an XOR gate will often produce glitches due to the skew between data and clock transitions. The D flip-flops in this encoder retime the clock and data such that the respective edges are closely aligned, effectively suppressing glitches. The retimed data and clock are then XORed to produce the Manchester encoded data, which is interfaced to telephone wire with an LTC1485 RS485 transceiver.

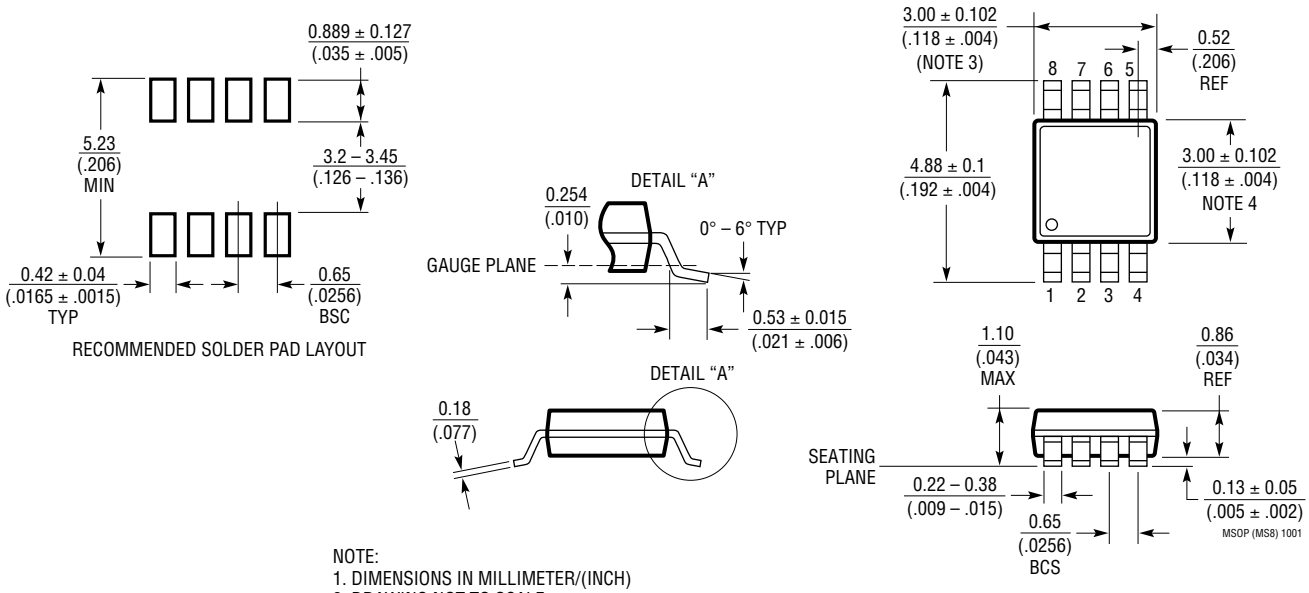
In order to synchronize to incoming data, the receiver needs a sequence to indicate the start of a data word. The transmitter schematic shows logic that will produce 31 zeros, a start bit, followed by the 16 data bits (one sample every 48 clock cycles) at a clock frequency of 1MHz set by the LTC1799 oscillator. Sending at least 18 zeros before each start bit ensures that if synchronization is lost, the receiver can resynchronize to a start bit under all conditions. The serial to parallel converter shown in Figure 7 requires 18 zeros to avoid triggering on data bits.

The Manchester receiver shown in Figure 7 was adopted from Xilinx application note 17-30 and would typically be implemented in an FPGA. The decoder clock frequency is nominally 8 times the transmit clock frequency and is very tolerant of frequency errors. The outputs of the decoder are data and a strobe that indicates a valid data bit. The data can be deserialized using shift registers as shown. The start bit resets the J-K/flip-flop on its way into the first shift register. When it appears at the QH_{IN} output of the second shift register, it sets the flip-flop that loads the parallel data into the output register.

With AC family CMOS logic at 5V the receiver clock frequency is limited to 20MHz; the corresponding transmitter clock frequency is 2.5MHz. If the receiver is implemented in an FPGA that can be clocked at 160MHz, the LTC1864 can be clocked at its rated clock frequency of 20MHz.

PACKAGE DESCRIPTION

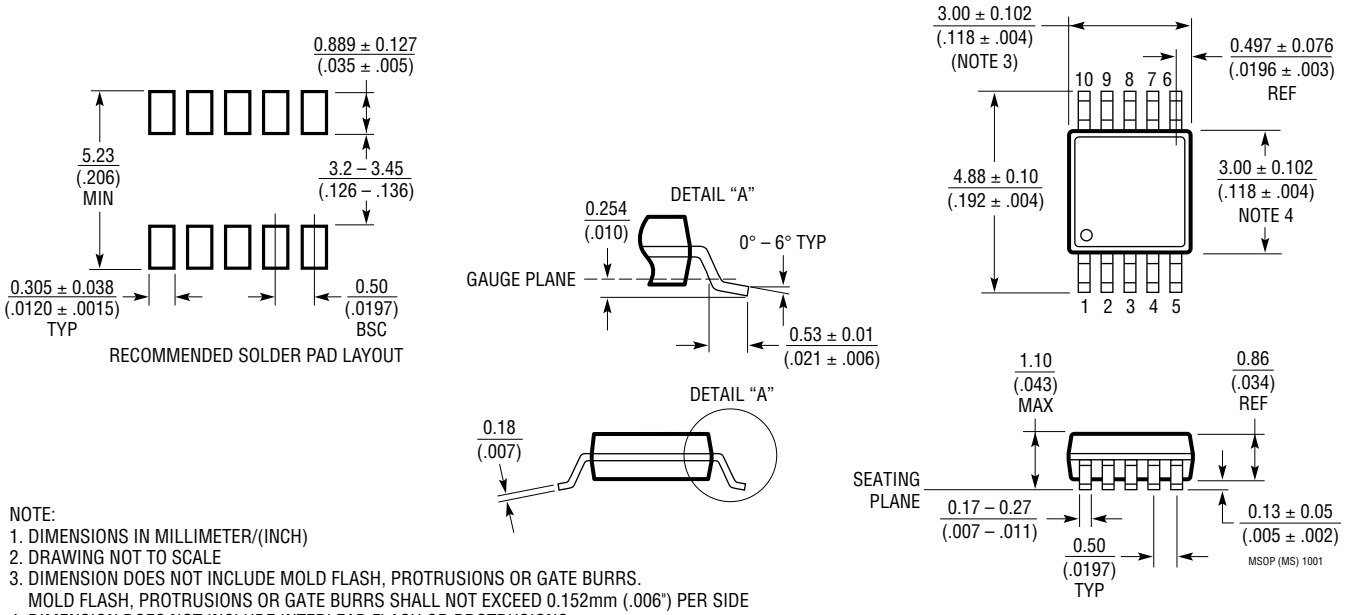
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

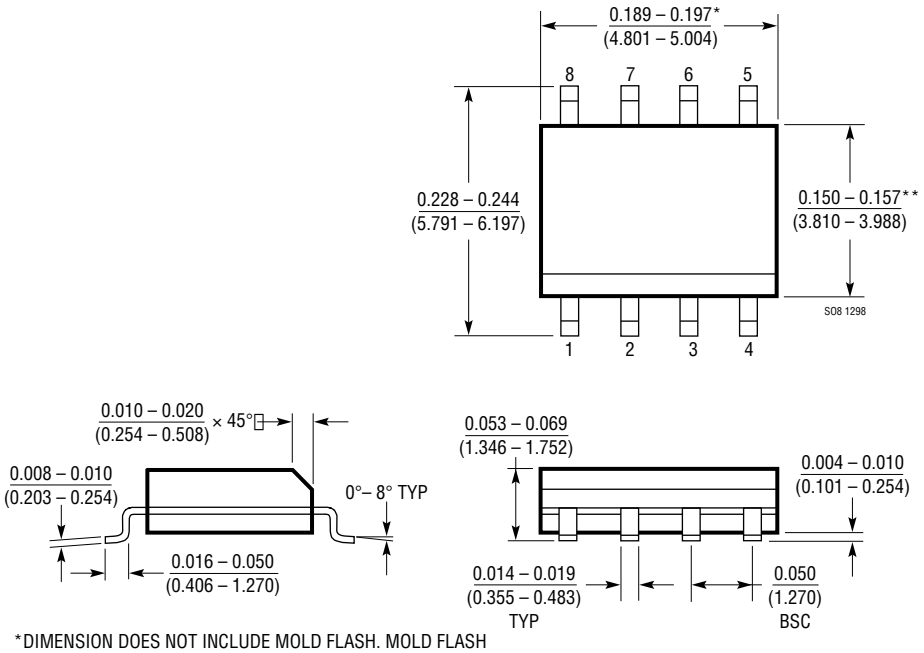
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

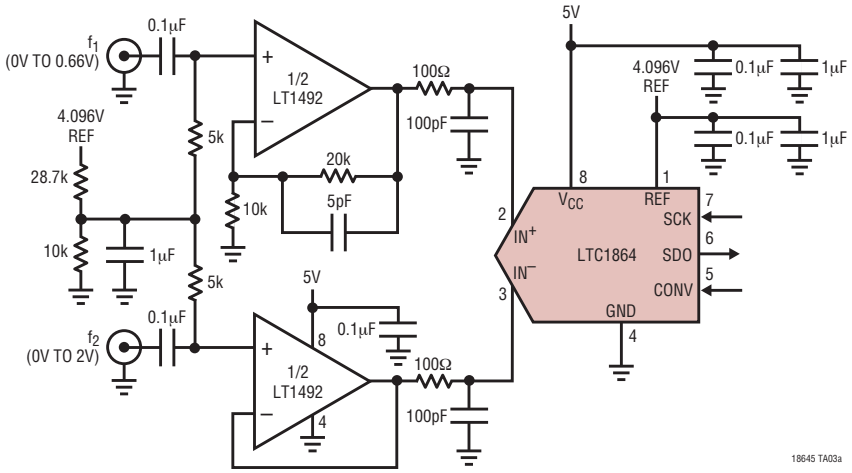


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

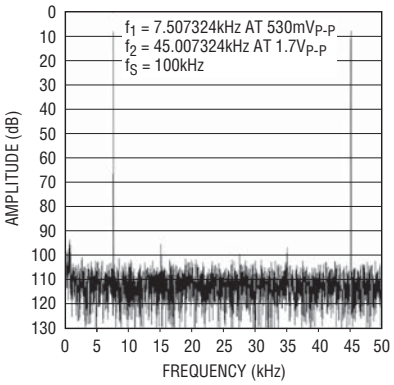
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Sample Two Channels Simultaneously with a Single Input ADC



4096 Point FFT of Output



RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V or ±5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V or ±5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
References			
LT1460	Micropower Precision Series Reference		Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference		60µA Supply Current, 10ppm/°C, SOT-23
Op Amps			
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps		22V/µs Slew Rate, 75µV/125µV Offset
LT1806/LT1807	Single/Dual 325MHz Low Noise Op Amps		140V/µs Slew Rate, 3.5nV/√Hz Noise, –80dBc Distortion
LT1809/LT1810	Single/Dual 180MHz Low Distortion Op Amps		350V/µs Slew Rate, –90dBc Distortion at 5MHz

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